Assignment 1

EEE2045F
Analog Electronics
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MLLDYL002

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1. VI Characteristics

A **1N914** diode was modeled in LTspice and the following test circuit built (Fig.1) to characterize the diode's VI response in both forward and reverse bias conditions.

A value of **1.2K** for **R** was chosen to provide approximately **~7.7mA** of forward bias current at **V1=+-10V DC** thereby allowing for a reasonable variation in the forward voltage **~[0,7.6]V** (independent variable) as can be seen in Fig. 2.

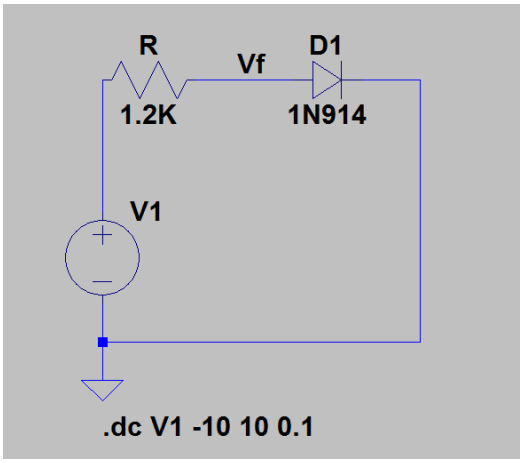

Fig. 1.
1N914 test circuit.

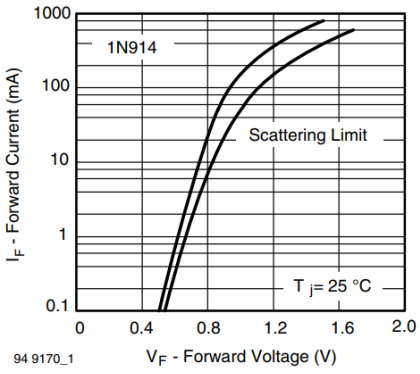

Fig. 1 - Forward Current vs. Forward Voltage

Fig 2.
1N914 Non-ideal VI characteristic

(a) 1N914 diode forward bias VI Characteristics

A linear DC sweep of source (**V1**) between **–10V** and **10V** was configured.

The resultant current **I(D1)/I_F** [fwd. current] vs **Vf/V_F** [fwd. voltage] was plotted (Fig. 3) to obtain the VI characteristic for the total duration of the linear sweep, together with a constrained x-axis plot **[-1,1]V** (Fig. 4) to better visualize the **~0.7V** fwd. bias 'knee'.

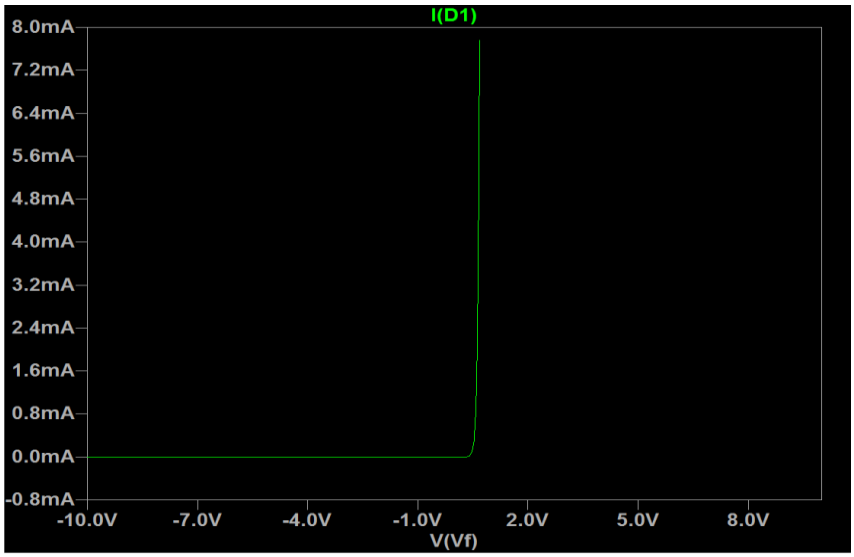

Fig. 3.
VI characteristic for full range DC sweep.

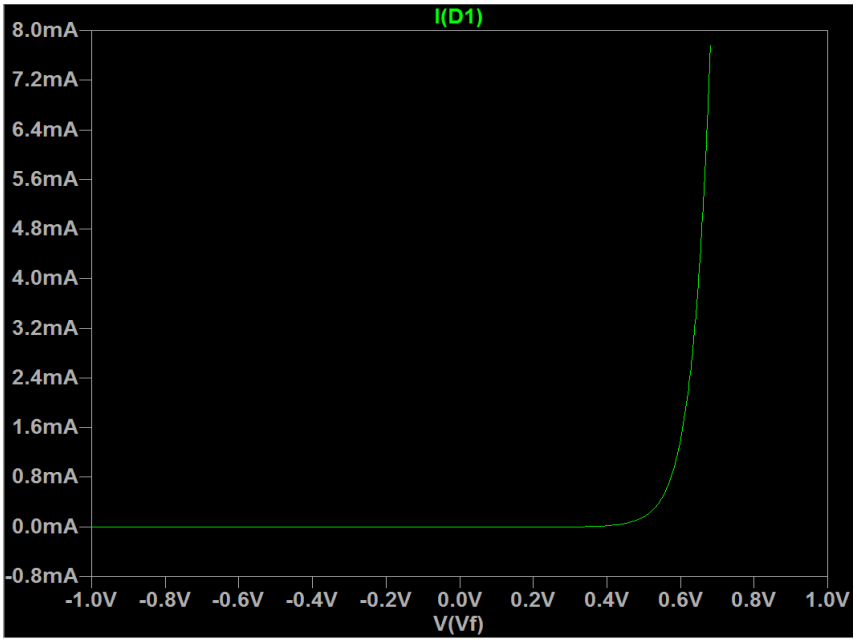

Fig. 4.
Constrained VI characteristic, visualizing the bias 'knee' @ 0.7V.

(b) 1N914 diode reverse bias VI characteristics

For this study, the **1N914** diode's reverse breakdown voltage attribute **(bv) -V_{BR}** was set to **5V D(bv=5)**. The resultant plot for the same **[-10,10] DC sweep** is shown in Fig. 5.

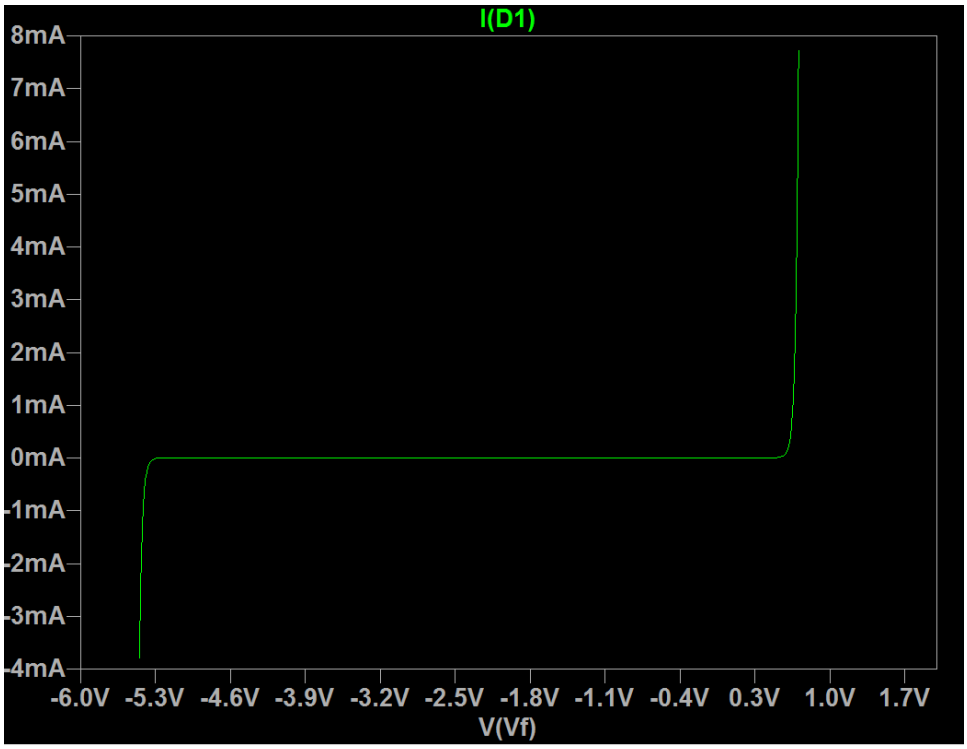

Fig. 5.
1N914 VI characteristic with bv=5 showing both bias 'knee's'

2. Clamping Circuits

(a) Description of results

A 1N750 zener clamper circuit was configured in LTspice (Fig. 6). The circuit consists of a **10Vp, 100Hz AC** sinusoidal voltage source, 1M current limiting resistor and two 1N750 zener diodes with a breakdown voltage attribute **(bv) set to 4.7V**.

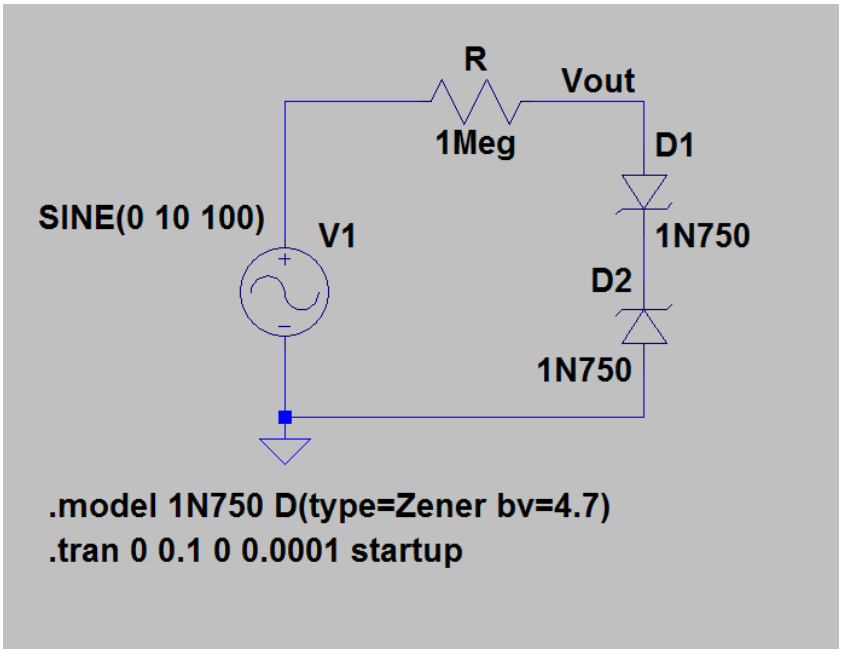

Fig. 6.
1N750 zener clamper circuit.

The resulting output plot is shown in Fig. 7. Both positive and negative regions of the waveform are clipped. The top waveform was measured to be at approx. **~5.4V** and the bottom **~ –5.4V**.

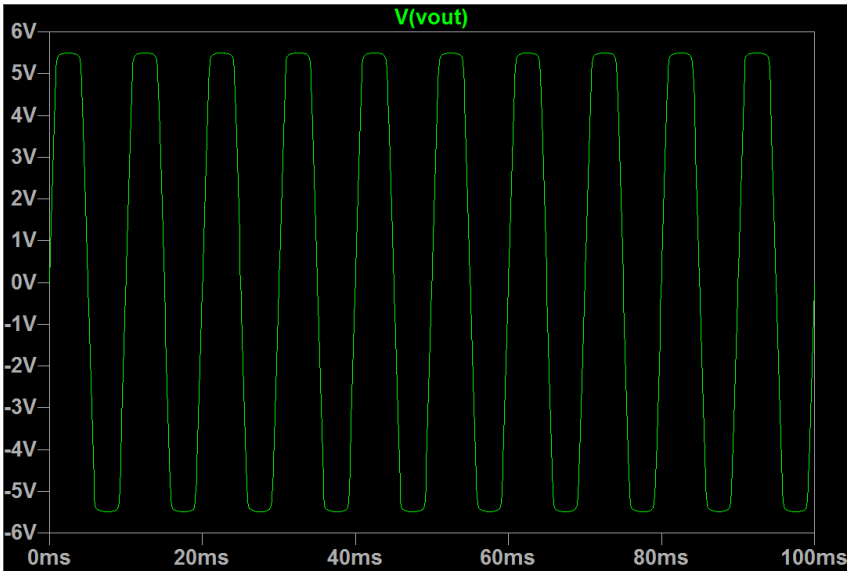

Fig. 7.

(b) Explanation of results

The **10V 100Hz AC** sinusoidal source consists of both positive and negative peaks that are applied at node A.

During a positive peak, the potential at A (diode anode) (Fig. 8) is higher than at the diode's cathode, since current is flowing clockwise. Thus, the upper zener diode is forward biased, with a forward voltage drop of approximately 0.7V. For the lower zener diode, it's cathode is at a higher potential than its anode (connected at node B). Thus, the lower diode is operating in its zener breakdown mode (Vz < 5), with an approximate voltage of **Vz = 4.7V** (nominal). Thus, the output voltage at A can be represented as a series of voltage sources using the practical zener diode model (Fig. 8), where **Va = 0.7V + 4.7V = 5.4V**.

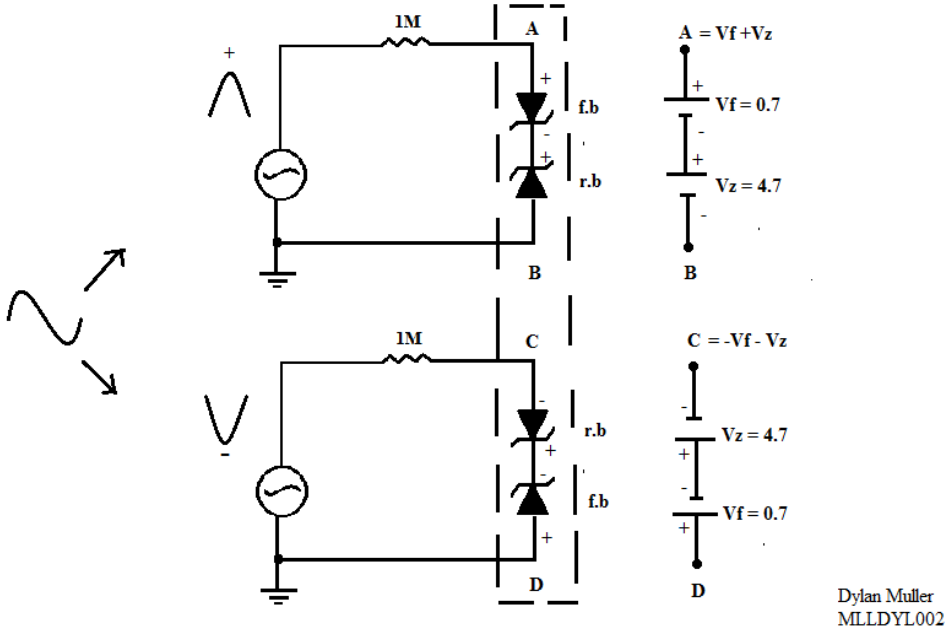

Fig. 8.

During a negative peak, the potential at C (diode anode) (Fig. 8) is lower than at the diode's anode, since current is flowing counter-clockwise. Thus, the upper diode is reverse biased and is operating in its zener breakdown mode (Vz < 5) with an approximate voltage of **Vz = 4.7V** (nominal). For the lower diode, its anode is at a lower potential than its anode and is thus forward biased with a forward voltage drop of approximately 0.7V. Thus, the output at C can be represented as the sum of series voltage sources, where **Vc = -4.7V - 0.7V = -5.4V**.

(c) Varying the breakdown voltage.

A new value for D(bv) was set (bv=2) and the results plotted (Fig. 9). The peak and trough of the waveform were clipped again. The peak of the waveform was measured to be approximately 2.7V and the bottom, -2.7V. Varying the zener breakdown voltage seems to have a predictable effect, in that, the top peak is still at **Vf + Vz** and the bottom through **–Vf – Vz**. Varying the zener breakdown voltage has the effect of increasing or decreasing the amplitude of the clipped waveform.

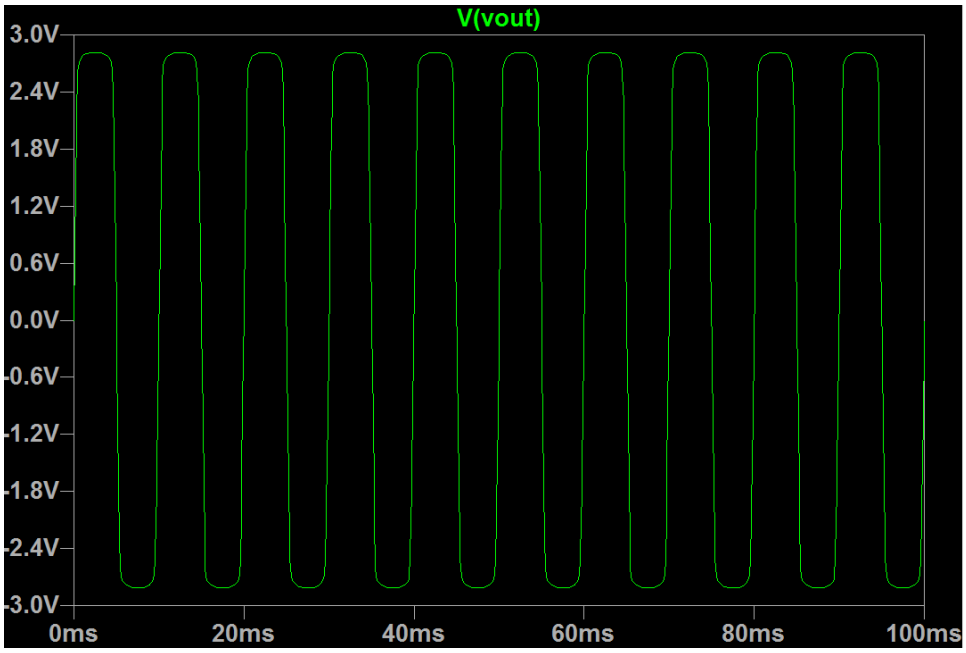

Fig. 9

3. Diode SPICE Parameters

(a) Which diode model parameter is causing the uncharacteristic waveform?

The plot obtained through simulation of the given circuit (Model.asc) exhibits a capacitive charging and discharging effect. This behavior originates due to the diode's p-n junction capacitance (CJO).

The specified diode in the schematic is not designed for high-frequency operation. The signal source has a period of 100ns which corresponds to a frequency of 10MHz. The RC time constant for the charging curve was measured to be approximately 7ns, which, together with the discharging presents significant distortion to the square wave input.

(b) Rectifying the problem

Thus, if we wish to lower the distortion of the output waveform, by reducing the RC time constant, we need to reduce C (the diode's p-n junction capacitance) for a fixed R. More efficient diodes with better values of CJO can be found and provide faster switching times and little distortion at high frequencies. One such diode is the 1N4148 fast switching diode with a maximum diode capacitance of 4pF.

To demonstrate the advantages of a lower diode capacitance, the LTspice directive for the diode in the simulation was modified, setting **Cjo=4pF**. The resulting waveform comparisons are shown in Fig. 10 and Fig. 11 .

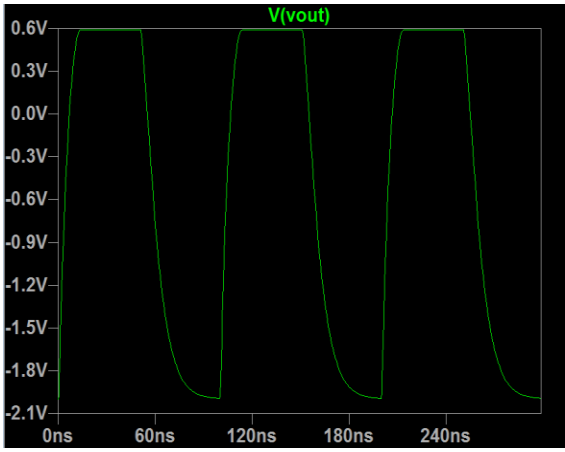

Fig. 10.
Cjo = 10pF

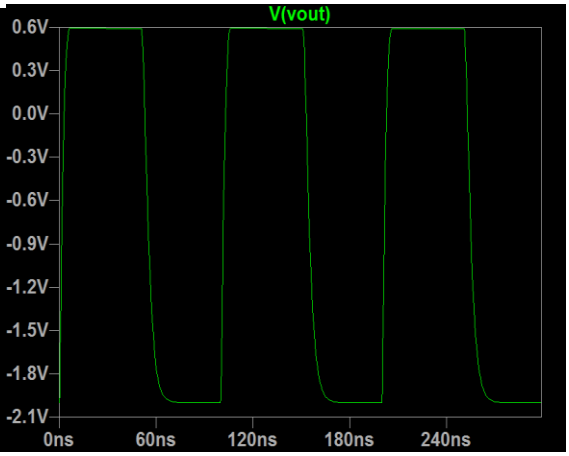

Fig. 11.
Cjo = 4pF

The result is a cleaner square wave with less distortion. Lowering Cjo further improves the output waveform.

4. Diode SPICE Parameters

a(i) The DC operating point simulation cmd. is used when it is convenient to know all nodal voltages and current's during an analysis.
a(ii) Transient is used to calculate voltages and currents in your circuit over time.
a(iii) AC analysis allows one to plot magnitude and/or phase with frequency.
a(iv) DC sweep is used when we would like to input a range of DC voltage values into our circuit and measure its response.

5. Common Emitter Amplifier

(a)

Microphone output voltages are typically within the range of **[5,50] mVp**, without any amplification. It is often a requirement in electronic systems to amplify this signal for further processing. This will be the design project.

The amplifier chosen will be a **BJT (Bipolar Junction Transistor) Common-Emitter amplifier** (Fig. 12). This type of amplifier provides high gain and allows for moderate input and output impedances.

The design parameters were as follows:

- **2N2222 NPN transistor**
- **100K OHM output load which shouldn't affect significantly.**
- **Average Gain of approximately [50 to 100] over signal bandwidth. 10mVpp -> 0.5 Vpp (can be processed further) - gain example of 50.**
- **Bandwidth of 20KHz.**
- **Power Supply of 5V**
- **Moderate input and output impedances. With a 50 ohm signal generator source load.**

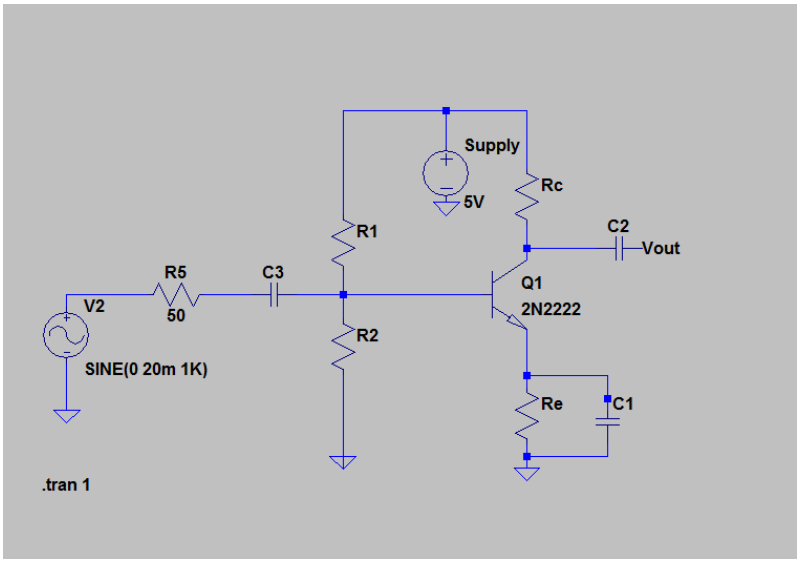

Fig. 12. Common-Emitter configuration.

The small signal ac gain is given by:
Av = Zout/r'e. (Eq. 1)

Hence, we are free to choose Zout which is Rc with no attached load. From an AC perspective:

Zout = Rc // Rload (DC is effectively grounded).

Thus, if **Rc << Rload**, Zout stays at Rc and so our gain stays relatively constant with respect to Rc. Since we know Zload = 100K, we take approx. Zload/20 as **Rc = 5K**. (Rc shouldn't be too small due to tolerances) -- Zload/10 might be preferred.

Since we want a gain in the region of [50,100] we need to determine what maximum or ideal gain is possible with our **5V supply and chosen unloaded output impedance (Zout)**.

r'e = 25mV/I(E)
Av = Rc/r'e

Rearranging for I(E) [mA] we get:
I(E) mA = [Av * 25] / Rc = **(Av * 25mV/5K)**

Since **I(E) ~= I(C)** ,
V(Rc) = **I(E) * 5K** = **Av * 25mV** = **0.025 * Av**. (Eq. 2)

For an ideal Q-point our V(CE) should be half of Vcc = 2.5V or halfway between the x-axis of the load-line.

This leaves us with **5 – 2.5V = 2.5V** to **split between Rc and Re**. It is usually good practice to give 20% of Vcc to Re and the rest to Rc to allow for greater ac voltage swing around the collector. This leaves us with 70% of the 2.5V = **1.75V for Rc**.

Next, using Eq. 2, we find the **ideal gain** corresponding to V(Rc) of 1.75V:
Av = 1.75/0.025 = 70.

Thus, we find our current I(C):
I(C) ~= I(E) = [70*25]/5000 = 0.35mA.

This leaves us with a voltage of **0.75V** across Re.
Since we know the current, **Re** = 0.75/0.35mA **= 2.1K.**
Rc = **5K** (from earlier).

Next, we must trade off Q-point stability for high source impedance. Using AC analysis our 50 ohm signal generator sees an input impedance of Zin = **R1 // R2 // Rbase(in)**

Assuming a **worst-case** ac/dc beta (both are approximately equal) **of 30:**
r'e = 25mV/I(E) = 25/0.35 = **71.4 OHMS.**
Rbase(in) = **beta * r'e .**
Rbase(in) = r'e * 30 = 2.1K.

Thus, **to maintain an input impedance of >= 2.1K**, R1 and R2 must **simultaneously** increase with **Rbase(in)**. However, for Q-point stability R2 should decrease relative to Re and so we have a **trade-off** between these two properties.

Since our signal generator has an internal impedance of 50 OHMS we can make room for a decrease in R2 without effecting our input impedance too much, allowing for higher Q-stability.

V(B) = V(Re) + 0.7 = 0.75 + 0.7 = 1.45V.

Since I(C) is known, 0.35mA, we can work out I(B) assuming the worst-case beta = 30 for 2N2222.

Thus, our maximum base current **I(BMAX) is 0.35mA/30 = 11.7uA**.

We assume that only **1%** of the divider current flows into the base. Thus, we have (1/100 * X) = 11.7uA. Solving for X (divider current through R1) we get **X = 1.17mA**.

Since we know the voltage across R1 (5-1.45) and the current 1.17mA we calculate the **R1 to be: 3K** and **R2 to be 1.45/(0.99 * 1.17)mA = 1.2K**.

Next the value of C1 was calculated. The capacitive reactance, at the signal frequency, of C1 is usually set to **10 times** less than Re. However, a value of 100 times less (higher capacitance) was chosen and rounded up, since it provided higher **Av** at lower signal frequencies (provided lower reactance path).

The value of C1, by experimentation cannot be too high since it was observed that setting C1 too high caused charging/discharging effects on the output waveform, probably due to the increased time-constant K, where 1/K begins to approach the signal frequency?

The values of C3 and C2 were chosen (10uF) to give approximately 8 ohms of reactance to the signal at 2kHz, which did not affect the output significantly.

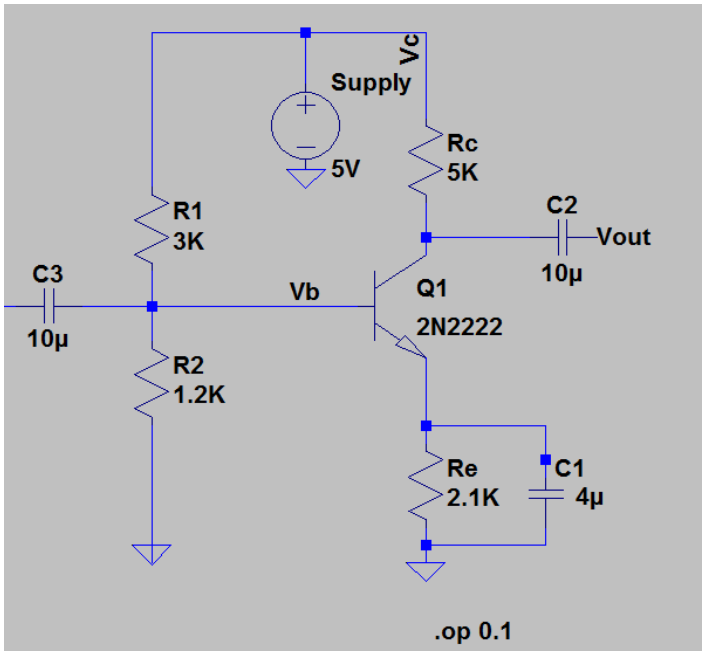

Fig. 13.
Completed front-end of amplifier.

Firstly, the DC operating point was examined for comparison against design data (Fig. 14).

```
        --- Operating Point ---

V(n001):        3.11088         voltage
V(vb):          1.42698         voltage
V(n004):        0.797338        voltage
V(vc):          5               voltage
V(vout):        3.11084e-005    voltage
V(n003):        1.42696e-005    voltage
V(n002):        0               voltage
Ic(Q1):         0.000377825     device_current
Ib(Q1):         1.86014e-006    device_current
Ie(Q1):         -0.000379685    device_current
I(C3):          1.42696e-017    device_current
I(C2):          -3.11084e-017   device_current
I(C1):          3.18935e-018    device_current
I(R2):          0.00118915      device_current
I(R1):          0.00119101      device_current
I(Re):          0.000379685     device_current
I(Rc):          0.000377825     device_current
I(V2):          0               device_current
I(Supply):      -0.00156883     device_current
```

Fig. 14.
DC operating point data.

The simulated collector current (Ic) obtained was 0.0003778A or ~0.38mA, compared to our **I(C) 0.35mA** design estimate.
The base voltage of ~1.43V was not too far off from our 1.45V design estimate. Thus, our DC bias was approximately met.

Next the signal generator as well as the 100K load were connected (Fig. 15.) and the resulting input vs output waveforms plotted. A 5mVp 2kHz signal was fed into C3 (Vin) and the output taken across R3 (Vout) (Fig. 16 & 17)

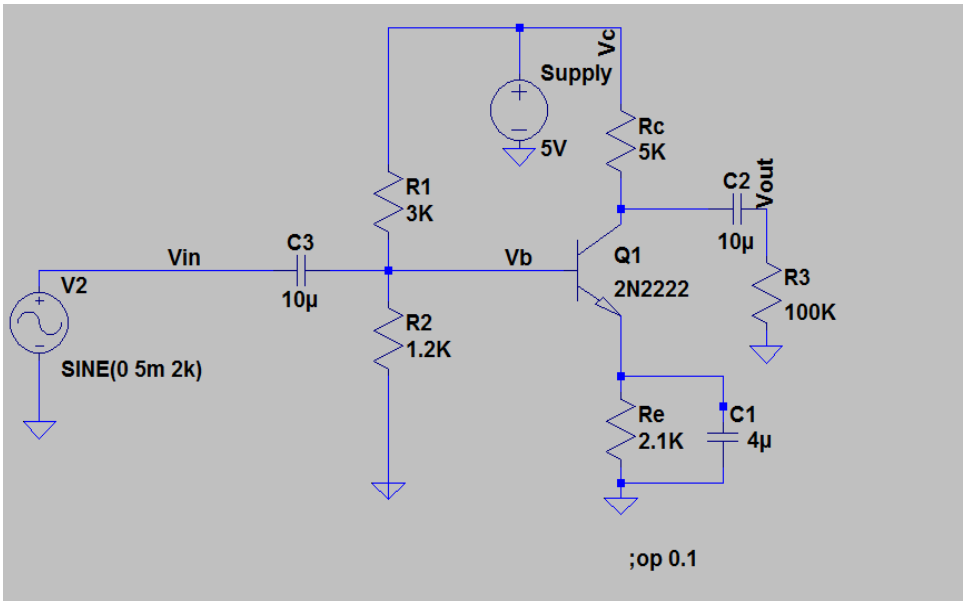

Fig. 15.
Completed CE BJT amplifier circuit.

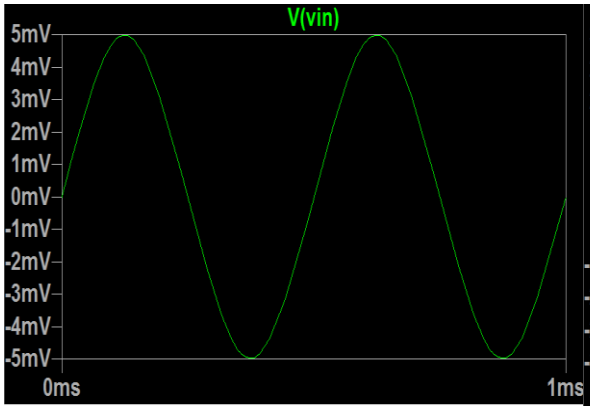

Fig. 16.
Amplifier input (Vin).

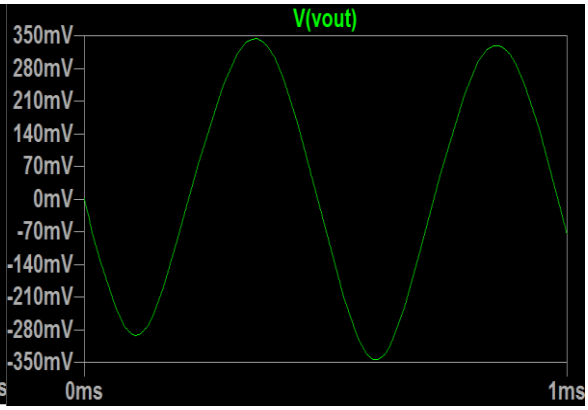

Fig. 17.
Amplifier output (Vout)

As can be seen from the graphs the amplifier produced a peak output of ~350mV with a peak input of ~5mV, **yielding a gain of 350/5 = ~70**, which is what we obtained through our design equations.

Questions:

(i) You can increase the gain of the amplifier without effecting DC bias by adding a bypass or blocking capacitor as I had in my design as C1.

(ii) At about 10mVp above the 5mVp input signal the waveform started to distort.

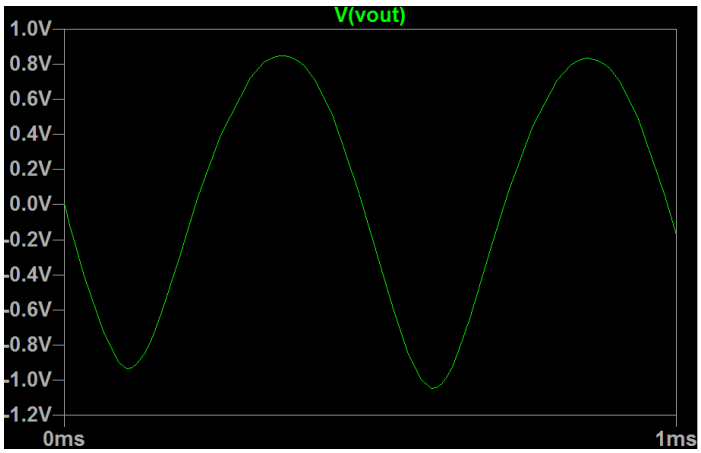

Fig. 17.
Distortion begins @ 10mVp above input.

(iii) Upper and lower cut-off frequencies were found to be 0 to 31 kHz. The lower cut-off frequency can be changed by the addition of a filter.