



Low-Noise, High-Precision, JFET-Input, OPERATIONAL AMPLIFIER

FEATURES

- **OFFSET:** 250 μ V (max)
- **DRIFT:** 1 μ V/ $^{\circ}$ C
- **LOW NOISE:** 4.5nV/ $\sqrt{\text{Hz}}$ at 1kHz
- **BANDWIDTH:** 18MHz
- **SLEW RATE:** 22V/ μ s
- **BIAS CURRENT:** 3pA
- **QUIESCENT CURRENT:** 4.5mA/Ch
- **WIDE SUPPLY RANGE:** \pm 4V to \pm 18V
- **SINGLE PACKAGES:** MSOP-8, SO-8
- **DUAL PACKAGES:** SO-8 PowerPAD

APPLICATIONS

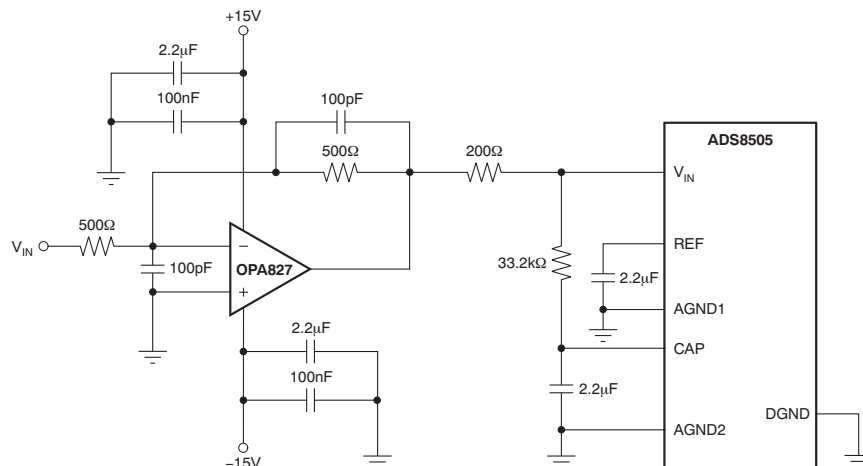
- **PRECISION \pm 10V INPUT FRONT-ENDS**
- **TRANSIMPEDANCE AMPLIFIERS**
- **INTEGRATORS**
- **ACTIVE FILTERS**
- **A/D CONVERTER DRIVERS**
- **DAC OUTPUT BUFFERS**
- **HIGH-PERFORMANCE AUDIO**
- **PROCESS CONTROL**
- **TEST EQUIPMENT**
- **MEDICAL EQUIPMENT**

DESCRIPTION

The OPA827 series of JFET operational amplifiers combines outstanding dc precision with excellent ac performance. It offers 100 μ V of offset, very low drift (1 μ V/ $^{\circ}$ C) over temperature, low bias currents, and very low flicker noise of 400nV_{PP} (0.1Hz to 10Hz). It operates over a very wide supply voltage range of \pm 4V to \pm 18V on a low 4.5mA supply current. A dual version is also available for the OPA827 family.

Excellent ac characteristics, such as 18MHz gain bandwidth (GBW) and 22V/ μ s slew rate, and precision dc characteristics make the OPA827 series well-suited for a wide range of applications such as 16- to 18-bit data acquisition systems, transimpedance (I/V-conversion) amplifiers, filters, precision \pm 10V front ends, and professional audio applications.

The single version (OPA827) is available in both MSOP-8 and standard SO-8 surface-mount packages. The dual version (OPA2827) is available in the SO-8 PowerPAD for increased power dissipation capability. All versions are specified from -40° C to $+125^{\circ}$ C.



PRODUCT PREVIEW



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
Standard Grade			
OPA827A	SO-8	D	OPA827A
	MSOP-8	DGK	TBD
OPA2827A	SO-8 PowerPAD	DDA	TBD
High Grade			
OPA827I	SO-8	D	OPA827
	MSOP-8	DGK	TBD
OPA2827I	SO-8 PowerPAD	DDA	TBD

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

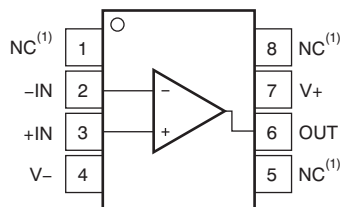
Over operating free-air temperature range (unless otherwise noted)

	VALUE	UNIT
Supply Voltage	±20	V
Signal Input Terminals		
Voltage ⁽²⁾	(V ₋) -0.7 to (V ₊) +0.7	V
Current ⁽²⁾	±10	mA
Differential Input Voltage	TBD	V
Output Short-Circuit ⁽³⁾	Continuous	
Operating Temperature	-55 to +125	°C
Storage Temperature	-65 to +150	°C
Junction Temperature	+150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.7V beyond the supply rails should be current-limited to 10mA or less.
- (3) Short-circuit to ground, one amplifier per package.

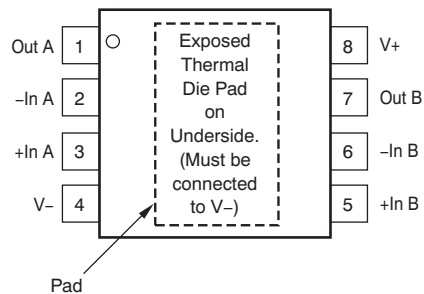
PIN ASSIGNMENTS

OPA827
SO-8, MSOP-8
(TOP VIEW)



(1) NC denotes no internal connection.

OPA2827
SO-8 PowerPAD
(TOP VIEW)



PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: $V_S = \pm 4V$ to $\pm 18V$

BOLDFACE limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$.

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER		CONDITIONS	Standard Grade OPA827A, OPA2827A			High Grade OPA827I, OPA2827I ⁽¹⁾			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE									
Input Offset Voltage	V _{OS}	V _{CM} = 0V, V _S = ±15V		TBD	250		TBD	TBD	μV
Drift	dV _{OS} /dT			1	3.5		TBD	TBD	μV/°C
vs Time				±0.2			±0.2		μV/month
vs Power Supply	PSRR	V _S = ±4V to ±18V, V _{CM} = 0V		TBD	10		TBD	TBD	μV/V
Over Temperature		V _S = ±4V to ±18V, V _{CM} = 0V			30			TBD	μV/V
Channel Separation, dc				TBD			TBD		μV/V
INPUT BIAS CURRENT									
Input Bias Current	I _B			±3	TBD		±3	TBD	pA
Over Temperature				TBD	TBD		TBD	TBD	pA
Input Offset Current	I _{OS}			±3	TBD		±3	TBD	pA
NOISE									
Input Voltage Noise:									
f = 0.1Hz to 10Hz	e _n	V _S = ±18V, V _{CM} = 0V		0.4			0.4		μV _{PP}
Input Voltage Noise Density:									
f = 1kHz	e _n	V _S = ±18V, V _{CM} = 0V		4.5			4.5		nV/√Hz
f = 10kHz	e _n	V _S = ±18V, V _{CM} = 0V		4.5			4.5		nV/√Hz
Input Current Noise Density:									
f = 1kHz	i _n	V _S = ±18V, V _{CM} = 0V		TBD			TBD		fA/√Hz
INPUT VOLTAGE RANGE									
Common-Mode Voltage Range	V _{CM}		(V–)+2.5		(V+)-2.5	(V–)+2.5		(V+)-2.5	V
Common-Mode Rejection Ratio	CMRR	(V–)+2.5V < V _{CM} < (V+)-2.5V	108			TBD			dB
Over Temperature				TBD			TBD		dB
INPUT IMPEDANCE									
Differential				10 ¹³ TBD			10 ¹³ TBD		Ω pF
Common-Mode				10 ¹³ 7			10 ¹³ 7		Ω pF
OPEN-LOOP GAIN									
Open-Loop Voltage Gain	A _{OL}	R _L = 2kΩ, (V–)+2.75V < V _O < (V+)-2.1V	114	120		TBD	TBD		dB
Over Temperature		R _L = 2kΩ, (V–)+2.75V < V _O < (V+)-2.1V	108	TBD		TBD	TBD		dB
FREQUENCY RESPONSE									
		C _L = 100pF							
Gain-Bandwidth Product	GBW			18			18		MHz
Slew Rate	SR	G = +1		22			22		V/μs
Settling Time, 0.1%	t _s	4V Step, G = +1		TBD			TBD		ns
0.01% (16-bit)		4V Step, G = +1		TBD			TBD		ns
Overload Recovery Time		V _{IN} • Gain > V _S		TBD			TBD		μs
Total Harmonic Distortion + Noise	THD+N	G = +1, f = 1kHz		TBD			TBD		%

(1) Shaded cells indicate different specifications from low-grade version of device.

ELECTRICAL CHARACTERISTICS: $V_S = \pm 4V$ to $\pm 18V$ (continued)

BOLDFACE limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$.

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER	CONDITIONS	Standard Grade OPA827A, OPA2827A			High Grade OPA827I, OPA2827I ⁽¹⁾			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT								
Voltage Output Swing from Rail	$R_L = 2\text{k}\Omega$, $A_{OL} > 114\text{dB}$	(V–)+2.75		(V+)-2.1	(V–)+2.75		(V+)-2.1	V
Over Temperature	$R_L = 2\text{k}\Omega$, $A_{OL} > 108\text{dB}$	(V–)+2.75		(V+)-2.1	(V–)+2.75		(V+)-2.1	V
Output Current I_{OUT}	$ V_S - V_{OUT} < 1.5\text{V}$		30			30		mA
Short-Circuit Current I_{SC}			±40			±40		mA
Capacitive Load Drive C_{LOAD}			TBD			TBD		pF
POWER SUPPLY								
Specified Voltage V_S		±4		±18	±4		±18	V
Quiescent Current (per amplifier) I_Q	$I_{OUT} = 0\text{V}$		4.5	TBD		4.5	TBD	mA
Over Temperature				TBD			TBD	mA
TEMPERATURE RANGE								
Specified Range		–40		+125	–40		+125	°C
Operating Range		–55		+125	–55		+125	°C
Thermal Resistance Θ_{JA}								
SO-8, MSOP-8			150			150		°C/W
SO-8 PowerPAD			TBD			TBD		°C/W

(1) **Shaded cells** indicate different specifications from low-grade version of device.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
OPA827AID	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI
POPA827AID	PREVIEW	SOIC	D	8	1500	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

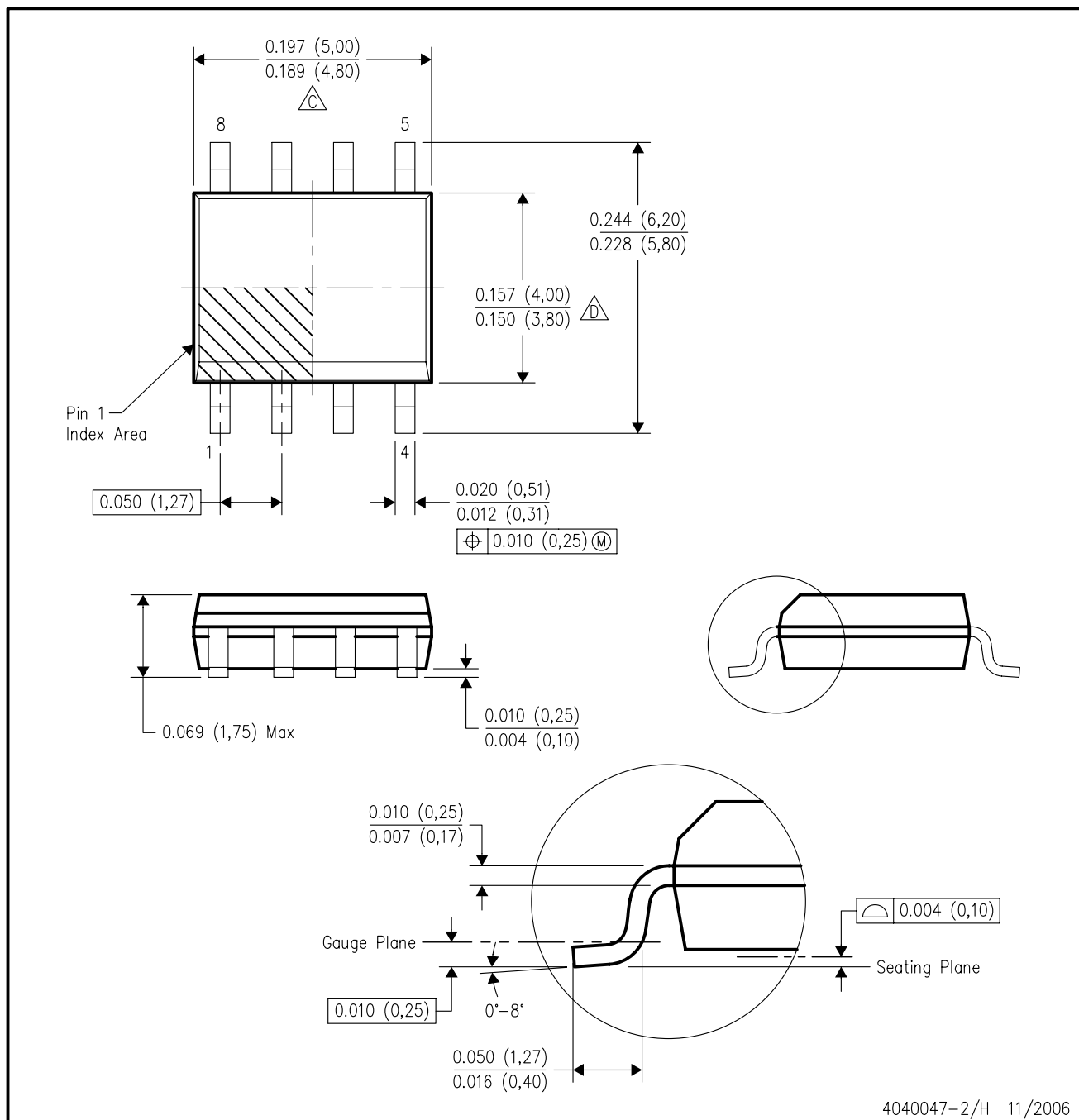
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AA.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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