General Standards Corporation

High Performance Bus Interface Solutions

Revision 032505

PMC- ADADIO

12-CHANNEL, 16-BIT
PMC ANALOG INPUT/OUTPUT BOARD

WITH SIMULTANEOUS INPUT SAMPLING

REFERENCE MANUAL

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION 1.0

INTRODUCTION

1.1 General Description

The PMC-ADADIO board is a single-width PCI mezzanine card (PMC) that provides system analog input/output capability for the PCI bus. In addition to containing eight analog input channels and four analog output channels, the board also has a general-purpose byte-wide digital port. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.2, is mechanically compatible with the IEEE compact mezzanine card (CMC) specification, and supports the "plug-n-play" initialization concept. Power requirements consist of +5 VDC and in accordance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling. Specific details of physical characteristics and power requirements are contained in the PMC-ADADIO product specification. Figure 1.1-1 shows the physical configuration of the board, and the arrangement of major components.

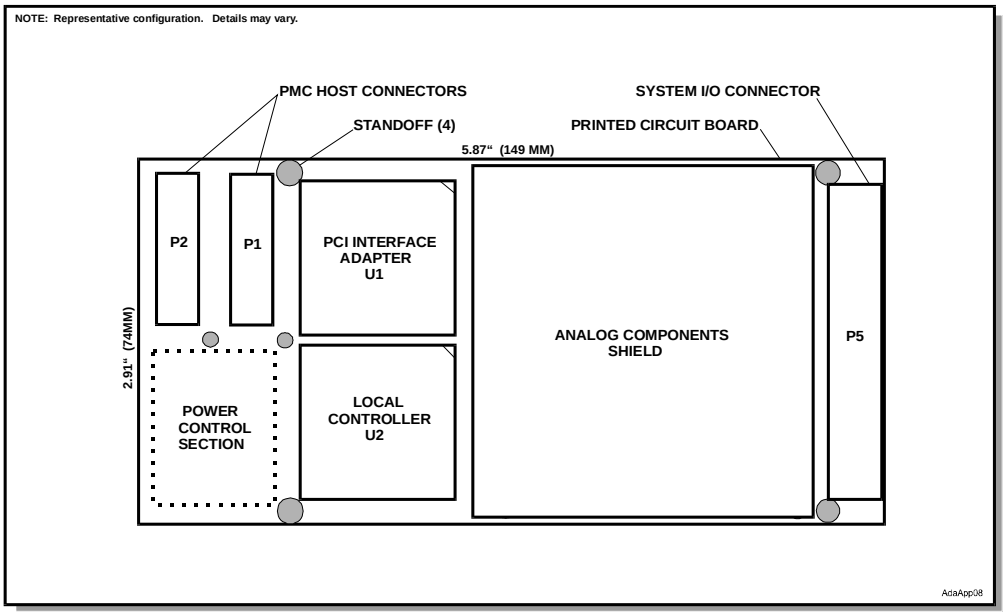

Figure 1.1-1. Physical Configuration

The board is designed for minimum off-line maintenance, and includes internal monitoring and loopback features that eliminate the need for disconnecting or removing the module from the system for calibration. All analog input and output system connections are made through a single 68-pin subminiature-D front-access I/O connector. The analog outputs can be internally disconnected from the system I/O connector under software control.

1.2 Functional Overview

The 12-channel PMC-ADADIO analog I/O board provides high-resolution 16-bit analog input and output resources in a high-density single-width PMC module. Principal capabilities of the board are summarized in the following list of features.

- ❑ 16-Bit Resolution; Analog Inputs and Outputs
- ❑ 8 Analog Input Channels, 4 Analog Output Channels
- ❑ 8-Bit Bidirectional Digital Port with Two Auxiliary Control Lines
- ❑ Autocalibration of all Analog Channels; Internally Controlled
- ❑ Input and Output Ranges of ±10V, ±5V or ±2.5V
- ❑ Simultaneous Analog Input Sampling; 16-Bit A/D Converter per Channel
- ❑ 32K-Sample Analog Input FIFO Buffer
- ❑ Continuous and Triggered-Burst Input Modes. Supports Multiboard Synchronization
- ❑ 16-Bit D/A Converter per Analog Output Channel
- ❑ Analog Outputs Disconnect from System Under Software Control
- ❑ Loopback Feature for Built-in-Test Support and Autocalibration
- ❑ Entirely Software-Configurable; No Field Programmable Jumpers or Switches
- ❑ Single-width PMC Form Factor.

Figure 1.2-1 outlines the internal functional organization of the board. Communication with the host PCI bus is provided by a PCI interface adapter which furnishes a 32-bit local bus for exchanging information between the adapter, the local controller, and the control and data registers.

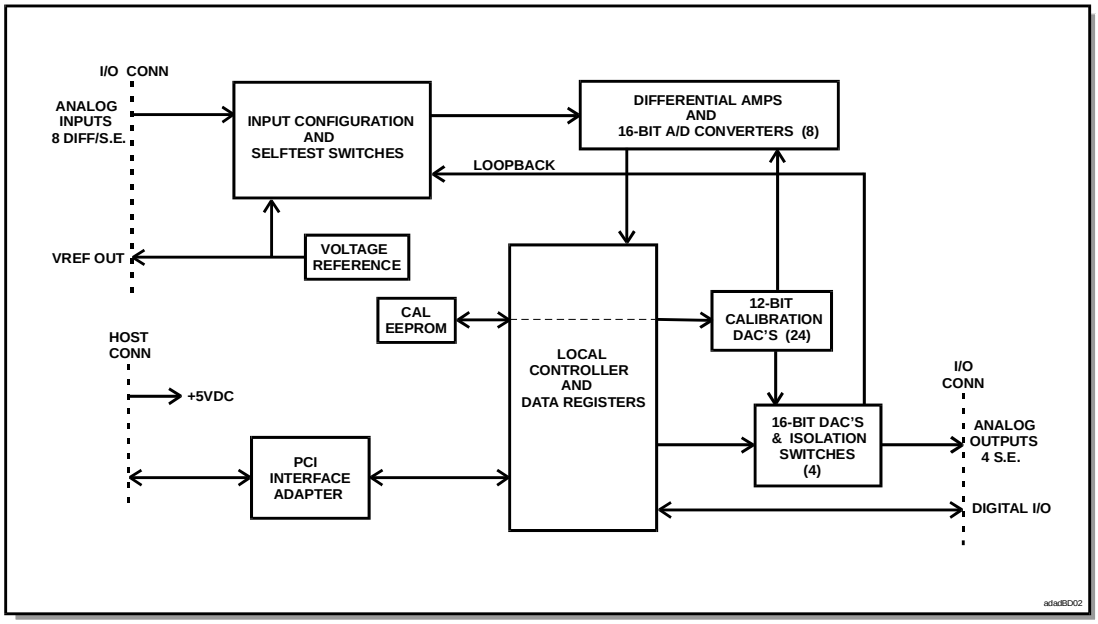

Figure 1.2-1. Functional Organization

All active analog input channels are sampled simultaneously, and are configurable as either differential or single-ended inputs. Input sampling can be performed continuously, or can be burst-triggered by either a software trigger or a hardware trigger. A FIFO buffer accumulates input data samples for subsequent transfer to the PCI bus. The four analog output channels are accessed through independent registers, and can be updated either synchronously or

asynchronously. Inputs and outputs have a factory-configured range of ±10V, ±5V or ±2.5V. A digital port provides eight bidirectional data lines and two auxiliary control lines.

All input and output channels are calibrated with a single internal voltage reference. This feature produces the optimum calibration situation, in which the board is calibrated in its actual operating environment. Software-controlled test configurations include a loopback mode for monitoring all analog output channels.

Offset and gain trimming of the 16-bit A/D converters (ADC's) and output D/A converters (DAC's) is performed by 12-bit calibration DAC's. System analog inputs pass through a selftest network which replace the system signals either with a precision voltage standard or with the four analog output channels, under software control. Offset and gain correction values are determined during autocalibration, and are stored in nonvolatile EEprom for subsequent transfer to the calibration DAC's during board initialization. Autocalibration can be invoked at any time from the PCI bus.

SECTION 2.0

INSTALLATION AND MAINTENANCE

5.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

5.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping envelope, position the board with the shield and standoffs facing the host (carrier) board, and with the 68-Pin I/O connector oriented toward the front panel. Align the two PCI connectors located at the end of the board opposite the I/O connector with the mating connectors on the host board, and carefully press the board into position on the host. Verify that the PCI connectors have mated completely and that the four standoffs are seated against the host board.

Attach the board to the host with four 2.5 x 6.5mm panhead screws. Pass the screws through the back of the host into the four standoffs mounted on the board. Tighten the screws carefully to complete the installation; do not overtighten.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2.2-1. Unused input pins may be left disconnected in most applications. However, if very long cables are used or if excessive cable noise is anticipated, the unused analog inputs should be grounded to the input return to minimize the injection of noise into the board.

I/O connector P5 is designed to mate with a standard male 68-pin 0.05" subminiature D connector, equivalent to AMP #1-750913-7. The insulation displacement (IDC) AMP cable connector accepts two 34-conductor ribbon cables in the configuration shown in Figure 2.2.2-1.

Fine-pitch standard SCSI cables, if used, would intersperse the digital I/O lines with the analog I/O lines, and are not recommended for analog I/O applications.

Table 5.2.2-1. System Connector Pin Functions

P5A	
PIN	SIGNAL
1	OUTPUT RETURN
2	OUTPUT CHANNEL 00
3	OUTPUT RETURN
4	OUTPUT CHANNEL 01
5	OUTPUT RETURN
6	OUTPUT CHANNEL 02
7	OUTPUT RETURN
8	OUTPUT CHANNEL 03
9	INPUT RETURN
10	INPUT RETURN
11	INPUT CHANNEL 00 LO (-)
12	INPUT CHANNEL 00 HI (+)
13	INPUT CHANNEL 01 LO (-)
14	INPUT CHANNEL 01 HI (+)
15	INPUT CHANNEL 02 LO (-)
16	INPUT CHANNEL 02 HI (+)
17	INPUT CHANNEL 03 LO (-)
18	INPUT CHANNEL 03 HI (+)
19	INPUT CHANNEL 04 LO (-)
20	INPUT CHANNEL 04 HI (+)
21	INPUT CHANNEL 05 LO (-)
22	INPUT CHANNEL 05 HI (+)
23	INPUT CHANNEL 06 LO (-)
24	INPUT CHANNEL 06 HI (+)
25	INPUT CHANNEL 07 LO (-)
26	INPUT CHANNEL 07 HI (+)
27	VREF RETURN
28	VREF ADJUST REFERENCE
29	VREF RETURN
30	VREF REMOTE ADJUST
31	VREF RETURN
32	RANGE VREF
33	VREF RETURN
34	VREF RETURN

P5B	
PIN	SIGNAL
1	DIGITAL RETURN
2	INPUT TRIGGER
3	DIGITAL RETURN
4	INPUT TRIGGER READY
5	DIGITAL RETURN
6	OUTPUT STROBE
7	DIGITAL RETURN
8	OUTPUT STROBE READY
9	DIGITAL RETURN
10	I/O DATA 00
11	DIGITAL RETURN
12	I/O DATA 01
13	DIGITAL RETURN
14	I/O DATA 02
15	DIGITAL RETURN
16	I/O DATA 03
17	DIGITAL RETURN
18	I/O DATA 04
19	DIGITAL RETURN
20	I/O DATA 05
21	DIGITAL RETURN
22	I/O DATA 06
23	DIGITAL RETURN
24	I/O DATA 07
25	DIGITAL RETURN
26	I/O CONTROL INPUT
27	DIGITAL RETURN
28	I/O CONTROL OUTPUT
29	DIGITAL RETURN
30	DIGITAL RETURN
31	DIGITAL RETURN
32	DIGITAL RETURN
33	DIGITAL RETURN
34	DIGITAL RETURN

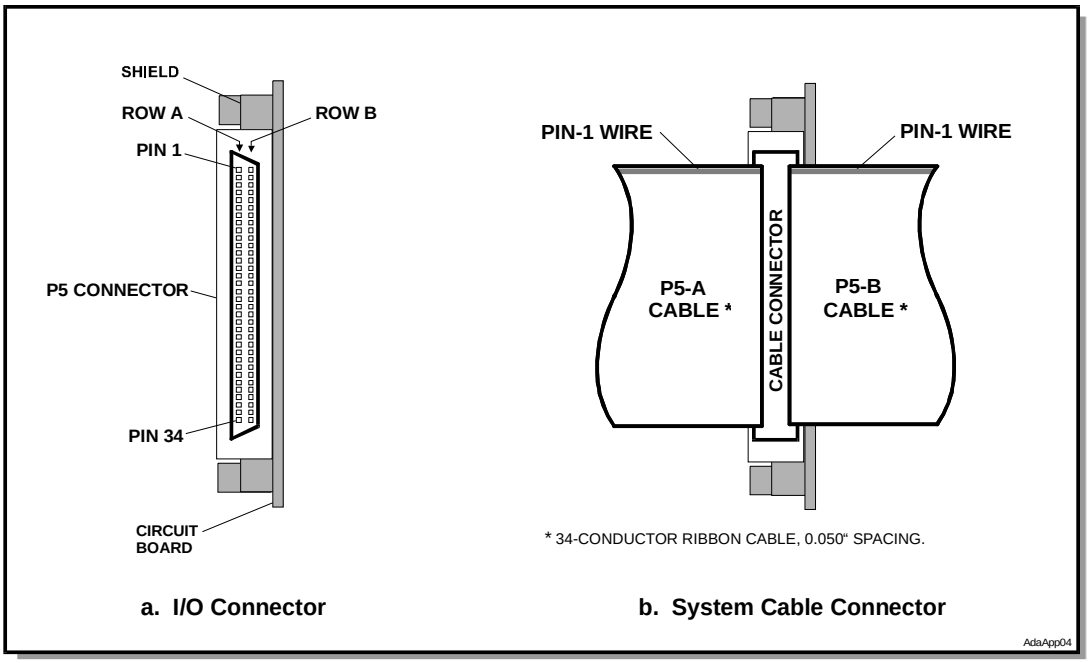

Figure 2.2.2-1. Input/Output Connector and Cables

2.3 System Configuration

2.3.1 Analog Inputs

2.3.1.1 Input Configuration

Analog inputs can be configured either as eight single-ended channels or as eight differential channels, as illustrated in Figure 2.3.1.1-1. The board also permits the inputs to be connected in an eight-channel pseudo-differential arrangement, which is a variation of the single-ended configuration. The hardware input configuration must be acknowledged by the control software, which configures the controller for either single-ended or differential operation. Pull-down resistors are provided on all analog inputs.

Single-ended and pseudo-differential operating modes generally provide optimum performance only when the input signal sources either are isolated from each other, or are common only to a single isolated signal return.

For applications in which the signal sources are isolated from each other (mutual isolation), single-ended operation usually is recommended. In this case, as shown in Figure 2.3.1.1-1a, the input return is connected to the internal VREF return, which provides a return path for all inputs. Isolation from system grounds is a critical issue in single-ended operation. If the signal sources are returned externally to system ground when operating in this mode, a potential difference between the system ground and the VREF return can generate excessive return current and cause erroneous measurements or possibly damage the board.

If the signal sources are connected to a common return, but the return is otherwise isolated from system ground, then pseudo-differential operation may produce acceptable results. Pseudo-differential operation provides a 'soft' return to system ground through an internal resistance, shown as Rrtn in Figure 2.3.1.1-1b. The VREF return pin is left disconnected in this mode. Rrtn is approximately 200 Ohms, and prevents excessive current from flowing into the VREF return, while still providing an input return path. The input return serves as a common differential return for all eight input channels. To prevent excessive dissipation in Rrtn, the potential between the input return and the VREF return must not exceed 3 Volts. INPUT RETURN serves as a remote-sense input in this configuration, and consequently is susceptible to both radiated and conducted system noise. If excessive noise is experienced, a large capacitance (10-100uF) between the INPUT RETURN and VREF RETURN lines may be necessary to alleviate the problem.

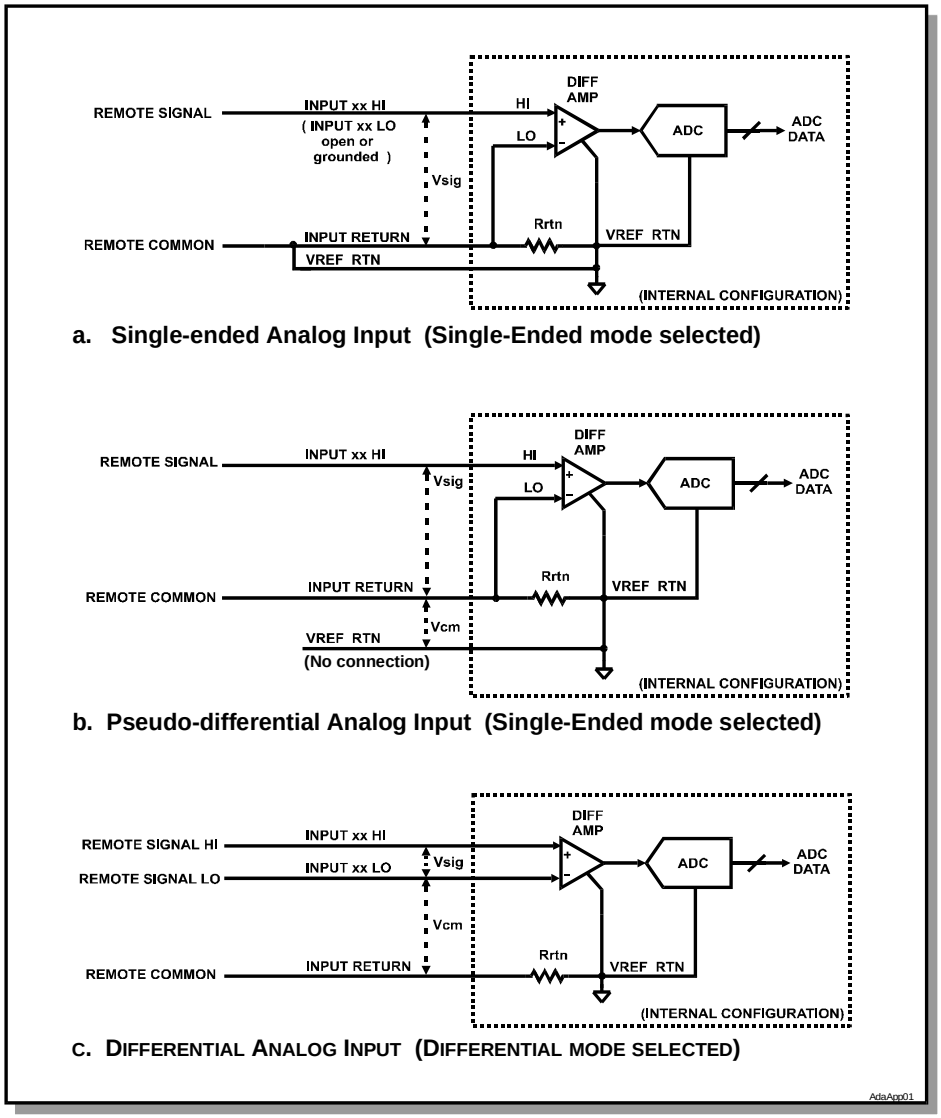

Figure 2.3.1.1-1. Analog Input Configurations

Differential operation is necessary when the input sources are not isolated from each other, and especially when the source returns may be at different potentials. This operating mode also offers the highest rejection of the common mode noise that is characteristic of long unshielded cables. When operating in the differential mode, shown in Figure 2.3.1.1-1c, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return is connected to system ground as closely as possible to the input sources, and the VREF return usually is left disconnected.

2.3.1.2 Input Trigger

Two signal lines in the I/O connector, INPUT TRIGGER and INPUT TRIGGER READY, support external triggering of input burst samples. A burst sample consists of a single sample of all active channels. If the board is software configured for burst sampling, a HIGH-to-LOW transition of INPUT TRIGGER while INPUT TRIGGER READY is HIGH will initiate a single sample of the active inputs. No other combination of these control signals will trigger a sample. The control levels are TTL compatible, with "HIGH" indicating a level above the TTL high-threshold. The INPUT TRIGGER, when asserted, must remain LOW for a minum interval of 0.5 microsecond.

For multiboard *initiator/target* operation, one board is designated as the initiator, and all remaining boards are designated as targets. In this mode of operation, the INPUT TRIGGER READY output from the designated initiator is connected to the INPUT TRIGGER inputs of all targets.

2.3.2 Analog Outputs

2.3.2.1 Output Configuration

The four analog output channels are single-ended and have a common signal return, referred to in Table 2.2-1 as OUTPUT RETURN. In general, single-ended outputs should drive only loads that are isolated from system ground. The best results are obtained when the loads also are isolated from each other. Analog outputs can be disconnected from the system I/O connector under software control. When disabled, each output appears as approximately 20-30 KOhms to OUTPUT RETURN.

The voltage drop in ribbon cable can be a significant source of error in 16-bit systems, even with relatively short cables driving low-current loads. Figure 2.3.2.1-1 shows the effect of load current on the voltage drop in copper wire of various sizes. A 2.0 milliamp load for example, will insert a voltage drop of approximately 130 microvolts *per foot* in conventional #28 AWG ribbon cable; twice that if the return line is also considered. Several feet of ribbon cable therefore can produce significant errors in a 16-bit system, in which 1 LSB may represent only 76 microvolts (±2.5 Volt range). High impedance loads generally will not produce significant DC line loss errors.

Figure 2.3.2.1-2 shows the primary sources of error in both isolated and nonisolated system configurations. For loads that are isolated from each other (Figure 2.3.2.1-1a), the total line-loss error is twice the loss produced in a single line, assuming equal wire size and length for output and return lines. For loads with a common return that is isolated from system ground, line loss in the common return appears as crosstalk between channels.

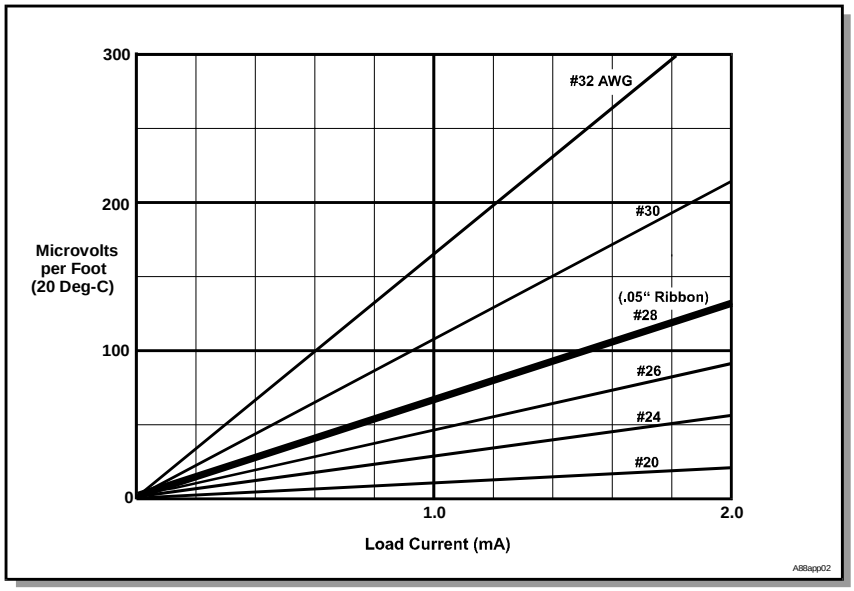

Figure 2.3.2.1-1. Line Loss Versus Load Current

If the load return is inadvertently connected to a remote system ground (Figure 2.3.2.1-1b), the potential difference Vgnd between the system ground and the internal signal return will introduce an error into the signal delivered to the load. The ground current Ignd developed in the return line is limited essentially only by Rgnd, and may damage the cable or the board if not controlled.

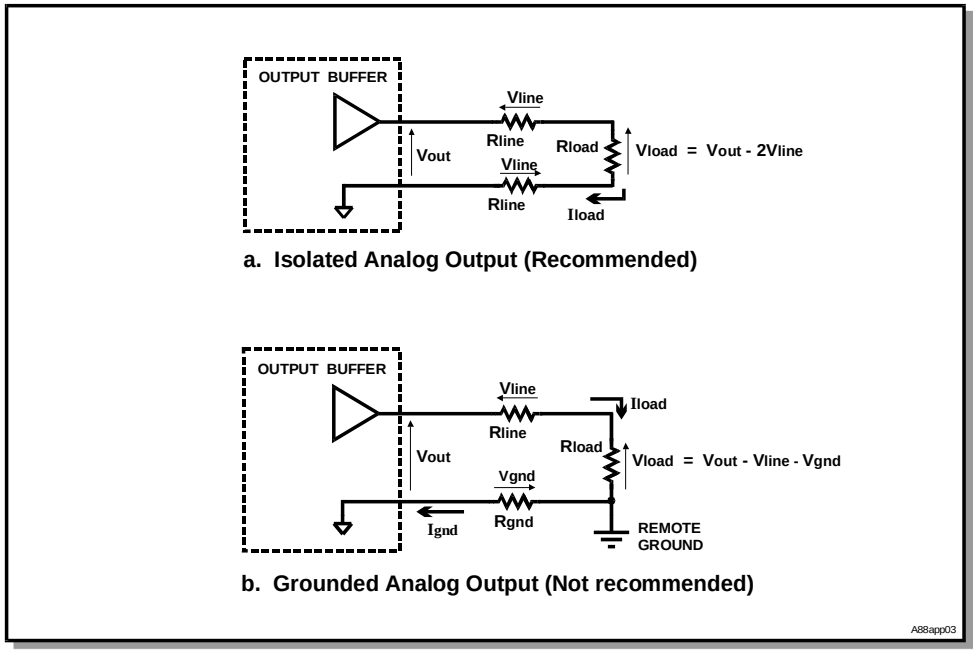

Figure 2.3.2.1-2. Output Configurations

2.3.2.2 Output Strobe

If the board is software-configured for output strobing, all outputs will update simultaneously to stored values if an external strobe occurs. Two signal lines in the I/O connector, OUTPUT STROBE and OUTPUT STROBE READY, provide the external strobing function. If the board is software-configured for output strobing, a HIGH-to-LOW transition of OUTPUT STROBE while OUTPUT STROBE READY is HIGH will generate an external strobe. No other combination of these control signals will generate a strobe. The control levels are TTL compatible, with "HIGH" indicating a level above the TTL high-threshold.

2.4 Digital Input/Output Port

The digital I/O port consists of eight bidirectional digital signals (I/O DATA 00-07), one dedicated output signal (I/O CONTROL OUTPUT) and one dedicated input signal (I/O CONTROL INPUT), all of which are TTL compatible. Bidirectional pins are software-configured as either inputs or outputs. All outputs have a source impedance of approximately 50 ohms. The function of each line is determined entirely by specific system requirements.

This port is intended to be used for general low-power command and status signaling, and is not designed for high speed communication through long cables. The source or sink current at each digital I/O pin must be limited to no more than 20 ma. Exceeding this limit may damage the board.

2.5 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference calibration. The optimum calibration interval will vary, depending upon the specific application, but in most instances an interval of one year is recommended.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and input signal levels, should be evaluated before troubleshooting of the board itself is attempted. If surface-mount repair capability is not available, a board that is suspected to be defective should be returned to the factory for problem analysis and repair.

2.6 Reference Adjustment

All input and output channels are software-calibrated to an internal voltage reference (Vrange) by an embedded autocalibration software utility. The procedure presented here describes the adjustment of the reference. For applications in which the system must not be powered down, the adjustment can performed under normal operating conditions while the board is installed on the host.

To eliminate the requirement for a special test connector, the two test points required for reference adjustment, RANGE VREF and VREF RETURN, can be made available at a system breakout connector or test panel. This arrangement also eliminates the necessity of disconnecting the system input/output cable for reference adjustment.

2.6.1 Equipment Required

Table 2.6.1-1 lists the minimum equipment requirements for adjusting the PMC-ADADIO reference. Alternative equivalent equipment may be used.

Table 2.6.1-1. Reference Adjustment Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±2.5 Volts to ±10 Volts.	Hewlett Packard	34401A
Host board with single-width PMC adapter	(Existing host)	---
Standard 68-Pin, 0.05", subminiature "D" connector, with test leads. (Not required if calibration test points are made permanently available at a system connection point)	AMP	1-750913-7

2.6.2 Adjustment Procedure

The following procedure describes the single adjustment that is necessary to ensure conformance to the product specification.

Adjustment of the internal reference (Vrange) can be performed locally with an internal trimpot, or remotely with a potentiometer connected to the P5A cable. If practical, the internal reference trimpot should be used to perform the Vrange adjustment. The adjustment trimpot is located under the shield, and is accessible from the side of the board as shown in Figure 2.6.2-1. The adjustment seal on the trimmer should be removed before beginning the procedure, and the trimmer should then be resealed with a suitable sealing agent after the adjustment has been completed.

If the internal Vrange trimmer is inaccessible, adjustment of the reference can be performed remotely by connecting a 20 KOhm potentiometer to the P5A system cable, as shown in Figure 2.6.2-2. The potentiometer must remain connected after the adjustment procedure has been completed.

This procedure assumes that the board to be adjusted is installed on a host board, and that the host is installed in an operating system. The board can be in any operating mode when the adjustment is performed.

1. Connect the digital multimeter between the RANGE VREF (+) and VREF RETURN (-) pins in the system I/O connector. Refer to Table 2-1 for pin assignments.

2. If power has been removed from the board, apply power now and wait at least 15 minutes before proceeding..

3. Adjust the REFERENCE ADJUSTMENT trimmer until the digital multimeter indication is within the appropriate range listed in the following table:

INPUT VOLTAGE RANGE	MULTIMETER INDICATION RANGE (DC Volts) .
±10 Volts	+9.9902 ±0.0009
± 5 Volts	+4.9951 ±0.0005
±2.5 Volts	+2.4976 ±0.0003.

4. Reference adjustment is complete. Remove all test connections.

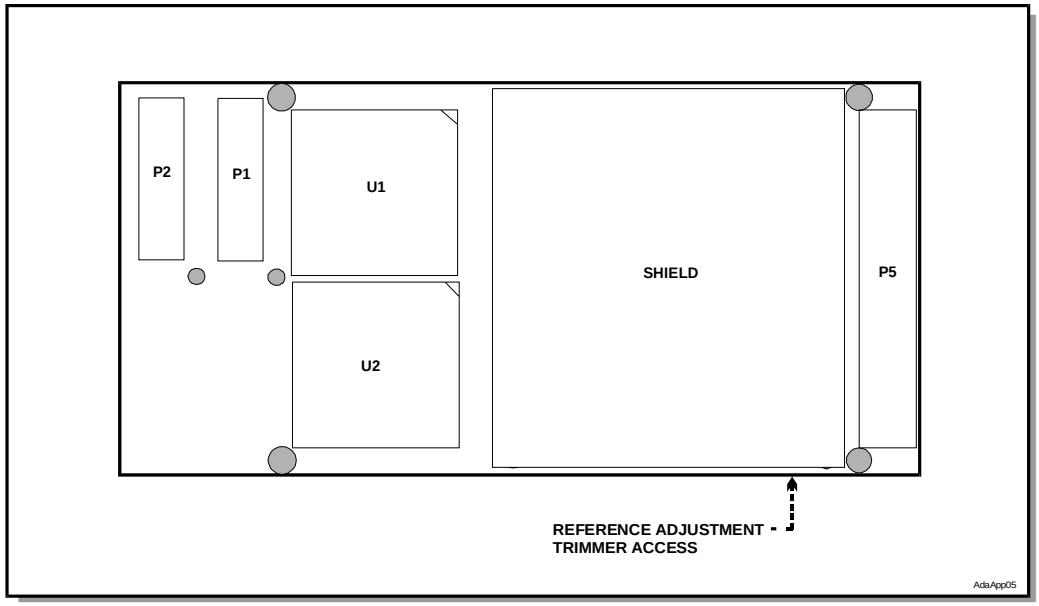

Figure 2.6.2-1. Range Reference Internal Adjustment Access

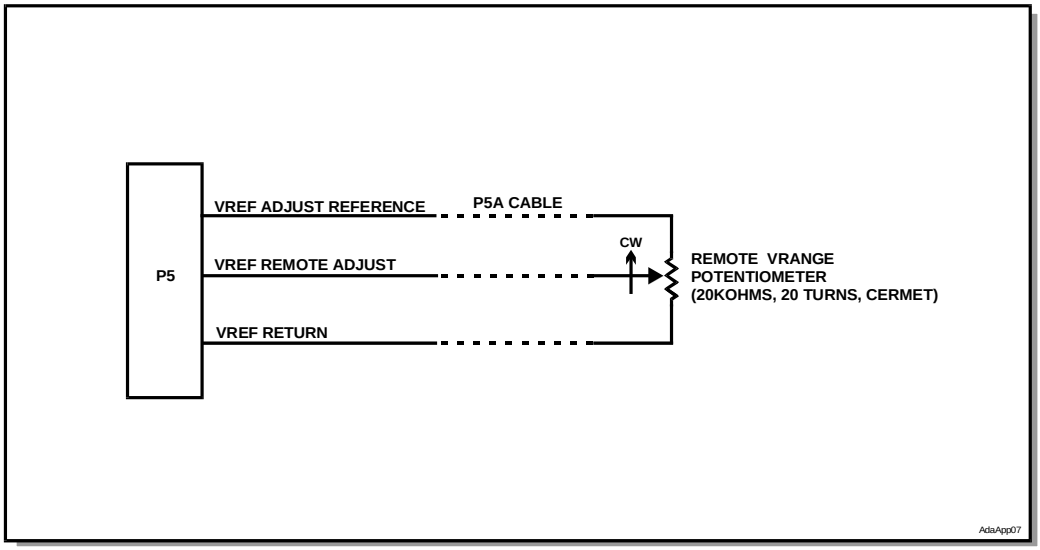

Figure 2.6.2-2. Vrange Remote Adjustment

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PMC-ADADIO board is compatible with the PCI Local Bus specification and supports "plug-n-play" autoconfiguration at the time of power-up. The PCI interface is controlled by a PLX™ PCI-9080 I/O accelerator device. Configuration-space registers are initialized internally to support the location of the board on any eight-longword boundary in memory space.

After initialization has been completed, communication between the PCI bus and the board takes place through the control and data registers shown in Table 3.1-1. All data transfers are long-word D32. Any one of the predefined operational conditions identified throughout this section can invoke a single interrupt request from the board.

Table 3.1-1. Control and Data Registers

RELATIVE ADDRESS	REGISTER *	ACCESS MODE	DESCRIPTION
00	BOARD CONTROL	Read/Write	Board Control Register (BCR)
04	DIGITAL I/O PORT	Read/Write	Byte-wide digital I/O port
08	ANALOG OUTPUT CHAN 00	Read/Write	Analog output (D/A) data input to board
0C	ANALOG OUTPUT CHAN 01	Read/Write	
10	ANALOG OUTPUT CHAN 02	Read/Write	
14	ANALOG OUTPUT CHAN 03	Read/Write	
18	ANALOG INPUT DATA	Read Only	Analog input (A/D) data from board
1C	SAMPLE RATE	Read/Write	---

* All registers are D32.

3.2 Board Control Register

The BCR controls all board functions except those associated with the bidirectional digital port. As Table 3.2-1 indicates, the BCR consists of 32 control bits and status flags, the upper five control bits (D31:27) of which are cleared automatically after the associated operations have been completed. Control and monitoring functions of the BCR are described in detail throughout the remainder of this section. The BCR initializes to the value 0413 87C1h.

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRYs. Configuration operations are executed in the sequence shown in Table 3.3.1-1.

Table 3.2-1. Board Control Register

DATA BIT	MODE	DESIGNATION	DESCRIPTION
D00	R/W	AIM0	Analog input mode. Selects single-ended or differential input configuration, or a selftest operational mode. Defaults to single-ended burst mode.
D01	R/W	AIM1	
D02	R/W	AIM2	
D03	R/W	LBC0	Loopback channel. Selects one of four analog output channels for loopback testing. Defaults to Channel-0.
D04	R/W	LBC1	
D05	RO	CAL STATUS FLAG	Records the status of autocalibration. LOW for pass, HIGH for fail. Initializes LOW.
D06	R/W	OFFSET BINARY	Selects offset binary analog input/output data format when asserted HIGH; two's complement when LOW. Defaults to offset binary format.
D07	R/W	SIZE0	Determines the size of the active analog input buffer. Defaults to the value Fh (maximum size).
D08	R/W	SIZE1	
D09	R/W	SIZE2	
D10	R/W	SIZE3	
D11	R/W	BUFFER CLEAR	Clears and disables the input buffer when HIGH. Defaults LOW. **Note**: Does not clear automatically.
D12-14	R/W	(Reserved)	Default to zero-state.
D15	R/W	LAST0	Establishes the number of active analog input channels. Defaults to a value of 7 (8 channels).
D16	R/W	LAST1	
D17	R/W	LAST2	
D18	R/W	ENABLE OUTPUTS	Connects the analog outputs to the I/O connector. Defaults to outputs-disconnected.
D19	R/W	ENABLE OUTPUT STROBE	Enables the internal/external analog output strobe. Disables automatic updating of outputs. Defaults to output strobe disabled.
D20	RO	INPUT BUFFER EMPTY	Analog input buffer status flags. Initialize to empty.
D21	RO	INPUT BUFFER HALF FULL	
D22	RO	INPUT BUFFER FULL	
D23	R/W	INTERRUPT A0	Interrupt source selection. Default is zero.
D24	R/W	INTERRUPT A1	
D25	R/W	INTERRUPT A2	
D26	R/W	INTERRUPT REQUEST FLAG	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.
D27	R/W	*CM0	Calibration mode. Selects either normal operation or a calibration mode. Defaults to normal operation.
D28	R/W	*CM1	
D29	R/W	*OUTPUT STROBE	Analog output software strobe
D30	R/W	*INPUT TRIGGER	Analog input internal (software) trigger. Initiates a single conversion of all active analog input channels. Active only in burst input modes, as selected by AIM2-0.
D31	R/W	*INITIALIZE	Initializes the board. Sets all defaults.

* Cleared automatically when operation is completed. R/W = Read/Write; RO=Read-Only.

Table 3.3.1-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

Board configuration terminates with the PCI interrupts disabled. Attempts to access the local bus during configuration should be avoided until the PCI interrupts are enabled and the initialization-complete interrupt request is asserted as described in Section 3.9.

3.3.2 Initialization

Internal control logic can be initialized without invoking configuration by setting the INITIALIZE control bit in the BCR. This action causes the internal logic to be initialized, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following conditions:

- Calibration D/A converters are initialized with values from internal EEprom
- The analog input buffer is reset to empty
- The local interrupt request is asserted (See Paragraph 3.9)
- The BCR is initialized; all defaults are invoked.

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

Loading of the PCI configuration registers is completed within 3 milliseconds or less after the assertion of a PCI bus reset, and should be required only once after the initial application of power. During this interval, the response to PCI target accesses is RETRYs. PCI register configuration terminates with the PCI interrupts disabled (Paragraph 3.9).

3.4 Analog Inputs

All active input channels are sampled simultaneously at the beginning of each conversion cycle, and the digitized values representing a selected group of *active channels* (Section 3.4.3) are transferred to the analog input buffer as a *conversion sample*. Each conversion sample commences with Channel-0, and proceeds in ascending order through all active channels. Table 3.4-1 describes the analog input data structure. Data formats are described further in Section 3.10.

Table 3.4-1. Analog Input Data

REG BIT	*MODE	DESCRIPTION
D00	RO	Least significant data Bit (LSB)
D01-D14	RO	Intermediate data Bits
D15	RO	Most Significant data bit (MSB)
D16-D31	RO	Extended sign in two's complement mode; all zero in offset binary mode.

* "RO" indicates read-only.

Configuration of the analog input networks is controlled by the BCR control bits designated as AIM[2:0], which are summarized in Table 6-4-2. The analog input selection arranges the input channels in either single-ended or differential configuration during normal operation, and establishes either a continuous or burst sampling mode. (The convention of "X:Y" indicating "the range from X down to Y" is used throughout this section).

Table 3.4-2. Analog Input Mode Selection

AIM[2:0]	FUNCTION OR MODE
0	Single-ended analog input configuration. Continuous conversion mode.
1	Single-ended analog input configuration. Burst mode (single conversion of all active input channels). Default state.
2	Differential analog input configuration. Continuous conversion mode.
3	Differential analog input configuration. Burst mode.
4	Loopback Selftest: The analog output channel selected by LBC[1:0] is connected to all analog input channels. Burst mode.
5	+VREF test. Internal voltage reference is connected to all analog input channels. Burst mode.
6	(reserved)
7	ZERO test. Internal ground reference is connected to all analog input channels. Burst mode.

In the continuous sampling modes, all active inputs are sampled continuously at the rate defined by RATE[3:0]. A burst sample consists of a single conversion of the active channels, and is initiated either by a software trigger or by an external hardware trigger. The default condition after initialization is the burst-sampling mode with single-ended inputs. Control bits AIM[2:0] also permit the board to be configured in any of several selftest modes for system level verification of operational integrity. Selftest operating modes are described in Section 3.5.

3.4.1 Continuous Input Sampling

Input sampling modes are selected with AIM[2:0] = 0, 1, 2 or 3. A sample consists of the digitized values of all active channels. Sampling rates can be adjusted from 305 SPS to 200 KSPS (100 KSPS with the 100 KSPS option).

In the continuous sampling modes, sampling occurs at the rate determined by the SAMPLE RATE control register (Table 3.4.1-1), according to the relationship:

Rs (Samples per Second) = 20,000,000 / Nrate ,

where Nrate is the decimal equivalent of the value in the SAMPLE RATE control register. Table 3.4.1-2 illustrates the effect of the Sample Rate control register on the sample rate. Nrate values less than 100 (64h) for the 200 KSPS option, or 200 (C8h) for the 100 KSPS option, may produce unpredictable results, and are not recommended.

The selected rate applies to all active channels simultaneously, and the total throughput in channels-per-second equals the sample rate times the number of active channels. The

SAMPLE RATE control register has no effect during autocalibration, nor when the board is operating in any of the burst sampling modes.

Table 3.4.1-1. Sample Rate Control Register

DATA BIT	MODE	DESIGNATION	DESCRIPTION
D00	R/W	**RATE00**	Least significant rate bit
D01-D14	R/W	**RATE01 - RATE14**	Intermediate rate bits
D15	R/W	**RATE15**	Most significant rate bit
D16-D31	*R/W	**---**	(Inactive)

* Active in write-mode only. Read-access retrieves all-zero.

Table 3.4.1-2. Sample Rate Selection

Nrate (RATE[15..0])		SAMPLE RATE Rs *
(Dec)	(Hex)	(Samples per Second)
100	0064	200,000 **
101	0065	198,020 **
200	00C8	100,000
201	00C9	99,502
---	---	Rs (Hz) = 20,000,000 / Nrate
---	---	
---	---	
65534	FFFE	305.19
65535	FFFF	305.18

* ±0.015 percent. ** With 200 KSPS option.

3.4.2 Burst Triggering

In the burst sampling modes, a single sample is initiated by setting the software trigger control bit (BURST TRIGGER) in the BCR. A conversion occurs immediately, and the BURST TRIGGER bit is cleared automatically when the sample has been completed and the board is ready to accept a subsequent trigger. A burst can be initiated also by a HIGH-to-LOW transition of the external hardware trigger (INPUT TRIGGER). An external output flag (INPUT TRIGGER READY) indicates to the external trigger source that the board is ready to accept a trigger. The external trigger, when asserted, must remain LOW for a minumum duration of 0.5 microsecond.

The software and hardware triggers both are edge-detected, and are ignored if asserted while a conversion is in progress. Completion of a conversion can be detected by selecting the Burst-Complete interrupt condition, and by then waiting for the associated interrupt request. External trigger sources can use the INPUT TRIGGER READY flag to avoid generating a trigger during a conversion.

3.4.3 Active Channels

Although all analog input channels are sampled simultaneously, only the conversion values for those channels designated as active by BCR control bits LAST[2:0] are written to the analog input buffer. Active channels are designated as shown in Table 3.4.3-1.

Table 3.4.3-1. Designation of Active Channels.

LAST[2:0]	ACTIVE CHANNELS
0	00
1	00-01
2	00-02
3	00-03
4	00-04
5	00-05
6	00-06
7	00-07

3.4.4 Analog Input Buffer

The analog input buffer has a physical capacity of 32,768 (8000h) 16-bit conversion values, and can be configured with a virtual size from a single data value up to the full physical buffer size. BCR control bits SIZE [3:0] adjust the size of the virtual buffer, as shown in Table 3.4.4-1. Operation is supported with buffer-empty, buffer half-full and buffer-full flags in the BCR, and with corresponding conditions available for an interrupt request. The buffer flags respond to the condition of the *virtual buffer*, not the physical buffer. Reading an empty buffer extracts the last value written to the buffer from the A/D converters. Setting the BUFFER CLEAR control bit HIGH in the BCR clears and disables the input buffer ***(This bit does not clear automatically***).

A full input buffer accepts no further input data, but all values acquired before the full condition occurred are retained in the A/D converters. The A/D conversion process is halted while the buffer is full, but values from the most recent conversion are moved into the buffer in consecutive order as buffer space becomes available. This arrangement retains the established channel order, regardless of the condition of the buffer.

Table 3.4.4-1. Virtual Buffer Size

SIZE[3:0]	BUFFER SIZE (Data Values)
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512
A	1024
B	2048
C	4096
D	8192
E	16384
F	32768

3.4.5 Multiboard Synchronization

Multiple boards can be synchronized to perform A/D conversions in 'lock-step' by connecting the INPUT TRIGGER READY output from one board, designated as the sync-initiator, to the INPUT TRIGGER inputs of a group of boards designated as sync-targets. The sync-targets are operated in the burst-sampling mode, and sample their respective active channels each time the sync-host performs a conversion. The initiator can be operated either in the continuous sampling mode or in the burst mode. If the initiator is operated in the burst-sampling mode, the triggers must not occur at a rate higher than the maximum sample rate specified for the board.

3.5 Selftest Configurations

Three selftest configurations are selectable with AIM[2:0], as shown in Table 3.4-2. In all selftest modes, analog inputs from the system input/output connector are disconnected and have no effect on board response. Analog outputs also can be disconnected from the system connector by clearing the ENABLE OUTPUTS control bit in the BCR.

Burst sampling is selected automatically in all selftest operating modes. To minimize the effects of noise, each selftest measurement should be acquired as an averaged value determined from at least sixteen samples.

3.5.1 Loopback Testing

When the loopback mode is selected (AIM[2:0] = 4), one of the four analog output channels is connected as a test channel to all analog input channels. The analog output test channel is selected by LBC[2:0] in the BCR, as shown in Table 3.5.1-1. Field inputs are disconnected while the board is in any selftest mode.

Table 3.5.1-1. Loopback Test Channel Selection

LBC[1:0]	FUNCTION
0	Analog Output Channel 00; Default state.
1	Analog Output Channel 01
2	Analog Output Channel 02
3	Analog Output Channel 03

The loopback mode can be used to verify the integrity of the analog input and output channels by writing specific values to each output channel, and by then verifying the accuracy of the responses measured through the analog input channels. The errors encountered during loopback testing will include the errors present in both the input and output test channels.

3.5.2 Positive Reference Selftest

When AIM[2:0] = 5, the internal precision voltage reference that is used during autocalibration is connected to all analog input channels. The voltage reference equals 0.99902 times the positive full scale value for the board (e.g.: +9.9902 Volts for the ±5V range). The nominal response for this input level is FFE0h in offset binary format.

3.5.3 Zero Input Selftest

When AIM[2:0] = 7, all analog input channels are connected to internal signal ground, which corresponds to zero-input level, or midrange. The nominal response for this input level is 8000h in offset binary format.

3.6 Analog Outputs

Writing a 16-bit value to the corresponding analog output data register (Table 3.1-1) controls each analog output channel. The output value can be formatted either in offset binary format or in two's complement format, as selected by the OFFSET BINARY control bit in the BCR. Table 3.6-1 describes the arrangement of data bits in the analog output data registers. Data formats are described further in Section 3.10.

Table 3.6-1. Analog Output Data Registers

REG BIT	MODE *	DESCRIPTION
D00	R/W	Least significant Bit (LSB)
D01-D14	R/W	Intermediate Bits
D15	R/W	Most Significant bit (MSB)
D16-D31	---	Inactive

* Active in write-mode only. Read-access retrieves all-zero.

3.6.1 Analog Output Strobe

The analog output channels can be controlled in either of two strobing modes. If the ENABLE OUTPUT STROBE software strobe control bit in the BCR is LOW (default), output strobing is disabled and each output register value is transferred directly to the associated output channel after a short serialization delay. If ENABLE OUTPUT STROBE is asserted HIGH, strobing is enabled and output register values are held in an intermediate output buffer until either the software OUTPUT STROBE control bit in the BCR is asserted HIGH, or the external hardware strobe undergoes a HIGH-to-LOW transition.

Assertion of either the software strobe HIGH or the hardware strobe LOW causes all values in the output buffer to be transferred immediately to their associated output channels. If multiple values are written to a single channel, only the last value received before the strobe occurs is transferred to the output channel. The software OUTPUT STROBE is cleared automatically after the outputs have been updated.

3.6.2 Analog Outputs Disconnect

The analog outputs are connected to the system I/O connector when the ENABLE OUTPUTS control bit is asserted HIGH. For applications in which driven devices must not be exposed to the voltage excursions present at the analog outputs during selftest operations, the analog outputs can be disconnected from the system I/O connector by clearing the ENABLE OUTPUTS control bit in the BCR. The analog outputs default to the disabled state (control bit LOW) after initialization and during autocalibration.

Disconnectable outputs also permit the board to be used in multiple-redundancy applications by connecting the outputs of two or more boards together, and by enabling only one board in the redundancy set.

3.7 Calibration Modes

Calibration functions are controlled by control bits CM[1:0] in the BCR, and are summarized in Table 3.7-1. In the default Normal Operation mode, selected with CM[1:0] = 0, all board functions respond to BCR control bits as described throughout this section. For nonzero values of CM[1:0], BCR control functions are preempted as necessary to implement the selected calibration operation.

The analog input buffer is reset to empty at the beginning of each calibration operation initiated by cm[1:0]. When the selected operation has been completed, CM[1:0] bits are automatically cleared to the default "0" state, and the single-ended burst sampling input mode is selected. To clear calibration data from the analog input buffer, the board should be initialized before resuming normal operation.

Table 3.7-1. Calibration Mode Selection

CM[1:0]	FUNCTION
0	Normal operation. No calibration activity. Default state.
1	Load calibration DAC's from EEprom. Performed automatically during initialization.
2	Invoke Autocalibration
3	(Reserved)

3.7.1 Loading Calibration DAC's

Setting CM[1:0] = 1 causes the calibration values stored in internal EEprom to be transferred to the calibration DAC's. The duration of the transfer is approximately 2 milliseconds. This operation occurs automatically during initialization.

3.7.2 Autocalibration

Calibration correction values for analog input and output channels are stored in nonvolatile EEprom, which retains the correction values when power is removed. The calibration values are transferred to volatile storage in calibration DAC's after power is applied.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the new values in both the EEprom and the calibration DAC's. Autocalibration can be invoked at any time, but should not be implemented while the system is experiencing a major environmental transition such as that which usually occurs directly after power is applied. Analog outputs are disabled during autocalibration.

Autocalibration is invoked by writing a value of "2" to CM[1:0], and has a duration of approximately 7-10 seconds. Completion of the operation can be detected by selecting the 'calibration-mode operation completed' interrupt condition and waiting for the interrupt request. Write-accesses from the PCI bus should be avoided during autocalibration. A

If a board is defective, the autocalibration process may be unable to successfully calibrate all input and output channels. If this situation occurs, the CAL STATUS FLAG bit in the BCR will be set HIGH at the end of the autocalibration interval, and will remain HIGH until a subsequent initialization occurs.

Note: Each autocalibration should be followed by initialization, in order to clear the contents of the analog input buffer and to restore the normal context of the sample rate control register (See Paragraph 3.12). All control registers can then be returned to their normal operational states.

3.8 Bidirectional Digital Port

The digital port is controlled by the Digital I/O Port register, and provides 8 bits of bidirectional input/output digital data, a dedicated output control bit and a dedicated input status bit, as shown in Table 3.8-1. The I/O DATA DIRECTION control bit establishes the direction of the eight bidirectional data bits, which are configured as outputs if the control bit is HIGH, or as inputs if the control bit is LOW. The dedicated input and output control bits are not affected by the direction control bit. Functions of all bits in this port are determined entirely by specific system requirements.

Table 3.8-1. Digital I/O Port Register

REG BIT	MODE	DESIGNATION	DESCRIPTION
D00	R/W	I/O DATA 00	Bidirectional digital I/O lines
D01	R/W	I/O DATA 01	
D02	R/W	I/O DATA 02	
D03	R/W	I/O DATA 03	
D04	R/W	I/O DATA 04	
D05	R/W	I/O DATA 05	
D06	R/W	I/O DATA 06	
D07	R/W	I/O DATA 07	
D08	RO	I/O CONTROL INPUT	I/O port dedicated input line
D09	R/W	I/O CONTROL OUTPUT	I/O port dedicated output line
D10	R/W	I/O DATA DIRECTION	HIGH => I/O DATA XX lines are outputs LOW => I/O DATA XX lines are inputs
D11-D31	---	(Reserved)	Inactive

3.9 Interrupt Control

In order for the board to generate a PCI interrupt, *both* of the following conditions must occur:

a. The board's internal controller must generate a Local Interrupt Request
b. The *PCI interrupt* must be enabled.

If the internal controller generates a local interrupt request, a PCI bus interrupt will not occur unless the PCI interrupt has been enabled as described in Paragraph 3.9.2.

To avoid interrupt conflicts, the PCI interrupt should be enabled only when it is necessary for operation of the board.

3.9.1 Local Interrupt Request

The single local interrupt request line is controlled by the INTERRUPT A[2:0] and INTERRUPT REQUEST FLAG control bits in the BCR. The source condition for the request is selected as shown in Table 3.9.1-1. When the selected condition occurs, a local interrupt request is generated and the INTERRUPT REQUEST FLAG bit is set in the BCR. The request remains asserted until the PCI bus clears the BCR request flag. A local interrupt request is generated automatically at the end of initialization.

Table 3.9.1-1. Interrupt Source Selection

INTERRUPT A[2:0]	INTERRUPT CONDITION
0	Idle. Interrupt disabled unless initializing. Default state.
1	Calibration-mode operation completed
2	Analog input active buffer empty
3	Analog input active buffer half full
4	Analog input active buffer full
5	*Analog input burst completed
6	Analog output strobe completed
7	(Reserved).

* Single conversion, all active channels.

Detection of an interrupt condition or event is *edge-sensitive*. An interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

3.9.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *PCI Local Interrupt Enable* control bits HIGH in the runtime *Interrupt Control/Status Register* described in Section 4 of the PLX^{TM} PCI-9080 reference manual..

3.10 Data Formats

Both analog input data and analog output data can be represented either in 16-bit offset binary format by asserting the OFFSET BINARY control bit HIGH in the BCR, or in two's complement format by clearing the control bit LOW. As Table 3.10-1 indicates, analog data input and output transactions are D32 (32-bit), but the data significance is 16 bits. In two's complement mode, the sign-bit of negative analog input values is extended through the most significant bit of the D32 register. Data bits D16 through D31 are ignored in analog output values.

Table 3.10-1. Analog Input/Output Data Coding

ANALOG INPUT OR OUTPUT LEVEL	DIGITAL VALUE (Hex)	
	OFFSET BINARY	TWO'S COMPLEMENT
Positive Full Scale minus 1 LSB	0000 FFFF	0000 7FFF
Zero plus 1 LSB	0000 8001	0000 0001
Zero	0000 8000	0000 0000
Zero minus 1 LSB	0000 7FFF	FFFF FFFF
Negative Full Scale plus 1 LSB	0000 0001	FFFF 8001
Negative Full Scale	0000 0000	FFFF 8000

Positive Full Scale is a positive level that equals the range option defined for the board (e.g.: +5.000 Volts for the ±5V option). *Negative Full Scale* is the negative equivalent of positive full-scale. *Full-scale Range* (FSR*)* is the total voltage range for the input or output. One LSB equals the full-scale range divided by 65,536. (e.g.: 152.59 microvolts for the ±5V option).

3.11 DMA Operation

DMA transfers from the analog input buffer are supported with the board operating as bus master in either of two DMA channels. Table 3.11-1 illustrates a typical PCI register configuration that controls a non-chaining, non-incrementing '***block-mode'*** DMA transfer, in which a PCI interrupt is generated when the transfer has been completed. Bit 02 (0000 0004h) in the PCI Command register must be set HIGH to select the bus mastering mode. Refer to a PCI-9080 reference manual for a detailed description of these registers.

Table 3.11-1. Typical DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

For most applications, the DMA Command Status register would be initialized to the value 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Bit-12 (0000 1000h) in the Channel-0 DMA Mode configuration register, when HIGH, selects ***'demand-mode'*** DMA operation, in which a DMA transfer is requested automatically when the number of values in the buffer ***equals or exceeds half of the selected virtual buffer size*** *(Table 3.4.4-1).*

The DMA request is sustained until one of the following events occurs:

(a) The data buffer goes empty,
(b) The number of values read from the buffer equals one-half the virtual buffer size,
(c) The buffer is cleared,
(d) The board is reset,
(e) Autocalibration is executed.

The first occurrence of any of these events terminates the DMA request.

NOTE: Demand-mode DMA is available only with ADADIO products that have a firmware revision value between 0x0001 8000 and 0x0001 8FFF (Paragraph 3.12).

3.12 Board Revision Register

The board revision register (Table 3.12-1) contains the existing firmware revision, and a status bit that indicates the availability of demand-mode DMA operation.

Table 3.12-1. Board Revision Register

REG BIT	MODE *	DESCRIPTION
D00-D16	RO	Firmware Revision
D17-D31	RO	(Reserved)

* RO = Read-only.

To access the board revision register:

(a) Perform autocalibration (paragraph 3.7). Wait for autocal completion,

(b) Read the board revision register at the location of the sample rate register (001Ch),

(c) To restore normal readback of the sample rate register, initialize the board through the BCR (Paragraph 3.3.2).

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

The PMC-ADADIO board contains eight 16-Bit A/D converters (ADC's), four 16-bit D/A converters (DAC's), and all supporting functions necessary for adding analog I/O capability to a PMC host. As Figure 4.1-1 illustrates, a PCI interface adapter provides an interface between the controlling PCI bus and an internal local controller through a 32-bit local bus. The local controller performs all internal configuration and data manipulation functions, including autocalibration.

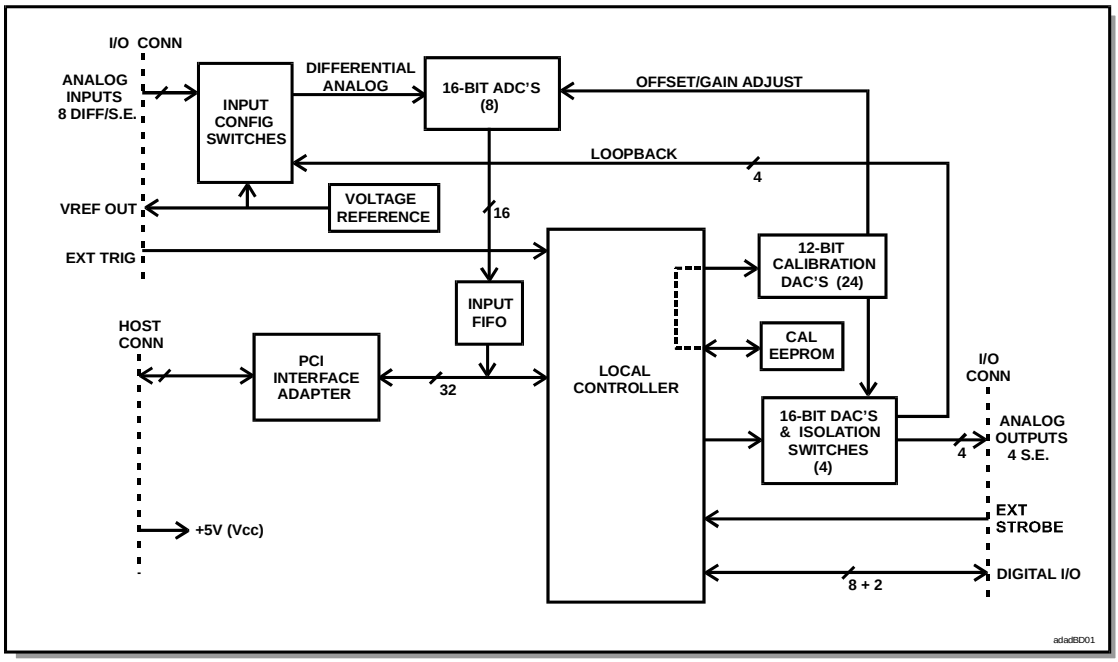

Figure 4.1-1. Functional Block Diagram

Input configuration switches allow the controller to select any of several signal sources as differential inputs to the ADC's. This feature is used to establish the internal connections necessary during autocalibration, and also permits verification from the PCI bus of the integrity of all analog input and output channels. All channels are calibrated against a single precision voltage reference.

Analog output channels are equipped with isolation switches that permit the outputs to be disconnected from the system I/O connector, either upon demand from the PCI bus, or automatically during autocalibration.

The offset and gain calibration of each input and output channel is adjusted with a pair of 12-bit Calibration DAC's, the control values for which are stored in nonvolatile electrically-erasable programmable read-only memory (EEprom). The EEprom and calibration DAC's provide the adjustment functions that would be associated with 24 trimpots in conventional analog configurations. Calibration control values are determined and stored in EEprom during autocalibration.

4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the input configuration switches shown in Figure 4.1-1. During normal operation, the analog input channels from the input/output connector are sampled and digitized simultaneously, and then are written sequentially to the input FIFO buffer. For selftest and autocalibration operations, the internal voltage reference can be routed through the switches to the ADC's, or the analog output channels can be monitored by selecting the loopback selftest mode. The configuration switches also establish the input configuration as either single-ended or differential, in response to software control.

The selected input signals pass through differential input amplifiers to eliminate common mode input voltages, and subsequently are digitized by the 16-bit ADC's. By routing all inputs through the same signal path, the errors introduced by components in that path are accounted for during autocalibration. Offset and gain trimming of each ADC is provided by a pair of 12-bit DAC's which are loaded with trim values that are determined during autocalibration.

During normal continuous input operation, the analog input sampling rate is adjusted in response to a 16-bit code from the PCI bus. All inputs are sampled simultaneously. The number of channels that are written to the input buffer is determined by a 3-bit code from the bus, which selects from one to eight channels to be placed in the buffer. Although the physical size of the buffer is 32K samples, the size of the virtual buffer that is accessible from the PCI bus is adjustable from 1 sample to 32K samples by a 4-bit code from the bus.

4.3 Analog Outputs

Each of the four analog output channels consists of a 16-bit output DAC and two 12-bit calibration DAC's. The local controller reads the 16-bit channel data for each channel from the associated analog output data register, and sends the data serially to the appropriate output DAC. The output DAC deserializes the data to obtain the original 16-bit data word, and holds that word in an internal buffer until commanded to transfer the data to the output register that drives the DAC conversion ladder. If the control software selects output strobing, the transfer command is generated either by a software flag or by the external hardware strobe. If output strobing is not selected, the transfer command is generated automatically by the local controller immediately after the serial data word is sent to the output DAC.

The two calibration DAC's in each output channel provide offset and gain trimming of the associated 16-bit output DAC, using trim values that are determined during autocalibration.

Each analog output channel contains a switching network that disables the output by disconnecting the output DAC from the system I/O connector, either upon demand from the PCI bus, or automatically during autocalibration. All output channels are enabled or disabled simultaneously.

4.4 Digital I/O port

Eight bits of bidirectional input/output digital data, and a pair of dedicated input and output control bits, are provided by the digital I/O port. The bidirectional data is configurable as an input or output byte by the bus. This port is intended to provide general-purpose command/status capability, and is not designed for high-speed communication over long cables. Signal return for the I/O port is connected directly to the digital ground supplied by the PCI bus.

4.5 Autocalibration

Autocalibration is an embedded software utility which calibrates all input and output channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

The internal voltage reference is adjusted as described in Section 2 to equal approximately 99.9 percent of the input/output voltage range. This in-range value ensures that the ADC's will provide the nonsaturated, or in-range, responses that are necessary during the calibration adjustment process. The voltage reference is used by the autocalibration utility to calibrate the eight analog input channels, one of which is used subsequently to calibrate the four analog output channels.

Each of the 24 calibration DAC's is adjusted in a successive approximation sequence that commences with the DAC in an all-zero state. The most significant bit is set to "1", and the resulting effect on the channel is measured. Depending upon the measured response, the bit either is cleared or is left in the "1" state. The next lower significant bit is then tested in the same manner, and this process continues until all 12 bits have been tested and adjusted. The final value in the calibration DAC is stored in the nonvolatile calibration EEprom for subsequent retrieval by the local controller.

4.6 Power Control

Regulated supply voltages of ±5 Volts and ±13 Volts are required by the analog networks, and are derived from the +5-Volt input from the PCI bus through a DC/DC converter. To obtain optimum performance from the internal supplies, all analog power voltages are produced by series regulation of the DC/DC converter preregulated outputs.

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