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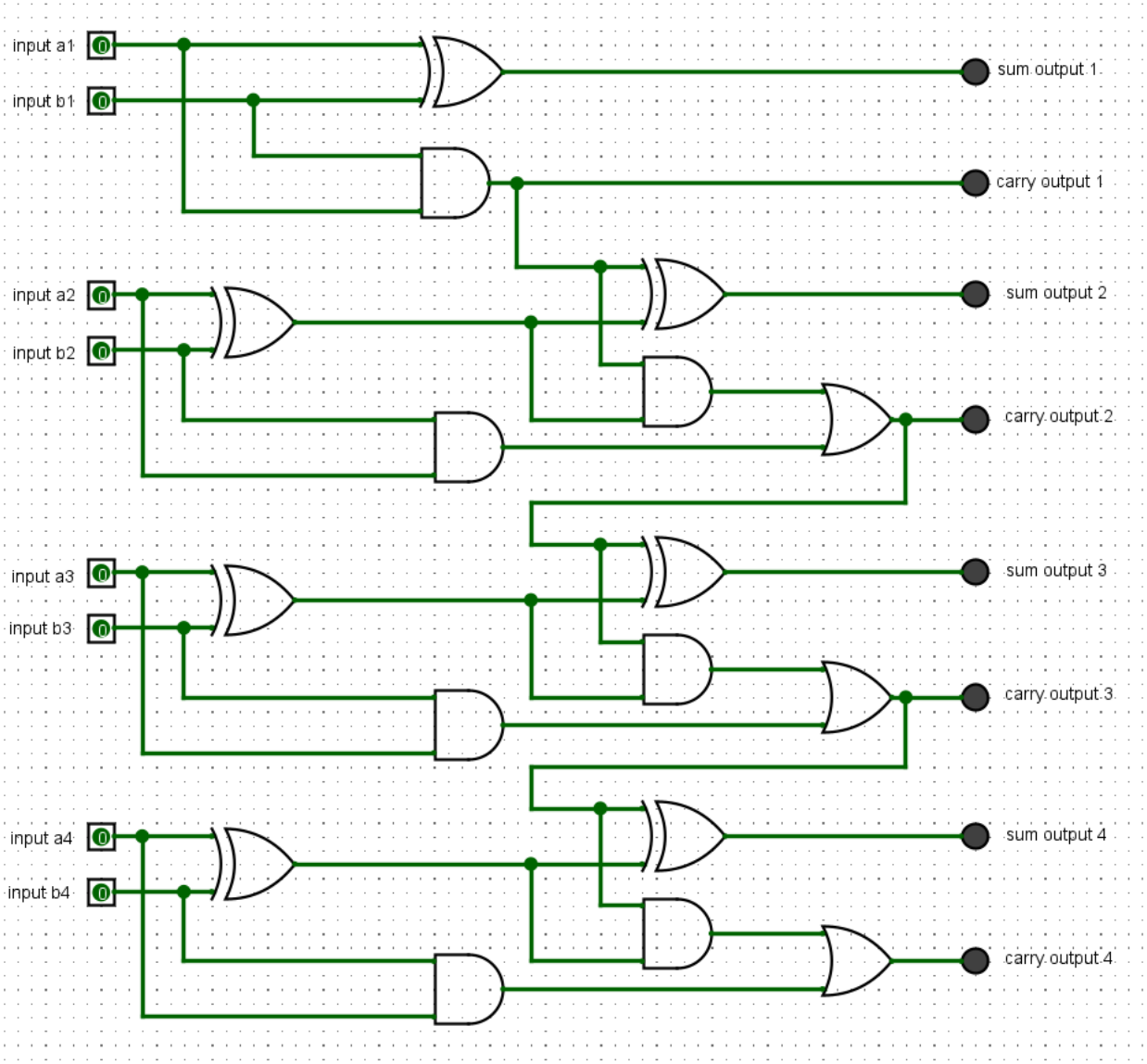
Lab 2

4-bit adder

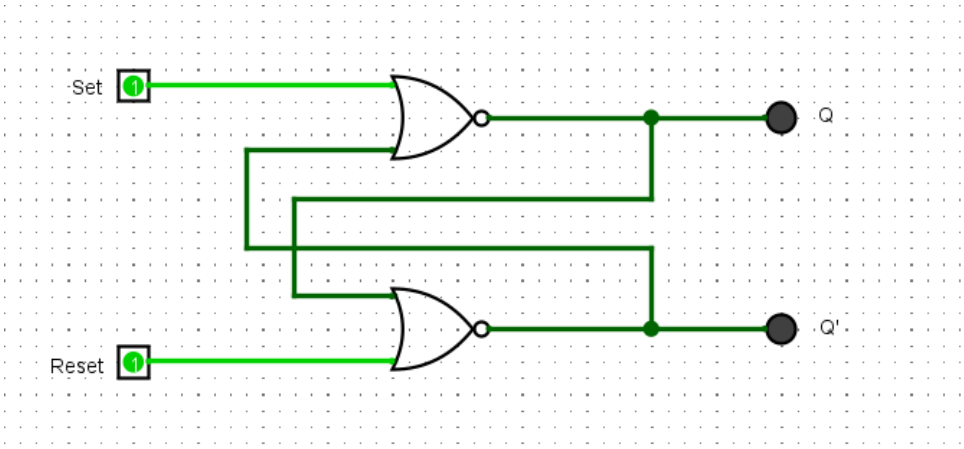


Input A	Input B	Output
0101	**0000**	**1100**
0101	**0001**	**1101**
0101	**0010**	**1101**

0101	**0011**	**1100**
0101	**0100**	**1110**
0101	**0101**	**1111**
0101	**0110**	**1111**
0101	**0111**	**1110**
0101	**1000**	**1110**
0101	**1001**	**1111**
0101	**1010**	**1111**
0101	**1011**	**1110**
0101	**1100**	**1101**
0101	**1101**	**1100**
0101	**1110**	**1100**
0101	**1111**	**1101**

Part 2: Storing bits with Flip Flops

R-S Flip Flop



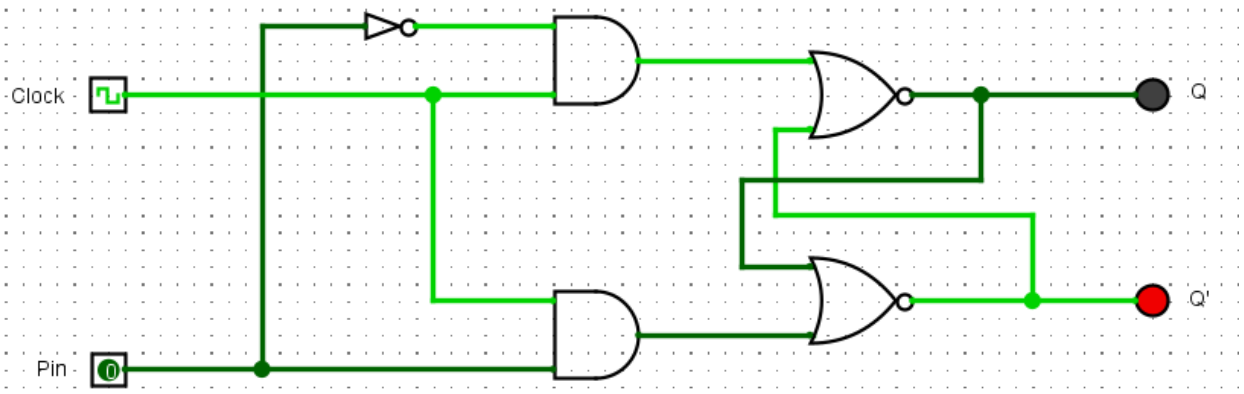
Set	**Reset**	**Q**	**Q'**

1	**0**	**0**	**1**
1	**1**	**0**	**0**
0	**1**	**1**	**0**
1	**1**	**0**	**0**

The R-S Flip Flop was built by linking 2 NOR gates as shown in the screenshot above. If we open the Set to 1 and close the Reset to 0, Q will turn off (0) and Q will turn on (1). If we open the Reset to 1 and close the Set to 0, Q will turn on (1) and Q' will turn off (0), as they have been reset.

If both inputs are set to 1, both LED lights will turn off (0). This is because they are going to an indeterminate state. This is an issue for digital circuit design because both inputs must not be active (pulled low) at the same time or else they will violate their own rule.

D Flip Flop



Clock	**Pin**	**Q**	**Q'**
0	**0**	**0**	**1**
0	**1**	**0**	**1**
1	**1**	**1**	**0**
1	**0**	**0**	**1**

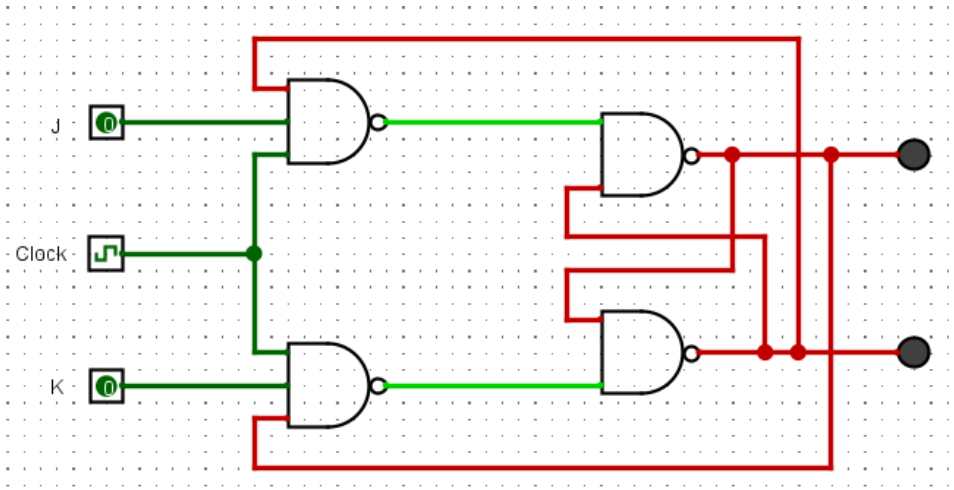
The D Flip Flop was built using a single data input and a clock to regulate the data signal. When the clock is on, Q is set to be inverted of D, and Q' is set to be the same state as D.

The clock is used to send a signal to the control signal. When the clock signal is LOW, the input

has no effect on the output. However, for the inputs to become active, the clock signal must be HIGH.

In RS Flip flop there are two inputs and both cannot be 1 simultaneously. This is eliminated in D by inverting R and S. The D, has only one input and output will be input whenever the clock signal appears. With Single input, the design process is comparatively easier.

J-K Flip Flop



J	K	Q (when clocked)	Q' (when clocked)
0	**0**	**No change**	
1	**0**	**1**	**0**
0	**1**	**0**	**1**
1	**1**	**Toggle**	

Conversion of J-K Flip-Flop into D Flip-Flop

1. Construct the characteristic table of D flip-flop and excitation table of JK flip-flop.

D	Qn	Qn + 1	J	K
0	0	0	0	x
0	1	0	x	1
1	0	1	1	x
1	1	1	x	0

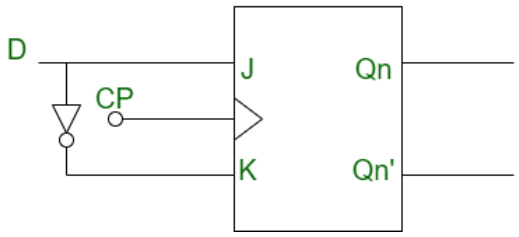
2. Using the K-map we find the boolean expression of J and K in terms of D.

D\Qn	0	1
0		x
1	1	x

D\Qn	0	1
0	x	1
1	x	

J = D
K = D’

3. Construct the circuit diagram of the conversion of JK flip-flop into D flip-flop.



Conversion of J-K Flip-Flop into T Flip-Flop

1. Construct the characteristic table of T flip-flop and excitation table of the J-K flip-flop.

D	Qn	Qn + 1	J	K
0	0	0	0	x
0	1	1	x	0
1	0	1	1	x
1	1	0	x	1

2. Using the K map, find the boolean expression for J and K in terms of T.

D\Qn	0	1
0		x

1	1	x

D\Qn	0	1
0	x	
1	x	1

J = T
K = T

3. Construct the circuit diagram for the conversion of the J-K flip-flop into a T flip-flop.