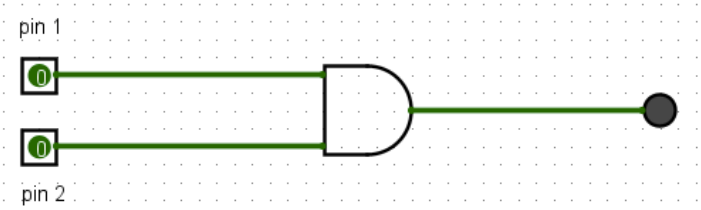
Trac Duc Anh Luong - 103488117

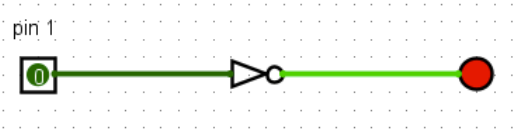
Lab 1: Gates

AND gate



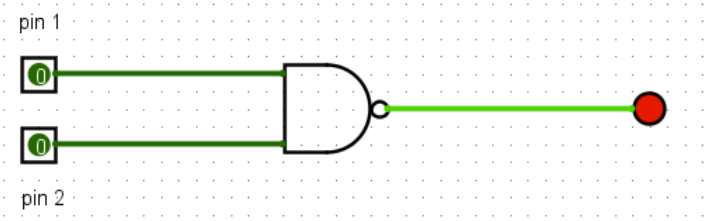
Pin 1	Pin 2	Output
1	1	1
1	0	0
0	1	0
0	0	0

NOT gate



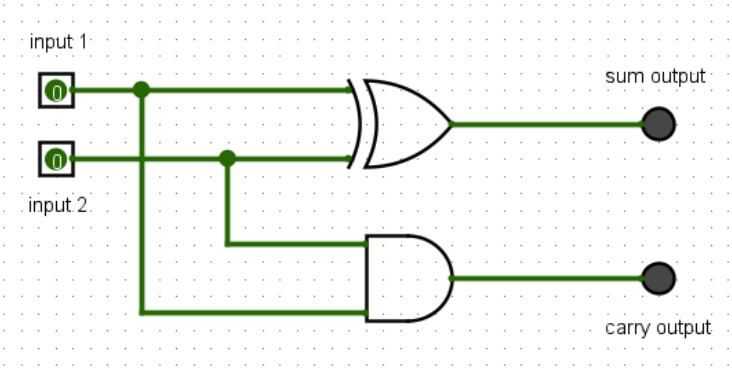
Pin 1	Output
1	0
0	1

NAND gate



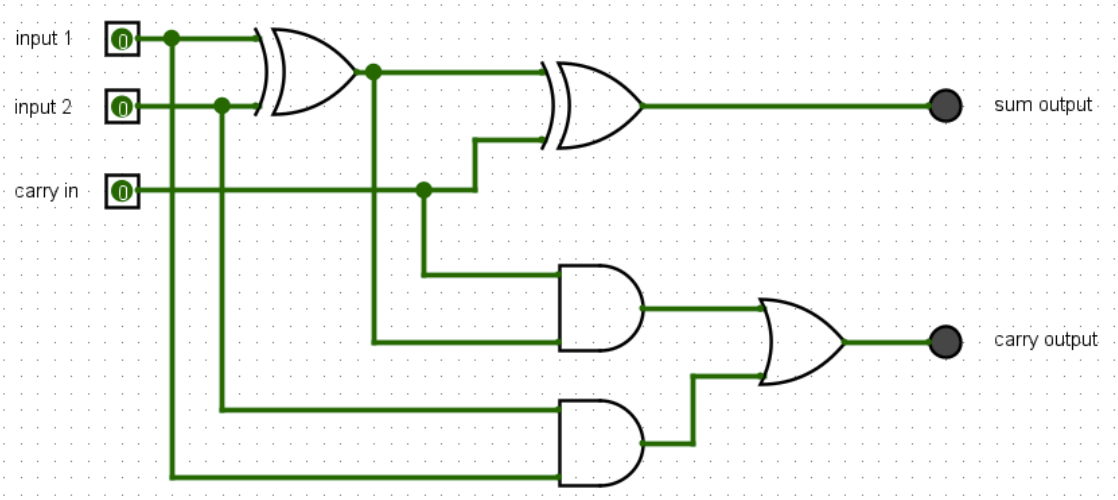
Pin 1	Pin 2	Output
1	1	0
1	0	1
0	1	1
0	0	1

Half adder



Input 1	Input 2	Sum Output	Carry Output
1	1	0	1
1	0	1	0
0	1	1	0
0	0	0	0

Full adder



Input 1	Input 2	Carry In	Sum Ouput	Carry Output
1	1	1	1	1
1	0	1	0	1
0	1	1	0	1
0	0	1	1	0
1	1	0	0	1
1	0	0	1	0
0	1	0	1	0
0	0	0	0	0