Post CMOS technologies: An Overview and Analysis

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ABSTRACT

The rapid evolution of computing is pushing the limits of traditional silicon-based electronics, necessitating the exploration of novel materials and architectural paradigms. This paper investigates three transformative technologies poised to redefine future computational systems: Carbon Nanotubes (CNTs), Spintronics, and Memristors. We explore how Carbon Nanotube Field-Effect Transistors (CNFETs) offer enhanced performance and energy efficiency by enabling scaling beyond conventional limits, exemplified by the development of sophisticated CNFET-based microprocessors. Concurrently, Spintronics, particularly through Magnetoelectric Spin-Orbit (MESO) devices, promises ultra-low power logic by leveraging electron spin, introducing innovative concepts like majority logic gates. Furthermore, we examine Memristors, which address the Von Neumann bottleneck by integrating memory and processing, facilitating advanced applications in neuromorphic and analog computing, as demonstrated by their use in artificial neural networks and threshold logic gates. While each technology presents unique challenges in fabrication and integration, their distinct advantages offer compelling pathways toward building faster, smaller, and more energy-efficient computing systems for the next generation. CMOS.

KEYWORDS

Do, Not, Us, This, Code, Put, the, Correct, Terms, for, Your, Paper

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1 INTRODUCTION

The pursuit of faster, smaller, and more energy-efficient computing has been a driving force for technological advancement since the creation of the transistor. For decades, CMOS (Complementary metal-oxide-semiconductor) technology has served as the foundation of of the modern computer. However, as we continue to approve our transistors and approach fundamental limits, the need for novel paradigms becomes increasinly urgent. This paper explores three technologies that could shape the future of computing: Carbon Nanotubes (CNTs), Spintronics, and Memristors. Each offers their own advantages that address the limitations of silicon transistors, varying from faster performance to significantly reduced power consumption.

Carbon Nanotubes, with their exceptional electrical and thermal properties, present a compelling alternative to silicon in field-effect transistors (FETs). The ability to scale devices beyond current limits, coupled with high carrier mobility and superior heat dissipation, positions Carbon Nanotube FETs (CNFETs) as a potential successor for high-performance, low-power logic. Recent advancements, such as the development of the RV16X-NANO microprocessor at MIT, demonstrate the practical viability of CNFET-based computing, showcasing their compatibility with existing design methodologies and their ability to execute complex instructions.

Beyond simply replacing silicon, Spintronics offers a revolutionary approach to information processing by leveraging the intrinsic spin of electrons in addition to their charge. Magnetoelectric Spin-Orbit (MESO) devices, a key development in spintronics, promise ultra-low power logic operations by directly coupling electron spin with its movement and enabling control through both electrical and magnetic properties. These devices offer superior switching energy, lower operating voltages, and enhanced logic density, with the potential to implement universal logic through majority gates, fundamentally transforming how logic functions are conceived and executed.

Finally, Memristors, often described as the "fourth fundamental circuit element," introduce a new dimension to computing by combining memory and processing capabilities within a single device. This integration directly addresses the Von Neumann bottleneck, the traditional separation of memory and logic that limits computational speed and efficiency. Memristor-based threshold logic gates and crossbar arrays hold immense promise for neuromorphic and analog computing, enabling highly efficient Vector-Matrix Multiplication (VMM) crucial for artificial neural networks. While challenges in manufacturing reliability and programmability persist, the ability of memristors to store multiple bits and their non-volatile nature offer a path toward more compact, power-efficient, and brain-inspired computing architectures.

This paper will delve into the principles, advancements, and challenges associated with each of these transformative technologies, highlighting their individual contributions and their collective potential to shape the next generation of computing systems.

2 CARBON NANOTUBES (CNTS) FOR ADVANCED ELECTRONICS

As the semiconductor continues its pursuit of miniaturization and greater performance, the fundamental limits of silicon-based transistors become increasingly apparent. This fundamental limit to the scaling of traditional transistors has given rise to many alternatives among them being Carbon Nanotubes (CNTs), one dimensional nanostructures that possess a unique combination of characteristics making them highly attractive for advancing electronics.

CNTs are composed of graphene sheets rolled into cylindrical tubes with their structure determining whether they behave as semiconductors or metals. his tunable electrical property, coupled with their nanoscale dimensions, high carrier mobility, and exceptional thermal conductivity, positions CNTs as a compelling material for high-performance computing. Their inherent flexibility also opens avenues for novel applications beyond traditional rigid electronics. This section will delve into the fundamental properties of CNTs, explore their application in Carbon Nanotube Field-Effect Transistors (CNFETs), highlight recent advancements that demonstrate their potential, and discuss the significant fabrication challenges that must be overcome for their widespread adoption.

2.1 Fundamental Properties of Carbon Nanotubes

Carbon nanotubes are made of an allotrope of carbon known as graphene.

Their structure can be characterized into to major types. Single-walled and multi-walled carbon nanotubes. Single-walled carbon nanotubes consist of a single graphene sheet rolled into a cylinder typically with a diameter between 0.5 to 2.0 nanometers. Multi-walled carbon nanotubes are comprised of multiple concentric graphene cylinders nested within each other. Their diameter can extend up to tens of nanometers.

The electrical properties can also vary depending on the structure and chirality (the angle at which the graphene sheet is rolled up) of the CNTs. This means that a CNT can behave either as metals with a high conductivity or semiconductors making them suitable for making transistors.

CNTs also have extremely high thermal conductivity making them suitable to overcome many of the power limitations of current CMOS scaling.

Finally, CNTs are among the strongest and stiffest materials known, possessing exceptional tensile strength and elastic modulus. Moreover, they are remarkably flexible, capable of withstanding considerable mechanical strain without fracturing. This flexibility is particularly advantageous for emerging flexible electronics and 3D integration.

2.2 Carbon Nanotube Field Effect Transistors (CNFETs)

The ability of semiconductor CNTs to conduct extremely effectively and their nanoscale dimensions make them ideal candidates for making the channel in field effect transistors. These properties allow CNFETs to offer several significant advantages over silicon based FETs:

- Aggressive Scaling: Their nanoscale dimensions allow for device scaling below the 5 nanometer limit.
- High Carrier Mobility: The ballistic or near-ballistic transport of carriers within CNTs leads to very high carrier mobility, which translates directly to faster switching speeds and improved device performance.
- Lower Power Consumption: CNFETs can operate effectively at lower voltages due to their superior electrical characteristics, resulting in significantly reduced power dissipation.
- Enhanced Gate Control: As one-dimensional materials, CNTs offer excellent electrostatic control by the gate, leading to lower off-state currents and steeper subthreshold swings.
- Superior Thermal Management: Their high thermal conductivity facilitates efficient heat dissipation, mitigating hot spots and improving reliability in densely packed circuits.
- Material Flexibility: The mechanical flexibility of CNTs enables the development of bendable electronics and facilitates potential three-dimensional chip stacking and integration, offering new avenues for compact and innovative designs.

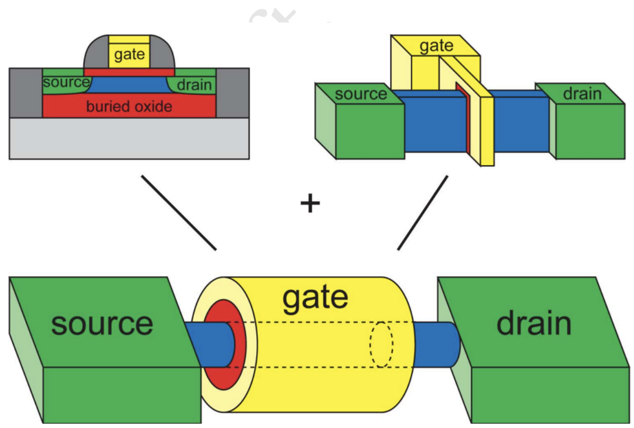

Figure 1: Diagram of CNFET as combination of MOSFET and FinFET

2.3 Logic Operations

Since CNFETs operate just like normal transistors their integration into creating logic gates is the exact same as a traditional transistor. They still follow CMOS architecture and their benefits come from their performance advantage compared to traditional transistors rather than new operating paradigms.

2.4 Recent Advancements: RV16X-NANO Microprocessor

The RV16X-NANO Microprocessor has been one of the biggest advancements in making a computer with CNFETs. The MIT Medical Electronic Device Realization Center were able to develop a 16 bit nanoprocessor which they named RV16X-NANO. The microprocessor was built of the RISC-V instruction set which was written through Bluespec and then compiled into Verilog, an RTL hardware description langauge. The microprocessor was comprised of over 14000 CMOS CNFETs that were made using more than 10 million CNTs.

On this microprocessor they were able to implement many standard logic blocks like multiplexers, arithmetic logic units, decoders, and encoders. Most notably, they were able to execute the famous "Hello World" program.

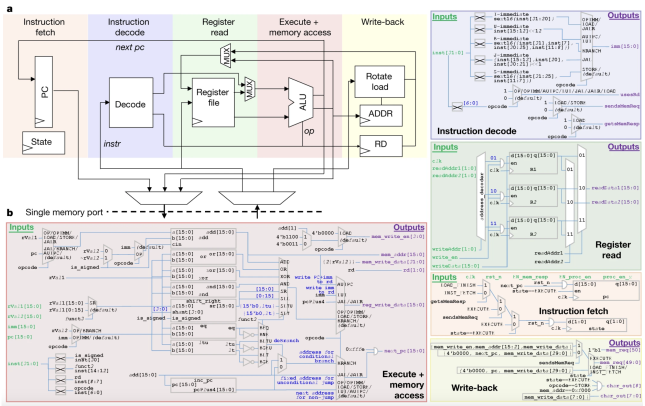

Figure 2: Architecture and Design of RV16X-NANO

2.5 Challenges in CNFET Fabrication and Integration

Despite the considerable amount of progress made, several challenges still need to be addressed before CNFETs can achieve widespread viability and meet yield requirements for very large scale integration (VLSI). Most signficantly, material and manufacturing defects are the current biggest challenge. Current methods of CNT fabrication lack a reliable way of controlling the chirality leading to many CNTs exhibiting metallic properties instead of being semiconductors. Even after achieving semiconducting CNTs, manufacturing processes still introduce defects and variability across a wafer. This includes variation in CNFET density and contact resistance leading to non uniform performance across an entire chip. In addition to manufacturing issues there still lacks a way of seamlessly integrating with traditional silicon CMOS components. Overcoming these challenges is crucial to achieving

3 SPINTRONICS: BEYOND CHARGE-BASED COMPUTING

Traditional electronics primarily rely on the charge of electrons to process and store information. 1s and 0s are coded by high and low volages which are determined by electric fields created by distributions of charges. However, this approach faces inherent limitations in terms of power consumption and switching speed as devices continue to shrink. Spintronics emerges as a new paradigm that seeks to overcome these limitations by exploiting not only electron's charge but also its intrinsic angular momentum, known as spin. This additional degree of freedom offers the potential for fundamentally new device functionalities, leading to ultra-low power consumption, higher operating speeds, and increased logic density.

3.1 Introduction to Spintronics

Spintronics is the study and exploitation of the spin of electrons in solid-state devices. Unlike charge, which is a scalar quantity, spin is a quantum mechanical property that can be oriented in different directions (e.g., "spin-up" or "spin-down"). This allows for the encoding of information in a non-volatile magnetic state. The promise of spintronics lies in its ability to enable novel functionalities and overcome the inherent energy dissipation associated with moving charges in conventional electronics. By manipulating spin currents and magnetic states, spintronic devices aim to perform logic operations with significantly reduced energy footprints.

3.2 Magnetoelectric Spin-Orbit (MESO) Devices

4 MEMRISTORS

5 COMPARATIVE ANALYSIS

6 CONCLUSION

7 ACKNOWLEDGMENTS

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The ACM Computing Classification System — https://www.acm.org/publications/class-2012 — is a set of classifiers and concepts that describe the computing discipline. Authors can select entries from this classification system, via https://dl.acm.org/ccs/ccs.cfm, and generate the commands to be included in the LaTeX source.

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9 SECTIONING COMMANDS

Your work should use standard LaTeX sectioning commands: `\section`, `\subsection`, `\subsubsection`, `\paragraph`, and `\subparagraph`. The sectioning levels up to `\subsusection` should be numbered; do not remove the numbering from the commands.

Simulating a sectioning command by setting the first word or words of a paragraph in boldface or italicized text is **not allowed.**

Table 1: Frequency of Special Characters

Non-English or Math	Frequency	Comments
Ø	1 in 1,000	For Swedish names
π	1 in 5	Common in math
$	4 in 5	Used in business
Ψ_1^2	1 in 40,000	Unexplained usage

Below are examples of sectioning commands.

9.1 Subsection

This is a subsection.

9.1.1 Subsubsection. This is a subsubsection.

Paragraph. This is a paragraph.
Subparagraph This is a subparagraph.

10 TABLES

The "`acmart`" document class includes the "`booktabs`" package — https://ctan.org/pkg/booktabs — for preparing high-quality tables.

Table captions are placed *above* the table.

Because tables cannot be split across pages, the best placement for them is typically the top of the page nearest their initial cite. To ensure this proper "floating" placement of tables, use the environment **table** to enclose the table's contents and the table caption. The contents of the table itself must go in the **tabular** environment, to be aligned properly in rows and columns, with the desired horizontal and vertical rules. Again, detailed instructions on **tabular** material are found in the *LaTeX User's Guide*.

Immediately following this sentence is the point at which Table 1 is included in the input file; compare the placement of the table here with the table in the printed output of this document.

To set a wider table, which takes up the whole width of the page's live area, use the environment **table*** to enclose the table's contents and the table caption. As with a single-column table, this wide table will "float" to a location deemed more desirable. Immediately following this sentence is the point at which Table 2 is included in the input file; again, it is instructive to compare the placement of the table here with the table in the printed output of this document.

Always use midrule to separate table header rows from data rows, and use it only for this purpose. This enables assistive technologies to recognise table headers and support their users in navigating tables more easily.

11 MATH EQUATIONS

You may want to display math equations in three distinct styles: inline, numbered or non-numbered display. Each of the three are discussed in the next sections.

11.1 Inline (In-text) Equations

A formula that appears in the running text is called an inline or in-text formula. It is produced by the **math** environment, which can be invoked with the usual `\begin . . . \end` construction or with the short form `$ . . . $`. You can use any of the symbols and structures, from α to ω, available in LaTeX [?]; this section will simply show a few examples of in-text equations in context. Notice how this equation: $\lim_{n\to\infty} x = 0$, set here in in-line math style, looks slightly different when set in display style. (See next section).

11.2 Display Equations

A numbered display equation—one set off by vertical space from the text and centered horizontally—is produced by the **equation** environment. An unnumbered display equation is produced by the **displaymath** environment.

Again, in either environment, you can use any of the symbols and structures available in LaTeX; this section will just give a couple of examples of display equations in context. First, consider the equation, shown as an inline equation above:

$$\lim_{n\to\infty} x = 0 \tag{1}$$

Notice how it is formatted somewhat differently in the **displaymath** environment. Now, we'll enter an unnumbered equation:

$$\sum_{i=0}^{\infty} x + 1$$

and follow it with another numbered equation:

$$\sum_{i=0}^{\infty} x_i = \int_0^{\pi+2} f \tag{2}$$

just to demonstrate LaTeX's able handling of numbering.

12 FIGURES

The "`figure`" environment should be used for figures. One or more images can be placed within a figure. If your figure contains third-party material, you must clearly identify it as such, as shown in the example below.

Figure 3: 1907 Franklin Model D roadster. Photograph by Harris & Ewing, Inc. [Public domain], via Wikimedia Commons. (https://goo.gl/VLCRBB).

Your figures should contain a caption which describes the figure to the reader.

Figure captions are placed *below* the figure.

Every figure should also have a figure description unless it is purely decorative. These descriptions convey what's in the image to someone who cannot see it. They are also used by search engine crawlers for indexing images, and when images cannot be loaded.

A figure description must be unformatted plain text less than 2000 characters long (including spaces). **Figure descriptions should not repeat the figure caption – their purpose is to capture important information that is not already provided in the caption or the main text of the paper.** For figures that convey important and complex new information, a short text description may not be adequate. More complex alternative descriptions can be placed in an appendix and referenced in a short figure description. For example, provide a data table capturing the information in a bar chart, or a structured list representing a graph.

Table 2: Some Typical Commands

Command	A Number	Comments
`\author`	100	Author
`\table`	300	For tables
`\table*`	400	For wider tables

For additional information regarding how best to write figure descriptions and why doing this is so important, please see https://www.acm.org/publications/taps/describing-figures/.

12.1 The "Teaser Figure"

A "teaser figure" is an image, or set of images in one figure, that are placed after all author and affiliation information, and before the body of the article, spanning the page. If you wish to have such a figure in your article, place the command immediately before the `\maketitle` command:

```
\begin{teaserfigure}
  \includegraphics[width=\textwidth]{sampleteaser}
  \caption{figure caption}
  \Description{figure description}
\end{teaserfigure}
```

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The use of BibTeX for the preparation and formatting of one's references is strongly recommended. Authors' names should be complete — use full first names ("Donald E. Knuth") not initials ("D. E. Knuth") — and the salient identifying features of a reference should be included: title, year, volume, number, pages, article DOI, etc.

The bibliography is included in your source document with these two commands, placed just before the `\end{document}` command:

```
\bibliographystyle{ACM-Reference-Format}
\bibliography{bibfile}
```

where "`bibfile`" is the name, without the "`.bib`" suffix, of the BibTeX file.

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```
\citestyle{acmauthoryear}
```

Some examples. A paginated journal article [**?**], an enumerated journal article [**?**], a reference to an entire issue [**?**], a monograph (whole book) [**?**], a monograph/whole book in a series (see 2a in spec. document) [**?**], a divisible-book such as an anthology or compilation [**?**] followed by the same example, however we only output the series if the volume number is given [**?**] (so Editor00a's series should NOT be present since it has no vol. no.), a chapter in a divisible book [**?**], a chapter in a divisible book in a series [**?**], a multi-volume work as book [**?**], a couple of articles in a proceedings (of a conference, symposium, workshop for example) (paginated proceedings article) [**? ?**], a proceedings article with all possible elements [**?**], an example of an enumerated proceedings article [**?**], an informally published work [**?**], a couple of preprints [**? ?**], a doctoral dissertation [**?**], a master's thesis: [**?**], an online document / world wide web resource [**? ? ?**], a video game (Case 1) [**?**] and (Case 2) [**?**] and [**?**] and (Case 3) a patent [**?**], work accepted for publication [**?**], 'YYYYb'-test for prolific author [**?**] and [**?**]. Other cites might contain 'duplicate' DOI and URLs (some SIAM articles) [**?**]. Boris / Barbara Beeton: multi-volume works as books [**?**] and [**?**]. A couple of citations with DOIs: [**? ?**]. Online citations: [**? ? ?**]. Artifacts: [**?**] and [**?**].

14 ACKNOWLEDGMENTS

Identification of funding sources and other support, and thanks to individuals and groups that assisted in the research and the preparation of the work should be included in an acknowledgment section, which is placed just before the reference section in your document.

This section has a special environment:

```
\begin{acks}
...
\end{acks}
```

so that the information contained therein can be more easily collected during the article metadata extraction phase, and to ensure consistency in the spelling of the section heading.

Authors should not prepare this section as a numbered or unnumbered `\section`; please use the "`acks`" environment.

15 APPENDICES

If your work needs an appendix, add it before the "`\end{document}`" command at the conclusion of your source document.

Start the appendix with the "`appendix`" command:

```
\appendix
```

and note that in the appendix, sections are lettered, not numbered. This document has two appendices, demonstrating the section and subsection identification method.

16 MULTI-LANGUAGE PAPERS

Papers may be written in languages other than English or include titles, subtitles, keywords and abstracts in different languages (as a rule, a paper in a language other than English should include an English title and an English abstract). Use `language=...` for every language used in the paper. The last language indicated is the main language of the paper. For example, a French paper with additional titles and abstracts in English and German may start with the following command

```
\documentclass[sigconf, language=english, language=german,
               language=french]{acmart}
```

The title, subtitle, keywords and abstract will be typeset in the main language of the paper. The commands `\translatedXXX`, `XXX` begin title, subtitle and keywords, can be used to set these elements in the other languages. The environment `translatedabstract` is used to set the translation of the abstract. These commands and environment have a mandatory first argument: the language of the second argument. See `sample-sigconf-i13n.tex` file for examples of their usage.

17 SIGCHI EXTENDED ABSTRACTS

The “`sigchi-a`” template style (available only in LaTeX and not in Word) produces a landscape-orientation formatted article, with a wide left margin. Three environments are available for use with the “`sigchi-a`” template style, and produce formatted output in the margin:

`sidebar`: Place formatted text in the margin.
`marginfigure`: Place a figure in the margin.
`margintable`: Place a table in the margin.

ACKNOWLEDGMENTS

To Robert, for the bagels and explaining CMYK and color spaces.

A RESEARCH METHODS

A.1 Part One

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A.2 Part Two

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B ONLINE RESOURCES

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