LOW-COST DC BUILT-IN SELF-TEST OF LINEAR ANALOG CIRCUITS USING CHECKSUMS

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Abstract

DC testing of analog circuits is inexpensive compared to AC testing and provides high coverage of many fault classes including some that are not detected by AC tests. It is also particularly effective in detecting catastrophic failures such as line opens and shorts. In this paper, we present an efficient low-cost built-in self-test (BIST) methodology for linear analog circuits that is targeted towards faults that can be detected with DC tests. The methodology is based on the use of checksum encodings of matrix representations of the DC transfer function of the circuit under test (CUT). A small amount of circuitry called the checking circuitry is appended to the CUT for the purpose of on-chip fault detection. The size of this circuitry is limited to one extra op-amp irrespective of the size of the CUT. In test mode, DC stimulus is applied to the CUT via low-cost on-chip BIST circuitry. The presence of a non-zero signal at the output of the checking circuit indicates the presence of a fault.

1.0 Introduction

In this paper, we present a new approach to a special kind of built-in self-test (BIST) of linear analog circuits using DC test stimulus. This provides coverage of all faults that affect the DC transfer characteristics of the output and selected internal nodes of the circuit under test at very low hardware cost. Fault coverage is very high for many classes of parametric and catastrophic faults.

The proposed BIST method is based on the use of matrix checksum codes for fault detection. The concept of algorithm-based fault tolerance for matrix operations using checksums was first discussed by Huang and Abraham in [1]. Redundant matrix computations with low overhead were performed to detect errors in the results of matrix operations. An extension of this idea was used to detect failures in FFT networks by Jou and Abraham in [2]. In [3], Jou and Abraham discuss methods for error detection in highly concurrent computing structures including linear digital filters. In [4], Nair and Abraham discuss a class of codes called real-number checksum codes for detecting and correcting errors in matrix-vector operations. The use of these codes for on-line detection of faults that affect the small-signal AC transfer function of linear analog circuits has been discussed by Chatterjee in [5]. As discussed earlier, the proposed BIST scheme detects faults that affect the DC transfer function of the CUT. Milor and Visvanathan [6] have studied mathematical models of faults that affect the DC transfer function of a CUT. In [7], they have further described an algorithm for optimizing functional test sets against test time. With regard to BIST, we believe our approach to low-cost BIST of linear analog circuits using checksum codes to be the first. In the following, we first present the basic concepts and theory. Then the BIST methodology is discussed along with a simple case study. Finally, results and conclusions are presented.

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2.0 Basic Concepts and Theory

For simplicity, we will consider first order linear analog systems consisting of integrators and summers [5]. We represent the outputs of each of n integrators of a linear analog circuit by the vector $X(s) = [x_1(s), x_2(s), ..., x_n(s)]$, called the state vector, where every element of the state vector is a state variable, $x_i(s)$ being the Laplace transform of the variable $x_i(t)$. For AC analysis, the behavior of a linear analog circuit can be analyzed by a state equation of the form shown in the equation, below, $X'(s) = [AX'(s)/s] + [Bu(s)/s]$. In this equation, the matrix A is of dimension $n \times n$ and the matrix B is of dimension $n \times 1$ assuming the circuit has a single input u. It is possible for the state equation to subsume the system output equation [5], hence, the latter is not considered here. In order to determine the DC transfer function of the linear analog circuit, assume that the DC gain of the inverting integrator corresponding to the i'th state variable is given by $-\alpha_i$. Also, let the DC value of the state vector

be given simply by X. Under these stipulations, it is possible to write a DC state equation of the form $X^T = \bar{A}X^T + \bar{B}u^T$, where the elements of the i'th rows of $\bar{A}$ and $\bar{B}$ are linear functions of $-\alpha_i$. Henceforth, for simplicity, we shall refer to $\bar{A}$ and $\bar{B}$ as simply, A and B.

Theorem 1: The steady-state DC values of the state variables are given by the solution $X^T = (I-A)^{-1}Bu$ under the limit $\alpha_i \to \infty$ for all $1 \le i \le n$.

Proof: From the state equation for the DC case given by $X^T = \bar{A}X^T + \bar{B}u^T$, the solution $X^T = (I-A)^{-1}Bu$ is easily obtained by solving for X^T. This solution contains the terms $-\alpha_i$ representing the gains of the inverting integrators corresponding to the state variables of the circuit. For AC analysis, $\alpha_i = 1/(sCR)$, where $s = j\omega$, ω is the frequency of operation, C is the capacitor value and R is the resistor value associated with the integrator corresponding to the i'th state variable. The DC case corresponds to $s=0$ for which $\alpha_i = \infty$. The proof follows. ❑

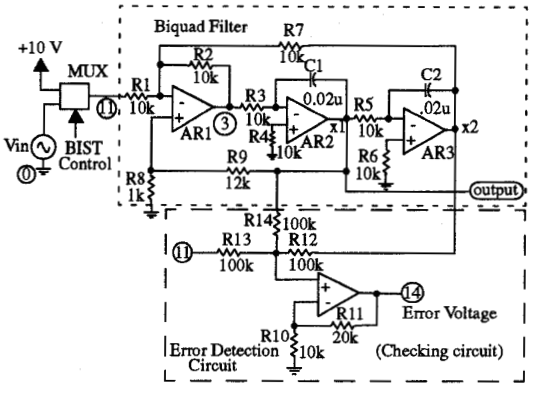

Figure 1. Biquadratic filter with checking circuit.

EXAMPLE 1: Consider the biquadratic filter shown in Figure 1 (shown with BIST circuitry to be described later). Its AC transfer function is given by the state equation given by Equation (1) below.

$$\begin{bmatrix} x_1(s) \\ x_2(s) \end{bmatrix} = \begin{bmatrix} -\omega_0 & \omega_0 \\ -\omega_0 & 0 \end{bmatrix} \begin{bmatrix} (x_1(s))/s \\ (x_2(s))/s \end{bmatrix} + \begin{bmatrix} \omega_0 \\ 0 \end{bmatrix} ((u(s))/s) \qquad (1)$$

If we replace ω_0/s by the symbol α, then Equation (2) is obtained as shown below.

$$\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} -\alpha & \alpha \\ -\alpha & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} \alpha \\ 0 \end{bmatrix} u \qquad (2)$$

To obtain the DC transfer functions for x_1 and x_2 we solve Equation (2) and obtain expressions for x_1 and x_2 in terms of α. Using the expression $X^T = (I-A)^{-1}Bu$ from Theorem 1, we obtain Equation (3), below.

$$\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} 1/(1+\alpha+\alpha^2) & \alpha/(1+\alpha+\alpha^2) \\ (-\alpha)/(1+\alpha+\alpha^2) & (1+\alpha)/(1+\alpha+\alpha^2) \end{bmatrix} \begin{bmatrix} \alpha \\ 0 \end{bmatrix} u \qquad (3)$$

Taking the limit of Equation (3) as $\alpha \to \infty$, we obtain the DC solution $x_1 = 0$ and $x_2 = -u$. Figure 2 shows an Hspice simulation (DC sweep) of the filter of Figure 1, where x_1 is given by the graph corresponding to node OUTPUT and x_2 is given by the graph corresponding to node 10. The other nodes displayed in the graph will be referred to later in the paper. As is evident, the Hspice simulation matches the DC transfer characteristics obtained by solving Equation (3) as dictated by Theorem 1.

The DC values of the state variables obtained by solving the expression $X^T = (I-A)^{-1}Bu$ as specified by Theorem 1 yield a set of linear relations that specify the state variables in terms of the input u. It is possible to represent these relations in matrix form by the equation $X^T = Cu$, where C is an $n \times 1$ matrix.

EXAMPLE 2: For the solution of Example 1, the matrix form representation is given by.

$$X^T = \begin{bmatrix} 0 \\ -1 \end{bmatrix} u \qquad (4)$$

In order to perform built-in self-test using checksum codes, we encode the matrix C as follows. The state vector X is modified to include the check variable c; the modified state vector being $X^* = [x_1, x_2, ..., x_n, c]$. The element r is added to the bottom of the matrix C so that the modified matrix form representation of the DC values of the state variables is given by,

$$X^{*T} = \begin{bmatrix} C \\ r \end{bmatrix} u \qquad (5)$$

The element r is computed as $r = CV \cdot X$, where $CV = [\beta_1, \beta_2, ..., \beta_n]$ consists of real-valued elements and is called the coding vector. The following theorem is stated without proof. For reference, similar results are proved in [5].

Theorem 2: In the modified DC state equation,

$$[CV, -1] \cdot X^{*T} = 0. \qquad (6)$$

Theorem 2 constitutes the basis for our BIST scheme. The check variable c is computed using additional circuitry and the quantity $CV \cdot X$ is subtracted from it to yield an *error signal* which is zero in the absence of faults and non-zero in the presence of faults. While the results above, have been stated for systems with only a single input, the extension of the above to multi-input systems is trivial. For a system with m inputs, the matrix C is an $n \times m$ matrix. Irrespective of the number of inputs, the checking circuit can be implemented using only *one* extra opamp. The reason for this is that the checking circuit

merely computes the arithmetic difference between two first-order polynomials of the state variables. Such a difference can always be computed using a single opamp.

EXAMPLE 3: For the biquadratic filter of Figure 1, with CV = [1, 1], the modified DC state equation is of the form given by Equation (5).

$$\begin{bmatrix} x_1 \\ x_2 \\ c \end{bmatrix} = \begin{bmatrix} 0 \\ -1 \\ -1 \end{bmatrix} u \qquad (7)$$

Hence, the error signal is simply $error = -u - x_1 - x_2$. The resulting error detection and checking circuit is shown in Figure 1 in the dashed box. Figure 2 shows the DC response of the output of the error detection circuitry (node 14 in Figure 1) for the fault-free case. Note that this is equal to 0 as dictated by our theory discussed earlier.

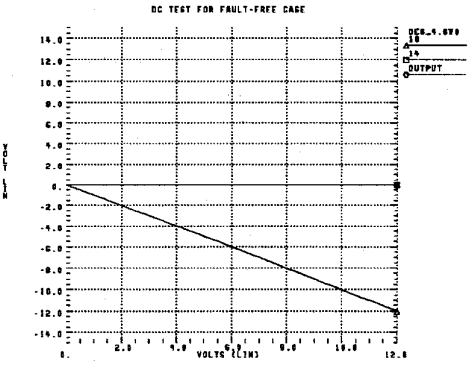

Figure 2. Simulated DC transfer characteristics.

3.0 BIST Issues, Justification of Approach and Results

There are several key issues in the use of the error detection and checking circuit proposed above for implementation of BIST. The BIST implementation involves use of the checking circuitry in conjunction with on-chip application of DC test stimulus. In order to enable low-cost BIST both the checking circuitry and the on-chip stimulus generation mechanisms must be very simple. We have already demonstrated the simplicity of the checking circuitry. For our test stimuli, we choose a set of DC voltages and apply these and the normal input stimulus to the CUT through an analog multiplexer. Figure 3 shows the general structure of the proposed BIST methodology. In BIST mode, the BIST control signal selectively applies the DC test signals one by one to the CUT.

If for any of the DC tests the output of the error detection/checking circuitry is non-zero, a fault is indicated. The key aspect of our test methodology is that d*ue to the*

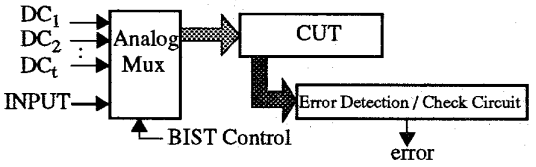

Figure 3. BIST structure.

insertion of the checking circuitry, the number of DC tests (inputs to analog multiplexer) is extremely small. In fact, for the biquadratic filter example, only a 2-input analog mux is required, one input connected to the normal filter input and the other connected to a 10V DC test stimulus.

In order to study the effectiveness of the proposed BIST scheme, we injected a large number of failures in to an Hspice model of the biquadratic filter using transistor level descriptions of each of the opamps of Figure 1 shown in Figure 4.

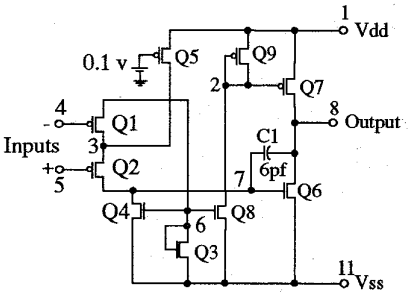

Figure 4. MOS Operational Amplifier.

Figure 5 shows a scatter plot of the results of some of the experiments. The vertical axis shows the error voltage (output of the error detection/checking circuit). The horizontal axis shows the DC voltage at the output of the biquadratic filter for the injected faults. The nominal value of the output is 0 volts. For some faults, the observed output voltage remains unchanged at 0 volts. However, the error voltage for these faults is non-zero. It was seen by simulation that while these faults were "redundant" from a DC testing perspective, they were not so from the standpoint of AC operation of the circuit.

Figure 6 shows the AC transfer characteristic of the filter, without and with the fault R7=2K AC_1.AC0 and AC_2.AC0, respectively). For the above fault, the DC value of the output was equal to its fault-free value of 0 volts, but the error signal voltage was non-zero. This illustrates a case in which the error signal is non-zero for a fault which affects the AC transfer function of the CUT, but not the DC transfer function. This also proves that merely monitoring the output voltage of a CUT under a DC test stimulus is not sufficient and that addition of the error detection circuitry greatly improves BIST efficiency

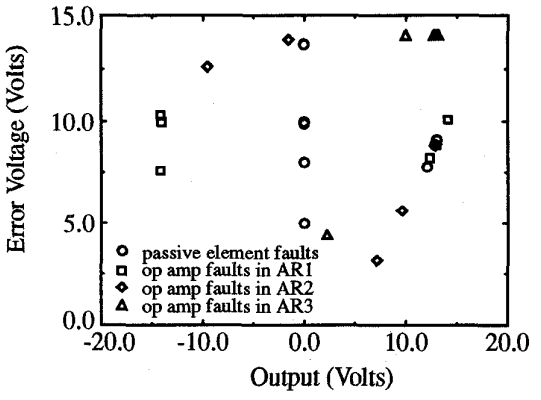

Figure 5. Result of Fault Injection Experiments.

(high fault coverage, low hardware cost).

Tables 1 and 2 show the results of injecting different kinds of faults into the biquadratic filter. Note that under the DC test stimulus of 10V, the fault free value of node "output" is 0 volts.

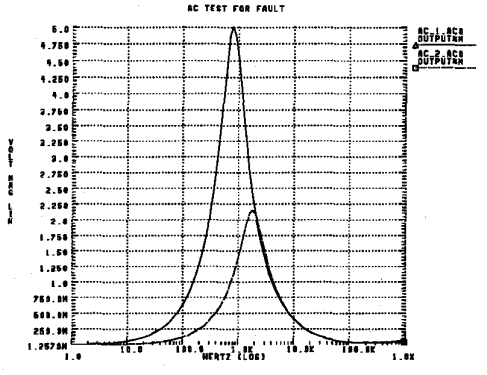

Figure 6. AC response of filter without and with fault R7=2K.

Table 1: Passive Element Faults.

Fault	*Output*	*Error*
R1 100Ω	13.06	9.12
R1 2kΩ	12.87	8.84
R1 20kΩ	0	5
R1 short	13.06	9.12
R1 open	0	10
R2 short	0	13.65
R7 100Ω	0	9.89
R7 2kΩ	0	8
R7 short	0	10
R7 open	12.11	7.78

To summarize, the proposed BIST circuitry of Figure 1 gave 100% fault coverage of all faults that affected the DC transfer characteristics of the filter. Moreover, it also detected faults that do not affect the DC transfer characteristics of the filter output but affect its AC response. This points to the power and the efficiency of the proposed BIST scheme.

Table 2: Faults in Op Amp AR1.

Fault	*Output*	*Error*
Rf1 6 4 100Ω	-14.15	7.59
Rf2 6 8 100Ω	12.35	8.22
Rf3 6 2 100Ω	-14.17	10.31
Rf4 7 8 100Ω	12.99	8.84
Rf5 8 1 100Ω	-14.07	10
Rf6 7 6 100Ω	-14.12	10.09

4.0 Conclusions

In this paper we have described a novel method for performing DC BIST of linear analog circuits. The technique provides high coverage of faults at very low hardware cost. The detected faults include some which do not affect the DC transfer function but affect the AC transfer function of the circuit under test. The key feature of the method is low-cost. We believe that this alone along with the high fault coverage it allows will make the proposed BIST method very attractive to designers.

5.0 References

[1] K. H. Huang and J. A. Abraham, "Algorithm-Based Fault Tolerance for Matrix Operations," *IEEE Transactions on Computers*, Vol. C-33, pp. 518-528, June 1984.

[2] J. Y. Jou and J. A. Abraham, "Fault Tolerant FFT Networks," *IEEE Transactions on Computers*, Vol. 37. pp. 548-561, May 1988.

[3] J. Y. Jou and J. A. Abraham, "Fault-Tolerant Matrix Arithmetic and Signal Processing on Highly Concurrent Computing Structures," *Proceedings of the IEEE*, Vol. 74, pp. 732-741, May 1986.

[4] V. S. S. Nair and J. A. Abraham, "Real-Number Codes for Fault-Tolerant Matrix Operations on Processor Arrays," *IEEE Transactions on Computers*, Vol. 39, pp. 426-435, April 1990.

[5] A. Chatterjee, "Concurrent Error Detection and Fault-Tolerance in Linear Analog circuits Using Continuous Checksums," *IEEE Transactions on VLSI Systems*, Vol. 1, No. 2, pp. 138-150, June, 1993.

[6] L. Milor and V. Visvanathan, "Detection of catastrophic faults in analog integrated circuits," *IEEE Trans. Computer-Aided Design*, pp. 114-130, February 1989.

[7] L. Milor and A. Sangiovanni-Vincentelli, "Optimal test set design for analog circuits," in *Proc. Int. Conf. on Computer-Aided Design*, pp. 294-297, November 1990.