Digital Components for Built-In Self-Test of Analog Circuits

Charles Stroud, Piyumani Karunaratna, and Eugene Bradley

Dept. of Electrical Engineering
University of Kentucky

Abstract: We describe the design and operation of a digital test pattern generator (TPG) along with three accumulator based output response analysis (ORA) circuits that are targeted for implementing Built-In Self-Test (BIST) for analog circuits in mixed signal based ASICs. The test patterns produced by the TPG include ramps, triangle and square waves, pseudo-random noise, and a frequency sweep capability for testing the frequency response of the analog circuit under test. The ORA circuits include single and double precision as well as residue accumulators for magnitude and phase measurements. We include an overview of the complete mixed signal based BIST architecture and simulation system along with the results of our initial application of the BIST architecture to an analog circuit under test.[1]

1. Introduction

The overall objective of this research and development project is to investigate, develop, and evaluate a Built-In Self-Test (BIST) approach for analog circuitry which resides in mixed signal VLSI devices and systems. Mixed signal circuits and systems provide an excellent environment to develop Built-In Self-Test (BIST) approaches for analog circuits and systems. Mixed signal environments allow the experience and expertise that has been gained over the past 17 years of BIST development in digital circuitry to be used as a platform for the investigation of analog BIST techniques. In particular, the basic components of most BIST structures may be incorporated into the digital portion of the design and without adverse effects on the analog circuit performance that would be incurred if the BIST circuitry were to be inserted in the analog portion of the design. These digital components include test pattern generator (TPG) and output response analyzer (ORA) functions as well as the necessary test controller function to initialize and control the BIST sequence and provide system level access for off-line testing of the circuit or system [1-3]. However, it is important to note that there are different requirements that must be considered in analog BIST which prevent the straight forward application of conventional digital TPG and ORA functions. In this paper, we discuss those issues with respect to the design of digital TPGs and ORAs targeted for the testing of analog circuits. We begin with the overview of the proposed mixed signal based BIST architecture for analog circuits in Section 2 followed by a more detailed discussion of issues associated with the TPG design in Section 3. In Section 4, we discuss ORA design issues and we present an overview of the BIST simulation environment in Section 5. The paper concludes in Section 6 with a summary of the results obtained with our initial application of the BIST approach to an analog circuit.

1. Effort sponsored by Rome Laboratory, Air Force Material Command, USAF, under agreement number F30602-97-1-0042. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright annotation thereon.

2. BIST Architecture

The proposed mixed signal based BIST architecture for analog circuits is shown in Figure 1 with the additional BIST circuitry shown in bold and the analog circuitry under test shown in shades of grey. The normal system components include the digital system functions (here we assume two-way transmission of both digital and analog signals) as well as the analog system functions along with the Digital-to-Analog Converters (DACs) and Analog-to-Digital Converters (ADCs) that would normally be required to convert the digital signals to analog waveforms and vice versa. The proposed additions to the mixed signal system include the digital TPG and ORA functions as well as a digital test controller and analog loopback capabilities to facilitate the return path for the test signals to the ORA. An additional multiplexer (MUX) is required for the insertion of the digital test patterns into the data stream. Since the target circuitry under test is the analog system circuits, including the DACs and ADCs, we incorporate the digital TPG and its associated MUX immediately prior to the digital inputs of the DAC.

One of the principle specifications that should be adhered to in order to maximize the value and effectiveness of this approach is that the complete BIST system be accessible and usable during system-level operation for off-line testing and system diagnostics. This, in turn, requires that the BIST circuitry be capable of proper initialization of the circuitry under test, isolation of system data inputs, and reproducible results from one execution of the BIST sequence to the next in the same manner as is required in digital systems [3]. These essential functions are typically governed by the test controller which is often implemented as part of or in conjunction with the TPG. The test controller, although often overlooked, is an important circuit in terms of its effect on analog BIST. Aside from controlling the length of the BIST sequence to ensure reproducible results, particularly during system level testing, the initialization sequence, also a function of the test controller, is just as important to obtaining reproducible results during system-level testing.

The length of the initialization sequence should be a function of the longest time constant in the analog circuit as well as the length of time required to clear the effects of previous system signals in the feedback circuits in the analog circuitry.

Control of the analog loopback function(s) may be assigned to the test controller, however, it is often best to control these loopback functions independently in order to achieve optimal diagnostic resolution in the analog circuit under test. For example, with the left-hand analog loopback shown in Figure 1 activated, any faults detected are isolated to the path from the TPG to the ORA, as shown by the dark grey bordered analog circuitry and paths in Figure 1. If the BIST sequence indicates a good circuit, then the left-hand analog loopback can be deactivated while the right-hand loopback function can be activated further down the output signal path and the BIST re-executed. Faults detected during this second BIST sequence would be isolated to the analogi circuitry shown in light grey in Figure 1. In this manner, the BIST sequence can be executed any number of times with various configurations of loopback functions to effectively isolate the fault(s) in the system to a given section of analog circuitry. However, to ensure that this diagnostic resolution can be realized, the length of the initialization sequence must be sufficient to accommodate the longest analog path in the circuit with its associated time constants and feedback circuits considered.

Within the constraints of the objective of accessibility and use of the BIST circuitry during system-level testing, high fault coverage along with minimal area overhead and performance penalties are critical for the practical application of this BIST approach [7]. In the subsequent sections, we describe the design and operation of the TPG and ORA functions we have designed and are currently evaluating for this BIST approach

3. Test Pattern Generation

Digital TPG functions offer a wealth of types of test patterns to evaluate for their effectiveness in mixed signal based analog BIST applications. We have designed, simulated, and verified an 8-bit TPG circuit that is modular such that it can be easily modified to create a TPG of any desired bit size. Our basic TPG design includes a binary counter and a Linear Feedback Shift Register (LFSR). The counter operates in a number of different modes to provide a variety of analog test patterns. For example, a single pass through the up-count range of the binary counter produces a ramp signal. Ramp input signals have been used in recent analog testing techniques and have been found to provide good fault detection results, in some cases, better results than sinusoid test signals [4,5]. It has been observed that faults in analog circuits can cause detectable variations in output response delay, rise/fall times, and overshoot when stimulated by certain input test signals. But it has also been observed that the detectability of faults with respect to the input test signal can vary with the type of analog circuit under test [5]. Multiple passes through the up-count or down-count range produces a saw-tooth analog test signal; combining the up-count and down-count generates a triangular waveform at the output of the DAC.

The LSFR mode of operation in the TPG, on the other hand, produces an analog signal that is more noise-like in it's properties. During analysis of the analog test patterns produced by internal and external feedback LFSRs, we found no significant difference in the two types of LFSR implementations. We had originally thought there would be a noticeable difference due to the way in which the feedback implementation of the two types of LFSRs differ. As a result, we concluded that only one type (we chose the internal-type feedback) LFSR with a programmable characteristic polynomial would be incorporated in the TPG design. In order to take into consideration the shifting of data values in the LFSR, we investigated the reversal of the ordering of the bits applied to the DAC for generation of the analog test patterns; in other words, the most significant bit of the binary value of the test pattern produced by the TPG becomes the least significant bit and vice versa. But, we found nothing of significance with respect to the LFSR test patterns. However, when we investigated the same bit reversal effect for the counter modes of operation we found that the test patterns looked much more like white noise. This is illustrated in Figure 2 where the triangular wave produced by a 4-bit up-down counter is shown along with the waveform produced by the reversal of the bits in the binary count value when applied to the DAC. As a result, we have included the bit reversal for all modes of operation of the TPG in order to study the fault detection capability of these patterns in the analog circuitry under test.

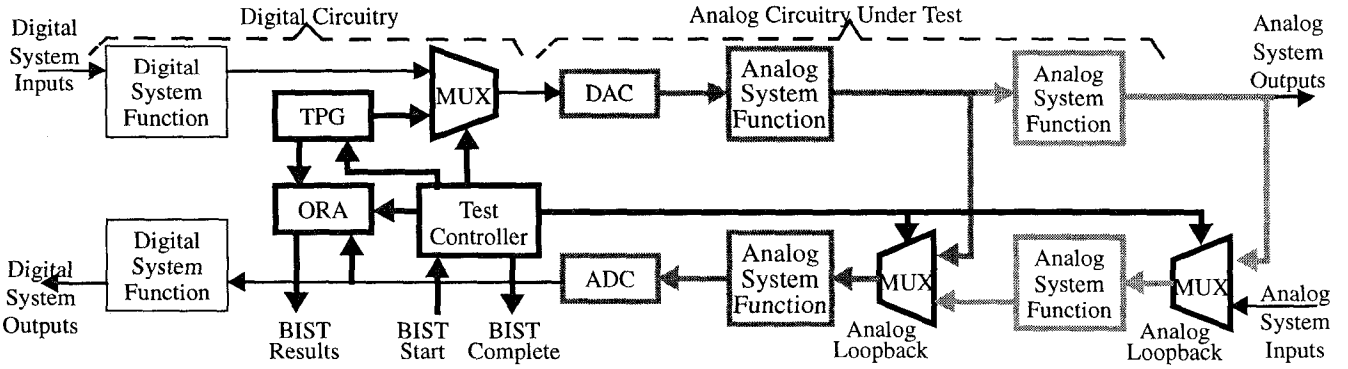


Figure 1. BIST Architecture for Mixed Signal Systems.

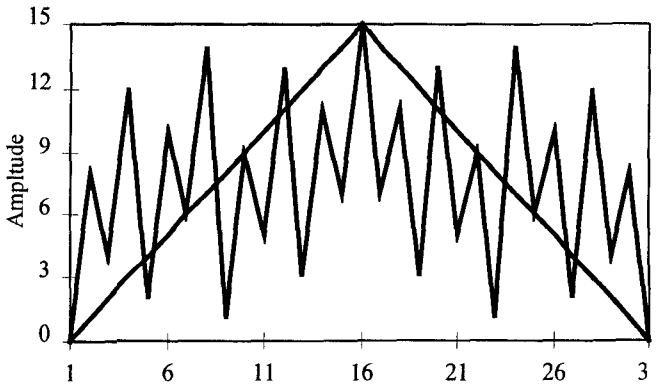


Figure 2. Triangle Wave with Bit Reversal

Since the frequency response of analog circuits can be expected to be important in terms of fault detection capability, square waves that span a wide frequency range are also produced from the TPG design. The frequency sweep mode of operation in the TPG provides a square wave test pattern which progressively increases in frequency. The square wave begins with a half period of 255 clock cycles and decreases by one clock cycle during each subsequent half cycle of the square wave until the last half period is one clock cycle in duration. At the same time, the amplitude increases by a value of 2 with each cycle of the square wave. This is illustrated in Figure 3 for a simple 4-bit counter design and can be understood more clearly from the following description of the TPG design.

The main components of the TPG design are shown in the block diagram of Figure 4 and include the 8-bit counter/LFSR, an additional 1-bit counter, multiplexers for bit reversal, multiplexers for the frequency sweep capability, and a count value holding register (also for the frequency sweep). The ordering of the bits of any set of test patterns can be reversed using the control input to the bit reversal multiplexer. The counter outputs (either reversed or not via the bit reversal multiplexer), are used to generate the frequency sweep. When the frequency sweep function is enabled, the TPG output multiplexer selects the outputs of the AND gates. These AND gates are used to set the magnitude of the square wave generated whenever the output of the 1-bit counter is a logic one. The output values of the count value holding register are loaded into the counter/LFSR and enable the TPG to generate a square wave which sweeps through a variety of

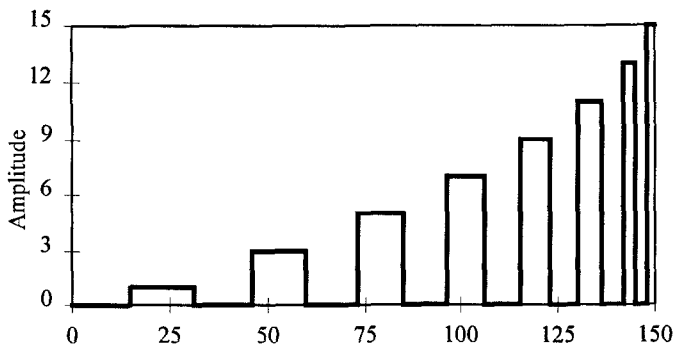


Figure 3. Frequency Sweep Waveform

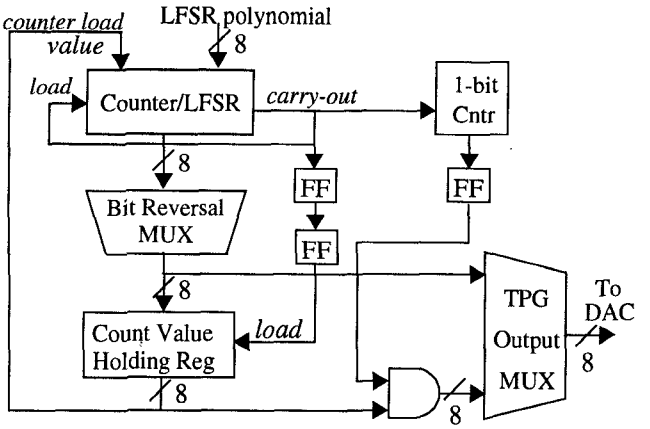


Figure 4. TPG Block Diagram

frequencies. The count value holding register is initialized to a value of all zeros at the beginning of the frequency sweep. Two clock cycles after the counter is loaded as a result of the carry-out of the counter, the count value holding register is loaded with the contents of the counter such that count value is incremented by the counter prior to being loaded into the holding register where it is held until the end of the current count. As a result, the square wave generated progressively becomes shortened in terms of the period. Enabling the bit reversal during a frequency sweep mode will load non-sequential values into the counter value holding register, instead of consecutively increasing numbers, such that the frequencies and amplitudes of the square wave signal being generated will appear to be more random in nature.

4. Output Response Analyzers

It is evident that traditional signature analysis using LFSR-based Signature Analysis Registers (SARs) and Multiple Input Signature Registers (MISRs) is unsuitable for application to analog BIST since the good circuit signature is based on the assumption that an exact sequence of output patterns is produced in every fault-free circuit. Similarly, traditional syndrome analysis, such as ones counting or transition counting, is also unacceptable since an exact output response sequence is assumed in every fault-free execution of the BIST sequence. In an analog circuit, the sampling noise in the DACs and ADCs as well as processing (i.e., tolerances) and environmental (i.e., temperature and voltage) variations in the analog circuitry will prevent reproducible traditional BIST signatures from one execution of the BIST sequence to the next.

A digital accumulator, on the other hand, can be used to obtain the sum of the magnitudes of the sampled output responses from the analog circuitry under test. The accumulator-based ORA facilitates the determination of the pass/fail status of the BIST by expecting the final sum to be within a predetermined range of values. Determination of this range of resultant values, which indicate that the circuit is fault-free, is based on specifications of the analog circuit responses to various input signals produced by the TPG under acceptable analog component parameter variations. An analog checksum circuit has been previously proposed for BIST of analog

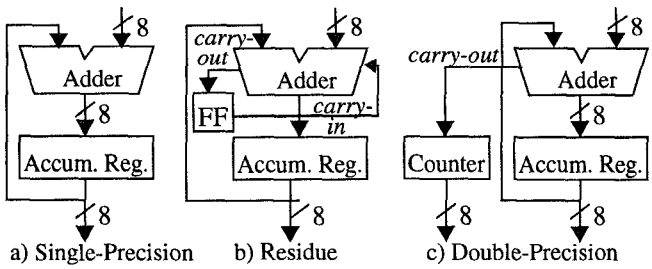


Figure 5. Accumulator based ORA circuits.

circuits [4] but the advantage of a digital ORA is that the results can be read directly through system digital interfaces without the need for additional ADCs to retrieve the BIST results during system level testing.

Three types of 8-bit accumulator based ORA circuits were designed, simulated, and verified; these are illustrated in Figure 3 and include: a) single-precision, b) residue, and c) double-precision accumulators. The design of each ORA is modular such that it can easily be modified to create an ORA of any desired size. Each ORA circuit has three modes of operation including clear, hold, and accumulate. In the single-precision accumulator, the 8-bit incoming binary value is added to the contents of the 8-bit accumulator register with the carry-in set to zero and the carry-out ignored. In the double-precision accumulator, the 8-bit incoming binary value is added to the contents of a 16-bit accumulator register with the carry-in set to zero; note that the carry-out of the 8-bit addition is not ignored but is accumulated by the additional 8-bit incrementing register. In the residue accumulator, the 8-bit incoming binary value is added to the contents of the 8-bit accumulator register while the carry-out is delayed by one clock cycle and used as the carry-in during the next addition.

5. BIST Simulation Environment

Digital fault simulations of the TPG with each of the three different ORAs provided greater than 96% single stuck-at gate level fault coverage in each case with the undetected faults resulting from invalid combinations of TPG control inputs. High fault coverage of the TPG/ORA combination ensures that the additional BIST logic is being thoroughly tested. However, in the application to analog circuitry, we expect that a range of resultant BIST values will be acceptable to account for variations in the analog components. This lead us to investigate how many (if any) of the faults in the TPG/ORA will go undetected as a result of considering a range of acceptable BIST result values and how the digital circuitry fault coverage will change with changes in the range of acceptable BIST result values. During digital fault simulation of the TPG and ORA (which is equivalent to assuming no variation in the analog circuit), we recorded the resulting ORA signature for each digital fault detected and compared the fault coverage to a possible range of acceptable BIST resul values to determine whether TPG/ORA faults will be detected. The results of these simulations are illustrated in Figure 6 where the fault coverage for the digital BIST circuitry is given as a function of the difference between the faulty circuit accumulator value and the fault-free circuit

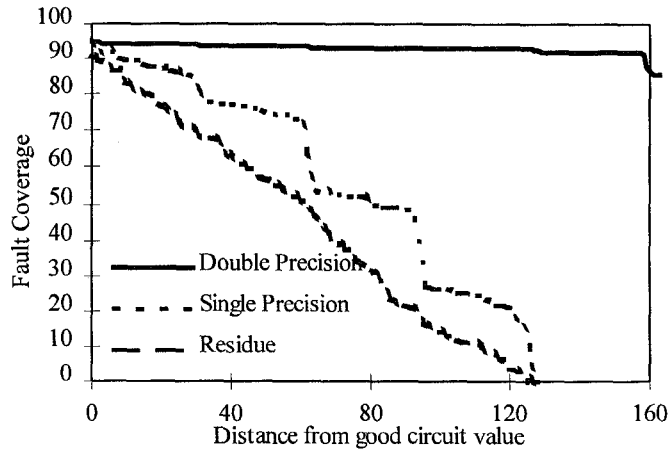


Figure 6. Digital Fault Coverage vs. Accumulator Value

accumulator value. As can be seen from the graph, the residue ORA is the worst performer with an almost linear decrease in fault coverage vs. the distance from the good circuit accumulator value. Conversely, the double precision ORA looses very little fault coverage within a range of +/-150 of the good circuit accumulator value, however, this is out of a possible range of +/-32,768 for the 16-bit double precision accumulator. As a result, we inserted a loopback multiplexer at the input to the ORA to facilitate testing the BIST circuitry independent of the analog circuitry (as shown in Figure 7). With this capability, the digital and analog fault simulations can be separated in order to use tools which are designed specifically for digital or analog simulation, but not necessarily for both.

Additional considerations related to the ORA design include detecting faults which result in phase shifts as well as faults which result in the superposition of noise on the analog signal. In the first case, summing the magnitudes of the sampled analog signal may only detect the fault at the beginning and end of the BIST sequence. In the latter case, the noise could average to zero such that there is no change in the resultant accumulator value from that of the fault-free circuit. However, summing the absolute value of the magnitude of the difference between the input test signal and the output response should allow detection of both of these cases. As a result, we have included a subtracter circuit in the ORA design which can be selected via BIST control signals for phase shift and noise detection. Therefore, the complete BIST session would consist of: 1) loopback of the TPG output directly to the ORA input to test the digital BIST circuitry, 2) summing the magnitudes of the analog response, and 3) summing the absolute value of the difference between the input test pattern and the analog output response. If any of the three

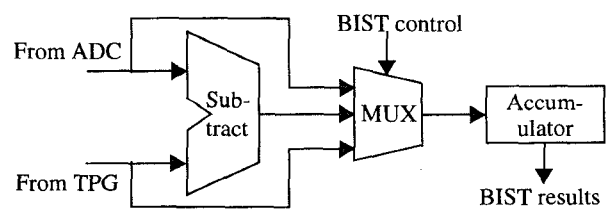


Figure 7. ORA Block Diagram

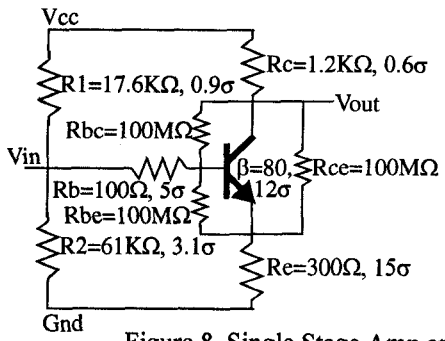
test sequences fails to produce the correct accumulator value (or a value within the acceptable range of values in the last two tests), the circuit is considered to be faulty.

We have developed a program which converts the digital output of the TPG simulation to SPICE signal statements which are then incorporated with the SPICE models for the analog circuitry under test (including the DAC and ADC) during analog simulation, verification, and fault simulation. We use the Statistical Fault Analyzer (SFA) from Rome Laboratory [8-11] to perform the analog fault simulations using the test patterns produced by the TPG. SFA performs Monte Carlo simulations of the faulty and fault-free circuits using the specified tolerances of the analog components. SFA also facilitates the determination of which faults in the analog circuit are detectable, however, we are most concerned with those detectable faults that may not be detected by the BIST approach. Therefore, we apply the output responses obtained from the SFA simulations of the fault-free analog circuit (these will be digital voltage levels since they have been produced by the ADC SPICE model) to the various ORAs (via an analysis program we developed) to determine the range of acceptable values for the BIST sequence. Similarly, we apply the digital values obtained from the faulty circuit SFA simulations to determine the range of values produced by the faulty circuit. For either of the analog BIST sequences (summing the magnitudes or summing the difference in magnitudes), if the two ranges do not overlap, the fault is considered to be detected, while the fault is considered to be undetected if the range of values of the faulty circuit falls within the range of acceptable values for the fault-free circuit. If the range of values for the faulty and fault-free circuit partially overlap, the fault is considered to be potentially detected with the probability of detection proportional to the percentage of resultant values of the faulty circuit that lie outside the range of values for the fault-free circuit.

6. Experimental Results and Summary

In the analog work thus far, we have investigated, selected, modeled, and simulated DAC and ADC designs for CMOS implementation. In addition we have obtained a number of circuits from analog testing literature and analog research projects to serve as the analog circuits under test in the SFA simulations. We have recently begun the analog fault simulation process with analysis of the ORA results and we include the following example or our preliminary results.

The single stage amplifier circuit shown in Figure 8 was simulated using the process described in the previous section using the triangular wave input test pattern. The allowable tolerances of the analog components are specified by the sigma variation next to each component value in the figure. The nine faulty circuit values are listed in the table; SFA simulations indicated that all nine faults are detectable. Eight of the nine faults were detected by the trianlgular wave in conjunction with the double-precision based ORA summing only the magnitudes of the sampled output response of the analog circuit under test (this does not include summing the absolute values of the difference in the magnitudes of the input test pattern and output response). The β-high fault was potentially



Fault List
Rc-open=1MΩ
Re-open=1MΩ
Rb-open=1MΩ
Rb-short=1Ω
Rbc-short=1Ω
Rce-short=1Ω
Rbe-short=1Ω
β-low=1
β-high=200

Figure 8. Single Stage Amp and Fault List

detected with a detection probability of 50%. These initial results indicate that the BIST approach presented in this paper offers considerable potential for testing analog circuits at all levels of testing from wafer through system level.

Acknowledgments

We wish to acknowledge the contributions of Chris Flynn, Paul Ratazzi, and Warren Debaney of Rome Laboratory for helpful suggestions and discussions regarding the TPG and ORA implementations as well as the future directions of this project. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either express or implied, of Rome Laboratory or the U.S. Government.

References

[1] V. Agrawal, C. Kime and K Saluja, "A Tutorial on Built-In Self-Test: Principles", IEEE Design & Test of Computers, Vol. 10, No. 1, pp. 73-82, 1993.

[2] V. Agrawal, K Saluja and C. Kime. "A Tutorial on Built-In Self-Test: Applications", IEEE Design & Test of Computers, Vol. 10, No. 2, pp. 69-77, 1993.

[3] C. Stroud and G. Liang, "Design Verification Techniques for System Level Testing Using ASIC Level BIST Implementations", Proc. IEEE International Application Specific Integrated Circuits Conf., pp. 140-143, 1993.

[4] A. Chatterjee, B. Kim and N. Nagi, "DC Built-In Self-Test for Linear Analog Circuits", IEEE Design and Test of Computers, Vol. 13, No. 2, pp. 26-33, 1996.

[5] A. Balivada, J. Chen and J. Abraham, "Analog Testing with Time Response Parameters", IEEE Design and Test of Computers, Vol. 13, No. 2, pp. 18-25, 1996.

[6] K. Arabi and B. Kaminska, "Oscillation-Test Strategy for Analog and Mixed Signal Integrated Circuits", Proc. of IEEE VLSI Test Symp., pp. 476-481, 1996.

[7] D. Vazquez, J. Huertas and A. Reuda, "Reducing the Impact of DFT on the Performance of Analog Integrated Circuits", Proc. of IEEE VLSI Test Symp., pp. 42-47, 1996.

[8] E. Ratazzi, "Fault Coverage Measurement for Analog Circuits", Proc. IEEE Custom Integrated Circuits Conf., pp. 17.2.1-4, 1992.

[9] E. Ratazzi, "Testability Concepts and Tools for Analog Circuits", Proc. IEEE Dual-Use Technology & Applications Conf., 1994

[10] B. Epstein, M. Czigler and S. Miller, "Fault Detection and Classification in Linear Integrated Circuits: An Application of Discrimination Analysis and Hypothesis Testing", IEEE Trans. on CAD, Vol. 12, No. 1, pp. 102-113, 1993.