Emerging Trends in VLSI Test and Diagnosis

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Abstract

As the move to very deep submicron VLSI devices pushes the threshold of semiconductor technology, conventional test and diagnosis methods become inadequate and costly. The new level of complexity driven by core-based system-chips demands that designers alter the way they approach chip development in order to keep up with diminishing time-to-market requirements and stay within budgets. Embedded test enables the production of higher-quality devices in less time. The use of embedded test raises margins and significantly reduces the time required for system verification, test and debug. This paper addresses discusses embedded test technology and analyzes its impact on time-to-market, product quality and cost.

1. Introduction

The electronics revolution we are witnessing today is driven by market demands to provide better, cheaper, smaller and faster products while meeting users' quality requirements. Meeting these quality requirements necessitates performing adequate test and diagnosis procedures. This article concentrates on the dynamic changes in the electronics industry and its impact on test and diagnosis.

The market driven electronics industry keeps introducing products with greater functionality, higher reliability, lower costs and shorter product realization intervals. These are realized by the unprecedented advancements in semiconductor IC technology. Semiconductor ICs are considered the foundation of modern products, even traditionally the non-electronic ones. Semiconductor transistors are becoming so cheap and commonly available that whole industries now live on continuously integrating more and more functions into smaller and smaller packages, hence creating system-on-chips. Being able to rapidly develop, manufacture, test, diagnose and verify complex new chips and products using such chips is crucial for the continued success of our economy at-large. This growth is expected to continue full force at least for the next decade, while making possible the production of 100 million transistor chips. However, to make its production practical and cost effective, the National Technology Roadmap for Semiconductors identified in 1997 a number of major hurdles to be overcome. Some of these hurdles are related to test technology. This article analyzes these hurdles, relates them to the advancements in semiconductor technology and presents potential solutions to address them. These solutions are meant to ensure that test contributes to the overall growth of the semiconductor industry and does not slow it down.

Test is a critical technology in the semiconductor production process. On the one hand, IC test is performed multiple times during volume production to screen the ICs upon their manufacturing. IC test starts with wafer probing even before patterned wafers are diced and goes into individually packaged chips. On the other hand, IC test also plays a key role in analyzing defects in the semiconductor manufacturing process. The feedback derived from the test is the only way to analyze and isolate many of the defects in today's processes. Time-to-yield, time-to-market, time-to-quality are all gated by test. Moreover, ICs are tested at each additional manufacturing step beyond IC production because each step can introduce new defects. With the increasing needs for high quality electronic products, at each new physical assembly level, such as board and system assembly, IC test is used for debugging, diagnosing and repairing the sub-assemblies in their new environment. Similarly with the increasing reliability, availability and serviceability requirements, most users of high-end product perform periodic tests in the field throughout the full life cycle. As the semiconductor technology keeps moving towards the creation of monster chips, we will continue to confront the key scaling trends: *greater complexities, increased performance, and higher densities.*

To allow advancements in each one of the above four scaling trends, fundamental changes are expected to emerge in different IC realization disciplines such as IC design, packaging and silicon process. These changes

have a direct impact on the test methods, tool and equipment adopted. Test must keep up with the pace of such changes to ensure that 100 million transistor monster chips adequately tested, diagnosed, measured, debugged and even sometimes repaired.

In the following, we will take the three key scaling trends one at a time, observe their implications on test, identify the key hurdles/challenges and discuss the potential solutions. Each of the three challenges our ability to efficiently create new products. It is not sufficient to address just one of the challenges; all must be met at the same time.

2. Implication of Increased Complexity

Moore's law predicts how the achievable transistor count per chip grows over time. The Semiconductor Industry Association's (SIA's) National Technology Roadmap of Semiconductors lay out the consequences of that prediction. The growth rate in IC transistor count is far higher than the rate for IC pins. The drastic increase in the ratio of transistor per pin continuously reduces the accessibility to the transistors from chip pins. The limited accessibility to internal transistors is a big problem for IC test.

The problem associated with limited Input/Outputs (I/O's) that have to be overcome do not end with access difficulties. There is a growing disparity between internal clock frequencies and the output capability of I/Os. This I/O limitation makes at-speed performance testing of an IC very difficult if not impossible. Combining the roadmap numbers for transistor count, chip I/O count, cost, chip internal frequency and I/O switching speeds, reveals the rate of growth for how much information can be generated and consumed inside a chip (internal bandwidth, defined as number of transistors per IC times internal switching frequency) outpaces by far the rate at which the available I/O bandwidth grows (number of I/Os times I/O switching speed), see Fig (1). At the same time the cost of package pins declines much more slowly than the cost of a transistor. The physical characteristics of I/Os must remain in macroscopic level dictated by chip attachment and board manufacturing constraints; whereas the silicon feature sizes are rapidly moving down from a micrometer to nanometer. In other words, the chip I/Os and board-level interfaces don't scale physically at nearly the rate of the internal circuits, contributing to a growing number of transistors behind each chip I/O and a widening performance gap between the chip internals and the I/O interface.

The data from SIA Roadmaps reveals that the gap between external bandwidth and internal bandwidth will grow in a fast pace, see Fig (1). This bandwidth gap is the main reason why we are starting to see processors and DRAMs being integrated into the same chip, rather than interacting with each other through the limited bandwidth of chip I/Os, as it was done traditionally when the bandwidth gap was negligible.

The I/O bandwidth had a major impact on chip test methods. In the very early days of IC technology (100 transistors per chip), the bandwidth gap was negligible. The test data was applied onto the chip I/Os directly from an external test data Source, and the response data received from the chip I/Os and evaluated for its correctness by an external Sink, see Fig (2-a). The combination of external Source and Sink, the test control software embedded in it, and the external test access mechanism (connecting the IC pins to the Source/Sink) represent the external test equipment.

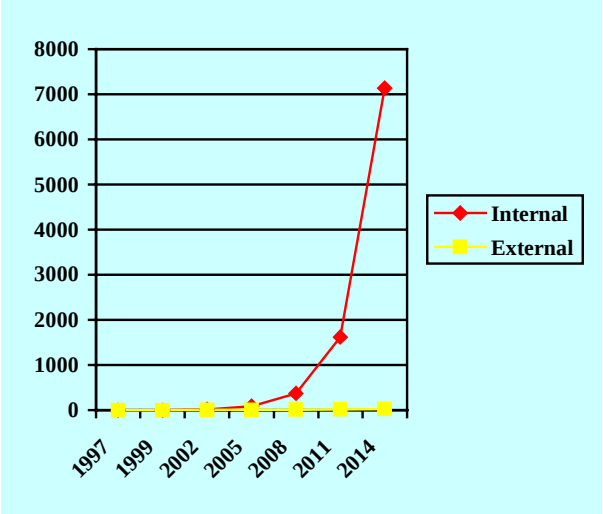


Figure (1) External vs. Internal I/O Bandwidth

With the next generation of IC technology, the transistor per pin ratio reached a level where the resulting IC complexity (10,000 transistors per IC) made the sole dependence on external test equipment insufficient. Hence, the concept of embedded test was introduced. This meant embedding test capabilities beyond the primary I/Os and into the internal transistors of the chip. One of the early embedded test techniques was scan path, which reduced the test complexity by extending the test access mechanism into the internal transistors, see Fig. (2-b). The process of incorporating embedded test circuits into the design of a chip became known as design-for-testability. Embedded test hardware, namely scan paths in this case, facilitated the transport of test data from the chip I/Os and applied it into a large number of internal transistors.

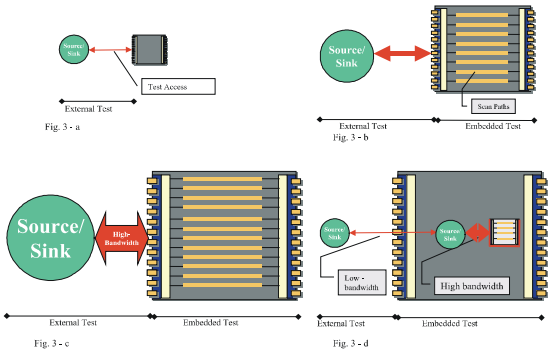
The amount of test data needed for testing an IC with a certain level of fault coverage grows with the

transistor count of the IC under test. For the embedded test based on scan paths, the growth rate is proportional to the growth in transistor count. When the external Source and Sink is providing all stimulus and response data through the chip I/Os, the pin buffer depth to apply the test need to grow with the number of transistors per pin. With complexities beyond a million transistors per IC, the pin buffer depth started to become a major concern. Moreover, with this same IC generation the external test equipment has started to confront another key hurdle, the drastic increase in silicon speed. In order to test an IC at its system speed, a semiconductor producer either had to stay with the existing approach of having external Source and Sink, but this necessitates high-bandwidth test interaction between the IC and its external Source and Sink, as in Fig. (2-c). Often external test equipment were unable of performing this capability; or introduce a low-bandwidth communication with the IC by shifting certain feature from the external Source and Sink to embedded Source and Sink. These shifted features were the test speed and data volume oriented ones Fig (2-d). The Source and Sink features that required low-bandwidth interaction remained in the external test equipment. This drastically reduced the complexity of external tester.

As in Fig (2-d), the embedded Source performs an expansion function generating an at-speed and large test data volume applies it on the circuit under test; whereas, the embedded Sink collects the response data and performs an at-speed compaction function. This results in reducing the complexity of the external Source and Sink and allowing at-speed performance test. Without such a scheme it may have been impossible, since external test equipment is often built using yesterday's technology and would result in slow test throughput with long scan paths. While embedded Source and Sink help avoid the bandwidth limitation of the external test equipment, but they do not perform total Built-In Self-Test (BIST), since they still depend on the external test equipment.

As the semiconductor technology moves to chips with over 100 million transistors, naturally the bandwidth gap between external test and embedded test will grow to levels, where more high-bandwidth test functions will need to migrate on-chip. This natural evolution of embedded test will result in a new partitioning of functions between external and embedded test. This partitioning will be an ongoing process of shifts from the functions of external test to the embedded one maintaining the two components as complementary test segments.

Figure (2) External and Embedded Test



Mixing Technologies

Another implication of high complexity is mixing circuit types on a single IC. Monster chips are expected to comprise of non-homogeneous types of circuits. Today's complex chips have already started to mix diverse circuits, such as digital logic, embedded DRAM and analog blocks into a single IC. As chip integration technologies continue, more advanced circuits will be added to this list, such as embedded FPGA, Flash, RF/Microwave, and may even move beyond the electronics domain to contain micro-electromechanical (MEMS) and optical elements.

Different types of circuits exhibit distinct defect behavior and require different test solutions. Each type require different test Sources to generate the test data and Sinks to compare the responses. Typically, distinct external test equipment is used for each type of circuit. For example one tester for logic testing, one for embedded memory test and another for analog. The use of three external testers to test a single chip is termed as triple insertion and is considered an expensive proposition. An alternate solution offered by test equipment vendors is to use a "Super" tester, which combines the test capabilities of all three above testers. The super testers do not assume embedded test capabilities in the chip under test, hence they tend to contain all test features and therefore turn this solution to an extremely expensive one.

An easier and more cost effective way to handle these mixed circuit chips is by inserting embedded hardware Sources and Sinks corresponding to each circuit type, for example an embedded Source/Sink for digital logic, another for memories and a third for the FPGA circuit. Such an IC will not require more than a single, existing and lower-cost external tester.

System-on-Chip Test

Embedded core-based system-on-chip (SOC) design implies the reuse of pre-designed complex functional blocks, also called Virtual Components, Intellectual Property (IP). These embedded cores can come with different degrees of readiness for reuse in SOC design, from different sources, and are designed for use in a multiplicity of different SOCs. Being pre-designed, an embedded core may not only originate in a different organization, but it is also developed at a different time than the SOC that will use it. The embedded core design must be able to anticipate the desired SOC-level test constraints for all target SOC designs. Further, it must be possible to package the results of any enabled core-test in a form that is compatible with the test methodology contexts, and with the test-development tools available to the SOC designers who wish to reuse the core.

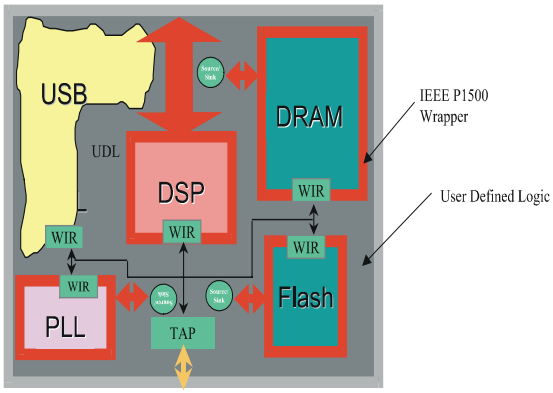
Core designs need to be more test-friendly to simplify the SOC integration task, while giving SOC designers more flexibility in choosing the best overall test methodologies for their chips. To ensure the test-friendliness and interoperability of cores from diverse sources, a standard for embedded core test in under development, namely IEEE P1500. The standard does not standardize a core's internal test methods or chip-level test access configuration. The standardization effort concentrates on:

- a standardized core test language (CTL), capable of expressing all test-related information to be transferred from core provider to core user; and
- a standardized - but configurable and scalable - core test wrapper, which allows easy test access of the core in a system chip design. The standard core test wrapper interfaces with an on-chip test access mechanism and may operates under several test modes (such as, internal, external, diagnosis, etc).

While it is possible to route the test access mechanism to the I/Os of the chips in order receive/transmit the test patterns from/to external test equipment, but it more practical and cost effective to use on chip test Sources and Sinks. They may be realized in two scenarios, either the embedded core would have a dedicated Source and Sink to perform its self-test; the test access mechanism connected to this core may obtain connect to a Source and Sink at the SOC or any other intermediate level. This is mainly meant for reusing the Source and Sink for more than one embedded core.

The most used cores today are the embedded memories. These cores have widely accepted the embedded Source and Sink approach. Most chip manufacturers have adopted memory BIST generation tools. As the monster chips incorporate more complex and larger numbers of embedded cores, such as microprocessors, analog blocks, and DSPs, the embedded Source and Sink approach need to be extended as the test solution of the other cores in an SOC.

Figure (5) System-on-Chip Test



The monster chips are expected to embed very dense memories of large sizes (256K - 64M bits). These dense memories may include: SRAMs, DRAMs and/or Flash memories. For more than a decade, the smaller scale memories have been embedded in mostly logic chips and became an integral part of the ASIC libraries. These memories were among the first to use on-chip Sources and Sinks. This is utilized during the manufacturing test to avoid using a dedicated external memory tester, in addition to the external logic tester used for the rest of ASIC. Beyond a certain size such as 256K bits, memories necessitate redundancy and repair during manufacturing test. This has been performed regularly for large stand-alone memory. This is typically a fuse blow process using external laser repair equipment.

Due to the large sizes of the its embedded memories, the monster chip needs to have redundant rows and columns to help reconfigure it, if there were faulty cells detected. For the same reasons as for the smaller memories, these will rely on embedded Sources and Sinks to generate and evaluate the test data. Moreover, since the memory response data is evaluated by the embedded Sink, the role of this Sink could be slightly expanded in order to perform diagnosis of the failed bits. Furthermore, to avoid sending a large failed bit map to the external test equipment via limited I/O bandwidth, the embedded Sink can be expanded further to perform built-in redundancy analysis in order to identify the actual rows and columns needed for reconfiguration. In this case, only the repair list can be

communicated to the external tester and hence the laser repair equipment can perform a hard repair.

The final augmentation of the embedded Source and Sink is to make the memory self-repairable. This is motivated by the fact that laser repair is often very expensive and some times continuous periodic field repair is desired. This will be achieved by expanding the embedded test resources even further to include a storage repair data and a soft reconfiguration mechanism. In summary, embedded test for very large memories may by required to move beyond fault detection to include failed bit diagnosis, redundancy analysis and self-repair.

3. Implications of increased Performance

With the continuous increase in IC internal speed, performance-related defect coverage has become increasingly important. The recent Sematech experiments have confirmed the criticality of performance-related tests. The 100 million transistor monster chip will necessitate a comprehensive performance test. Moreover, it has been predicted that Iddq test will lose its effectiveness for such chips due to higher sub-threshold currents. Most Iddq failures will probably be observed also as timing/performance anomalies.

A performance test that is applied from an external test equipment can not adequately and cost effectively test the high clock speeds and provide the necessary performance-related defect coverage. Because these equipment are typically made of older technology compared to the chips they test, and the higher speed test equipment are substantially more expensive. The SIA roadmap indicates that major yield losses and cost increases are related to the slower growth of external test equipment speeds versus the ever improving internal chip speed. While the external tester accuracy has improved at a rate of 12% per year, internal chip speeds have improved at 30% per year. Typical headroom of external testers five times faster than internal chip speeds have all but disappeared. With the current trend, cycle time of manufactured chips will approach external tester timing accuracy, see Fig. (6), in less than ten years. A crossover may occur near 2010, but by 2001, yield losses due to external test inaccuracy will be unacceptable.

If external test accuracy cannot keep up with the internal chip speed, our monster chip need to leverage the internal speed of its silicon and utilize dedicated embedded test resource for the tests that require timing precision. Because it is built on the same piece of silicon as the monster chip, an embedded test resource will have a cycle time comparable to the chip internal speed. Therefore, it will allow accurate performance-related tests and precision measurements, and eliminate the potential yield losses predicated by the SIA roadmaps.

4. Implications of Higher Density:

The continuous advancement in semiconductor technology will keep increasing the silicon density. The number of millions of transistors per sq. cm. will increase by a factor of three in the next five years. The density level resulted in a monster chip will have a number of test-related implications.

According to the SIA roadmaps, the increase in semiconductor density causes reduction in defect sizes. The complexity of monster chips on the one hand, and the reduction in their defect sizes on the other, cause a drastic increase in the difficulty in fault localization. The difficulty in localizing faults increases one order of magnitude every six years.

The best tool to perform fault localization and defect analysis in semiconductor manufacturing is the test process. The feedback loop derived from the test process is the only way to analyze and isolate many of the defects in manufacturing. Understanding failure mechanisms and providing corrective actions cannot occur without the ability to localize faults to an area that can be inspected in a practical and cost-effective manner.

The increased density in monster chips will severely challenge the physical fault localization processes. The hardware for embedded test scales with the chip itself. The existing embedded test resources whether in embedded memories, cores, user defined logic or analog blocks can act as the infrastructure to collect the faulty data from the block under test. This helps to quickly isolate faults. Leveraging the embedded test hardware resources can aid in defect isolation. The failure pattern must map to a physical location on a circuit. Software-based test tools compatible with major embedded test methodologies (such as, scan or BIST) are needed to save failure pattern information so that it can be analyzed based on predetermined failure mode information. This allows yield engineers to more quickly and precisely determine the location and causes for circuit failures.

Collecting more parametric data as measured on external test equipment will aid in sourcing unmodeled defect types. The continuous increase in density and in multi-level metal layers result in new fault models, which make the traditional stuck-at fault less effective. Recent studies show that few large-area spot defects are causing single defects, which affect multiple transistors and gates simultaneously. In general, to reduce the test escapes due to such unmodeled faults, pseudo-random

test patterns are used. A number of experimental studies showed the effectiveness of such pseudo-random patterns in reducing test escapes.

Signal integrity and electromagnetic phenomena will become an increasingly important test issue with the appearance of monster chips. New fault models including soft error models that incorporate the effects of electromagnetic fields need to be developed. The increase in soft errors is due to the reduction in device size and voltage supply, which cause an increase in noise sensitivity and an increase in susceptibility to cosmic variations, such as alpha particle radiation. The resulting soft errors, while not new for space oriented applications, will start to cause considerable risks on see level altitude. Due to their transient nature, soft errors need to be continuously monitored during the field operation of a chip. Hence, this will require dedicated hardware for embedded test, which performs on-line testing technique.

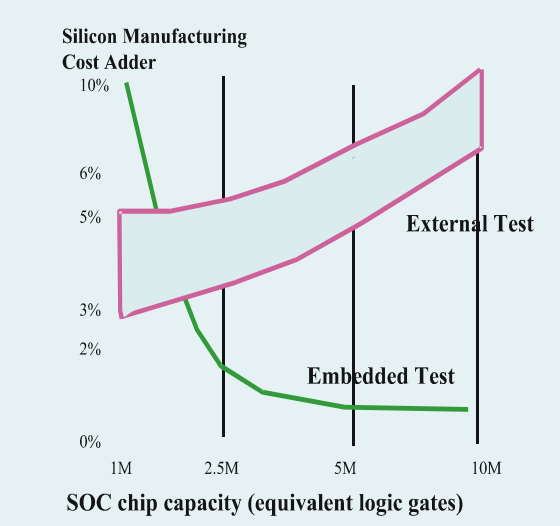
New embedded sensors to monitor different on-chip parameters should be developed to identify race conditions and other failure modes that are functions of parametric variations. These sensors will be an integral part of the embedded test infrastructure and leverage the existing chip level test data and control mechanisms. Handling the test data through signature analysis techniques would significantly reduce the need for hardware failure analysis. In fact, the more embedded test monitoring and on-chip data acquisition resources are used the less hardware diagnostics is required for silicon debug and failure analysis. Especially with the high density packages, such as flip-chips, hardware diagnosis will become more and more constrained. Because the conventional electron beam or thermal imaging technique will not apply to flip-chip attach technologies due to the fact that there is no front side accessibility. Very limited back side accessibility hardware diagnosis techniques can be used, such photon emission and scanned lasers, if defects are sensitive to them. New back side accessibility tools and solutions are needed.

In addition to fault localization and failure analysis, producing the monster chip requires integrated yield analysis capabilities that make use of the defect and failure analysis data. These capabilities need be in software tools to automatically access multiple databases and establish correlation between data of different types. Some data sources are time-based, others are chip-based or wafer-based. Automated data reduction algorithms to source defects from multiple data sources must be developed to reduce defect sourcing time. The SIA roadmap identified this as one of the key requirements for yield learning and improvement.

5. Implications of Reduced Cost:

Increasing cost of capital for external test equipment is one of three major test-related problems the SIA roadmaps had predicted. While the cost per pin for external test has remained essentially flat for the past 20 years at around $10K/pin. The demands for higher speed, greater accuracy, more time sets and increased data volume offset all the goals in cost reduction seen for improving external test equipment cost. In its 1997 roadmaps, SIA indicates that tester cost will reach $20M in year 2010, unless there is change in IC design incorporating more embedded test. It also predicts that by the same year, it may cost more to test a transistor than it costs to manufacture the transistor.

Figure (7) External vs. Embedded Test Cost



The cost of embedded test is in terms of additional silicon needed to incorporate the test functions and a limited impact on yield. A set of embedded Sources and Sinks for a state-of-the-art mixed circuit IC is about 10,000 logic gate equivalent, assuming that a scan infrastructure is already in place. For designs of about 400,000 to 500,000 gates, the relative silicon cost of embedded test is equals the cost of external test. For chips above this size, the silicon investment constitutes less than 1 percent of the silicon manufacturing costs, See Fig. (7). As for the yield impact, the Embedded Sources and Sinks increase the silicon area and hence can reduce manufacturing yield. Because, the bigger the chip area, the more chance of a particle falling on that chip and causing a defect. However, with the addition

of 10,000 gates on a monster chip of tens of Million of gates causes a negligible impact.

After it is successfully produced, a monster chip is deemed to become an integral part of a larger electronic system. The cost of test and diagnosis for such electronic systems, typically, reaches 40-50% of total product realization cost. If embedded test resources were incorporated into the chip, these resources can be reused hierarchically during board and system manufacturing. This reduces the time and cost required to develop diagnostic firmware and interfaces for board and system test and maintenance features. The concept of embedded test can be applied to every electronic assembly level, for instance, using chip level embedded test during board test; using board level embedded test during system/box test; and hardware/software use of the total embedded solution in the field test.

6. Conclusions:

The semiconductor scaling trends such as complexity, performance and density have major implications on testing the 100 million transistor chips. The industry has identified a number of hurdles as a result of such implications. Solving these hurdles require a new approach to testing, where the test functions are partitioned to two main components: embedded test and external test. The two complementary test components are needed, but the balance of functions in each component depends on numerous technological and economical factors.

The usage of embedded test hardware, which is invested on-chip, goes beyond plain chip test. This hardware provides a number of crucial test-related functions, such diagnosis, measurement, debug, failure analysis, and even repair. Also, the embedded test hardware is reused from cores test level, to chip, to board and system test levels.

External test and embedded test will be used simultaneously on most chip designs. As chips become more complex new functions will be transfer from the external test component to the embedded one.