Oscillation-Test Strategy for Analog and Mixed-Signal Integrated Circuits

Karim ARABI and Bozena KAMINSKA

Department of Electrical and Computer Engineering, École Polytechnique de Montréal
P.O.Box 6079, Station Centre-Ville, Montreal, Quebec, Canada H3C 3A7.

Abstract

A new low-cost test method for analog integrated circuits, called oscillation-test, is presented. During the test mode, the circuit under test (CUT) is converted to a circuit that oscillates. Faults in the CUT which cause a reasonable deviation of the oscillation frequency from its nominal value can be detected. Using this test method, no test vector is required to be applied. Therefore, the test vector generation problem is eliminated and the test time is very small because a limited number of oscillation frequencies is evaluated for each CUT. Due to its digital nature, the oscillation frequency can be easily interfaced to boundary scan. This characteristics imply that oscillation-test strategy is very attractive for wafer-probe testing as well as final production testing. In this paper, the validity of the proposed test method has been verified throughout some examples such as operational amplifiers and analog-to-digital converter (ADC).

1 Introduction

Due to the development of integrated circuit technology and the market requirements, the trend of designing mixed-signal ASICs has been increased. Analog testing is a chalenging task and is considered as one of the most important problems in analog and mixed-signal ASIC design. Unlike the digital systems, the specifications of analog circuits are usually very broad which results in long testing time, poor fault coverage and the requirement of a dedicated test equipment.

Testing analog circuits can be accomplished using, functional (and/or parametric) testing [1][2][3][4], DC testing [5][6], power-supply current (I_{DDQ}) monitoring [7][8], and digital signal processing (DSP) techniques. Various design for testability (DFT) rules have been used in conjunction with the mentioned test methods to increase the controllability and observability and to simplify the test problem.

The effectiveness of the above methods strongly depends on the selection of suitable test vectors. When the complexity of the CUT increases, the problem of generating optimal test vectors assuring high fault coverage becomes critical. Furthermore, the process of choosing a suitable form of excitation signals and results evaluation is time consuming. Built-in self-test structures based of the existing test methods require the use of specialized input stimuli generation and output evaluation hardware which introduce a significant area overhead. Some applications require a stimuli generator which guarantees a very good accuracy or supports a wide range of frequencies.

In an attempt to overcome some of the cited problems, a new vector-less test method for analog circuits has been developed and presented in this paper [9]. This test method has a digital output compatible with test methods employed for the digital part of the system. The paper is organized as follow. Section 2 is dedicated to present the new test method. Then, in the section 3, the proposed test strategy is applied to some analog and mixed-signal circuits. Fault coverage of the presented method is discussed in the section 4.

2 Oscillation Test Strategy (OTS)

We present, here in this paper, a new test method for analog and mixed-signal circuits based on rearranging the CUT to an oscillator [9]. In this method, the complex analog circuit is partitioned into functional building blocks such as: amplifier, operational amplifier (opamp), comparator, Schmitt trigger, filter, voltage reference, oscillator, phase lock loop (PLL), etc. or a combination of these blocks. During the test mode, by adding some additional circuitry, each building block is converted to a circuit producing sustained oscillations. The oscillation frequency f_{OSC} can be expressed either as a function of the CUT components or as a function of its important parameters. The building blocks that inherently generate a frequency such as oscillators do not need to be rearranged and their output frequency is directly evaluated. All operations are managed using control logic (CL).

Fig. 1 illustrates the application of the proposed test method as DFT technique to improve the testability and ease the test problem. In the test mode, the CUT is partitioned into building blocks that are converted to oscillators using some additional circuitry. Analog multiplexer (AMUX) selects the output of the building block under test and its oscillation frequency is externally evaluated using a test equipment. Before starting the test procedure, the functionality of the test circuitry is verified by activating *STest* signal.

0-8186-7304-4/96 $05.00 © 1996 IEEE

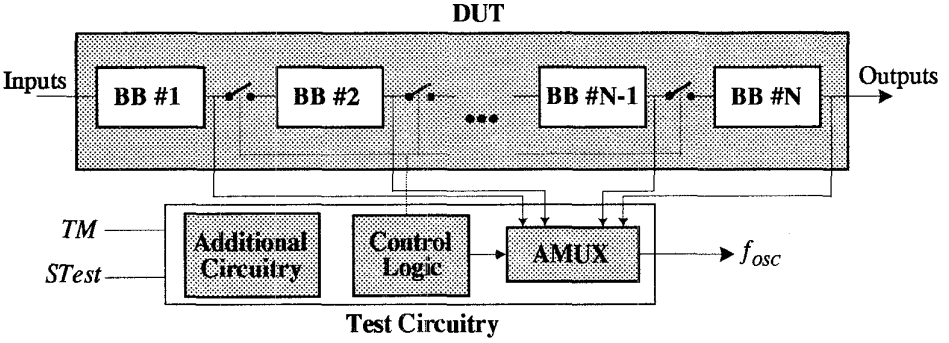

Fig. 1: Simplified test structure of oscillation-test strategy (BB: Building Block, *TM*: Test Mode, *STest*: Self-Test Mode, AMUX: Analog Multiplexer).

The most effective approach of converting an analog building block to an oscillator consists of adding an appropriate feedback loop to its structure and then to adjust the feedback elements to establish sustained oscillations. Depending on the CUT the feedback loop can be negative, positive or a combination of them.

We define the observability of a fault in a component C_i (or a parameter P_i) as the sensitivity of the oscillation frequency f_{OSC} with respect to the variations of the component C_i (or the parameter P_i). To increase the observability of a defect in a component (or a fault in a parameter), the sensitivity of the oscillation frequency with respect to that component (or parameter) should be increased. In the other words, during the conversion process of the CUT to an oscillator, the oscillator architecture must be chosen to insure the maximum possible of CUT components contribution in determining the oscillation frequency. Existing faults in the CUT related to components (or parameters) that are involved in the oscillator structure manifest themselves as a deviation of the oscillation frequency. Therefore, the deviation of the oscillation frequency from its nominal value may be employed to testify a fault. In this paper we address the problem of single fault detection.

The tolerance band of f_{OSC} for each CUT is determined using a Monte Carlo analysis taking into account the nominal tolerance of all important technology and design parameters. The accuracy necessary for additional circuitry is around the same accuracy provided for other CUT components.

3 Case Studies and Results

To be able to evaluate the proposed test method we first define our fault modeling. Then some analog and mixed-signal building blocks are used as test vehicles to examine the efficiency of the test method, but the method is by no means constrained to these examples in its application.

3.1 Analog Fault Modeling

In order to quantify the fault coverage of the presented test method an accurate and realistic fault list is required. A fault can be either parametric (soft) or catastrophic (hard). Parametric faults, caused by statistical fluctuations in the manufacturing process, comprise the small deviation of CUT parameters from their tolerance band. Catastrophic faults are introduced by random defects and result in failures in various components. They are provoked, for example, by dust particles on a photolitographic mask and cause either short and open circuits or large deviation of CUT parameters from their tolerance band such as width-to-length (W/L) ratio of a MOS transistor [10],[11].

Many studies have been devoted to determine the dominant fault type and to define the appropriate fault models. Research results denote that 80-90 percent of observed analog faults were catastrophic faults consisting of shorts and opens in diodes, transistors, resistors and capacitances [12],[13]. It was also found that a test method which detects 100% of catastrophic faults did also find the majority of soft faults depending on the deviation value of the soft fault [11]. The occurrence probability of faults has been also considered [14]. As a conclusion the studies indicate that catastrophic faults, and especially short faults, are dominant in both bipolar and CMOS processing technologies. Therefore, a comprehensive list of catastrophic faults is inducted and simulated for all case studies. A set of parametric faults is also injected depending on the CUT.

The catastrophic faults considered in this study comprise all possible shorts between circuit nodes and open faults at all circuit nodes excluding the transistor gates. An open fault is simulated by introducing a 10 M ohms resistor. A short fault is modeled by a 10 ohms resistor.

3.2 Operational Amplifier Testing

Operational amplifier is the most widely used linear circuit in analog and mixed-signal systems. For analog functional blocks with embedded opamps, the test procedure will be easier and the fault coverage will be higher if we assume that the opamps are fault-free. Therefore, the importance of developing an efficient technique to test opamps is obvious.

Fig. 2 shows the schematic presentation of a two-stage CMOS operational amplifier that is considered as the CUT. Before introducing the test technique, important characteristics of the opamp will be summarized.

The total amplifier dc open-loop gain is given by

$$a_V = \frac{g_{m3}g_{m9}}{(g_{ds6}+g_{ds7})(g_{ds8}+g_{ds9})} \quad (1)$$

where the channel conductances, g_m and g_{ds}, are defined as:

$$g_m = \frac{\partial i_D}{\partial v_{GS}}\Big|_{I_D} \cong \sqrt{(2\mu_o C_{OX} W/L)|I_D|} \quad (2)$$

$$g_{ds} = \frac{\partial i_D}{\partial v_{BS}}\Big|_{I_D} \cong I_D\lambda \quad (3)$$

in which, μ_o is the channel surface mobility, C_{OX} is the capacitance per unit area of the gate oxide, W and L are effective channel width and length respectively, and λ is the channel length modulation parameter of the transistor. I_D represents the quiescent current and is provided by M1, M2, and M5 transistors.

The unity-gain bandwidth of the opamp is calculated as follow

$$\omega_T = -a_V p_1 = g_{m1}/C_c \quad (4)$$

As the opamp is compensated, its transfer function can be approximated to a single pole transfer function given by

$$a_V(s) = \frac{a_V}{1-s/p_1} \quad (5)$$

$$a_V(s) = \frac{-a_V p_1}{s} \quad (s/p_1 >> 1) \quad (6)$$

in which p_1 represents its dominant pole.

Table 1 summarizes its important characteristics obtained using hspice in Analog Artist® environment with a 5 pF capacitor load.

In this example both positive and negative feedback loops have been added. Fig. 3 shows the schematic view of this oscillator. The positive feedback loop consists of an RC delay and the negative feedback comprises a voltage divider. To facilitate the mathematical analysis the combination of feedback loops is presented by a single negative feedback block in which the positive feedback appears as a term with negative sign. The feedback block converts the opamp under test to a second order system which has the potential of oscillation. The new transfer function is derived as follows

$$A_V(s) = \frac{a_V(s)}{1+a_V(s)f(s)} \quad (7)$$

where,

$$f(s) = G - \left(\frac{-s/p_2}{1-s/p_2}\right) \quad (8)$$

in which $G = R_2/(R_1+R_2)$ and p_2=-1/RC.

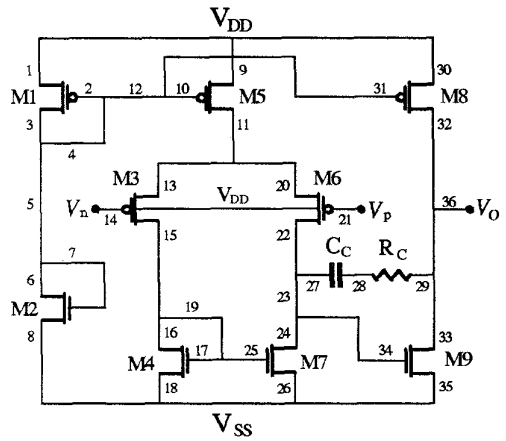

Fig. 2: Compensated CMOS operational amplifier.

Table 1: Important characteristics of the opamp.

Parameter	Simulation Results
Unity-gain bandwidth (f_T)	26 MHz
Gain at dc (a_V)	91.6 dB
Phase margin (φ_M)	72°
Slew rate (SR)	> 110 V/μs
Offset voltage (V_{OS})	2.8 μV

By substituting $a_V(s)$ and $f(s)$ in $A_V(s)$ we obtain

$$A_V(s) = \frac{a_V p_1(p_2-s)}{s^2+((1-G)a_V p_1-(p_1+p_2))s+(Ga_V p_1 p_2+p_1 p_2)} \quad (9)$$

The system poles are obtained by equating the denominator of the new transfer function to zero. In order to construct an oscillator from this new transfer function, its poles must be placed on the imaginary axis on the s domain by forcing the coefficient of the term s to zero which is realized by proper selection of the value of G as follow

$$G = 1 - \frac{p_1+p_2}{a_V p_1} \quad (10)$$

The natural oscillation frequency for the new system is given by

$$\omega_{osc}^2 = Ga_V p_1 p_2 + p_1 p_2 = a_V p_1 p_2 - p_2^2 \quad (11)$$

Assuming RC = 10^{-7}, we found G ≈ 0.94 to establish sustained oscillations. The oscillation frequency, f_{OSC}, obtained by simulation is approximately 6 MHz. This oscillation frequency strongly depends on important characteristics of the opamp under test which are determined by all components of the opamp. Existing faults in the opamp will deviate its characteristics from their nominal value which can be monitored by observing the oscillation frequency. We have practically implemented the above oscillator to verify the equation (11) using μA 741 operational amplifier and discrete components. Practical result is very close to predicted theoretical oscillation frequency.

In order to quantify the fault coverage of the presented test solution for operational amplifiers a comprehensive list of catastrophic faults has been injected and the oscillation frequency has been evaluated. In this particular case the majority of injected faults resulted in loss of oscillation. The remaining injected faults caused significant deviation of the oscillation frequency from its tolerance band. Table 2 presents the result of the fault simulation for the faults which preserve the oscillations. For the sake of simplicity, faults which result in the loss of oscillation are not presented in this table. Besides, only one fault of each schematically redundant fault set is presented in the table. As the results demonstrate, all injected faults have been manifested themselves by affecting the oscillation frequency and can be therefore detected. The output oscillation frequency f_{OSC} in presence of some typical faults is depicted in Fig. 6.

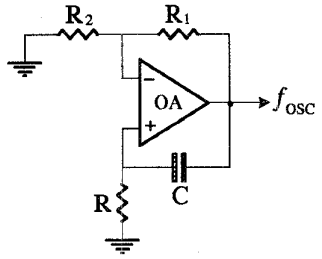

Fig. 3: Single-opamp sinusoidal oscillator.

Table 2: CMOS opamp faults which preserve the oscillations

Fault	Output Voltage Level (V)	Output Oscillation Frequency
N9,11-S*	<-4.01 , 3.03>	$f_O \approx 1.2\, f_{OSC}$
N31,32-S*	<-2.47 , 2.8>	$f_O \approx 0.85\, f_{OSC}$
N28,29-S*	<-4.53 , 4.76>	$f_O \approx 0.86\, f_{OSC}$
N28-O*	<-4.63 , 4.72>	$f_O \approx 1.85\, f_{OSC}$

N9,11-S: Short between nodes 9 and 11. N28-O: Open at node 28. *: Representing a set of schematically redundant faults.

Many other simple opamp-based oscillators can be employed to test operational amplifiers. An oscillator structure [15] which is suitable for testing two opamps together is shown in Fig. 4. This oscillator is a simple sinusoidal oscillator using opamps compensation poles and therefore its oscillation frequency tightly depends on the opamps internal structure. This oscillator represents a smaller area overhead than the previous oscillator. The condition of oscillation and the frequency of oscillation (f_{OSC}) are given by

$$p_2 = a_{V_{OA1}} p_{OA1} \quad (12)$$

$$\omega_{osc}^{\ 2} = a_{V_{OA1}} p_{OA1} a_{V_{OA2}} p_{OA2} \quad (13)$$

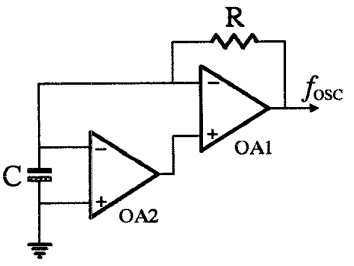

Fig. 4: A DFT technique of OTS to convert two opamps to a sinusoidal oscillator (R= 7 KΩ and C= 1 pF).

where $a_{V_{OAi}}(s) = -a_{V_{OAi}} p_{OAi} / s$ and the term $a_{V_{OAi}} p_{OAi}$ represents the unity-gain bandwidth of the ith op-amp (OAi).

The oscillation frequency is equal to the geometric mean of gain band-width of two op-amps. We have applied the procedure of exhaustive catastrophic fault injection and detection as explained for the single-opamp oscillator. The faults maintaining oscillation frequency are shown in Table 3. As the faults which result in the loss of oscillation are very numerous, they are not presented in this table. To simplify the presentation, only one representing fault of each set of schematically redundant faults is presented in the table. A simple oscillation frequency evaluation process detects around 99% of the exhaustive list of injected faults. The majority of undetected faults can be monitored by analyzing the voltage level of the oscillating signal.

3.3 Dual-Slope ADC testing

The test strategy proposed in this paper has been applied to a dual-slope ADC system as an example of a more complete mixed-signal circuit. Fig. 5 illustrates the block diagram of a testable dual-slope ADC based on oscillation-test method. The property of integrating the input signal, makes this converter immune to noise. The analog part of the converter comprises an integrator and a comparator.

At the first test phase, by adding R_a and R_b, the existing integrator and comparator are rearranged to a multivibrator whose oscillation frequency and oscillation condition are given by

$$f_{osc} = \frac{1}{4RC}\left(\frac{R_b}{R_a}\right) \quad (14)$$

$$R_b > R_a \quad (15)$$

Equation (14) assumes that the opamps are ideal and does not include the effect of opamps internal characteristics. These effects can be neglected when the opamps are fault-free, but when there is a fault in the opamps they influence the oscillation frequency. The output voltage of OA1 oscillates between -4.7 V and 4.8 V at the frequency of 0.717 MHz.

Table 3: Comprehensive list of catastrophic faults in OA1 and OA2 which deviate the oscillation frequency.

Fault	Output Voltage Level (V)	Output Oscillation Frequency	Fault	Output Voltage Level (V)	Output Oscillation Frequency
OA1N1-O	<-1.98 , 3.1>	$f_O \approx 1.49\, f_{OSC}$	OA1N28-O*	<-4.51 , 4.67>	$f_O \approx 2.23\, f_{OSC}$
OA1N3-O	<-2.01 , 3.19>	$f_O \approx 1.50\, f_{OSC}$	OA2N1-O	<-4.05 , 4.2>	$f_O \approx 1.01\, f_{OSC}$
OA1N6,8-S*	<-2.03 , 3.12>	$f_O \approx 1.49\, f_{OSC}$	OA2N3-O	<-4.05 , 4.2>	$f_O \approx 1.01\, f_{OSC}$
OA1N6-O	<-0.48 , 0.33>	$f_O \approx 0.12\, f_{OSC}$	OA2N6,8-S*	<-4.02 , 3.8>	$f_O \approx 1.02\, f_{OSC}$
OA1N8-O	<-0.47 , 0.35>	$f_O \approx 0.11\, f_{OSC}$	OA2N16-O	<-0.7 , 4.55>	$f_O \approx 0.04\, f_{OSC}$
OA1N16-O	<-4.49 , 4.97>	$f_O \approx 0.6\, f_{OSC}$	OA2N18-O	<-1.6 , 4.58>	$f_O \approx 0.04\, f_{OSC}$
OA1N18-O	<-4.57 , 4.99>	$f_O \approx 0.7\, f_{OSC}$	OA2N9,11-S*	<-4.58 , 3.26>	$f_O \approx 0.9\, f_{OSC}$
OA1N9,11-S*	<-4.59 , 4.68>	$f_O \approx 1.59\, f_{OSC}$	OA2N10,11-S*	<-2.74 , 3.34>	$f_O \approx 1.29\, f_{OSC}$
OA1N10,11-S*	<-4.1 , 2.28>	$f_O \approx 1.34\, f_{OSC}$	OA2N31,32-S*	<-4.23 , 3.97>	$f_O \approx 0.92\, f_{OSC}$
OA1N31,32-S*	<-2.68 , 2.89>	$f_O \approx 1.26\, f_{OSC}$	OA2N5,22-S*	<-4.51 , 2>	$f_O \approx 1.08\, f_{OSC}$
OA1N5,15-S*	<-3.35 , 4.33>	$f_O \approx 1.39\, f_{OSC}$	OA2N28,29-S*	<-4.8 , 4.50>	$f_O \approx 0.83\, f_{OSC}$
OA1N28,29-S*	<-4.58 , 4.14>	$f_O \approx 0.76\, f_{OSC}$	OA2N28-O*	<-4.50 , 3>	$f_O \approx 0.93\, f_{OSC}$

OA1N1-O: Open at the node 1 of the OA1, OA1N6,8-S: Short between nodes 6 and 8 of the OA1, *: Representing a set of schematically redundant faults.

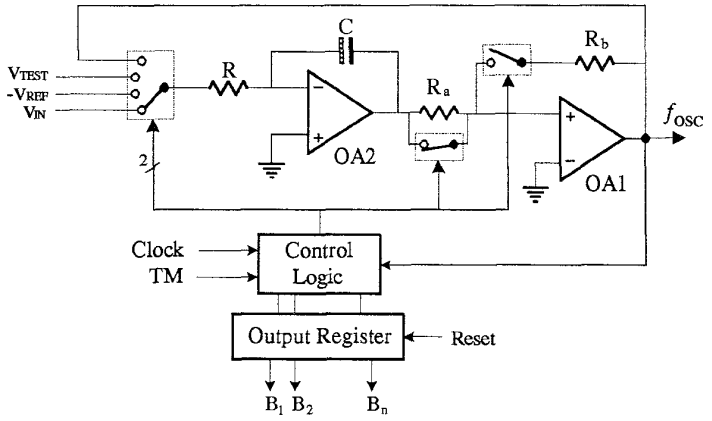

Fig. 5: Block diagram of a testable dual-slope ADC system based on OTS.

The oscillation frequency is converted to a number by the existing counter. The obtained number is compared with a predetermined test signature to verify whether there is a fault in the analog part of the ADC or not. At the second test phase the ADC is rearranged to its functional mode and a test voltage (V_{TEST}) is converted to digital. The digital number is compared with the second test signature to verify the functionality of the digital part of the ADC and also the V_{REF}. All operations are directed by the control logic. In this way, the ADC internal blocks which contribute in the test structure are tested. The simplicity and efficiency of this test architecture is obvious. The area overhead is related to two resistors (R_a and R_b) and a small part of the control logic. The test time is very short because the test is performed in two phases equivalent to the time needed to convert two analog signals using the ADC under test.

This example proposes an approach which consists of combining different building blocks such as Schmit trigger, comparator, integrator and amplifier to construct an oscillator. Fault induction and simulation procedure has been exercised for a complete list of catastrophic faults completed by some parametric faults. The results, show that a high fault coverage can be achieved. Table 4 illustrates the result of fault injection and simulation for the analog part.

Oversampled and sigma-delta ADCs have similar analog part and therefore can be tested using the same technique.

4 Fault Coverage

For all case studies presented in this paper, a comprehensive list of hard faults have been inducted and simulated. The results confirm that a high fault coverage can be achieved by only output frequency value evaluation. The reason for such a good fault coverage resides in the following facts.

Table 4: Typical list of possible faults in the analog part of the ADC which preserve the oscillations.

Fault	Output Voltage Level	Output Oscillation Frequency
OA1N14-O	<-4.48 , 4.65>	$f_O \approx 0.69 f_{OSC}$
OA1N10,11-S*	<-4.7 , 4.8>	$f_O \approx 0.91 f_{OSC}$
OA2N10,11-S*	<-4.6 , 4.84>	$f_O \approx 1.1 f_{OSC}$
R-S	<-4.65 , 4.6>	$f_O \approx 9.89 f_{OSC}$
C-O	<-4.67 , 4.82>	$f_O \approx 7.11 f_{OSC}$
R (30%↓)	<-4.7 , 4.8>	$f_O \approx 1.43 f_{OSC}$
R (30%↑)	<-4.7 , 4.8>	$f_O \approx 0.77 f_{OSC}$
C (30%↓)	<-4.7 , 4.8>	$f_O \approx 1.25 f_{OSC}$
C (30%↑)	<-4.7 , 4.8>	$f_O \approx 0.83 f_{OSC}$

OA1N14-O: Open at node 14 of OA1, OA1N10,11-S: Short between nodes 10 and 11 in OA1', *: Representing a set of schematically redundant faults.

1. Operational amplifiers have at least two stages of amplification which results in a very high gain. In the majority of applications, a feedback loop is added to establish the gain to a small but stable value which causes the redundancy in the opamp-based analog circuits. In that case the faults which decrease the open loop gain by a factor of 2, for example, will not affect the opamp-based circuit performance. In the test structures presented in this paper the oscillation frequency depends directly on the intrinsic characteristics of the opamps and therefore such kind of faults can be also monitored.
2. There are three sources of imprecision in analog testing: the imprecision related to the analog test vectors, the acceptable tolerance of the CUT, and the imprecision of voltage references and signature evaluations. During the test process the acceptable performance deviation range must be enlarged to allocate these three sources of error because they may exist even if the CUT is fault free. In the OTS based test structures, the first source of error is eliminated because no test vector is required to be applied. The third error source is also minimized, because the reference value is normally a frequency rather than a voltage which is easily converted to a number without significant precision degradation.
3. In a given oscillator, the oscillation frequency depends on a wide range of the ac behavior of its transfer function with variable sensitivities. For example, in a band-pass based oscillator, the oscillation frequency depends on the entire range of its open-loop ac behavior having greater than unity gain. In fact, the oscillation frequency can be considered as the sum of frequency components which can pass through the band-pass system with an amplification. Therefore a change in any of this components will affect the oscillation frequency. When testing this band-pass system with a specified test frequency, based on conventional test methods, reliable information about the ac behavior of the rest of the transfer function can not be achieved. In practice, many test frequencies should be applied to assure a complete coverage over the ac behavior of the CUT. The sum of this test frequencies can be applied to the band-pass system as a multitone test frequency. In this case the ac behavior coverage is comparable to the coverage obtained by the evaluation of the oscillation frequency in oscillation-test strategy.

5 Conclusion

A new vector-less dynamic test strategy based on converting the CUT to a circuit which is easier to test has been proposed and evaluated for some typical analog and mixed-signal building blocks. The experimental results affirm the robustness of oscillation-test method and show that a high fault coverage, reduced test time, very simple test procedure can be obtained. This test technique eliminates the need for costly specification tests and may be considered as a low-cost test method because no complicated circuit overhead is required. In order to increase the efficiency of oscillation-test method, the testability must be considered early during design process. As the results indicate, the quantity of information about the CUT can be increased by simultaneous frequency and voltage level value evaluation of the output oscillation frequency or applying FFT technique to analyze the output oscillating signal. Our future work is to apply the proposed test method as a practical BIST solution for mixed-signal circuits.

References

[1] Wey, C.-L, "Built-In Self-Test Structure for Analog Circuit Fault Diagnosis," *IEEE Transactions on Instrumentation and Measurement*, vol. 39, no. 3, 1990, pp. 517-521.

[2] Milor, L. *et al.*, "Optimal Test Set Design for Analog Circuits," *IEEE ICCAD*, 1990, pp. 294-297.

[3] Fasang, P.P., D. Mulins, and T. Wong, "Design for Testability for Mixed Analog/Digital ASICS," *IEEE Custom Integrated Circuit Conf.*, 1988, pp. 16.5.1-16.5.4.

[4] Wagner, K.D., and T.W. Wiliams, "Design for Testability of Mixed Signal Integrated Circuits," *IEEE Int. Test Conf., 1988*, pp. 823-829.

[5] Marlett, M.J., and J.A. Abraham, "DC IATP-An-Iterative Analog Circuit Test Generation Program for Generating Single Pattern Tests," *IEEE Int. Test Conf.*, 1988, pp. 839-844.

[6] Devarayanadurg, G., and M. Soma, "Analytical Fault Modeling and Static Test Generation for Analog ICs," *IEEE ICCAD*, 1994, pp. 44-47.

[7] Gielen, G., Z. Wang, and W. Sansen, "Fault Detection and Input Stimulus Determination for the Testing of Analog Integrated Circuits Based on Power-Supply Current Monitoring," *IEEE ICCAD*, 1994, pp. 495-498.

[8] Nigh, P., and W. Maly, "Test Generation for Current Testing," *IEEE Design & Test of Computers*, vol. 7, no. 2, 1990, pp. 26-38.

[9] Arabi, K. and B. Kaminska, "Oscillation-Based Test Strategy (OBTS) for Analog and Mixed-Signal Circuits," *US Patent Application*, 1995.

[10] Milor, L. and V. Visanathan, "Detection of Catastrophic Faults in Analog Integrated Circuits," *IEEE Trans. on Computer Aided Design*, vol. 8, no. 2, 1989, pp. 114-130.

[11] Ohltz, M.J., "Hybrid Built-In Self-Test (HBIST) structure for Mixed Analog/Digital Integrated Circuits," 2nd European Test Conference, 1991, pp. 307-316.

[12] Stapper, C., F. Armstrong, and K. Saji, "Integrated Circuit Yield statistics," *Proc. IEEE*, vol. 71, 1983, pp. 453-470.

[13] Wilson, Q.F., and D.B. Day, "Practical Automatic Test Program Generation Constraints," *Proc. Automatic Test Conf. and Workshop*, 1987.

[14] Banerjee, P., and J.A. Abraham, "Fault Characterization of VLSI MOS Circuits," *IEEE Int. Conf. Circuits and Computers*, 1982, pp. 564-568.

[15] Senani, R. "Simple Sinusoidal Oscillator Using Opamp Compensation Poles," *Electronic Letters*, vol. 29, no. 5, 1993, pp. 452-453.

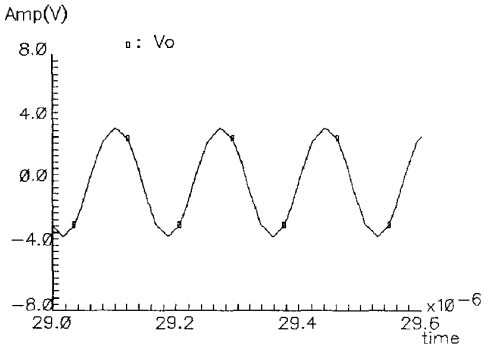

Fig. 6(a)

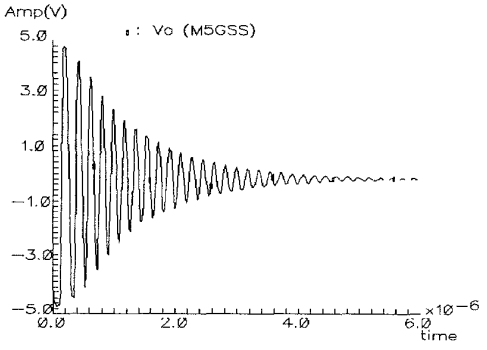

Fig. 6(b)

Fig. 6: Single opamp oscillator output. (a) without fault, (b) with the fault M5GSS (Short circuit between gate and source of tansistor M5)

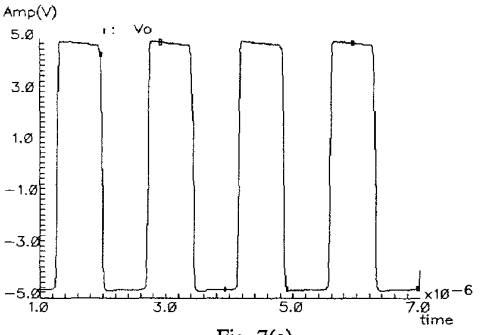

Fig. 7(a)

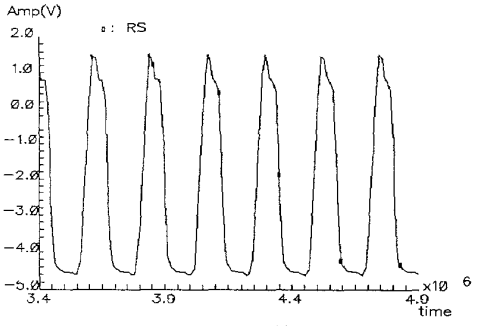

Fig. 7(b)

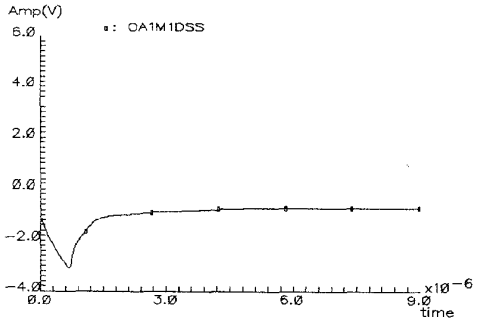

Fig. 7(c)

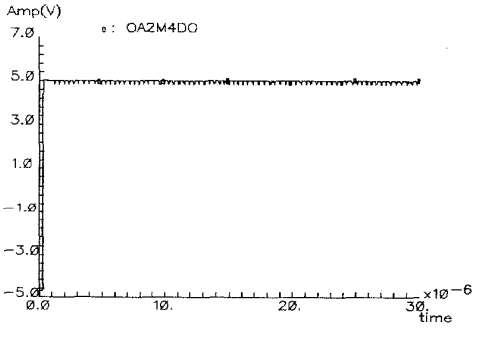

Fig. 7(d)

Fig. 7: Multivibrator output signal for some typical faults. (a) without fault, (b) Short fault at resistor S, (c) Short between drain and source of transistor M1 of OA1, (d) Open fault at drain of transistor M4 of OA2