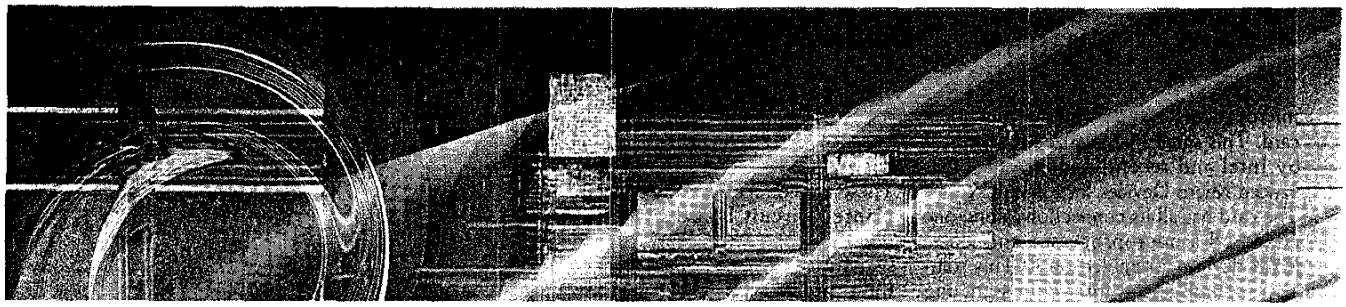

Testing the

Chips with 100 million transistors demand a new approach to testing—*complementary* embedded and external test

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The market-driven electronics industry never slackens. Thanks to the swift advance of semiconductor technology, companies can and continually do introduce products with more functions, higher reliability, lower costs, and at shorter intervals. ICs are considered the foundation of even traditionally nonelectronic products. So cheap are they, and so widely available, that whole industries now live off integrating ever more functions into ever smaller packages, even to creating entire systems-on-a-chip.

Arguably, some success of the economy-at-large for at least the next decade hinges on the speed with which complex new chips, and the products using them, not only can be developed and manufactured but also have their performance tested, diagnosed, and verified. At some point, 100-million-transistor monster chips are expected to emerge. But before then, as the National Technology Roadmap for Semiconductors spelled out in 1997, major hurdles must be overcome, some of which are related to test technology. Hardly surprisingly, the obstacles tie in with semiconductor advancements, and a variety of solutions is possible. One goal they share is to ensure that test methods contribute to the growth of the semiconductor industry and do not slow it down.

Testing serves twin functions in IC manufacturing: go/no-go testing at the end of the production line and defect analysis during diagnosis. Performed repeatedly during volume production, testing screens the ICs, probing wafers even before they are diced and the chips installed in packages. Feedback from IC test "informs" the analysis and diagnosis of many of the defects that occur in semiconductor manufacturing. Time-to-yield, time-to-market, and time-to-quality are all gated by test.

IC test is also used for debug, diagnosis, and repair of subassemblies at each new physical assembly level: board, subsystem, and system. Most users of high-end products even use it in the field, performing periodic tests throughout a product's full life cycle, to enhance reliability, availability, and serviceability,.

On the thorny road to the fabrication of monster chips, semiconductor technology will challenge IC test as never before. Complexities, performance, and densities, not to mention cost, will all increase.

To keep these scaling trends going, IC realization methods are expected to change fundamentally, directly affecting the test methods, tools, and equipment adopted. Otherwise, 100-million-transistor chips will not be adequately tested, debugged, diagnosed, measured, or even sometimes repaired. All four scaling trends have implications for test: every one of them challenges present ability to efficiently create new products. It is not sufficient to address just one of the challenges; all must be dealt with at the same time.

What complexity implies

Progressively greater IC complexity raises several new problems and exacerbates others. One is the bandwidth gap between a chip's internal performance and the output capability of its package pins. Another is the increasing use of mixed circuitry on a chip. Then there is the difficulty of repairing a chip-embedded memory.

Moore's law predicts the growth rate of transistor count per chip over time. The consequences of that prediction are laid out in the 1998 update to the International Technology Roadmap of Semiconductors (ITRS), produced under the sponsorship of the Semiconductor Industry Association (SIA), in San Jose, Calif. The growth rate in IC transistor count is far higher than the rate for IC pins and

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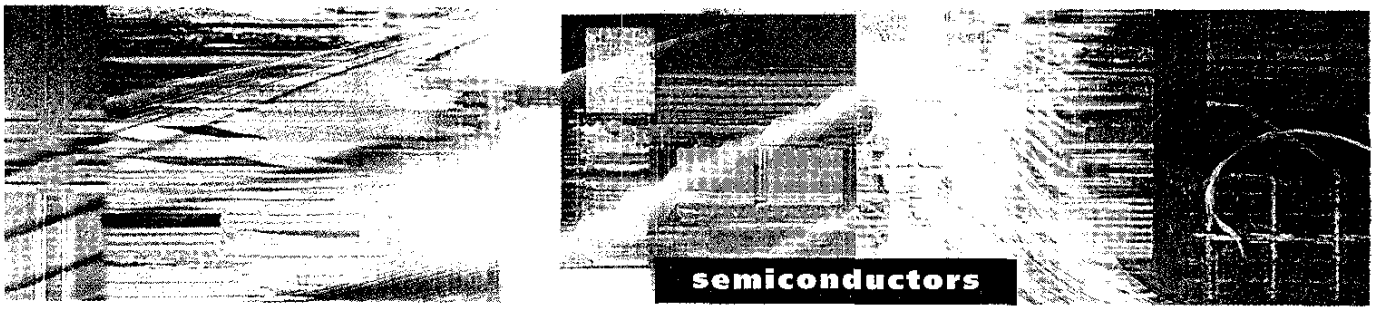
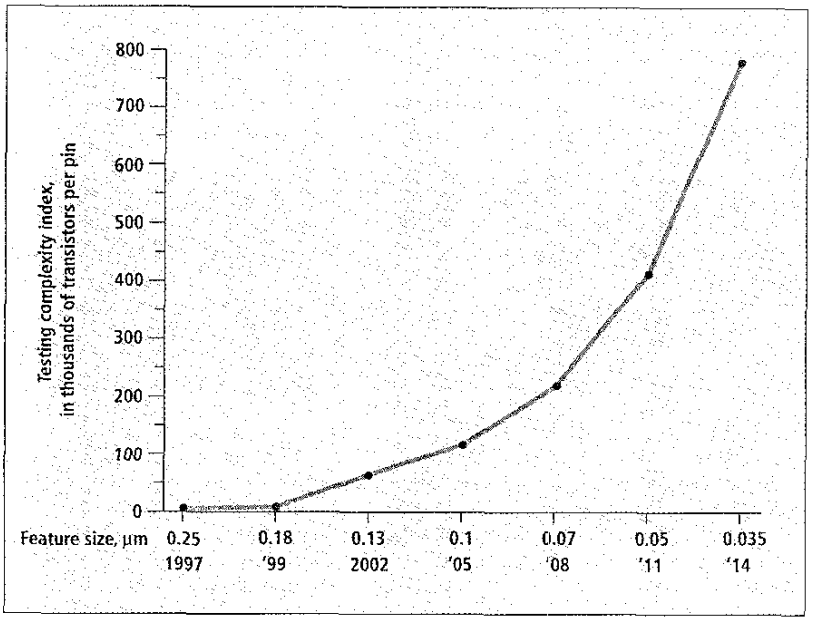


monster chip



[1] The 1998 update of the International Technology Roadmap for Semiconductors, sponsored by the Semiconductor Industry Association, San Jose, Calif., predicts significant increases in the number of transistors per pin even as the feature size shrinks dramatically—exacerbating the test process by constricting the accessibility of the transistors through the chip pins.

Bandwidth:	Internal	1	3.165	19.52	85.26	375.35	1621.62	7132.76
	External	1	1.97	3.59	6.14	10.5	17.24	28.89
		1997	1999	2002	'05	'08	'11	'14

Source: 1998 International Technology Roadmap for Semiconductors

[2] The ability to reach into a chip for (external) test is hampered by an I/O, or external, bandwidth (the number of I/Os times the I/O switching rate in megahertz) far smaller than the internal bandwidth (the number of transistors per chip times the internal switching rate).

steadily reduces the accessibility of transistors from chip pins—a big problem for IC test [Fig. 1]. The ITRS was a collaborative effort among interested parties (industry manufacturers and suppliers, government organizations, consortia, and universities) aimed at updating the SIA's 1997 roadmap.

Further complicating test is the number of state spaces created as a result of all the state machines deployed in a monster chip. If all of the transistors (gates) were combinational in nature, this would not be so; for a finite (if large) number of transistors, only the input and output would matter during test. In reality, however, the "middle" counts, too, and those gates, transistors, and state machines must be tested somehow. Obviously, the more middle pieces there are, the greater the test complexity, and the greater value the test results have.

Limited I/O portends more than access difficulties. The growing disparity between internal clock frequencies and the output capability of I/Os makes at-speed testing of IC performance extremely difficult, if not impossible. Combine the

roadmap numbers for transistor count, chip I/O count, chip internal frequency, and I/O switching speeds, and it is clear that the rate at which the available I/O bandwidth grows (number of I/Os times I/O switching speed) lags far behind the rate at which information can be generated and moved inside a chip (referred to as internal bandwidth and defined as the number of transistors per IC times internal switching frequency) [Fig. 2].

At the same time, the cost of package pins declines much more slowly than transistor cost. After all, chip attachment and board manufacturing constraints dictate that the physical characteristics of I/Os stay on the macroscopic level, while silicon feature sizes dive from a micrometer to a nanometer world. In other words, the crowd of transistors behind each chip I/O keeps swelling, as does the performance gap between them.

This widening gap between external and internal bandwidth is the main reason why processors and dynamic RAMs are now being integrated into the same chip. In the dawn of IC technology, 100 transistors might sit on a chip, interacting through the not-so-much-smaller bandwidth of chip I/Os. This negligible bandwidth gap was a boon to chip test methods. Test data was applied to chip I/Os directly from an external source, and the response data was received from the chip I/Os and evaluated for its correctness by an external sink [Fig. 3, top left]. The external test equipment consisted of this combination of source and sink, its test control software, plus an external test access mechanism for connecting the IC pins to the source and sink.

With the next generation of IC technology, the transistor-per-pin ratio became 1000:1. As dependence solely on external test equipment was out of the question, there arose the idea of embedding test capabilities in the chip's internal transistors, beyond its primary I/Os. An early embedded-test technique was scan path, which reduced test complexity by extending the test access mechanism into the internal transistors [Fig. 3, top right]. The process of embedding test circuits into a chip design became known as design-for-testability. Embedded test hardware—scan paths, in this case—facilitated the transport of test data from the chip I/Os and applied it to numerous internal transistors.

Clearly, the volume of test data needed for a certain level of fault coverage grows with the transistor count of the IC under test. For embedded test based on scan paths, the growth rate in test data is proportional to the growth in transistor count. Because the external source and sink supply all stimulus and response data through the chip I/Os, the pin buffer depth needed to apply the test must keep pace with the transistor-to-pin ratio. Complexities beyond a million transistors per IC, however, began to exceed the scope of pin buffer depth. With this same IC generation, too, external test equipment was confronting another unavoidable hurdle: the truly drastic increase in silicon speed.

To test an IC at its system speed, a semiconductor producer might try to depend on the external source and sink. But the approach necessitates high-bandwidth test interaction between the IC and its external source and sink—a feat often beyond external test equipment [Fig. 3, bottom left].

An alternative was to introduce low-bandwidth communication with the IC by shifting certain external test features onto the IC. The external test equipment kept those source and sink features requiring only low-bandwidth interaction and surrendered those features oriented to test speed and data volume, in the process becoming far less complex [Fig. 3, bottom right].

In operation, the embedded source performs an expansion function by generating at speed a large volume of test data for application to the circuit under test; the embedded sink collects the response data and performs an at-speed compaction function. The result: at-speed performance test. Without some such scheme, at-speed test might have been impossible, since external test equipment is often built using yesterday's technology. But while embedded source and sink circumvent the bandwidth limit of the external test equipment, they do not perform total built-in self-test (BIST) because they still depend on that equipment.

As technology graduates to chips with 100 million transistors and more, the gap in bandwidth between external and embedded test will again widen. Still more high-bandwidth test functions will need to migrate on chip, and a new partitioning of functions between external and embedded test will be in order. The partitioning will be an ongoing shifting of functions between the two test locations while maintaining them as complementary test segments.

Mixed-circuits test

High complexity also implies leeway to mix assorted circuit types on a single IC. Monster chips are expected to comprise nonhomogeneous types of circuits. Today's complex chips have already started to mix, say, digital logic, embedded dynamic RAM, and analog blocks on a single IC. As chip integration technologies press ahead, this list will accrue more advanced circuits—such as embedded field-programmable gate arrays (FPGA), flash memory, and RF/microwave types—and may even move beyond the electronics domain to include optical and microelectromechanical (MEM) elements.

This development brings new complications. Different circuit types exhibit distinct defect behavior and call for distinct testing. Each type requires different test sources and sinks, the first to generate the test data and the second to compare the responses, and usually dedicated external test equipment—one tester for logic testing, say, one for embedded memory test, and still another for analog testing. The use of three external testers for a single chip is known as triple insertion and is held to be an expensive proposition [Fig. 4, left]. An alternative solution proffered by test equipment vendors is to use a so-called super-tester, which combines the test capabilities of all three of those testers. But again this solution is extremely expensive: as the super-testers do not assume embedded test capabilities in the chip under test, they tend to contain all test features.

An easier and more cost-effective way to handle mixed-circuit ICs is to embed hardware sources and sinks that correspond to each circuit type—perhaps an embedded source or sink for digital logic, another for memories, and a third for the analog blocks. Such an IC will require only a single, existing, and lower-cost external tester [Fig. 4, right].

System-on-chip test requirements

System-on-chip (SOC) design based on embedded cores implies reuse of previously designed complex functional blocks, also called virtual components or intellectual property (IP) blocks [Fig. 5]. These embedded cores may have varying degrees of readiness for reuse in SOC design, may stem from varied sources, and are designed for use in a multiplicity of diverse SOCs. An embedded-core design may not only originate in another organization, but have been developed at a different time from the SOC that will use it. Yet it must be able to anticipate the desired SOC-level test constraints for all target SOC designs. Further, it must be possible to disseminate the results of any enabled core-test to SOC designers who wish to reuse the core. So they must be packageable in a form compatible with both the test methodology contexts and the test-development tools available to would-be reusers.

The SOC integration task would be simpler if core designs were more test-friendly, and SOC designers would have more flexibility in choosing the best overall test methodologies for their chips. Consequently, the IEEE P1500 standard for embedded-core test is under development. Its goal is to ensure the test-friendliness and interoperability of cores from diverse sources. But instead of standardizing a core's internal test methods or chip-level test access configuration, it concentrates on a standardized core test language (CTL) and a standardized, but configurable and scalable,

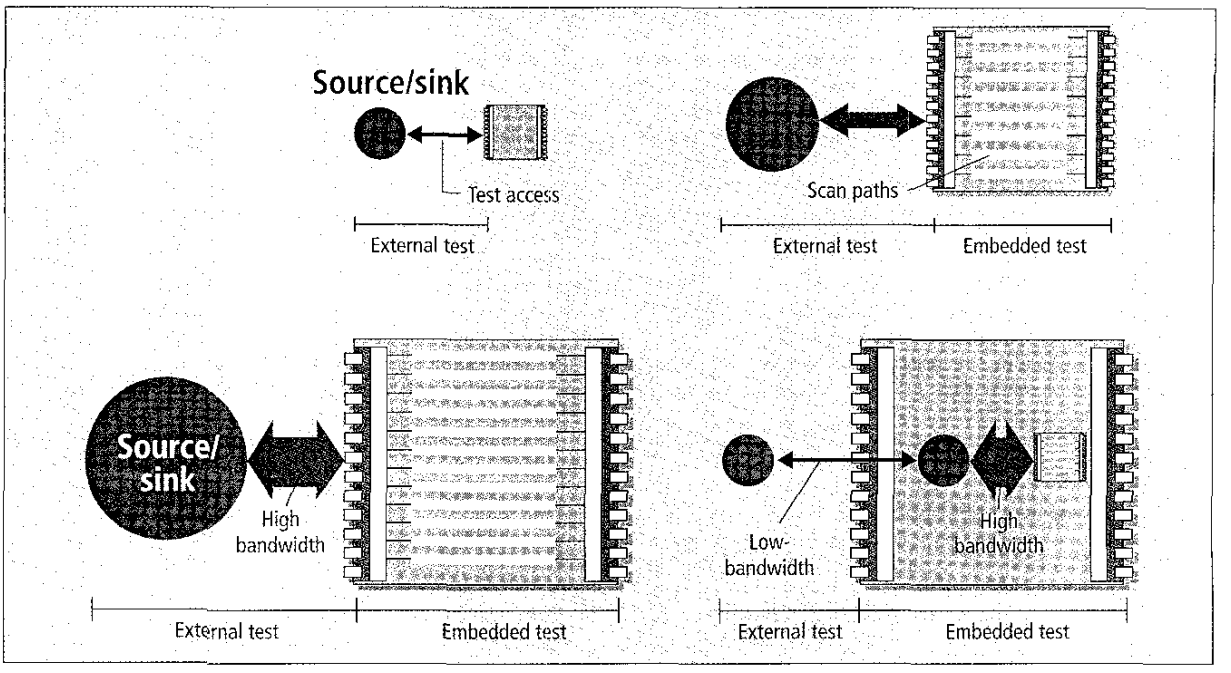
core test wrapper. The CTL must be capable of expressing all test-related information to be transferred from core provider to core user. The wrapper must allow easy test access to the core in a system chip design, interfacing with an on-chip test access mechanism and maybe operating in several test modes, say, internal, external, or diagnostic. These wrapper test modes are switched via the IEEE P1500 wrapper instruction register (WIR).

To repeat, routing the test access mechanism to the chip I/Os so that test patterns are received from and transmitted to external test equipment is not feasible. The use of on-chip test sources and sinks is more practical and cost-effective. There are two scenarios. The embedded core may have a dedicated source and sink to perform its self-test. Alternatively, the test access mechanism connected to this core may connect to a source and sink at the system on a chip or any other intermediate level. The latter approach is mainly for use with more than one embedded core.

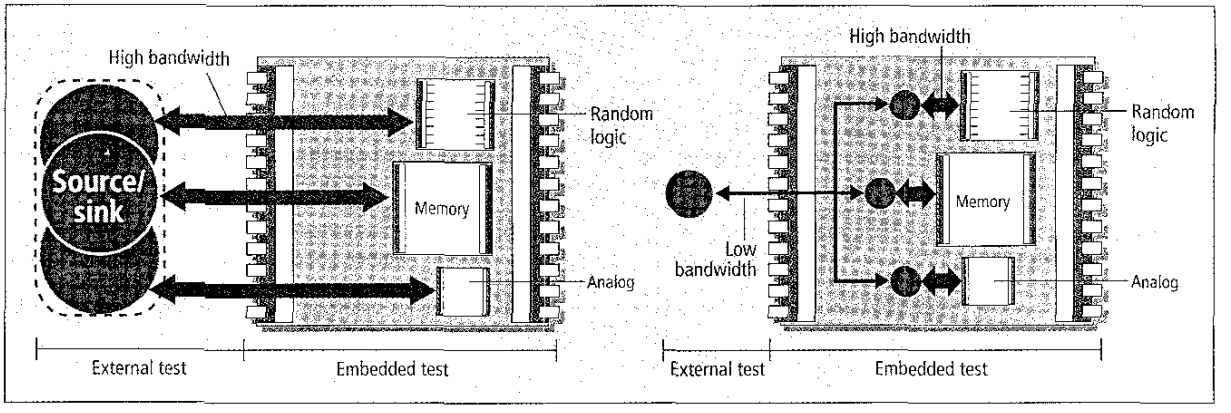
The cores most used today are embedded memories, many of which employ the embedded source and sink approach. Most chip designers have adopted memory built-in self-test (BIST) generation tools. As the monster chips embrace larger numbers of more complex embedded cores, from microprocessors and analog blocks to digital signal processors, the embedded source and sink approach needs extending to become the test solution of the other cores in an SOC.

Embedded memory repair

Monster chips are expected to embed large, very dense memories storing anywhere from 256Kb to 256Mb. Static and



[3] In the beginning, internal and external bandwidth were alike enough to make the use of external test sources and sinks practical [top left]. But at 1000 transistors per pin, external test needed to be supplemented with embedded test through scan paths [top right]. For at-speed testing, external test requires high-bandwidth interaction between ICs and sources/sinks [bottom left]. A better option puts the test features that require high-bandwidth test access onto the chip. Low-bandwidth access handles the remaining items with the external source/sink [bottom right].



[4] Mixed circuits provide a test conundrum all their own in that each type of circuit needs its own type of test. One costly option [left], known as triple insertion, uses three external testers, one each for logic, memory, and analog test. Embedding the hardware sources and sinks for each circuit type on the chip [right] and adding high-bandwidth connections to the circuits makes it possible to use a single low-bandwidth external tester.

dynamic RAMs and flash memories are cases in point. For more than a decade, smaller static RAMs were embedded mostly in logic chips and became an integral part of application-specific IC libraries. These smaller memories were among the first to use on-chip sources and sinks during manufacturing test to obviate use of a dedicated external memory tester as well as the external logic tester needed for the rest of the ASIC. Beyond a certain size, say, 256Kb, memories necessitate redundancy and repair during manufacturing test. Repairs have been performed regularly for large stand-alone memory—typically a fuse-blow process using external laser equipment.

Owing to the large size of its embedded memory, a monster chip needs the memory to have redundant rows and columns of cells, to help in its reconfiguration if faulty cells are detected. For the same reasons as for the smaller memories, the monsters will rely on embedded sources and sinks to generate and evaluate the test data. Expansion of the sinks is one answer. Because the embedded sink evaluates memory-response data, that role could be slightly extended to diagnose failed bits. Expansion of the sink could eliminate the need to funnel a large failed-bit map to external test equipment across limited I/O bandwidth; an expanded embedded sink can perform built-in redundancy analysis and thus identify the actual rows and columns in need of reconfiguration. In this case, only the repair list is communicated to the external tester, for relay to the laser repair equipment for a hard repair.

The final augmentation of the embedded source and sink enables the memory to repair itself. Laser repair can often be very expensive and sometimes, too, field repair is desired. To this end, the embedded test resources should be expanded to include storage of repair data and soft reconfiguration mechanisms. In sum, embedded test for very large memories may have to move beyond fault detection to include failed-bit diagnosis, redundancy analysis, and self-repair.

Implications of increased performance

With the unceasing increase in IC internal speed, performance-related defect coverage keeps growing in importance. Recent Sematech experiments having confirmed the criticality of performance-related tests, the 100-million-transistor chip will necessitate a comprehensive performance test. Moreover, it has been predicted that I_{DDQ} (quiescent drain current) test will lose its effectiveness for such chips because of their higher subthreshold currents. Most I_{DDQ} failures will probably be observed also as timing/performance anomalies.

No performance test applied by external test equipment to a 100-million-transistor IC will be satisfactory. It cannot adequately or cost-effectively test the chip's high clock speeds or provide the necessary performance-related defect coverage. External testers are typically made of older technology than the chips they test, and higher-speed test equipment is distinctly more expensive. Major yield losses and sizable cost increases are related to the discrepancy between the slower growth of external automated test equipment speeds and the ever improving internal chip speed: that much is evident from the SIA roadmap. While external tester accuracy has improved at a rate of 12 percent per year, internal chip speeds have risen by 30 percent per year. The headroom typical of external testers—five times faster than internal chip speeds—has all but disappeared. With the current trend, the cycle time of manufactured chips will approach external tester timing accuracy in less than a decade [Fig. 6]. The actual crossover may occur near 2010, but even by 2001, yield losses due to external test inaccuracy will be unacceptably large.

Given internal chip speed that eludes external test accuracy, the monster chip can still get the timing precision required by lending its embedded test resources the speed of its silicon. Being built on the same piece of silicon as the chip, an embedded test resource will have a cycle time comparable to the internal chip speed. Accurate performance-related tests and precision measurements become possible, and the potential yield losses predicted by the SIA roadmap are eliminated.

Implications of higher density

Steady advances in semiconductor technology include growing silicon density. In the next five years, the number of transistors per square centimeter, already in its millions, will triple. Such density implies a number of test-related impacts.

According to the SIA roadmap, the decline in defect sizes causes a rise in semiconductor density. That is, the yield for the narrower geometry will be lower if the number of defects stays the same. There would be no incentive to go into deeper submicron realms. This combined with the complexity of monster chips adds enormously to the difficulty of fault localization—it increases by one order of magnitude every six years.

The best tool for fault localization and defect analysis in IC manufacture is the test process. In fact, the only way to analyze and isolate many manufacturing defects is with the feedback loop derived from the test process. Failure mechanisms are impossible to understand and corrective action impossible to take without the ability to localize faults in an area open to practical and cost-effective inspection.

In effect, the increased density in monster chips will do battle with the physical fault localization processes. On the plus side, the embedded test hardware scales with the chip itself. Existing embedded-test resources, whether in embedded memories, cores, user-defined logic, or analog blocks, can act as the infrastructure to collect the faulty data from the block under test. This helps to quickly isolate faults.

Leveraging embedded-test hardware resources can further aid in defect isolation. In this case, the failure pattern must map to a physical location on a circuit. Software-based test tools compatible with major embedded-test methodologies (such as scan path or BIST) are needed to save failure pattern information for analysis on the basis of predetermined failure mode data. This information allows yield engineers to more quickly and precisely determine the location and causes of circuit failures.

Unmodeled defect types are another problem. The continuous increase in device density and in levels of metal layers results in new fault models, which reduce the effectiveness of the traditional stuck-at fault test. Collecting more parametric data as measured on external test equipment can be an aid in sourcing the newcomers. Recent studies show that a few large spot defects cause single defects that affect multiple transistors and gates simultaneously. Often, to reduce the test escapes due to such unmodeled faults, pseudo-random test patterns are used. Experimental studies have demonstrated their effectiveness in reducing test escapes. Other approaches include deterministic test generation for alternative fault models, critical-area analysis, and probabilistic methods.

Signal integrity and electromagnetic phenomena will come into new prominence with the appearance of monster chips. New fault models, including soft-error models that incorporate the effects of electromagnetic fields, need to be developed. Soft errors increase in number as devices shrink and supply voltage declines, and as they do, boost both noise sensitivity and susceptibility to such things as alpha particle radiation. Being transient, they need to be continuously monitored during field operation of a chip—a task that will require dedicated embedded-test hardware that performs on-line testing.

Nor is that everything. New embedded sensors to monitor various on-chip parameters should be developed to identify failure modes that are functions of parametric variations. The sensors should be integral to the embedded-test infrastructure and lever-

[5] System-on-chip designs based on embedded processor cores call for a new test approach. The embedded-core test standard (IEEE P1500) under development hinges on a configurable and scalable wrapper and core test information model that allows easy test interoperability and access to embedded cores. Embedded test sources and sinks result in a self-contained and cost-effective test solution.

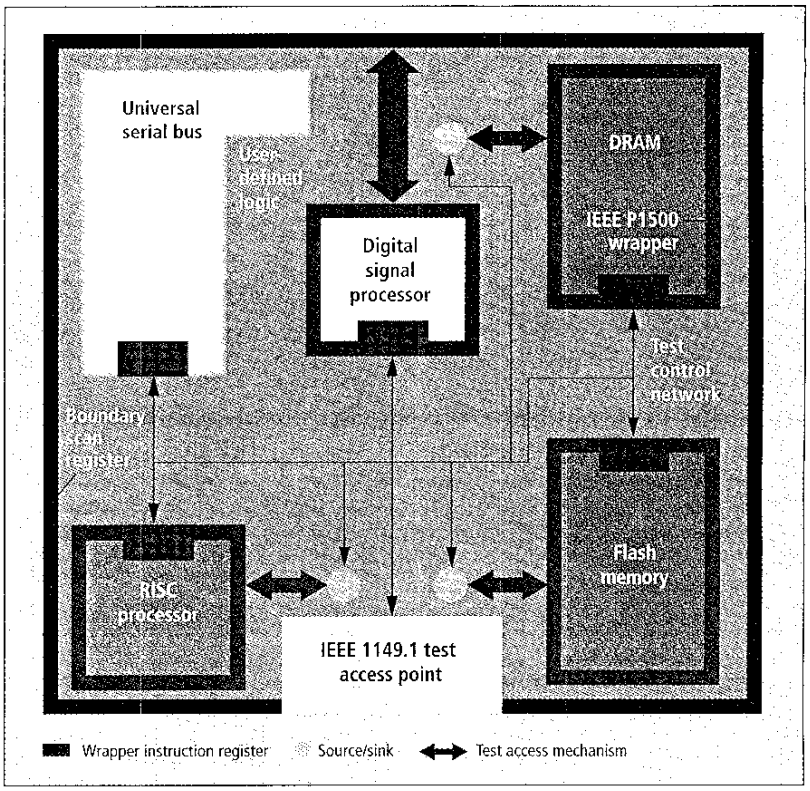
age the existing chip-level test data and control mechanisms. Handling the test data through signature analysis techniques would significantly reduce the need for hardware failure analysis. In fact, the more use is made of embedded-test monitoring and on-chip data acquisition resources, the less in the way of physical hardware diagnostics is required for silicon debug and failure analysis.

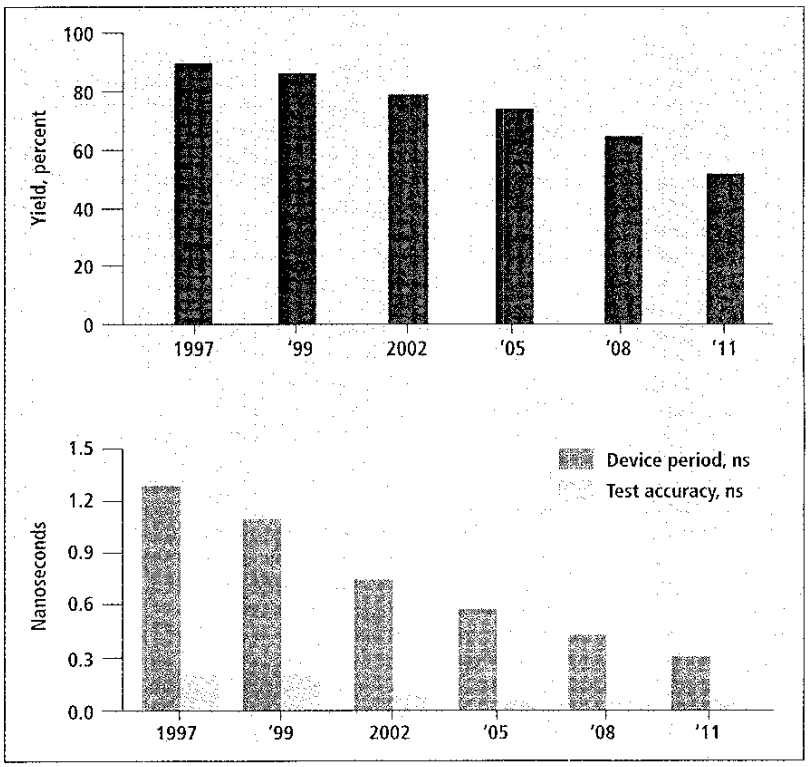
Especially with such high-density packages as flip-chips, hardware diagnosis will get ever more constrained. Conventional electron-beam or thermal-imaging techniques are inapplicable to flip-chip attach technologies because such chips are not accessible from the front. Back-side diagnosis techniques, involving, for example, photon emission and scanned lasers, can be used to a limited extent and only if defects are sensitive to them. On the plus side, the tools and solutions needed for this are under development.

Producing the monster chip requires not just fault localization and failure analysis but also integrated yield analysis based on the defect and failure analysis data. These capabilities need to be embodied in software tools for automatically accessing multiple databases and correlating different types of data. Some data sources are time based, some are chip based, and still others are wafer based. Data reduction algorithms for automatically sourcing defects from several data sources must be developed to shorten defect sourcing time—a key requirement for yield learning and improvement.

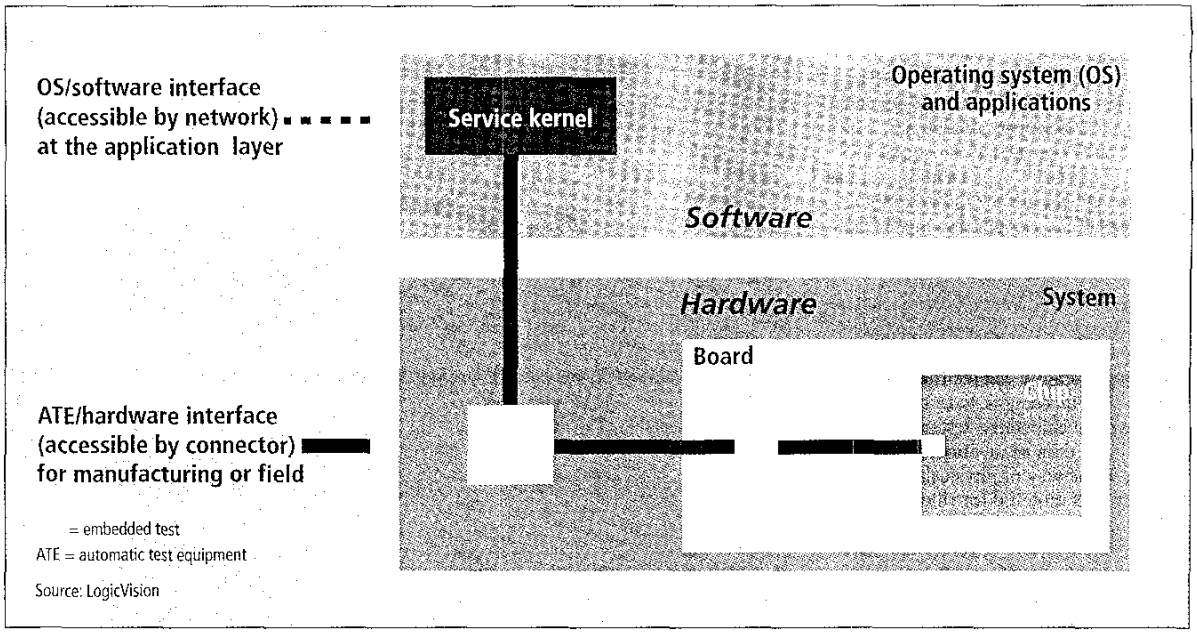
Implications of reduced cost

Increasing cost of external test equipment is one of three major test-related problems the SIA roadmap predicts. For the past 20 years, the cost per pin for external test has remained essentially flat, at around US $10 000, but the demands for higher speed, greater accuracy, more time sets, and increased data volume run counter to the cost-reduction goals of external test equipment. In its 1997 Roadmap, SIA indicates that tester cost will reach $20 million in year 2010, unless IC design incorporates more embedded test. It also predicts that by the same year, it may cost more to test than to manufacture a transistor.





[6] The Semiconductor Industry Association's 1998 update of the International Technology Roadmap for Semiconductors warns that the narrowing difference between external test accuracy and internal chip period [indicated in the lower bar chart] could to lead to unacceptably large losses in yield [upper bar chart], dropping toward 50 percent by 2011.



[7] Embedded test could be extended beyond the chip level to board and system manufacturing and farther—to field test in the final system or product. Reusing embedded test resources hierarchically translates into cost and productivity savings for manufacturers. Here chip-level embedded test is used during board test; board-level embedded test during system/box test; and hardware/software use of the total embedded solution in field tests.

So what price embedded test? It boils down to the silicon added to incorporate the test functions, plus a limited impact on yield. A set of embedded sources and sinks for a state-of-the-art mixed-circuit IC is about 10 000 logic-gate equivalents, given a scan infrastructure already in place. The cost of full scan can be 10–15 percent of the full die, depending on implementation. For designs of about 400 000–500 000 gates, the silicon cost of embedded test equals the cost of external test. For larger chips, the silicon investment constitutes less than 1 percent of the silicon manufacturing costs. As for the effect on yield, the larger the chip area, the more chance that a particle will fall on that chip and cause a defect. So the fact that embedded sources and sinks increase the silicon area can reduce manufacturing yield. Even so, the addition of 10 000 gates to a monster chip's tens of millions of gates has a negligible impact.

A monster chip has a life after its successful production—it becomes part of a larger electronic system. The cost of test and diagnostics for such systems, typically, reaches 40–50 percent of total product cost. If test resources were embedded into the chip, they can be reused hierarchically during board and system manufacture [Fig. 7]. This means less time and money spent on developing diagnostic firmware plus interfaces for board and system test and maintenance features. The concept of embedded test can be applied to every electronic assembly level.

In summary, the semiconductor scaling trends of complexity, performance, and density have thrown up a number of roadblocks to the testing of 100-million-transistor chips. Overcoming them calls for a new approach to testing, where test functions are partitioned basically into two complementary components used simultaneously: embedded test and external test. The balance of functions in each component depends on technological and economic factors. But as chips become more complex, new functions likely will migrate from the external test component to the embedded one. The use of embedded-test hardware will exceed plain chip test. Its crucial test-related functions, such as diagnostics, measurement, debug, failure analysis, and even repair, can be reused to test at all levels: core, chip, board, and system. ◆

To probe further

Many of the advances in IC test have been published in the *Proceedings of the International Test Conference* and *Proceedings of the VLSI Test Symposium*, available from the IEEE Computer Society Press.

Trends and prediction in semiconductor technology are covered in the 1998 International Technology Roadmap for Semiconductors, sponsored by the Semiconductor Industry Association, San Jose, Calif. Roadmap updates and news are available on the World Wide Web at http://notes.sematech.org/ntrs/Rdmpmem.nsf.

Design and test aspects of system-on-chip are covered in *IEEE Design & Test of Computers, Special Issue on Embedded Core-based Systems*, Vol. 14, no. 4, 1997, and in *IEEE Computer Magazine, Special Issue on System-on-Chip*, June 1999.

Much of the leading-edge work in embedded core test is presented in the *Digest of Papers* of the International Workshop on Testing Core-based System-Chips (TECS), available from the IEEE Test Technology Technical Council at http://computer.org/tttc, while details about the IEEE P1500 Embedded Core Test standard are presented on the Web at http://grouper.ieee.org/groups/1500/.

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Yervant Zorian (F) is the chief technology advisor of LogicVision Inc., in San Jose, Calif. He was previously a distinguished member of technical staff at Bell Laboratories, Lucent Technologies. He has authored or coauthored over 130 publications, including two books, and he holds a number of U.S. patents. He currently chairs the IEEE Test Technology Technical Council and serves as the editor-in-chief of *IEEE Design & Test of Computers*.

Spectrum editor: Elizabeth A. Bretz