Economics of Built-in Self-Test

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Using built-in self-test at the right level offers users significant cost savings, but determining which level, if any, is best for BIST can be complex. A detailed economic analysis can unravel heterogeneous costs and benefits so that designers and managers can make the right decision.

A DISCUSSION ABOUT BIST can invoke emotions in the otherwise dispassionate field of electronics test. Zealots claim it is the utopia of test solutions, while skeptics dismiss it as "pie in the sky" with exorbitant costs and few benefits. The truth lies somewhere in between these two extremes. The ideal solution is a sound economic model that lets designers—who have products with various production volumes, design complexities, specifications, support requirements, and customer stress levels—better determine what type of BIST, if any, is best for their applications.

IC manufacturers evaluate the benefits and costs of wafer-, intellectual-property-, system-on-a-chip-, and IC-level BISTs based on profit margin impact. Board manufacturers typically focus on the economics of boundary scan and board-level BIST implementations, although they should also consider the benefits derived from IC-level BIST. Board-level BIST, a relatively new phenomenon,[1] integrates IC-level, boundary scan, and board-level logic BIST for both circuit card vendors and system integrators. System manufacturers consider system-, board-, and IC-level BIST in determining the economics of the various approaches available,[2] and should also consider the economics of BIST in field support. In this article, we view the economics of BIST from the product users' perspective.

Test cost

Test cost strikes at all levels—from device design, through board and system test, to field service. This cost's effect can be substantial, depending on diverse factors such as complexity and production volume. Consider the PC manufacturer with high-end products, enormous production volumes, and worldwide product distribution as one example. Consider the military, with smaller volumes of higher-complexity items but an urgent requirement for maintainability.[3] Test must economically span both extremes.

As one indication of test's impact on cost, consider the trend shown in Figure 1.[4] As the performance of today's circuits approach and surpass that of automatic test equipment, it becomes increasingly difficult for ATE to accurately test devices and circuits. As the figure shows, yield decreases dramatically as a result, driving up cost per unit. This critically disturbing trend could require all designers to cultivate a more detailed knowledge of design for testability (DFT).

The greatest danger, though, is perhaps a lack of real awareness of the totality of the test economic picture. Despite myriad ATE cost considerations, including operation costs, software, training, product distribution, maintenance, and retirement and disposal, only ATE acquisition costs are visible to many organizations. The situation is much like an iceberg with just a small proportion of the entire entity visible above the surface.

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Economic analysis

An economic analysis of BIST must consider both benefits and costs. Benefits include

- better test access, fault detection, and diagnosis;
- higher unit-under-test yields;
- improved design and verification;
- lower test program development costs;
- less or no dependence on ATE;
- shorter time to market;
- shorter test times;
- design and test reuse;
- better product support; and
- increased revenue.

Costs include those incurred in

- design;
- implementation;
- parts and area overhead;
- test equipment, including ATE;
- BIST technologies and added tools; and
- BIST-induced failures and false alarms.

Quantifying these benefits and costs of BIST and then subtracting benefits from costs determines economic value. Such an analysis, however, does not address the most critical issue: An organization is more interested in its own bottom line than the economic benefit to society. An IC vendor incurring substantial costs to implement BIST that has great economic value to the board or system vendor may justifiably ask how this implementation helps its business.

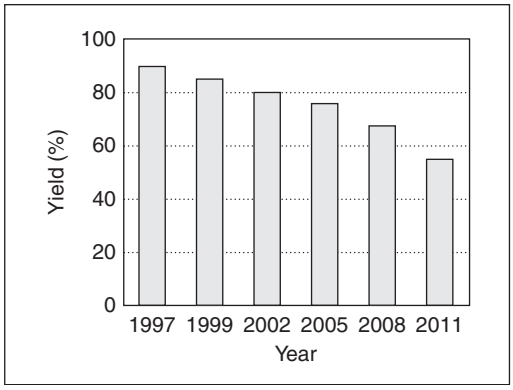

Figure 1. Lower yield due to tester inaccuracy. Tester accuracies are lagging circuit complexity and performance.

Therefore, BIST's economic value must be evaluated separately by each organization using it.

A board manufacturer that finds using BIST-enabled ICs beneficial might buy such ICs at a premium price—one that might also encourage the IC vendor to implement BIST. The premium price the IC vendor charges will depend on its costs less any benefits it enjoys from BIST. Ultimately, the company purchasing the system must be convinced that the benefits gained from BIST-enabled ICs, boards, and systems are worth the higher price. Such an interactive economic calculation depends on inputs from the IC vendor, board vendor, system vendor, field service organization, and system purchaser.

Detailed cost analysis

Test cost is an amalgam of a wide variety of detailed cost effects, listed in Table 1, some of

Table 1. Various costs contribute to the total cost of test.

Cost area	Costs involved
Design and test	Design, design for testability (DFT) and test time, budgeting considerations, marketing, quality and reliability, target throughput, training, packaging technology, circuit layout, silicon, pin out, CAD tools, designers' skills, performance degradation, computing equipment, and capital investment
DFT and ATE	Purchasing, depreciation and maintenance, operator and programming salaries, other labor rates, setup time, test program length, pin memory, program fault coverage, program preparation time, test and diagnosis time, test fixtures, manufacturing yield, production volume, and number of board types
Field service	Repair depot, logistics support, field repair, downtime, repeat visits, and design for maintainability

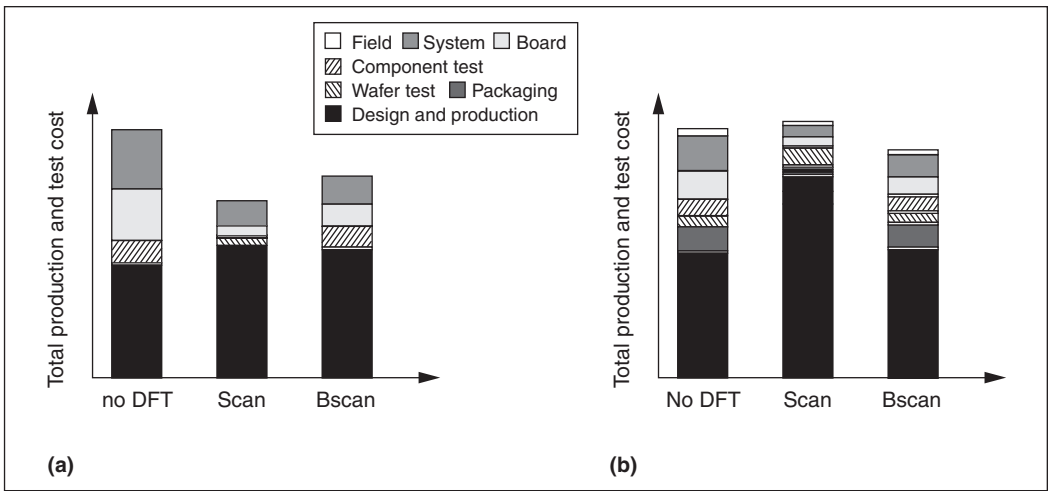

Figure 2. Comparison of costs for different board test methods with 5,000 (a) and 50,000 (b) systems.

which may appear trivial on a first pass.

For a given design, all the considerations listed in Table 1 affect the test strategy selection, and vice versa. Time-to-market implications are also present.

Because the parameters in the table have different units of measurement, a simple cost comparison is impractical. For example, comparing DFT methods might require balancing the improvement in fault coverage with the associated increase in silicon area. An objective way to compare these different values would be useful.

If we let Cost (in dollars) be a common reference point as a direct or indirect implication, we can compare the relative importance of each parameter in financial terms. Doing so turns an "apples and oranges" comparison into one using a common unit of measure.

Consider an analysis of board-level design.[5] Figure 2 shows an analysis of three boards with different test strategies: All devices either have

- no DFT,
- internal scan only, or
- boundary scan but no internal scan.

The results in Figure 2a are what you might expect from a direct comparison. However, when the same comparison uses 10 times the production volume, the results (shown in Figure 2b) are quite different. Indeed, increasing production volume further (not shown) could eventually make the no-DFT option the cheapest. Production volume is a major factor in the economic viability of test methods.

Of course, implementing various strategies requires consensus across organizational boundaries. For example, perhaps the design department bears the cost of introducing design features that will let the test department reduce its costs: The project benefits as a whole, but the design department does not. An economics model is crucial in such situations to show management the likely economic benefit to the company and the perceived cost penalties to certain individual departments.

BIST implementations

Figure 3 illustrates how BIST can occur at various levels. For specific BIST implementations (such as those for logic, memory, and D/A converters; I_{DDQ} testing; and boundary scan), we encourage you to investigate further.[6-8]

System BIST accesses boards through an IEEE-1149.5 controller. Although a daisy chain of IEEE-1149.1 test access ports (TAPs) could be used instead, the failure of any board in the chain would complicate diagnosis.[9] Although not all boundary-scanned ICs have IC BIST, ICs with internal BIST can usually get their information directly to the 1149.1 TAP. In Figure 3, boards are also equipped with board-level BIST. A single-chip universal board BIST mech-

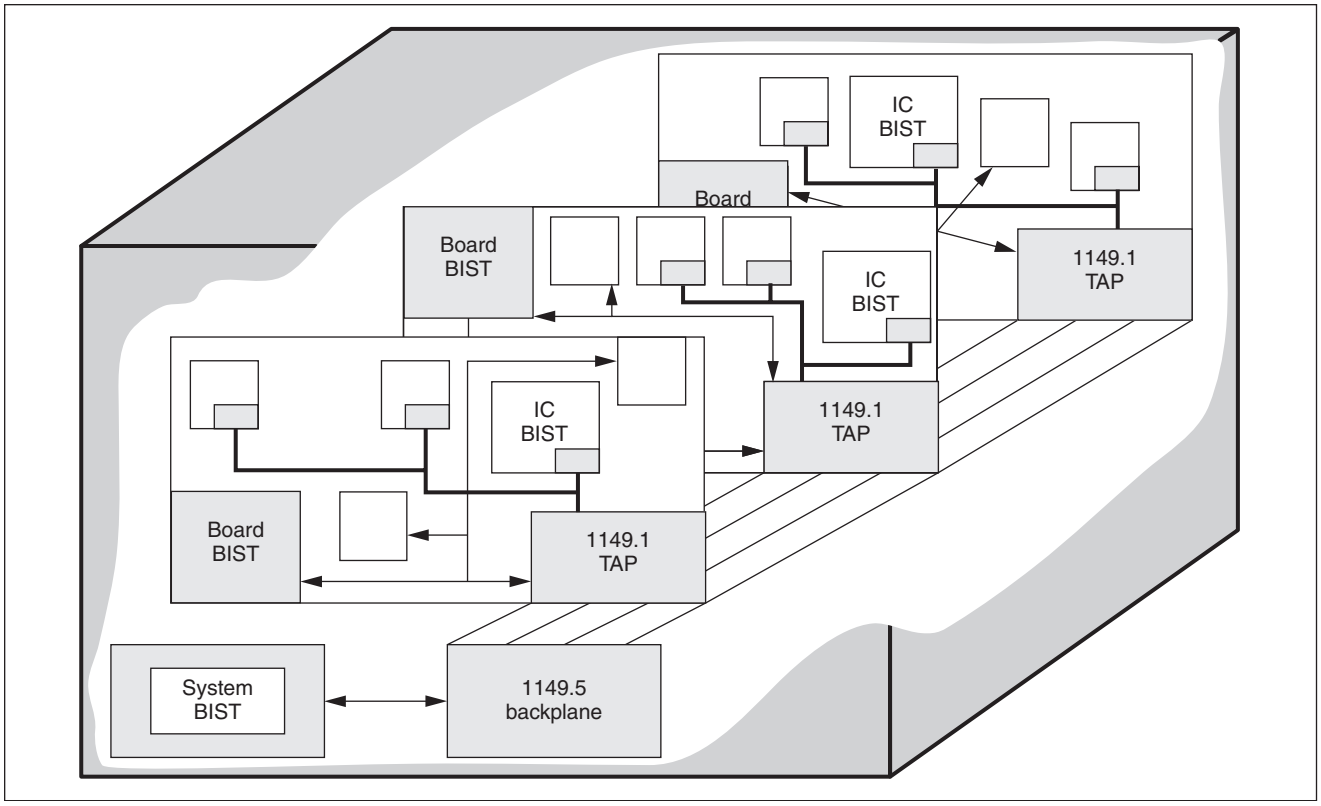

Figure 3. Hierarchical control of built-in self-test at IC, board, and system levels, showing a box controlled by system-level BIST through the IEEE-1149.5 backplane, individual boards controlled by IEEE-1149.1 boundary scan and board-level BIST, and individual ICs controlled by the 1149.1 TAP and/or IC-level BIST. The 1149.5 and 1149.1 ports integrate and communicate with the various BIST levels. (Blank boxes indicate non-boundary scan devices.)

anism, called Built-in Test Exerciser and Sensor, has been designed not only to test collections of nonboundary-scanned chips on the board but also to connect with every existing boundary scan cell by way of the 1149.1 TAP.[10] Other board-level BISTs have been proposed, but board BIST is typically custom designed. In a hierarchical setting, such as that shown in Figure 3, board BIST acts as an intermediary between IC- and system-level BIST.

Test economics

Economics, as we use the term here, refers to comparing alternatives and expressing the results in monetary terms. For test, an inherent cost exists before any action is taken. An untested product has a potential fault that can cost the manufacturer even after it has been delivered, accepted, and paid for. Eliminating the probability that the system user will detect such a fault, especially during the warranty period, is the main motivation for testing before the product is shipped. If the fault was not present in the first place, the effort and cost of testing seems wasted. As the law of averages catches up, however, a few failures inevitably occur, and the havoc they create is far greater than the cost of judiciously planning prevention through careful and comprehensive testing. In short, it makes economic sense to test, because it costs less to test than not to test.

Using this rationale, managers can more accurately assess the extent to which they should test. Besides knowing the economic impact of not testing, they must also know the maximum cost of testing that they can sustain. If testing costs less than this amount, the testing operation can be considered desirable—in fact, profitable.

Once a company establishes the maximum budget for this testing, the remaining questions have to do with determining a test strategy. The

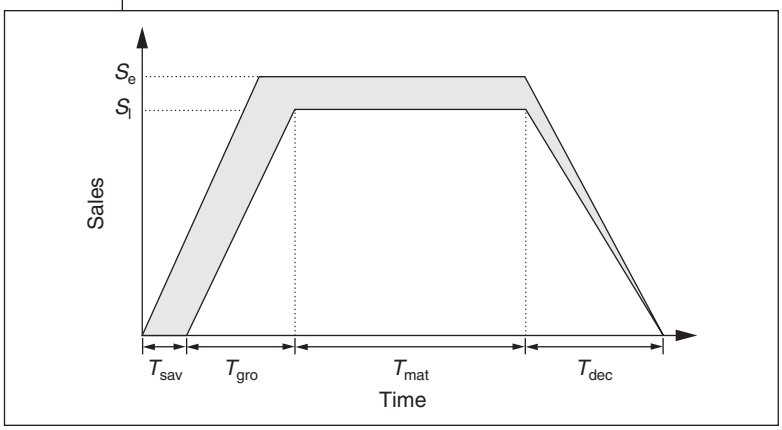

Figure 4. Market life cycle model, showing sales during various product phases: growth (T_{gro}), maturity (T_{mat}), and decline (T_{dec}), with early (S_e) and late (S_l) product release. T_{sav} is the time saved through early product delivery. The shaded area shows the benefit gained through early product release.

right test strategy will achieve the desired goals at the lowest possible cost, yielding the highest possible profit from test.

Improving time to market

Getting a product out more quickly has the greatest economic benefit. Product obsolescence is a reality in our fast-changing electronics market. Several sources exist for calculating the market life cycle model. For example, Lu and Wu put forth a model specifically applied to BIST economics.[11] Figure 4 shows a somewhat altered version of this market life cycle model.

Figure 4 shows two sales patterns. With early product release (because of BIST), the sales pattern maximizes at S_e. With later release, maximum sales are at S_l. The area under each curve represents the revenue generated by that sales pattern. The benefit, B_{EM}, derived from reaching the market early (by time T_{sav}) because of BIST is the difference in the revenues produced between the two scenarios:

$$B_{EM} = R_B - R_{NB} \quad (1)$$

where R_B is the revenue generated by the early-release sales pattern with BIST, and R_{NB} is the revenue generated by the late-release sales pattern without BIST. The shaded area in Figure 4 represents this benefit.

We divide the life cycle market into three phases: growth, maturity, and decline. Sales increase during growth phase T_{gro}, maintain a steady rate during maturity phase T_{mat}, and decrease (possibly due to product obsolescence) during decline phase T_{dec}. The revenue R_{NB} without early-to-market BIST benefits is

$$R_{NB} = (1/2)S_l(T_{gro} + 2T_{mat} + T_{dec}) \quad (2)$$

The revenue R_B with early-to-market BIST benefits is

$$R_B = (1/2)S_e(T_{sav} + T_{gro} + 2T_{mat} + T_{dec}) \quad (3)$$

Substituting equations 2 and 3 into equation 1 gives benefit B_{EM} of early market delivery as

$$B_{EM} = (1/2)[(S_e - S_l)(T_{gro} + 2T_{mat} + T_{dec}) + (S_e \times T_{sav})] \quad (4)$$

Effect of higher fault coverage

Using BIST can partly arrest the expected reduction in yield shown in Figure 1. Better fault coverage FC leads to higher outgoing quality Q, yielding an economic benefit. The Williams and Brown model[12] relates defect level DL to fault coverage and first-pass yield Y as

$$DL = 1 - Y^{1-FC} \quad (5)$$

Let quality Q be the lack of defects: $1 - DL$. The revenue R generated on N units of price P at quality $(1 - DL)$ is

$$R = N \times P(1 - DL) \quad (6)$$

A vendor delivering faulty units charges for them but also incurs penalty cost C_{FU}. So the revenue is actually

$$R = N \times [P(1 - DL) - (C_{FU} \times DL)] \quad (7)$$

Substituting equation 5 into equation 7 gives the revenue affected by fault coverage:

$$R = N \times [(P \times Y^{1-FC}) - C_{FU}(1 - Y^{1-FC})] \quad (8)$$

We express the benefit of higher fault coverage through BIST as

$$B_{FC} = R_B - R_{NB} \quad (9)$$

where R_B is the revenue with BIST, and R_{NB} is the revenue without BIST. Because N, P, Y, and C_{FU} are the same regardless of whether or not BIST is used, substituting equation 8 into equation 9 for both R_B and R_{NB} and then reducing gives

$$B_{FC} = N \times (P + C_{FU}) \times [Y^{1-FC_B} - Y^{1-FC_{NB}}] \quad (10)$$

Equation 10 relates the improved fault coverage achieved by BIST (FC_B) to economic benefit. Better fault coverage also affects on-time delivery, as shown in Figure 5.[13]

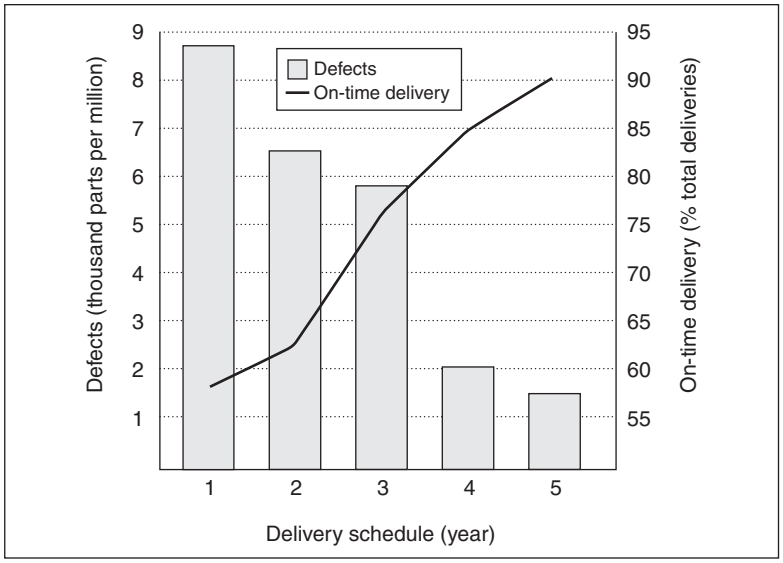

Figure 5. On-time delivery as a function of better fault coverage.

Effect of deeper fault isolation

Each time we isolate a fault to a single replaceable unit, k, the cost of repair, C_{Rk}, will be at least as high as the unit's replacement cost, RU_k:

$$C_{Rk} \geq RU_k$$

To simplify the analysis, we will assume that the cost of repairing is only the cost of replacing the unit called out, so the above inequality becomes an equation. If it is not possible to tell which of two units, m or n, is faulty, then we say that m and n form an *ambiguity group* with replacement costs RU_m plus RU_n:

$$C_{Rmn} = RU_m + RU_n$$

Fault isolation requirements are generally expressed as isolated to one replaceable unit in some percentage of cases, say 95%; to two or fewer units in, say, 97% of cases; and to three or fewer units in, say, 100% of cases. So, in this example, we would have an ambiguity group of no larger than three in all cases.

We can express the cost of repairs for each ambiguity group separately. Let C_{R1} be the cost associated with repairing replaceable units in the ambiguity group where we can distinguish a single replaceable unit as faulty. Let C_{R2} be the cost associated with repairing replaceable units in the ambiguity group where we cannot distinguish between two replaceable units as faulty. Let C_{Rf} be the cost associated with repairing the ambiguity group with the largest indistinguishable elements f. Then

$$C_{R1} \geq \sum RU_1,\ C_{R2} \geq 2\sum RU_1, \text{ and } C_{Rf} \geq f\sum RU_f$$

Economic benefit B_{FI} gained from better fault isolation as a result of BIST is

$$B_{FI} = C_{RNB} - C_{RB}$$

Where C_{RNB} is the cost of repair without BIST, and C_{RB} is the cost of repair with BIST. In a unit under test (IC, board, module, or system) consisting of several replaceable units, this benefit is

$$B_{FI} = (\sum RU_{1NB} + 2\sum RU_{2NB} \ldots + f\sum RU_{fNB}) - (\sum RU_{1B} + 2\sum RU_{2B} \ldots + f\sum RU_{fB})$$

Effect of lower development costs for test program sets

Development costs for a test program set include those for programs, fixtures, debugging and verification, operator involvement, and program maintenance. From these factors, we can estimate the test program set's overall cost.

Programs. Lu and Wu[11] found from empirical data that test development time for circuits containing logic BIST, T_{tdLB}, takes only 1/590th the time it would take without BIST, T_{td}:

$$T_{tdLB} = (1/590)T_{td}$$

So the benefit to test programming is

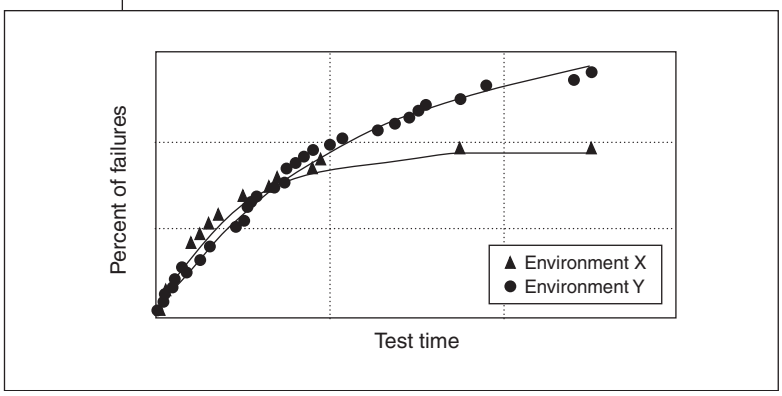

Figure 6. Inconsistency in test environments can cause different test results.

$$B_{TP} = T_{td} - T_{tdLB}$$

or

$$\begin{aligned} B_{TP} &= T_{td} - (1/590)T_{td} \\ &= (589/590)T_{td} \\ &= (0.9983)T_{td} \end{aligned}$$

Thus, BIST eliminates 99.83% of the test program development time.

Fixtures. Test fixtures depend on the number of I/O pins (IO) and the fixture complexity affected by the technology, frequency, and target pin size. Let α_f be the complexity factor of the test fixture. Cost T_f associated with building a test fixture is

$$T_f = \alpha_f \times IO$$

The benefit to test fixtures from using BIST is then

$$B_{TF} = T_f - T_{fB}$$

or

$$B_{TF} = (\alpha_f \times IO) - (\alpha_{fB} \times IO_B)$$

where α_{fB} represents the test fixture complexity factor with BIST, and IO_B represents the number of I/O pins with BIST. (If $IO_B \geq IO$, then B_{TF} may be negative, and we would treat the effect of building test fixtures with BIST-enabled pins as a cost rather than a benefit.)

Debugging and test program verification. Lu and Wu showed that the factor of 590 representing the test development reduction ratio from use of logic BIST is also appropriate for test program debugging and verification:[11]

$$T_d = T_{vi} + (1/590)T_{vd}$$

where T_d is the time it takes to debug and verify the test program, T_{vi} is the part of the debugging effort that is independent of testability, and T_{vd} is the part of the debugging and verification time that is testability (and BIST) dependent.

In calculating the benefit of BIST to test program verification, we subtract the cost of T_d with BIST from the cost of T_d without BIST, and T_{vi} cancels out, resulting in

$$\begin{aligned} B_{TPV} &= [T_{vd} - (1/590)T_{vd}] \\ &= (589/590)T_{vd} \\ &= (0.9983)T_{vd} \end{aligned}$$

Thus, BIST eliminates 99.83% of the test program verification and debugging time.

Operator involvement. Test process consistency is another major factor in test cost. Farren and Ambler described the case where identical products manufactured and tested in different locations can have markedly different test results.[2] Although this case can arise from different handling procedures or other causes, the lack of detailed accuracy in the test can also cause the inconsistency. Applying BIST can greatly reduce this variation.

Figure 6 shows that there were significant differences in the number of failures detected by supposedly equivalent test environments at two manufacturing plants. An investigation identified the training and experience of test operators as one factor that accounted for these differences.

We can develop a formula to account for test operator involvement, which increases with test length T_l and test complexity. Test complexity is directly related to test development time T_{td} and debugging time T_{vd}. If we assign parameter α_{to} to test operator involvement, we can formulate test operator cost T_{to} as

$$T_{to} = \alpha_{to} \times T_l(T_{td} + T_{vd})$$

We can also calculate the benefit of BIST to the test operator:

$$B_{TO} = T_{to} - T_{toB}$$

We can make some assumptions here to simplify the equation that results when we redefine the preceding equation in terms of α_{to}, T_l, T_{td}, and T_{vd}. First, it is likely that the same person will be performing the test regardless of whether or not BIST exists, so we can assume that $\alpha_{to} = \alpha_{toB}$. We can also assume that the same relationship of 1/590 that we have used before exists in T_{td}, T_{vd}, and in T_l. Making these assumptions gives

$$B_{TO} = [\alpha_{to} \times T_l(T_{td} + T_{vd})] - [\alpha_{to} \times T_l(1/590)(T_{td} + T_{vd})]$$

$$B_{TO} = (0.9983)\alpha_{to} \times T_l(T_{td} + T_{vd})$$

Thus, BIST eliminates 99.83% of the test operator's involvement.

Program maintenance. Test program maintenance is some percentage α_{tpm} of test program development and test program verification, so

$$B_{TPM} = \alpha_{tpm} \times (B_{TP} + B_{TPV})$$

Because $B_{TP} = (0.9983)T_{td}$, and $B_{TPV} = (0.9983)T_{vd}$, we get

$$B_{TPM} = (0.9983)\alpha_{tpm} \times (T_{td} + T_{vd})$$

Test program set's overall cost. We can now combine the benefits derived from lower test costs for programs, fixtures, debugging and verification, operator involvement, and program maintenance, as

$$B_{TPS} = B_{TP} + B_{TF} + B_{TPV} + B_{TO} + B_{TPM} \quad (11)$$

Substituting the appropriate equations into equation 11 gives

$$B_{TPS} = (0.9983)(T_{td} + T_{vd}) \times [1 + (\alpha_{to} \times T_l) + \alpha_{tpm}] + [(\alpha_f \times IO) - (\alpha_{fB} \times IO_B)] \quad (12)$$

From equation 12, we see that a minimum savings of 99.83% of the test program development time T_{td} and test verification time T_{vd} is guaranteed in addition to possible savings from the test operator and test program maintenance. Savings from test fixtures, $(\alpha_f \times IO) - (\alpha_{fB} \times IO_B)$, is not guaranteed and may actually detract from the overall benefit.

Effect of lower IC ATE cost

The following analysis was performed for chip-level ATE; it may apply to board-level ATE as well, with some modifications possibly needed. BIST reduces off-chip communication, so the external tester can be greatly simplified. Lu and Wu translated the benefits of BIST into terms that relate to tester cost:[11]

$$B_{ATE} = N(R_{dep}/T_{s/yr})[(U_{eq} \times T_t) - (U_{eqB} \times T_{tB})]$$

where B_{ATE} is the benefit in terms of tester (ATE) cost, N is production volume, R_{dep} is the tester's annual depreciation rate, $T_{s/yr}$ is 31,536,000 seconds/year, U_{eq} is the purchase price of the external test equipment (ATE) when BIST is not available, U_{eqB} is the purchase price of ATE when BIST is available, T_t is the test time when testing a chip without BIST, and T_{tB} is the test time when testing the chip with BIST.

We extend Lu and Wu's equation by considering two important factors that affect the pricing of external test equipment. First, we must consider test length:

$$T_{tB} = (1/590)T_t$$

According to Lu and Wu, the test program length has this 1/590 factor.[11] Second, test equipment price increases with increasing pin count, operating frequency, and memory size. Because frequency and memory size influence the price of the equipment, we contend that both of these factors will have lower requirements when BIST is used. We use parameters $\alpha_{freq} < 1$ and $\alpha_{mem} < 1$ to account for the latter two effects in the following equation for test equipment price:

$$U_{eqB} = \alpha_{freq} \times \alpha_{mem} \times U_{eq}(IO_B/IO)$$

Given these assumptions, our equation for the

equipment benefit becomes

$$B_{ATE} = N(R_{dep}/T_{s/yr})U_{eq} \times T_t[1 - \alpha_{freq} \times \alpha_{mem}(IO_B/IO)(1/590)]$$

Cost implications beyond the manufacturing process

The lack of automation that testability design and BIST seek to solve has implications beyond manufacturing test. When it comes to field service, the differences are immense. A lack of testability design and BIST hampers field service, making it necessary to have expensive field test equipment and/or highly trained service engineers. It could also mean that engineers inadequately diagnose field problems, yielding no satisfactory solution for the customer after repeated visits. This situation could lead to degradation of a system's reliability if the problem goes unsolved. These problems increase the need for costly human intervention. Costs at this level—for labor, staff training, repeated service visits, and maintenance of a spare parts inventory—far outweigh most costs mentioned thus far.

Such costs can be substantial, even without considering costs associated with downtime, penalty clauses, loss of revenue from missed sales, and other consequential losses. The increased reliability provided by testability design and BIST alleviates many of these problems.

Cost analysis

Analyzing testability design's effect on cost is neither simple nor straightforward. However, considerable work in this area is available, including economics models for use as standalone spreadsheets or incorporated into computer-aided design tools.[5] Such analytical tools, while complex, can help explain the array of apparently conflicting data.

In all walks of life, people tend to rely on some erroneous, preconceived ideas. Some of the common ones used in our profession are:

- "But we've always done it this way."
- "Just add scan path and it will be all right."
- "Board and system test are someone else's problem."
- "Improving quality means testing more, which costs more money."

Such preconceptions can impede objective engineering and economic analyses; designers and managers should stay clear of them. Economic analysis, on the other hand, can help. It is a strong tool—although only one tool—that designers and managers can use. Other factors significantly affect product economics and are directly attributable to the use of testability-enhancing features like BIST. But the impact of these factors remains difficult to even attempt to quantify accurately.

THE COST OF TEST is impossible to ignore. Detailed analysis of this cost and its implications can be useful and financially fruitful. Only by carefully analyzing design and test goals can designers achieve satisfactory results.

If properly planned, the benefits of BIST can outweigh its costs. The economic analysis, however, is far more complex when you consider BIST's impact on a particular organization. As the product develops from the IC to system level and its complexity increases, so does the complexity of successfully identifying a failure's root cause. So it makes economic sense for system owners and perhaps system producers to implement BIST. The problem is that the system designer can do little if the IC and board vendors have not already implemented BIST. Those vendors, however, may not have found BIST to be profitable for them. Thus, an overall economic analysis is necessary to determine the premium that a system user or vendor can feasibly pay IC and board vendors so that everyone profits. Despite the substantial savings that the formulas in this article suggest are possible, BIST must perform well across organizational boundaries. A model that can view BIST's benefits for various organizations has been developed. See the "Sample Economic Analysis" sidebar for more information.

Successful design and test involves many factors—time to market, quality perception, marketplace, product lifetime, and so on. Economic analysis is one such factor and can give design managers an extra data point in decision making. ■

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Sample Economic Analysis

Louis Ungar has agreed to distribute a beta sample BIST economic analysis at no cost for individuals to use. The analysis comes in the form of an Excel spreadsheet template.

The analysis uses formulas similar to the ones in this article, to enable BIST economic analysis across organizational boundaries. For example, BIST implemented at the IC level can be analyzed for benefits to the IC, board, system, and field-support organizations. The spreadsheet model uses untested formulas and hypothetical data, so users are cautioned against relying on it for their own operations.

If you would like a copy of the spreadsheet, contact Ungar at LouisUngar@ieee.org.

Louis Y. Ungar is president of A.T.E. (Advanced Test Engineering) Solutions. His consulting, training, and research interests include economically sound test methods, DFT, ATE, and BIST approaches in manufacturing operations and support. Ungar has completed the course work toward an MA in management at the University of Redlands in Redlands, Calif., and has a BS in electronics engineering and computer sciences from the University of California at Los Angeles. He is president of the Los Angeles chapter of the American Society of Test Engineers, chair of the Surface Mount Technology Association's Testability Committee, and a member of the IEEE Test Technology Committee. Contact him at LouisUngar@ieee.org.

The biography of **Tony Ambler** appears on page 59 of this issue.

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