# Lucien **Gheerbrant**

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## Career Objective

Final-semester M.Eng. student completing an international dual degree in computer science, electronics, and telecommunications. Seeking a graduate role or internship to leverage 10 months of experience, including modelling a custom RISC-V microcontroller during a CPU architecture engineering internship. Developed leadership, communication, and planning skills through leading role in a student art association.

## Education

**Master of Engineering** *Aug 2024- May 2025*
University of Technology Sydney *Sydney, Australia*
- Majoring in Telecommunications and Electronics
- Dual degree with a focus on managerial and professional engineering knowledge

4G/5G Mobile Technologies | Electronic Components and Fabrication | Risk Management

**Master of Engineering** *Sep 2022 - May 2025*
École des Mines de Saint-Étienne *Gardanne, France*
- Majoring in Microelectronics and Computer Science
- Highly selective, esteemed and historical engineering institution in France

Machine Learning | Microcontroller Systems | CPU Architecture | Semiconductor Physics

**Bachelor of Engineering** *Sep 2019 - Jun 2022*
Lycée Henri Wallon *Valenciennes, France*
- Undergraduate courses in Mathematics, Physics, Chemistry, Engineering Sciences

Self Confidence | Stress Management | Resilience | Thinking & problem-solving skills

## Technical Skills

| | |
|---|---|
| **Languages** | English (C1), French (Native) |
| **Programming** | C/C++, embedded C, Python, OoP, MATLAB, TensorFlow, bash |
| **Software** | Linux, git, CI/CD, gem5, VSCode, Podman, Docker, S-Edit, L-Edit, MPLAB, STM32CubeIDE, TrueStudio, Proteus, LabVIEW, Keil, ModelSim |
| **Hardware** | SystemVerilog, gem5, PIC18, STM32, I2C, ARM-Cortex, Wi-Fi, Bluetooth, LoRa, 4G/5G, 8051, RISC-V, oscilloscope |

## Professional Experience

**Digital Systems Simulation Engineering Intern (full-time)** *Mar 2024 - Aug 2024*
PROPHESEE *Paris, France*
- Modeled and developed a RISC-V-based embedded system within 4 months using a discrete-event computer architecture simulator, integrating it with an event-based camera system for more efficient testing
- Achieved a 1:25 simulation-to-real-time ratio, reducing time spent on testing
- Optimised easier further development for engineers without access to a RISC-V board, streamlining integration and testing phases

C++ | Python | gem5 | RISC-V | Object-Oriented Programming | SystemVerilog | git

**Validation Engineering Intern** *Jan 2023*
Microchip Technology Inc *Rousset, France*

- Developed Python and Bash scripts to automate tasks within validation department, increasing productivity
- Established communication between a work computer and an embedded Linux-based micro-controller using SSH and I2C protocols for seamless data exchange during validation procedures with a latency of 5ms
- Implemented automated data readings by establishing communication between a multi-meter and a work computer using Python scripts, enhancing efficiency and accuracy

Python Bash Multimeter Oscilloscope Embedded Systems Embedded Linux I2C/TWI git

## Projects

**Development of a motorized robot with IR and ultrasonic sensors using a STM32 microcontroller** *Mar 2024 – Apr 2024*
Auto-parking fleet of on-wheel robots *École des Mines de Saint-Étienne*

- Implemented an auto-park function for a fleet of robots, via robot-to-robot Zigbee communication
- Developed firmware for a STM32 microcontroller within 3 weeks, including extensive research and study of a datasheet, allowing a fleet of 10 robots to be automated
- Gained knowledge in embedded C programming, and use of STM32CubeIDE

Embedded C Bluetooth Zigbee STM32 STM32CubeIDE

**Modeling of an ASCON-128 encryption system** *Oct 2023 - Nov 2023*
Design of a digital system in SystemVerilog *École des Mines de Saint-Étienne*

- Utilised SystemVerilog to create and validate module with test benches, integrating a finite-state machine for encryption within 2 months
- Tested and verified signal processing with ModelSim software for machine containing 20+ states

SystemVerilog Digital Design HDL Encryption ModelSim

## Extracurricular Involvements

**Vice President** *Mar 2023 - Mar 2024*
Bureau of the Arts *Gardanne, France*

- Organised a student organisation promoting cultural awareness by organising various artistic events for 50+ members
- Collaborated with 7 other executive board members to provide strategic leadership, establish goals, and allocate resources

Event Planning Management Responsibility Taking Teamwork Communication

**Volunteer** *Mar 2023 - Jun 2023*
Collectif AGIR *Aix-en-Provence, France*

- Volunteered in association providing assistance to 30+ people in precarious situations
- Organised and facilitated weekly computer classes for vulnerable persons
- Taught beneficiaries essential digital skills such as email communication, web browsing, and office software usage

## Referees

*Available upon request*

## Personal information

**Hobbies** Drawing, Animation, Cooking, Fitness, Fashion
Holder of a Full Driver's License
luciengheerbrant.com