CSE 331 Computer Organization

Project 1 – MIPS Assembly & Structural Verilog

Due date: October 27, Friday 17:00 (Moodle)

1. (80pts) Write a full assembly program that takes two floating point numbers and record each as two integer variables before the decimal point and after the decimal point. Your program will have three subroutines: add, subtract and multiply. You are not allowed to use floating point instructions. You can only use integer instructions. Handling negative numbers will get extra 15 points. Ex: `3.735 + 7.22` will output `= 10.955` (Assume all parts can be represented by 32-bit integers)

2. (40pts)
   a. Design a digital circuit that takes two 5-bit input numbers (**InA** and **InB**) and one 2-bit input (**Select**). The circuit will output a 5-bit signal called **Out** such that:

Select	Out
00	InA AND InB
01	InA + InB (Addition)
10	InA OR InB
11	InA XOR InB

   Use structural Verilog and Quartus for designing that circuit.
   Don't use ": ?" operator. Design multiplexer with AND, OR, NOT logic gates.

   b. Write a Verilog testbench for your circuit and simulate by ModelSim to see the correctness of your design.

   c. Bonus (15pts): Upload your design to DE0 FPGA board and verify it on the board.

Rules:

1. All project details (even the schematic) will be announced at next PS (October 16). So attend the PS for your own good!
2. Behavioral Verilog is not permitted. Thus, first draw your schematic on a paper.
3. Assembly that cannot be executed or designs that are not even simulating can at most get 20pts.
4. You should show your simulation and board execution during demo hour and be graded accordingly. Demo hour will be announced on Moodle.
5. No late submissions even if 1 minute.
6. The input-output names must be exactly the same as given above.
7. *Honor code*: It is not a group project. Do not take any code from Internet. Any cheating means at least -100 for both sides. Do not share your codes and design to any one in any circumstance. Be honest and uncorrupt <u>not to win</u> but because <u>it is RIGHT</u>!