

# AN0002.2: EFR32 Wireless Gecko Series 2 Hardware Design Considerations



This application note details hardware design considerations for EFR32 Wireless Gecko Series 2 devices. For hardware design considerations for EFM32 and EZR32 Wireless MCU Series 0 and EFM32 and EFR32 Wireless Gecko Series 1 devices, refer to *AN0002.0: EFM32 and EZR32 Wireless MCU Series 0 Hardware Design Considerations* and *AN0002.1: EFM32 and EFR32 Wireless MCU Series 1 Hardware Design Considerations*, respectively.

Topics specifically covered are supported power supply configurations, supply filtering considerations, debug interface connections, and external clock sources.

For more information on hardware design considerations for the radio portion of EFR32 Wireless Gecko Series 2 devices, see *AN930.2: EFR32 Series 2 2.4 GHz Matching Guide*, *AN933.2: EFR32 Series 2 2.4 GHz Minimal BOM* and *AN928.2: EFR32 Series 2 Layout Design Guide*.

## KEY POINTS

- Decoupling capacitors are crucial to ensuring the integrity of the device's power supplies.
- The debug interface consists of two communication pins (SWCLK and SWDIO).
- External clock sources must be connected to the device correctly for proper operation.

## 1. Device Compatibility

This application note supports multiple device families, and some functionality is different depending on the device.

EFR32 Wireless Gecko Series 2 consists of:

- EFR32BG21
- EFR32MG21
- EFR32BG22
- EFR32FG22
- EFR32MG22

## 2. Power Supply Overview

### 2.1 Introduction

Although the EFR32 Wireless Gecko Series 2 devices have very low average current consumption, proper decoupling is crucial. As for all digital circuits, current is drawn in short pulses corresponding to the clock edges. Particularly when several I/O lines are switching simultaneously, transient current pulses on the power supply can be in the order of several hundred mA for a few nanoseconds, even though the average current consumption is quite small.

These kinds of transient currents cannot be properly delivered over high impedance power supply lines without introducing considerable noise in the supply voltage. To reduce this noise, decoupling capacitors are employed to supplement the current during these short transients.

### 2.2 Decoupling Capacitors

Decoupling capacitors make the current loop between supply, MCU, and ground as short as possible for high frequency transients. Therefore, all decoupling capacitors should be placed as close as possible to each of their respective power supply pins, ground pins, and PCB (Printed Circuit Board) ground planes.

All external decoupling capacitors should have a temperature range reflecting the environment in which the application will be used. For example, a suitable choice might be X5R ceramic capacitors with a change in capacitance of  $\pm 15\%$  over the temperature range -55 to +85 °C (standard temperature range devices) or -55 to +125 °C (extended temperature range devices).

For regulator output capacitors (DECOUPLE, VREGSW, and VREGO, if available), the system designer should pay particular attention to the characteristics of the capacitor over temperature and bias voltage. Some capacitors (particularly those in smaller packages or using cheaper dielectrics) can experience a dramatic reduction in capacitance value across temperature or as the DC bias voltage increases. Any change pushing the regulator output capacitance outside the data sheet specified limits may result in output instability on that supply.

### 2.3 Power Supply Requirements

An important consideration for all devices is the voltage requirements and dependencies between the power supply pins. The system designer needs to ensure that these power supply requirements are met, regardless of power configuration or topology. These internal relationships between the external voltages applied to the various EFR32 supply pins are defined below. Failure to observe the below constraints can result in damage to the device and/or increased current draw. Refer to the device data sheet for absolute maximum ratings and additional details regarding relative system voltage constraints.

#### EFR32 Wireless Gecko Series 2 Power Supply Requirements

- AVDD and IOVDD — No dependency on each other or any other supply pin
- VREGVDD  $\geq$  DVDD
- DVDD  $\geq$  DECOUPLE
- PAVDD  $\geq$  RFVDD

## Power Supply Pin Overview

Note that not all supply pins exist on all devices. The table below provides an overview of the available power supply pins.

**Table 2.1. Power Supply Pin Overview**

Pin Name	Product Family	Description
AVDD	All devices	Supply to analog peripherals
DECOUPLE	All devices	Output of the internal digital LDO and digital logic supply input
IOVDD	All devices	GPIO supply voltage
VREGVDD	All DC-DC-enabled devices	Input to the DC-DC converter
VREGSW	All DC-DC-enabled devices	DC-DC powertrain switching node
VREGVSS	All DC-DC-enabled devices	DC-DC ground
DVDD	All devices	Input to the internal digital LDO
RFVDD	All devices	Supply to radio analog and HFXO
PAVDD	All devices	Supply to radio power amplifier

### 2.4 DVDD and DECOUPLE

All EFR32 Wireless Gecko Series 2 devices include an internal linear regulator that powers the core and digital logic. The DECOUPLE pin is the output of the digital LDO, and requires a 1  $\mu\text{F}$  capacitor. For better high frequency noise suppression a 0.1  $\mu\text{F}$  capacitor can be placed in parallel with the 1  $\mu\text{F}$  capacitor on the DECOUPLE pin.

As mentioned in section [2.2 Decoupling Capacitors](#), care should be taken in the selection of decoupling capacitors for regulator output, such as DECOUPLE, to ensure that changes in system temperature and bias voltage do not cause capacitance changes that fall outside of the data sheet specified limits, which could destabilize the regulator output.

#### EFR32 Wireless Gecko Series 2 DVDD Pin

On EFR32 Wireless Gecko Series 2 devices, the input supply to the digital LDO is the DVDD pin and the DECOUPLE pin is the output of the LDO. Decoupling of DVDD should include a bulk capacitor of  $C_{\text{DVDD}}$  and this bulk capacitor should be at least 2.7  $\mu\text{F}$  for EFR32xG22 and 2.2  $\mu\text{F}$  for EFR32xG21. For better high frequency noise suppression a 0.1  $\mu\text{F}$  capacitor ( $C_{\text{DVDD1}}$ ) can be placed in parallel with the  $C_{\text{DVDD}}$  capacitor on the DVDD pin.

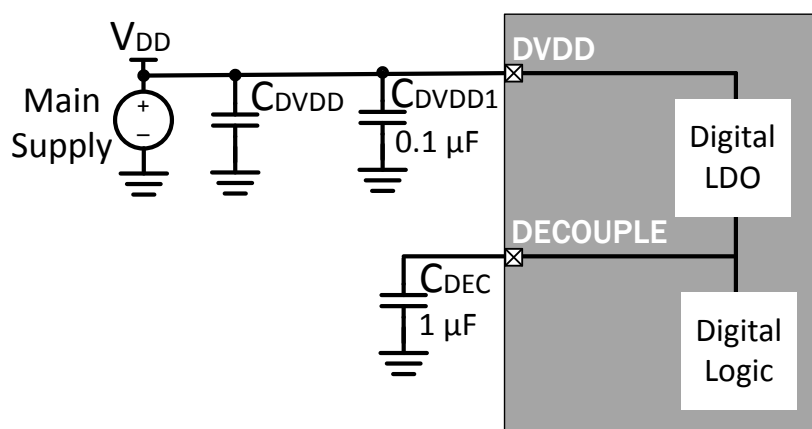


Figure 2.1. DVDD and DECOUPLE on EFR32 Wireless Gecko Series 2 Devices

**Note:**

- The DECOUPLE pin should not be used to power any external circuitry. Although DECOUPLE is connected to the output of the internal digital LDO, it is provided solely for the purposes of decoupling this supply and is not intended to power anything other than the internal digital logic of the device.
- On EFR32xG22, if DVDD is directly connected to the DCDC, then proper decoupling of DVDD should include a bulk capacitor of 4.7  $\mu\text{F}$  as shown in [3.4 EFR32 Wireless Gecko Series 2 — DCDC Example](#). This capacitor should be placed closer to the  $L_{\text{DCDC}}$  inductor and the VREGSW pin.

## 2.5 IOVDD

The IOVDD pin(s) provide decoupling for all of the GPIO pins on the device. For proper decoupling IOVDD should include a 0.1  $\mu\text{F}$  capacitor per IOVDD pin, along with a 1  $\mu\text{F}$  bulk capacitor. Increase the bulk capacitor value in applications using GPIO to drive heavy and dynamic loads.

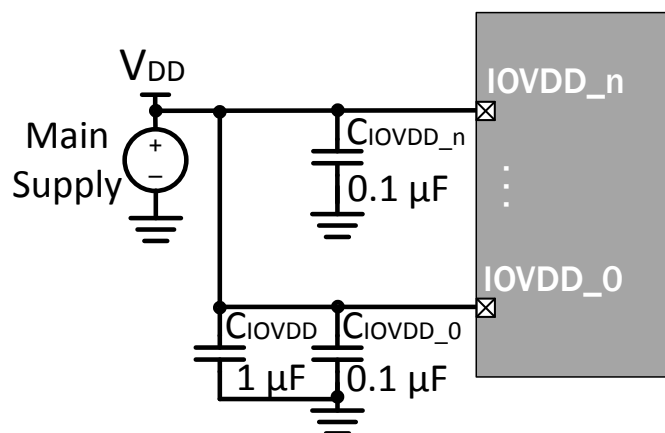


Figure 2.2. IOVDD Decoupling

**Note:** IOVDD can be driven by the output of the DC-DC converter when present on a device.

## 2.6 AVDD

The analog peripheral performance of the device is impacted by the quality of the AVDD power supply. For applications with less demanding analog performance, a simpler decoupling scheme for AVDD may be acceptable. For applications requiring the highest quality analog performance, more robust decoupling and filtering is required.

Note that the number of AVDD analog power pins may vary by device and package.

### 2.6.1 AVDD Standard Decoupling

The figure below illustrates a standard approach for decoupling the AVDD pin(s). In general, one 1  $\mu\text{F}$  bulk capacitor ( $C_{\text{AVDD}}$ ), as well as one 10 nF capacitor for each AVDD pin ( $C_{\text{AVDD}_0}$  through  $C_{\text{AVDD}_n}$ ), must be provided.

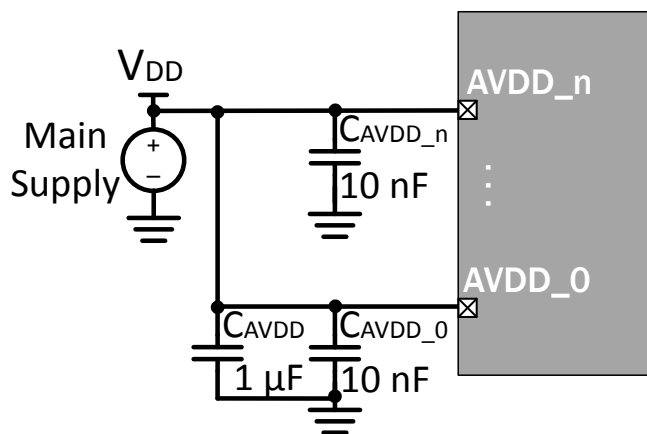


Figure 2.3. AVDD Standard Decoupling

### 2.6.2 AVDD Improved Decoupling

The figure below illustrates an improved approach for decoupling and filtering the AVDD pin(s). In general, one 1  $\mu\text{F}$  bulk capacitor ( $C_{\text{AVDD}}$ ), as well as one 10 nF capacitor for each AVDD pin ( $C_{\text{AVDD}_0}$  through  $C_{\text{AVDD}_n}$ ), must be provided. In addition, a ferrite bead and series 1  $\Omega$  resistor provide additional power supply filtering and isolation and is preferred when higher ADC accuracy is required.

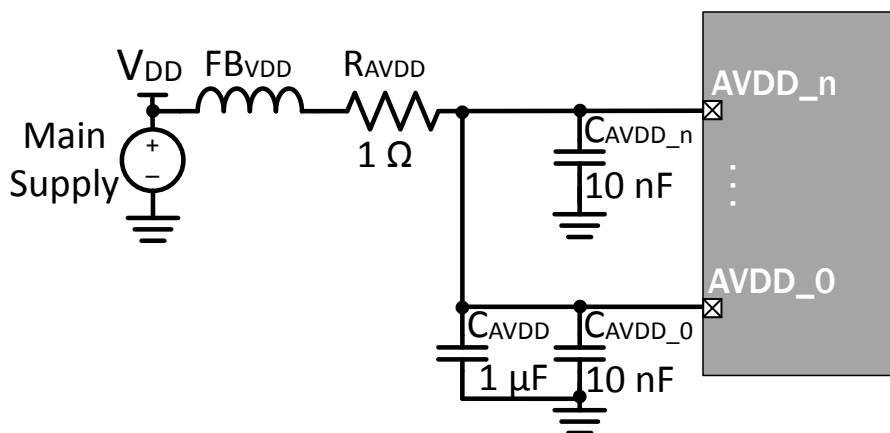


Figure 2.4. AVDD Improved Decoupling

**Note:** AVDD can be driven by the output of the DC-DC converter when present on a device, so long as analog peripheral inputs are limited to the lower of AVDD and IOVDD. For example, in a system with 3.3 V digital I/O, the current draw of analog peripherals, such as the IADC, can be reduced by allowing the DC-DC converter to supply AVDD with and limiting the analog inputs to 1.8 V.

The table below lists some recommended ferrite bead part numbers suitable for AVDD filtering.

**Table 2.2. Recommended Ferrite Beads**

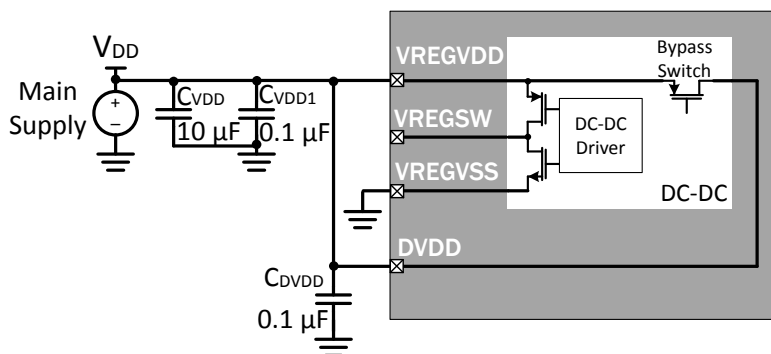
Manufacturer	Part Number	Impedance	$I_{MAX}$ (mA)	DCR ( $\Omega$ )	Operating Temperature ( $^{\circ}\text{C}$ )	Package
Würth Electronics	74279266	1 k $\Omega$ @ 100 MHz	200	0.600	-55 to +125	0603/1608
Murata	BLM21BD102SN1D	1 k $\Omega$ @ 100 MHz	200	0.400	-55 to +125	0805/2012

## 2.7 DC-DC

Some EFR32 Wireless Gecko Series 2 devices provide an on-chip DC-DC converter that can be used for improved power efficiency. However, the additional switching noise present on the DC-DC converter output ( $V_{DCDC}$ ), necessitates the use of specific filtering components.

### 2.7.1 DC-DC — Unused

When the DC-DC converter is not used, the DVDD pin should be shorted to the VREGVDD pin. VREGSW must be left floating, and VREGVSS should be grounded.



**Figure 2.5. Configuration when the DC-DC converter is unused**

### 2.7.2 DC-DC — Powering DVDD

For the lowest power applications, the DC-DC converter can be used to power the DVDD supply (as well as RFVDD and PAVDD on EFR32 Wireless Gecko Series 1) as shown in the figure below. In this configuration, the DC-DC Output ( $V_{\text{DCDC}}$ ) is connected to DVDD. In addition to being the DC-DC converter feedback path, the DVDD pin powers the internal digital LDO, which in turn powers the digital circuits.

The system designer should pay particular attention to the characteristics of the DC-DC output capacitor ( $C_{\text{DCDC}}$ ) over temperature and bias voltage. Some capacitors, particularly those in smaller packages or using cheaper dielectrics, can experience a dramatic reduction in nominal capacitance in response to temperature changes or as the DC bias voltage increases. Any change pushing the DC-DC output capacitance outside the datasheet specified limits may result in output instability on that supply.

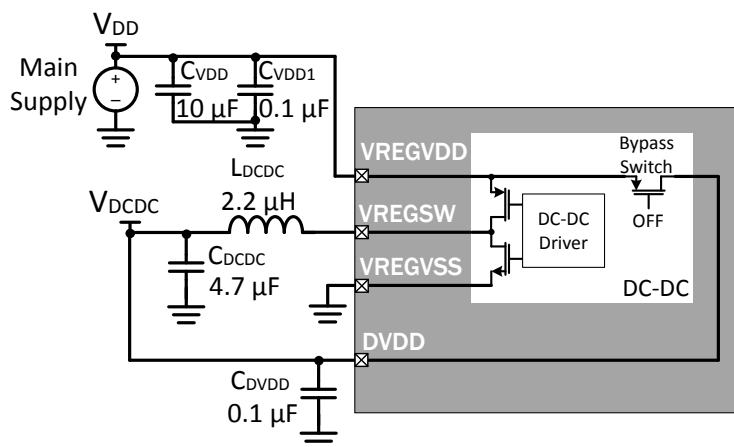


Figure 2.6. DC-DC Converter Powering DVDD

**Note:** For some Series 2 devices, there are additional DC-DC operating limits which should be observed for performance and reliability. Refer to the device datasheet for additional details.

### 2.8 Radio (RFVDD & PAVDD) — EFR32 Wireless Gecko Series 2

On EFR32xG21 devices, the recommended configuration for the radio power supplies (PAVDD and RFVDD) is as follows:

- Connect both PAVDD and RFVDD to the main supply. This configuration supports transmit power up to 20 dBm.

On EFR32xG22 devices, the radio power supplies (PAVDD and RFVDD) are typically powered from one of two sources:

1. The integrated DC-DC converter. This option provides improved power efficiency and supports up to 6 dBm transmit power.
2. The main supply. This option is less efficient and supports up to 6 dBm transmit power.



## 2.8.1 RFVDD and PAVDD — Powered from Main Supply

PAVDD and RFVDD can be powered directly from the main supply on both EFR32xG21 and EFR32xG22 devices. The component values for each device can be found in [Table 2.3 RFVDD & PAVDD Decoupling Values, Powered from Main Supply on page 9](#).

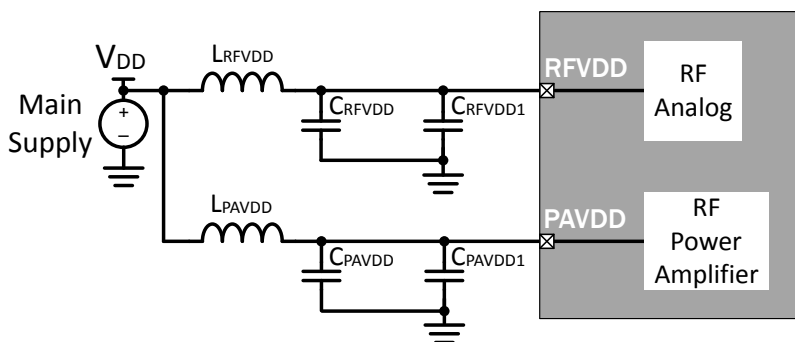


Figure 2.7. RFVDD and PAVDD Decoupling (2.4 GHz application, both supplies powered from main supply)

Table 2.3. RFVDD & PAVDD Decoupling Values, Powered from Main Supply

Device	Application	L <sub>RFVDD</sub>	C <sub>RFVDD</sub>	C <sub>RFVDD1</sub>	L <sub>PAVDD</sub>	C <sub>PAVDD</sub>	C <sub>PAVDD1</sub>
EFR32xG21	2.4 GHz	9.1 nH	47 nF	12 pF	9.1 nH	47 nF	12 pF
EFR32xG22		Ferrite bead (BLM15AG102 SN1 or similar)	100 nF	120 pF	Ferrite bead (BLM15AG102 SN1 or similar)	100 nF	120 pF

## 2.8.2 RFVDD and PAVDD — Powered from DCDC

On EFR32xG22 devices, improved power efficiency is achieved using the on-chip DC-DC converter to supply RFVDD and PAVDD.

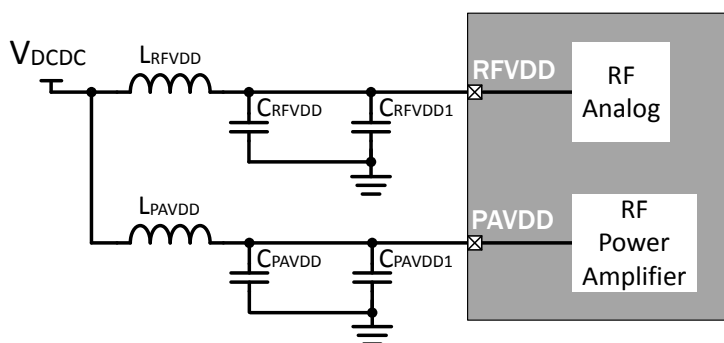


Figure 2.8. RFVDD and PAVDD Decoupling (2.4 GHz application, both supplies powered from DC-DC converter output)

Table 2.4. RFVDD & PAVDD Decoupling Values, Powered from DC-DC Converter

Application	L <sub>RFVDD</sub>	C <sub>RFVDD</sub>	C <sub>RFVDD1</sub>	L <sub>PAVDD</sub>	C <sub>PAVDD</sub>	C <sub>PAVDD1</sub>
2.4 GHz	Ferrite bead (BLM15AG102 SN1 or similar)	100 nF	120 pF	Ferrite bead (BLM15AG102 SN1 or similar)	100 nF	120 pF

### 3. Example Power Supply Configurations

#### 3.1 EFR32 Wireless Gecko Series 2 — Standard Decoupling Example

The figure below illustrates a standard approach for decoupling a EFR32 Wireless Gecko Series 2 device. The component values for RFVDD and PAVDD for each device can be found in [Table 3.1 RFVDD & PAVDD Decoupling Values, Powered from Main Supply](#) on [page 10](#). Refer to [2.4 DVDD and DECOUPLE](#) section for  $C_{DVDD}$  component value.

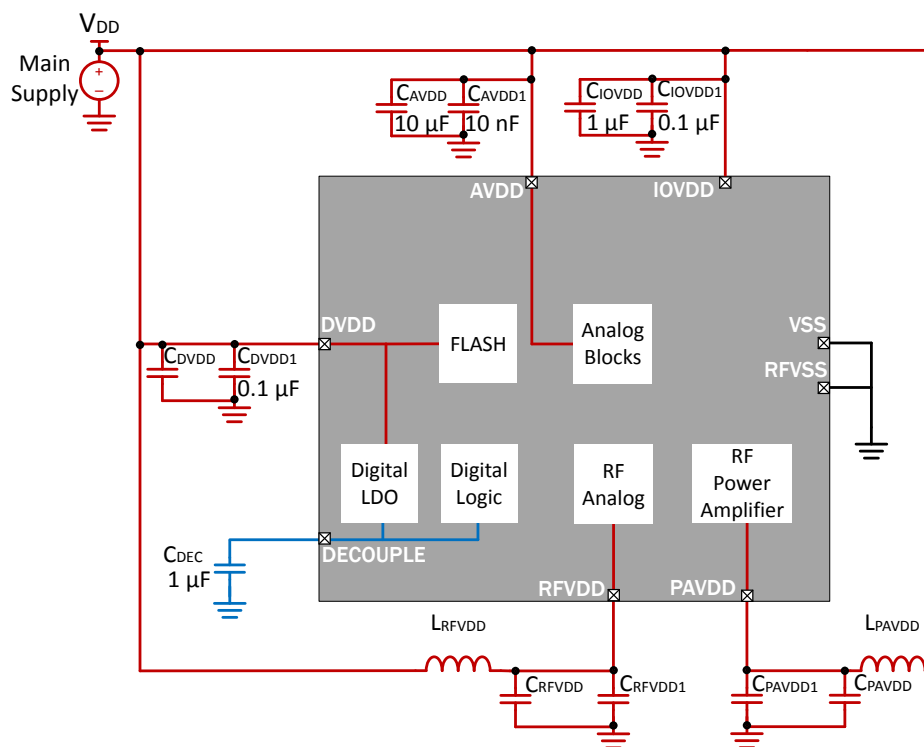


Figure 3.1. EFR32 Wireless Gecko Series 2 Standard Decoupling Example

Table 3.1. RFVDD & PAVDD Decoupling Values, Powered from Main Supply

Device	Application	L <sub>RFVDD</sub>	C <sub>RFVDD</sub>	C <sub>RFVDD1</sub>	L <sub>PAVDD</sub>	C <sub>PAVDD</sub>	C <sub>PAVDD1</sub>
EFR32xG21	2.4 GHz	9.1 nH	47 nF	12 pF	9.1 nH	47 nF	12 pF
EFR32xG22		Ferrite bead (BLM15AG102 SN1 or similar)	100 nF	120 pF	Ferrite bead (BLM15AG102 SN1 or similar)	100 nF	120 pF

### 3.2 EFR32 Wireless Gecko Series 2 — Improved AVDD Filtering Example

In the following figure, a decoupling approach providing better noise suppression and isolation between the digital and analog power pins using a ferrite bead and a resistor is illustrated. This configuration is preferred when higher ADC accuracy is required. Refer to [Table 2.2 Recommended Ferrite Beads on page 7](#) for recommended ferrite bead part numbers. The component values for RFVDD and PAVDD for each device can be found in [Table 3.2 RFVDD & PAVDD Decoupling Values, Powered from Main Supply on page 11](#). Refer to [2.4 DVDD and DECOUPLE](#) section for  $C_{DVDD}$  component value.

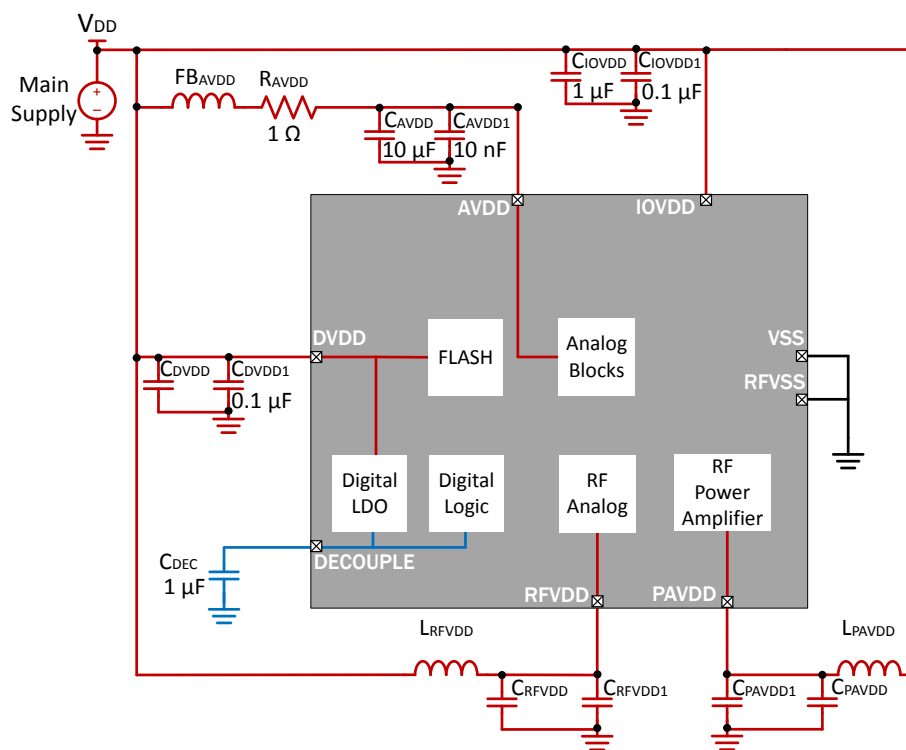


Figure 3.2. EFR32 Wireless Gecko Series 2 Improved AVDD Filtering Example

**Note:** Note that during power-on for EFR32 Wireless Gecko Series 2 devices, the AVDD\_x pins must not be powered up after the IOVDD\_x and DVDD pins. If the rise time of the power supply is short, the filter in the figure above can cause a significant delay on the AVDD\_x pins.

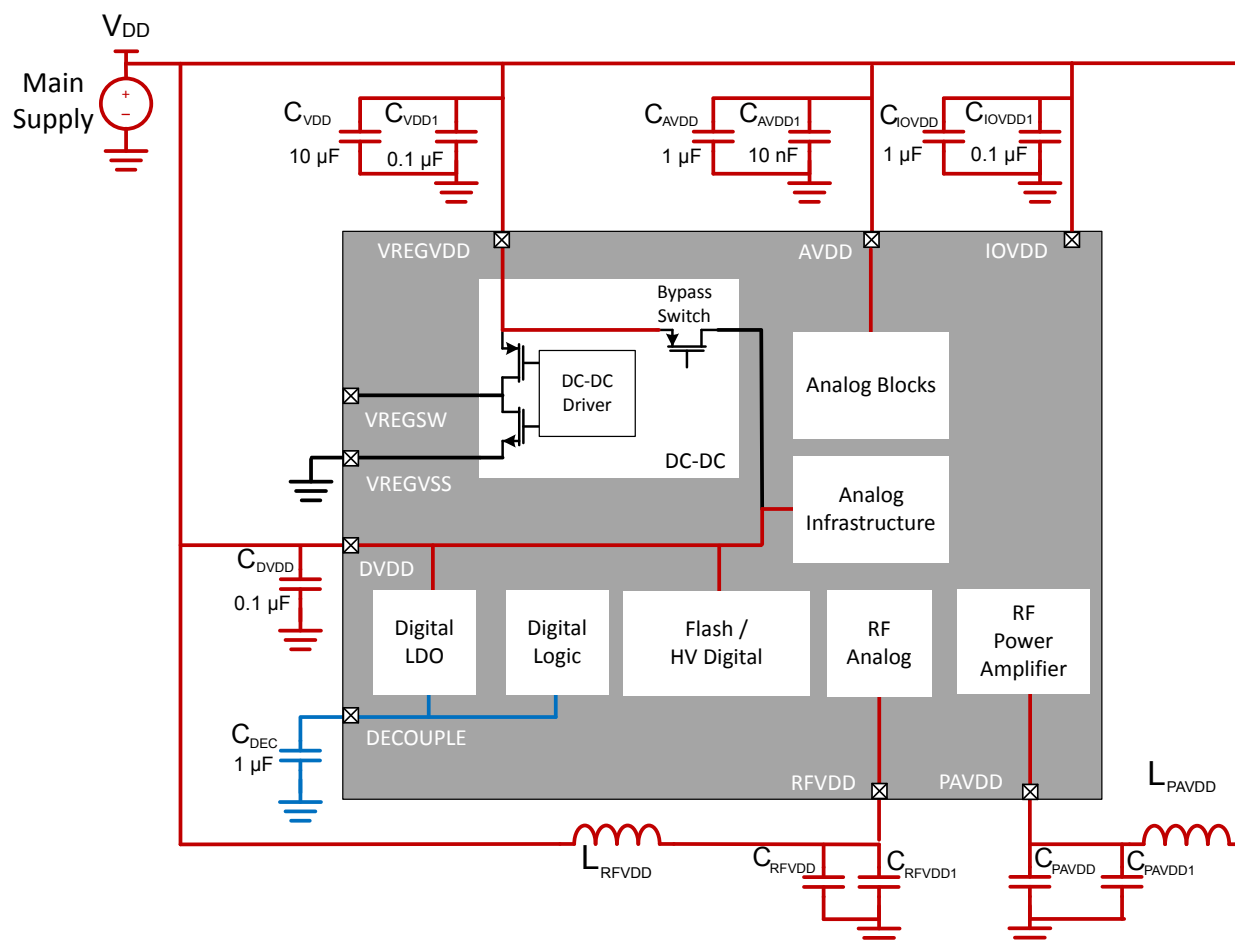
Table 3.2. RFVDD & PAVDD Decoupling Values, Powered from Main Supply

Device	Application	$L_{RFVDD}$	$C_{RFVDD}$	$C_{RFVDD1}$	$L_{PAVDD}$	$C_{PAVDD}$	$C_{PAVDD1}$
EFR32xG21	2.4 GHz	9.1 nH	47 nF	12 pF	9.1 nH	47 nF	12 pF
EFR32xG22		Ferrite bead (BLM15AG102 SN1 or similar)	100 nF	120 pF	Ferrite bead (BLM15AG102 SN1 or similar)	100 nF	120 pF

For space- or cost-sensitive applications or when power efficiency is not a factor, the DC-DC converter may be left unused. In this configuration:

- The DVDD pin must be shorted to VREGVDD
- In addition, AVDD, IOVDD, RFVDD, and PAVDD are all connected to the main supply.
- VREGSW should be left disconnected.

The RFVDD and PAVDD component values for each device can be found in [Table 3.3 RFVDD & PAVDD Decoupling Values, Powered from Main Supply on page 12](#).



**Figure 3.3. EFR32 Wireless Gecko Series 2 No DC-DC**

**Table 3.3. RFVDD & PAVDD Decoupling Values, Powered from Main Supply**

Device	Application	L <sub>RFVDD</sub>	C <sub>RFVDD</sub>	C <sub>RFVDD1</sub>	L <sub>PAVDD</sub>	C <sub>PAVDD</sub>	C <sub>PAVDD1</sub>
EFR32xG21	2.4 GHz	9.1 nH	47 nF	12 pF	9.1 nH	47 nF	12 pF
EFR32xG22		Ferrite bead (BLM15AG102 SN1 or similar)	100 nF	120 pF	Ferrite bead (BLM15AG102 SN1 or similar)	100 nF	120 pF

### 3.4 EFR32 Wireless Gecko Series 2 — DCDC Example

EFR32 Wireless Gecko Series 2 applications should use the DC-DC converter to maximize power savings when it is present on a device. When the DC-DC converter is used, supply voltages up to 3.3 V are supported without restriction. For supply voltages between 3.3 V and 3.8 V, see the device datasheet. The DC-DC converter requires an external inductor and capacitor, in addition to the standard decoupling capacitors on each power net. For detailed information on the DC-DC converter operation, emlib programming, recommended DC-DC components, and supported power configurations, see application note *AN0948: Power Configurations and DC-DC*.

For the lowest power radio applications, use the DC-DC converter to supply DVDD, as well as RFVDD and PAVDD. In this configuration:

- The DC-DC output ( $V_{\text{DCDC}}$ ) is connected to DVDD, which powers the internal digital LDO
- Both radio power supplies (RFVDD and PAVDD) are also powered from the DC-DC output.
- AVDD and IOVDD are connected to the main supply to support higher voltage external interfaces.

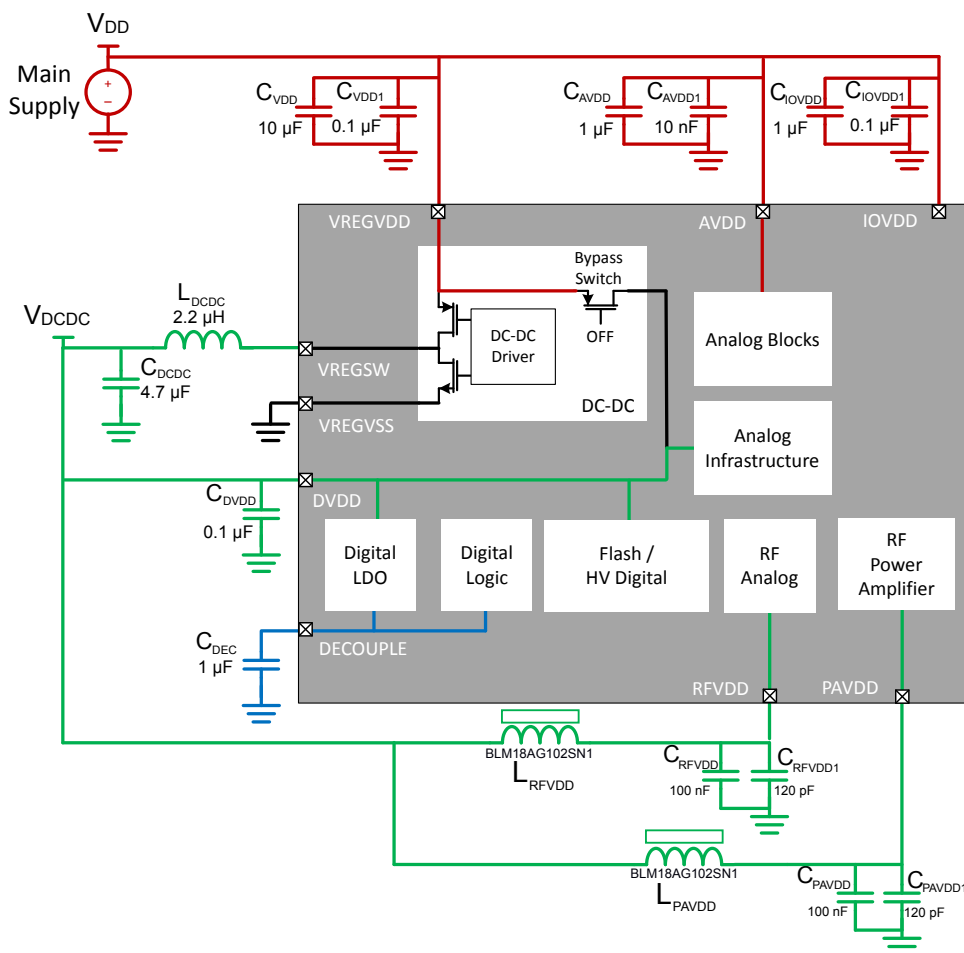


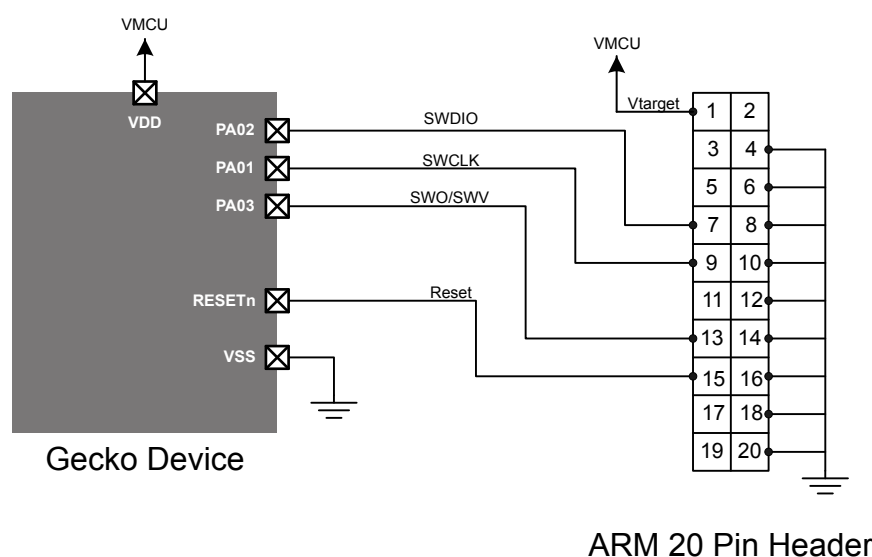
Figure 3.4. EFR32 Wireless Gecko Series 2 DCDC Power Configuration

## 4. Debug Interface and External Reset Pin

### 4.1 Serial Wire Debug

The Serial Wire Debug (SWD) interface is supported by all EFR32 Wireless Gecko Series 2 devices and consists of the SWCLK (clock input) and SWDIO (data in/out) lines, in addition to the optional SWO/SWV (serial wire output/serial wire viewer). The SWO/SWV line is used for instrumentation trace and program counter sampling, and is not needed for flash programming and normal debugging. However, it can be valuable in advanced debugging scenarios, and designers are strongly encouraged to include this along with the other SWD signals.

Connections to the standard ARM 20-pin debug header are shown in the following figure. Pins that are not connected to the microcontroller, power supply, or ground should be left unconnected.



**Figure 4.1. EFR32 Wireless Gecko Series 2 SWD Connection to the ARM 20-pin Debug Header**

**Note:** The  $V_{\text{target}}$  connection does not supply power. The debugger uses  $V_{\text{target}}$  as a reference voltage for its level translators.

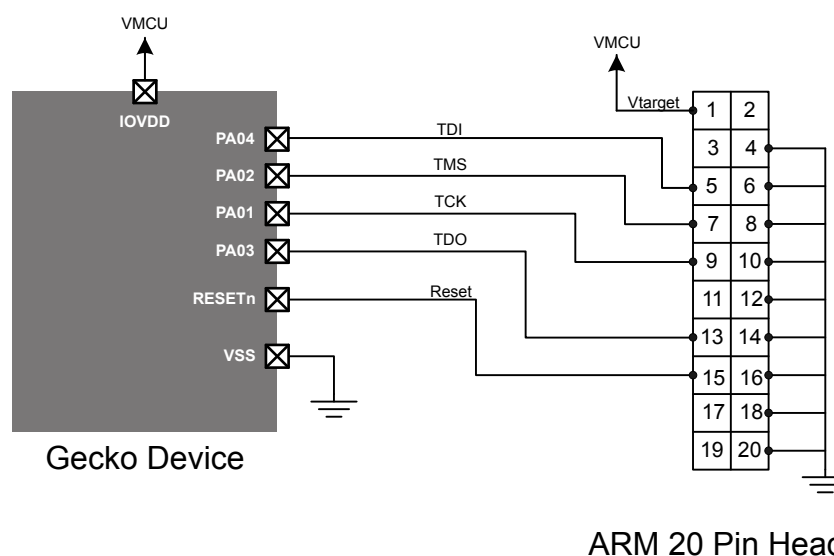
For additional debug and programming interfaces, see Application Note *AN958: Debugging and Programming Interfaces for Custom Designs*.

## 4.2 JTAG Debug

EFR32 Wireless Gecko Series 2 devices optionally support JTAG debug using the TCK (clock), TDI (data input), TDO (data output), and TMS (input mode select) lines. TCK is the JTAG interface clock. TDI carries input data, and is sampled on the rising edge of TCK. TDO carries output data and is shifted out on the falling edge of TCK. Finally, TMS is the input mode select signal, and is used to navigate through the Test Access Port (TAP) state machine.

**Note:** The JTAG implementation on EFR32 Wireless Gecko Series 2 devices does not support boundary scan testing. It can operate in pass-through mode and participate in a chain with other devices that do implement JTAG for firmware programming or boundary scan purposes.

The connection to an ARM 20-pin debug connector is shown in the following figure. Pins with no connection should be left unconnected.



**Figure 4.2. EFR32 Wireless Gecko Series 2 JTAG Connection to the ARM 20-pin Debug Header**

**Note:** The  $V_{\text{target}}$  connection does not supply power. The debugger uses  $V_{\text{target}}$  as a reference voltage for its level translators.

For additional debug and programming interfaces, see Application Note AN958: *Debugging and Programming Interfaces for Custom Designs*.

## 4.3 External Reset Pin (RESETn)

EFR32 Wireless Gecko Series 2 processors are reset by driving the RESETn pin low. A weak internal pull-up device holds the RESETn pin high, allowing it to be left unconnected if no external reset source is required. Also connected to RESETn is a low-pass filter to prevent noise glitches from causing unintended resets. The characteristics of the pull-up device and input filter are identical to those present on any GPIO pin and are specified in the device data sheet.

### Note:

1. The internal pull-up ensures that the reset is released. When the device is not powered, RESETn must not be connected through an external pull-up to an active supply or otherwise driven high as this could damage the device.
2. The RESETn pin is pulled up internally to DVDD. In the case where RESETn is connected to an external signal capable of driving the pin at a voltage different from  $V_{\text{DVDD}}$ , this internal pull up represents a possible current path, which could cause unwanted power consumption. Examples include connection of RESETn to an external supply/reset monitor, debugger, or coprocessor/multi-chip design. It is recommended that if RESETn is connected to an external device, it be connected only to open drain signals in order to avoid unwanted current consumption when RESETn is not being driven low.

## 5. External Clock Sources

### 5.1 Introduction

EFR32 Wireless Gecko Series 2 devices support different external clock sources to provide the high- and low-frequency clocks in addition to the internal LF and HF RC oscillators. Possible external clock sources for both the LF and HF domains are crystals and external oscillators (square or sine wave). This section describes how external clock sources are connected.

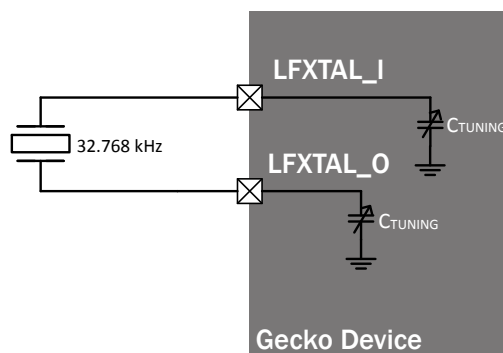
For additional information on the external oscillators, refer to the application note, [AN0016.2: Oscillator Design Considerations](#). Application notes can be found on the Silicon Labs website ([www.silabs.com/32bit-appnotes](http://www.silabs.com/32bit-appnotes)) or in Simplicity Studio.

### 5.2 Low-Frequency Clock Sources

An external low-frequency clock can be supplied from a crystal or from an external clock source.

#### 5.2.1 Low-Frequency Crystals

A crystal is connected as shown in the figure below across the LFXTAL\_I and LFXTAL\_O pins on EFR32 Wireless Gecko Series 2 devices.



**Figure 5.1. Low-Frequency Crystal Oscillator**

Low frequency crystals connected to EFR32 Wireless Gecko Series 2 devices do not require external load capacitors, as these load capacitors are included on-chip and can be tuned by register bit fields under software control, thus reducing BOM cost and saving space in the PCB footprint. The EFR32 Wireless Gecko Series 2 LFXO supports 32.768 kHz crystals. Check device-specific data sheets for supported crystal load capacitance and ESR values and refer to device-specific reference manuals for on-chip load capacitor tuning instructions.



### 5.2.2 Low-Frequency External Clocks

EFR32 Wireless Gecko Series 2 devices can source a low-frequency clock from an external source such as a TCXO or VCXO. To select a proper external oscillator, consider specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle, and signal levels. The external clock signal can be either a square wave or a sine wave with a frequency of 32.768 kHz. The external clock source must be connected as shown in [Figure 5.2 Low-Frequency External Clock on page 17](#).

Bypass and buffered input modes are supported for external clock sources. A CMOS square wave that toggles between 0 and  $V_{IOVDD}$  volts with a duty cycle of 50% can be used when `LFXO_CFG_MODE = DIGEXTCLK`, which bypasses the LFXO. An external sine wave source (`LFXO_CFG_MODE = BUFEXTCLK`) having minimum and maximum amplitudes of 100 mV and 500 mV, respectively, can be connected in series with the `LFXTAL_I` pin and is AC-coupled internally. The sine wave minimum voltage must be higher than ground and the maximum voltage less than  $V_{IOVDD}$ . When using either `DIGEXTCLK` or `BUFEXTCLK` mode, the `LFXTAL_O` pin is free to be used as a general purpose GPIO.

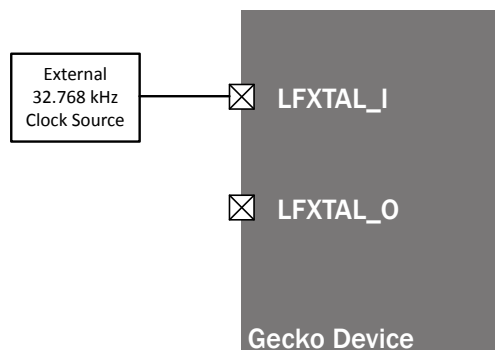


Figure 5.2. Low-Frequency External Clock

### 5.3 High Frequency Clock Sources

An external high-frequency clock can be supplied from a crystal or from an external clock source.

#### 5.3.1 High-Frequency Crystals

A crystal is connected as shown in [Figure 5.3 High-Frequency Crystal Oscillator on page 17](#) across the `HFXTAL_I` and `HFXTAL_O` pins on EFR32 Wireless Gecko Series 2 devices.

External load capacitors are not required on EFR32 Wireless Gecko Series 2 devices. These have been moved on-chip and can be tuned by register bit fields under software control, thus reducing BOM cost and saving space in the PCB footprint. Check device-specific data sheets for the supported range of crystal frequencies, load capacitance tuning, and ESR values. In particular, specific crystal frequencies are mandatory when using on-chip radios and their associated protocol stacks; use of other values is expressly **not** supported.

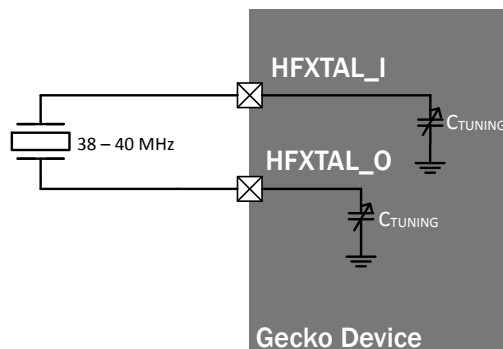
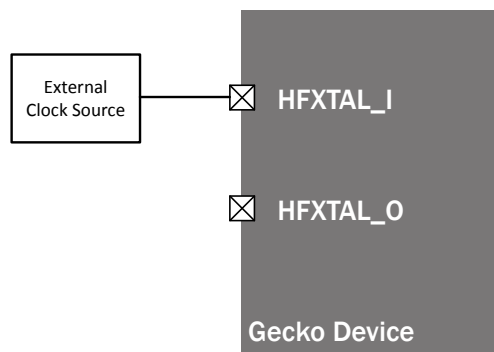


Figure 5.3. High-Frequency Crystal Oscillator

### 5.3.2 High-Frequency External Clocks

EFR32 Wireless Gecko Series 2 devices can source a low-frequency clock from an external source such as a TCXO or VCXO. To select a proper external oscillator, consider specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle, and signal levels. The external clock signal can be either a square wave or a sine wave with a frequency in accordance with the device data sheet. The external clock source must be connected as shown in [Figure 5.4 High-Frequency External Clock on page 18](#).

Unlike the LFXO, which has specific modes for a buffered or digital external clock, the HFXO has more limited external clock input flexibility. When a crystal is not used, the external clock signal must be a sine wave (HFXO\_CFG\_MODE = EXTCLK) having minimum and maximum amplitudes of 100 mV and 500 mV, respectively, can be connected in series with the HFXTAL\_I pin and is AC-coupled internally. The sine wave minimum voltage must be higher than ground and the maximum voltage less than 1.4 V.



**Figure 5.4. High-Frequency External Clock**

## 6. Revision History

### Revision 0.5

June, 2020

- Added required amplitude of a sine wave oscillator input in [5.2.2 Low-Frequency External Clocks](#) and [5.3.2 High-Frequency External Clocks](#).

### Revision 0.4

April, 2020

- Added information about EFR32xG22 in [2.4 DVDD and DECOUPLE](#), [2.5 IOVDD](#) and [2.6 AVDD](#) sections.
- Added reference to [2.4 DVDD and DECOUPLE](#) section for  $C_{DVDD}$  value in [3.1 EFR32 Wireless Gecko Series 2 — Standard Decoupling Example](#) and [3.1 EFR32 Wireless Gecko Series 2 — Standard Decoupling Example](#) sections.
- Updated  $C_{IOVDD}$  value in [3.3 EFR32 Wireless Gecko Series 2 — No DCDC Example](#) and [3.4 EFR32 Wireless Gecko Series 2 — DCDC Example](#) sections.

### Revision 0.3

March, 2020

- Added reference to AN933.2 in the front page.
- Updated Device Compatibility to add support for EFR32xG22.
- Added [2.7 DC-DC](#) to add support for EFR32xG22.
- Added information regarding powering RFVDD and PAVDD from Main Supply and DC-DC converter output in [2.8 Radio \(RFVDD & PAVDD\) — EFR32 Wireless Gecko Series 2](#).
- Added information about EFR32xG22 in [3. Example Power Supply Configurations](#).
- Removed references to ceramic resonator in [5. External Clock Sources](#).
- Removed references to external square wave source in [5.3 High Frequency Clock Sources](#).

### Revision 0.2

December, 2019

- Added reference to AN958 in [4.1 Serial Wire Debug](#) and [4.2 JTAG Debug](#).

### Revision 0.1

February, 2019

- Initial revision.

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