



BMD101 Product Brief (Preliminary)

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Table of Contents

| | |
|--|-----------|
| Features and Benefits | 3 |
| High Performance Bio-Signal System-on-Chip (SoC) | 3 |
| Advanced Analog Signal Processing | 3 |
| Powerful Digital Processing Capability | 3 |
| Flexible Interface | 3 |
| Low Power Consumption | 3 |
| ESD Protection with External Diodes | 3 |
| Clocking Scheme | 4 |
| Small Form Factor | 4 |
| Target Applications | 4 |
| Sensor Electrode Requirements | 4 |
| Device Overview | 5 |
| System Function | 5 |
| Analog Front End | 5 |
| Digital Signal Processing | 6 |
| Notch Filter | 6 |
| Low Pass Filter | 6 |
| Electrical Characteristics | 7 |
| Absolute Maximum Ratings ^{(1),(2),(3)} | 7 |
| BMD101 Specifications, (Preliminary) | 8 |
| Digital Output Packets Format | 9 |
| Data Payload Format | 10 |
| Step-By-Step Guide to Parsing a Packet | 11 |
| Application Block Diagram | 12 |
| Document Conventions | 12 |
| Acronyms Definition | 12 |
| Packaging Information | 13 |
| Package Pin Assignments | 13 |
| Appendix A: BMD101 SON8-3mm x 3mm x 0.6mm Package Outline | 13 |

Features and Benefits

High Performance Bio-Signal System-on-Chip (SoC)

- Single Chip Solution for accurate Bio-Signal Detection and Processing
- Mixed Signal SoC with Integrated Analog Front End (AFE) and DSP
- Accurate ECG raw signals output

Advanced Analog Signal Processing

- High Performance AFE for Bio-Signal Detection Ranging from μV Level to mV Level
- Advanced Low-Noise Amplifier (LNA) and Anti-alias Filtering
- High Resolution (16-bit) ADC
- Low Input-Referred Noise
- Automatic Sensor-Off Detection
- Fully integrated high pass filter with DC drifts removal

Powerful Digital Processing Capability

- Reliable detection ($24 \sim 200\text{bpm}$)¹ and real time heart rate ($\pm 1\text{bpm}$)
- Strong notch filter with at least -60dB rejection for both 50Hz and 60Hz power supply
- Built-in low pass filter with stable passband to the cutoff frequencies and -40dB at the stop frequency

Flexible Interface

- UART (57600 Baud Rate) with 64 Byte TX FIFO

Low Power Consumption

- Single 3.3V ($3.3 \pm 10\%$) Power Supply with On-Chip 1.2V Regulator
- Low Current Consumption – 0.8mA

ESD Protection with External Diodes

- 8kV Air Discharge
- 4kV Contact Discharge

¹ Any heart rate greater than 200bpm or less than 24bpm can be calculated by raw ECG data

Clocking Scheme

- Built-In RC Oscillator

Small Form Factor

- SON8

Target Applications

Medical Equipment

- Health care center/Clinic ECG monitor and analysis
- HRV monitor
- Mobile ECG monitor and expert system

Portable Heart Rate Monitor

- Regular usage
- Long term care
- Sleep study
- Potential irregular heart rhythm detection

Sports and Training

- Heart rate monitor for recreation
- Heart rate guidance and alarm device for athlete training

Sensor Electrode Requirements

Sensor Materials

- Stainless Steel
- Silver-Silver Chloride (Ag-AgCl)

Sensor Dimensions

- Recommended Diameter of Sensor is ~10mm

Device Overview

System Function

BMD101 is NeuroSky's 3rd generation bio-signal detection and processing SoC device. BMD101 is designed with an advanced analog front-end circuitry and a flexible, powerful digital signal processing structure. It targets bio-signal inputs ranging from μV to mV level and deployed with NeuroSky proprietary algorithms.

The Low-Noise-Amplifier and ADC are the main components of the BMD101 analog front end. Because of the BMD101's extremely low system noise and programmable gain, it can detect bio-signals and convert them into digital words using a 16-bit high resolution ADC. The AFE also contains a sensor-off detection circuit.

The heart of the BMD101 digital circuit is a powerful system management unit. It is in charge of overall system configuration, operation management, internal/external communication, proprietary algorithm computation, and power management. BMD101 also comes with hardwired DSP blocks to accelerate calculations, such as various digital filtering, under the supervision of the system management unit.

Analog Front End

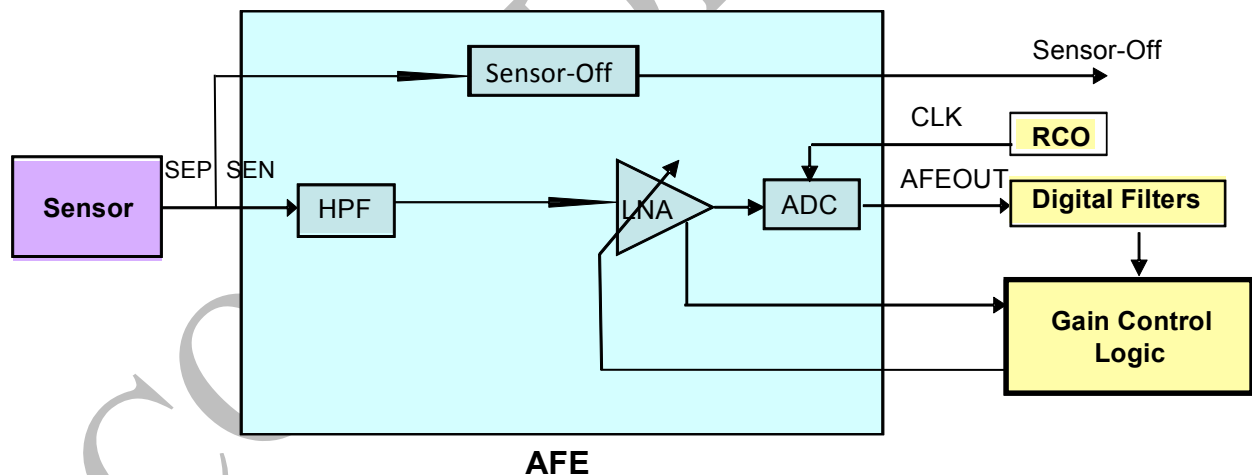


Figure 1. Block Diagram of AFE and its Interfaces to Sensor and ASIC Digital Section

The AFE receives low amplitude differential analog input signals. In case this signal contains large, slowly varying DC components, the DC is removed by a fully integrated high pass filter (HPF). The signal is then amplified by a programmable-gain low noise amplifier (LNA). The LNA output is converted to a digital bit stream by the 16-bit ADC.

BMD101 has built-in sensor-off detection capability. Any resistance between two sensor input pins that exceeds typically 19-25 Meg Ohms will trigger the sensor-off status.

Also, the BMD101 contains an internal LDO which consists of a bandgap cell to generate a 1.2V reference followed by two separate unity gain buffers, for the analog and digital supplies.

A digitally controlled oscillator (DCO) is included in the BMD101 as well, which provides a fully integrated 22.1MHz clock reference signal.

The majority of the filtering of the bio-signal in this system will be done in the digital domain. It is expected that the main interference is due to pick-up of the local power-supply frequency, i.e. 50Hz or 60Hz, depending on the geographical region.

The BMD101 has low DC offset levels as referred to the input of the ASIC, very low input referred noise and a low noise floor. It has good SNR and very good ENOB for the ECG application ranges. BMD101 CMRR levels are also very low.

Digital Signal Processing

After data leaves the ADC it goes through the digital filters per Figure 2.

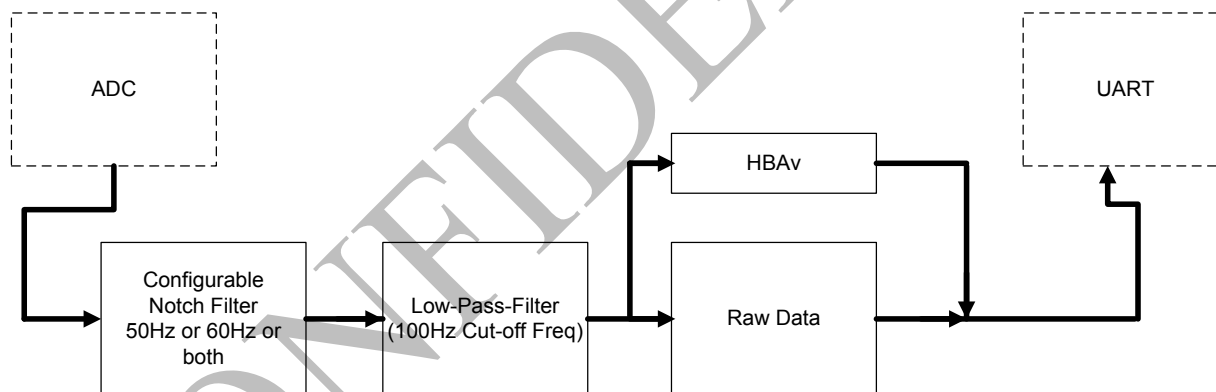


Figure 2. Digital Signal Processing Data Path

Notch Filter

The Notch Filter is typically customized to be a 50Hz or 60Hz or both notch through configuration. The notch rejection is usually -63dB for both 60Hz and 50Hz.

Low Pass Filter

The Low Pass Filter has 100Hz cutoff frequency. It provides a stable passband to the cutoff frequency, and -40dB at the stop frequency.

Electrical Characteristics

Absolute Maximum Ratings ^{(1), (2), (3)}

| Symbol | Parameter | Min | Max | Units |
|--------------------|--|------|-----|--------|
| VDD | Input Voltage | -0.1 | 3.6 | V |
| V _{sense} | Analog Input Voltage , Differential Mode | -1.0 | 1.0 | V |
| T _{op} | Operating Temperature ⁽⁴⁾ | 0 | 70 | deg. C |

⁽¹⁾ The Absolute Maximum Ratings listed are the limits above which permanent damage to the device may, or will, occur. Continued normal operating performance is not guaranteed if the Absolute Maximum levels are exceeded.

⁽²⁾ Unless otherwise noted, all Absolute Maximum Ratings listed apply within the normal BMD101 operating temperature.

⁽³⁾ The Absolute Maximum Ratings listed include only the BMD101. No external circuitry is included.

⁽⁴⁾ Entire ASIC

Table 1. BMD101 Absolute Maximum Ratings

BMD101 Specifications, (Preliminary)BMD101 specifications under normal operating conditions ^{(1),(2),(3)}

| Symbol | Parameter | Min | Typical | Max | Units |
|----------------------|---|--------------------|---------|------|-----------|
| VDD | Input Operating Power Voltage | 2.5 | 3.3 | 3.6 | V |
| IDD | Input Operating Power Current | 700 | 870 | 1100 | uA |
| I _{Standby} | Standby Current(CS pin tied low) | 190 | 225 | 255 | uA |
| V _{OH} | Digital Output Voltage | 2.4 | | 3.6 | V |
| V _{OL} | Digital Output Voltage | -0.1 | | 0.4 | V |
| V _{IH} | Digital "1" Input Voltage | 1.6 | | 3.6 | V |
| V _{IL} | Digital "0" Input Voltage | 0 | | 0.8 | V |
| N/A | UART Baud Rate | | 57600 | | bits/sec. |
| V _{sense} | Analog Input Operating Voltage | -8 | | 8 | mV |
| G _{Notch} | Notch Filter Gain (50 Hz and 60 Hz) | -62 ⁽⁴⁾ | -69.6 | N/A | dB |
| F _{LCO} | Low Cutoff Frequency | | 0.5 | | Hz |
| F _{HCO} | High Cutoff Frequency | | 103 | | Hz |
| CMRR | Common Mode Rejection Ratio | | 82 | N/A | dB |
| SNR | Signal to Noise Ratio | | 68.2 | N/A | dB |
| PSRR | Power Supply Rejection Ratio | | 82 | N/A | dB |
| T _{op} | Operating Temperature ⁽⁵⁾ | 0 | 25 | 70 | deg. C |
| HBM | Analog Input ESD Voltage ⁽⁶⁾ | -2000 | | 2000 | V |

⁽¹⁾ Unless otherwise indicated, all parameter limits listed apply within the normal BMD101 operating temperature range.

⁽²⁾ The limits listed include only the BMD101. No external circuitry is included.

⁽³⁾ Gain = 128 linear for all cases.

⁽⁴⁾ With respect to Mid Band Gain, (Mid Band is 20 Hz)

⁽⁵⁾ Entire ASIC

⁽⁶⁾ (Human Body Model) per ANSI/ESDA/JEDEC JS-001-2010

Table 2. BMD101 Specifications, (Preliminary)

Digital Output Packets Format

BMD101 communicates through UART interfaces.

The main digital interface of BMD101 is the UART interface (TX/RX). It is a standard UART interface that deploys a 1 start bit, 8 data bits, and 1 stop bit format. Applications of UART can be built based on this UART interface.

The digital output packet of the UART/TX interface follows the following scheme:

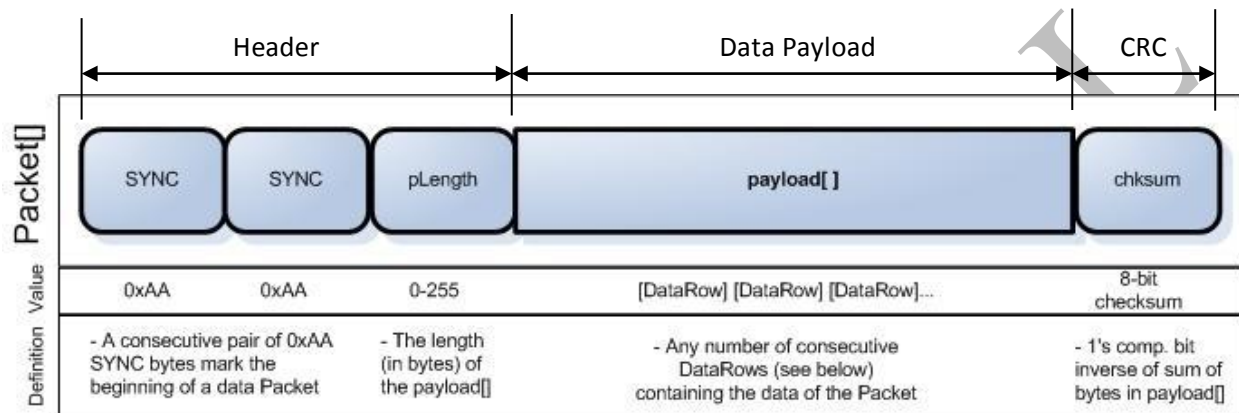


Figure 3. Digital Output Packet Format

Packets are sent as an asynchronous serial stream of bytes. Each packet begins with its Header, followed by its Data Payload, and ends with its CRC checksum byte.

The Header of a Packet consists of 3 bytes: two synchronization [SYNC] bytes (0xAA 0xAA), followed by a payload length [PLENGTH] byte. The two [SYNC] bytes are used to signal the beginning of a new arriving Packet. The [PLENGTH] byte indicates the length, in bytes, of the Packet's Data Payload.

The Data Payload of a Packet is simply a series of bytes. The number of Data Payload bytes in the Packet is given by the [PLENGTH] byte from the Packet Header. The interpretation of the Data Payload bytes is defined in detail in the "Data Payload Format" section below. Note that the Data Payload should NOT be parsed until AFTER the [CRC] Checksum is verified.

The CRC Checksum of a Packet must be used to verify the integrity of the Packet's Data Payload. The CRC Checksum is defined as:

- 1) Summing all the bytes of the Packet's Data Payload
- 2) Taking the lowest 8 bits of the sum
- 3) Performing the bit inverse (one's compliment inverse) on those lowest 8 bits

A receiver receiving a Packet must calculate the CRC Checksum of the Data Payload they received, and then compare it to the [CRC] Checksum byte received with the Packet. If calculated and received CRC values do not match, the entire Packet should be discarded as invalid. If they do match, then the Data Payload can then be parsed.

Data Payload Format

The Data Payload itself consists of a continuous series of DataRow. Parsing a Data Payload involves parsing each DataRow until all the bytes of the Data Payload have been parsed.

A DataRow consists of bytes in the following format:

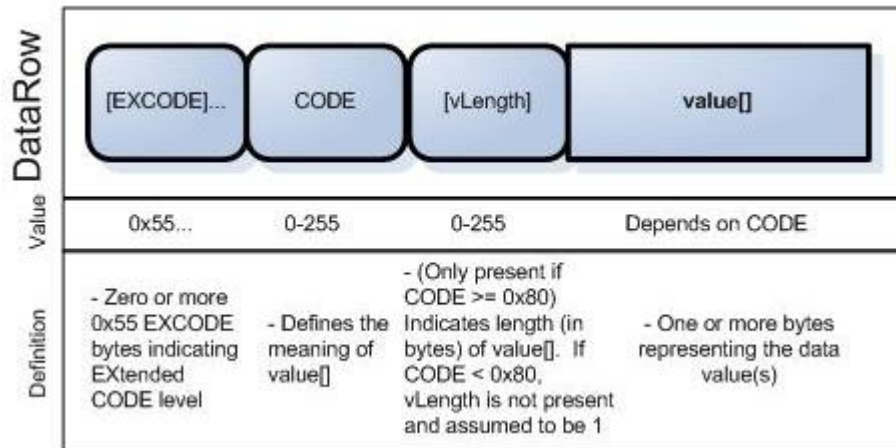


Figure 4. DataRow Format

The DataRow may begin with zero or more [EXCODE] (extended code) bytes, which are bytes with the value 0x55. The number of EXCODE bytes indicates the Extended Code Level. The Extended Code Level, in turn, is used in conjunction with the [CODE] byte to determine what type of data this DataRow contains.

The [CODE] byte indicates the type of data encoded in the DataRow. For example, a [CODE] of 0x03 indicates that the DataRow contains a heart rate value. For a list of defined [CODE] meanings, see the "[CODE] Definitions Table" below. Note that the meaning of the [CODE] is dependent on the Extended Code Level. Also note that the [EXCODE] byte of 0x55 will never be used as a [CODE] (nor will the [SYNC] byte of 0xAA).

If the [CODE] byte is between 0x00 and 0x7F, then there is no [LENGTH] byte, and the [DATA] byte immediately after the [CODE] is the 1-byte [DATA] value and the end of the DataRow.

If, however, the [CODE] byte is between 0x80 and 0xFF, then it is followed by a [LENGTH] byte indicating the number of bytes of [DATA...]. These higher [CODE]s are used for returning arrays of values, values that cannot fit in a single byte, or values that need a varying number of bytes to represent.

The format is defined in this way so that any properly implemented parser will not break in the future if new [CODE]s representing arbitrarily long [DATA...] values are added (they simply ignore unrecognized [CODE]s, but do not break in parsing), if the order of [CODE]s is rearranged in the Packet, or if some [CODE]s are not always transmitted in every Packet.

[CODE] Definitions Table

| Extended Code Level | [CODE] | (Byte) [LENGTH] | Data Value Meaning |
|---------------------|--------|--------------------|--|
| 0 | 0x02 | N/A | Signal Quality (0—sensor off, 200—sensor on) |
| 0 | 0x03 | N/A | Real-time Heart Rate (Beats Per Minute) |
| 0 | 0x08 | N/A | Don't Care |
| 0 | 0x80 | 2 | 16-bit Raw Data (2's Complement) |
| 0 | 0x84 | 5 | Don't Care |
| 0 | 0x85 | 3 | Don't Care |

Step-By-Step Guide to Parsing a Packet

1. Keep reading bytes from the stream until a [SYNC] byte (0xAA) is encountered.
2. Read the next byte and ensure it is also a [SYNC] byte (if not, return to step 1).
3. Read the [PLENGTH] byte.
4. Read the next PLENGTH bytes of the [PAYLOAD...], saving them into a storage area (such as an unsigned char payload [256] array). Sum up each byte as it is read by incrementing a checksum accumulator.
5. Take the lowest 8 bits of the checksum accumulator and invert them. Here is the C code:


```
checksum &= 0xFF;
checksum = ~checksum & 0xFF;
```
6. Read the [CRC] byte and verify that it matches your calculated checksum (if not, return to step 1).
7. Loop until all bytes (and hence, DataRow) have been parsed from the data payload[] array:
 - a) Parse and count the number of [EXCODE] bytes (0x55) that may be at the beginning of the current DataRow.
 - b) Parse the [CODE] byte for the current DataRow.
 - c) If applicable, parse the [LENGTH] byte for the current DataRow.
 - d) Parse and handle the [DATA...] byte(s) of the current DataRow, based on the DataRow's [EXCODE] level, [CODE], and [LENGTH].
 - e) If not all bytes have been parsed from the payload[] array, return to 7a. to parse the next DataRow.

Application Block Diagram

BMD101 is a total single chip solution with very small form factor and low power consumption, suitable for portable applications. It requires almost zero effort to integrate with target systems.

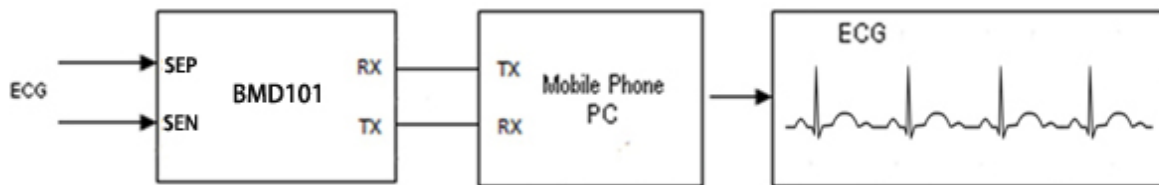


Figure 5. BMD101 Application Example

Document Conventions

Acronyms Definition

| | |
|-------|---|
| AFE | Analog Front End |
| ASIC | Application Specific Integrated Circuit |
| CMRR | Common Mode Rejection Ratio |
| CRC | Cyclic Redundancy Check |
| ECG | Electrocardiography |
| IP | Intellectual Property |
| LDO | Low Drop Out |
| POR | Power-On-Reset |
| SNR | Signal to Noise Ratio |
| TX/RX | Transmit/Receive |
| UART | Universal Asynchronous Receiver/Transmitter |

Packaging Information

| Orderable Device | Status | Package Type | Pins | Eco Plan ⁽¹⁾ | MSL, Peak Temp ⁽²⁾ | Storage Temp ⁽³⁾ |
|------------------|--------|--------------|------|-------------------------|-------------------------------|-----------------------------|
| NS BMD101 | ACTIVE | SON | 8 | Pb-Free (RoHS) | Level-3-260C-168 HR | 5°C - 30°C |

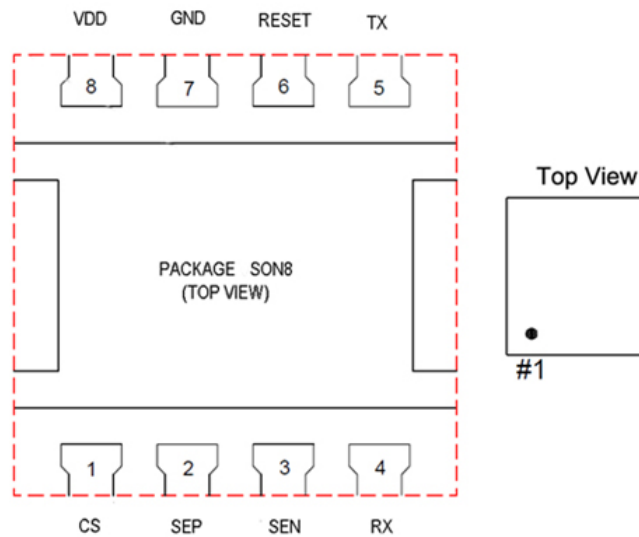


Figure 6. BMD101 Pinout

Package Pin Assignments

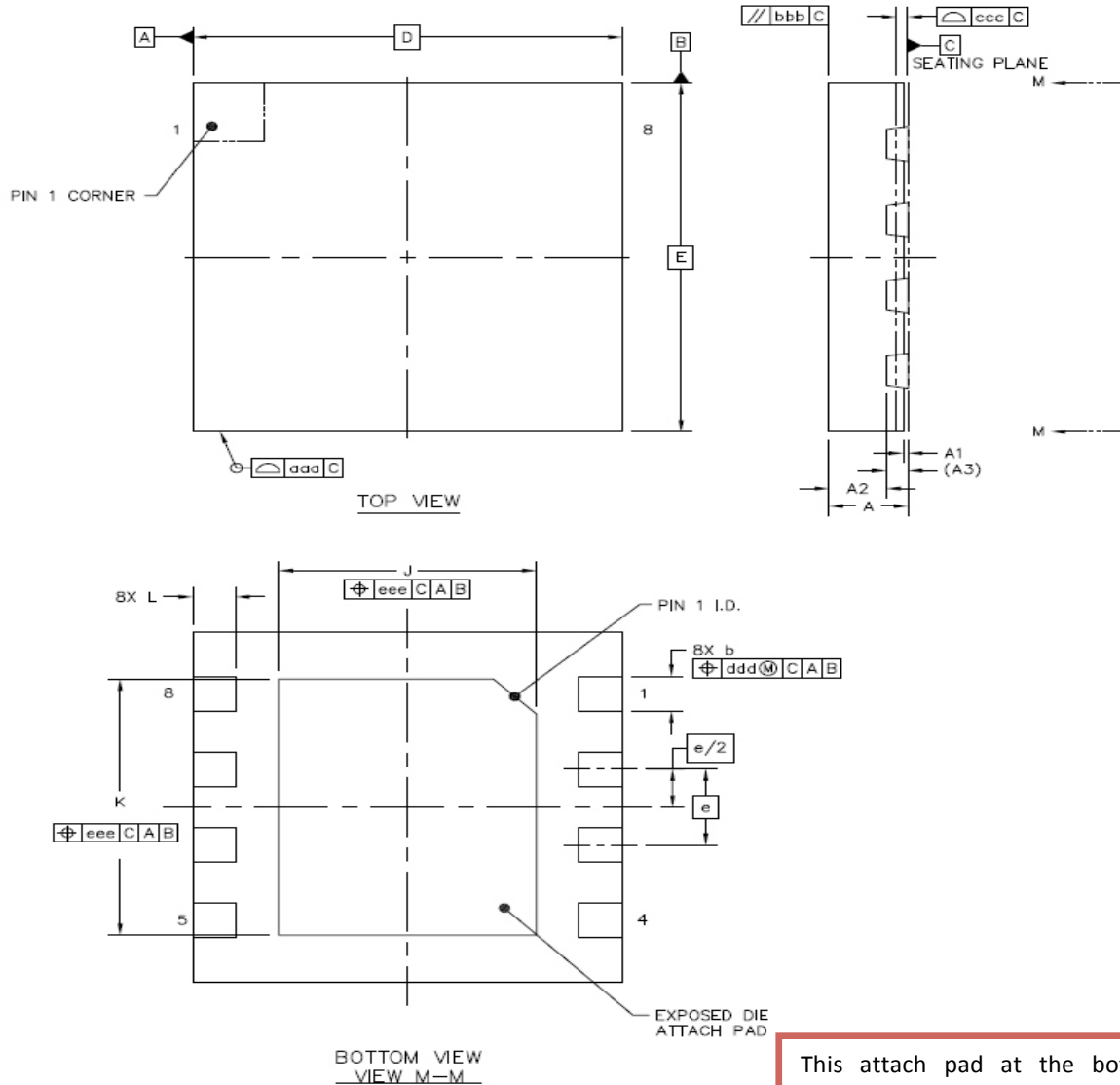
| Terminal | Name | Function | Direction | Comment |
|----------|-------|---------------------------------|-----------|-------------|
| 1 | CS | Power up or down control of LDO | Input | Active high |
| 2 | SEP | Positive ECG analog input | Input | |
| 3 | SEN | Negative ECG analog input | Input | |
| 4 | RX | UART RX | Input | |
| 5 | TX | UART TX | Output | |
| 6 | RESET | System reset pin | Input | Active low |
| 7 | GND | Ground | Supply | |
| 8 | VDD | 3.3V power supply | Supply | |

⁽¹⁾ Pb-Free (RoHS) -- The term "Lead-Free" or "Pb-Free" means semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials.

⁽²⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications and peak solder temperature.

⁽³⁾ Recommended Temperature: room condition around 5 °C to 30 °C (can be stored for 1 year).

Appendix A: BMD101 SON8-3mm x 3mm x 0.6mm Package Outline



This attach pad at the bottom does not need to connect to GND.

| | | SYMBOL | MIN | NOM | MAX |
|------------------------|---|--------|-----------|-------|-------|
| TOTAL THICKNESS | | A | 0.5 | 0.55 | 0.6 |
| STAND OFF | | A1 | 0 | 0.035 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.4 | 0.425 |
| L/F THICKNESS | | A3 | 0.152 REF | | |
| LEAD WIDTH | | b | 0.25 | 0.3 | 0.35 |
| BODY SIZE | X | D | 3 BSC | | |
| | Y | E | 3 BSC | | |
| LEAD PITCH | | e | 0.65 BSC | | |
| EP SIZE | X | J | 1.7 | 1.8 | 1.9 |
| | Y | K | 2.1 | 2.2 | 2.3 |
| LEAD LENGTH | | L | 0.25 | 0.3 | 0.35 |
| PACKAGE EDGE TOLERANCE | | aaa | 0.1 | | |
| MOLD FLATNESS | | bbb | 0.1 | | |
| COPLANARITY | | ccc | 0.08 | | |
| LEAD OFFSET | | ddd | 0.1 | | |
| EXPOSED PAD OFFSET | | eee | 0.1 | | |

Figure 7. BMD101 Physical Dimensions