Design and Prototyping a Fast Hadamard Transformer for WCDMA

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Abstract

In this paper, the design and implementation of a Fast Hadamard Transformer (FHT) on a field programmable gate array (FPGA) is described. Two possible schemes which use 256 and 16 chip input sequences are compared on a Xilinx Virtex-E XCV1000E FPGA. The results indicate that the 16 chip sequence achieves 90% reduction in hardware resources and more than double the maximum frequency of operation as compared to 256 chip sequences. An application of the proposed FHT design used to perform cell search for Wideband Code Division Multiple Access (WCDMA) system is also presented.

1.Introduction

In CDMA systems, each user is identified by a scrambling code. Orthogonal (Walsh-Hadamard) codes are used in order to minimize the interference due to two users trying to transmit at the same time. The codes are generated using a Hadamard matrix. When these codes are transmitted over the air channel, they are affected by interference, distortion and noise which may be the additive white gaussian noise (AWGN), Rayleigh fading or multipath channel fading. At the receiver a decoding logic is required which will correctly interpret the received vectors. A Fast Hadamard Transformer (FHT) can be used to provide such a low hardware complexity decoding circuitry [1]. The FHT is used for detecting and correcting errors during the transmission of Walsh-Hadamard codewords.

The FHT is an orthogonal transform and requires only addition and subtraction operations. This leads to savings in hardware resources as no multiplier is used. In this study a FHT is designed for WCDMA systems to be used in achieving synchronization with the base station. Previous FHT implementations consume a lot of hardware resources in terms of memory requirements and are not easily scalable for different input lengths [2,3,4]. The work presented by Amira et al and Nayak et al uses distributed arithemetic and systolic architectures in their implementations of the FHT [2,3]. A detailed comparison of their architectures and the present design is part of the future work. If the previous FHT designs are used in a cell search processor, the hardware circuitry cannot be re-used for other signal processing applications as the architecture presented in this paper. The design proposed in this paper minimizes the hardware resources used and also saves hardware resources in a cell search processor by re-using the circuitry to perform Discrete Fourier Transform (DFT). The DFT design is explained by the author in [5]. The second part of this study also suggests means for further reducing the hardware resources while decoding the 256 chip Walsh-Hadamard sequences by reducing the sequence length to 16 chips. The proposed designs in this study lead to considerable savings in hardware resources. The significance of this work is that it presents a novel hardware efficient architecture for a FHT and also presents an innovative application of the FHT for performing cell search in WCDMA.

2.Background

In a CDMA system, the coded data sequence is multiplied by orthogonal codes generated using the Hadamard matrix at the base stations. While at the mobile station, the same sequence must be multiplied by the received signal after removing the spreading sequence. Hadamard matrices are used to generate the orthogonal codes. A Hadamard matrix of order 1 and 2 is shown below. This matrix is then used to generate Hadamard matrices of higher order.

$$H_1 = \begin{bmatrix} 1 \end{bmatrix}, H_2 = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$$

In general, a Hadamard matrix is defined iteratively as,

$$H_{2N} = \begin{bmatrix} H_N & H_N \\ H_N & -H_N \end{bmatrix}$$

where H_{2N} is a matrix of order N. Hadamard transformation of an input vector X can be expressed as,

$$Y = HX \quad (1)$$

As each element of the Hadamard matrix is either a +1 or a -1 the operation of multiplication given in equation (1) can be reduced to a series of addition/subtraction operations. In general, for a N-point input sample the FHT algorithm needs to perform $N\log_2 N$ addition and subtraction operations.

3.FHT Design

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The FHT is used to calculate a correlation coefficient for each received codeword which expresses the likelihood that a received codeword is the correct Walsh-Hadamard code. The Walsh-Hadamard code having the largest coefficient is then selected as the most likely code that was transmitted. There are a number of stages in the FHT design depending on the length of the Walsh-Hadamard sequence. Figure 1 shows an individual stage of the FHT. Each stage has an upper and a lower input terminal. The output of each stage of the FHT is then given to the next stage. The technique used to generate the correlation coefficients will become clear when we discuss the design for a 256 chip FHT.

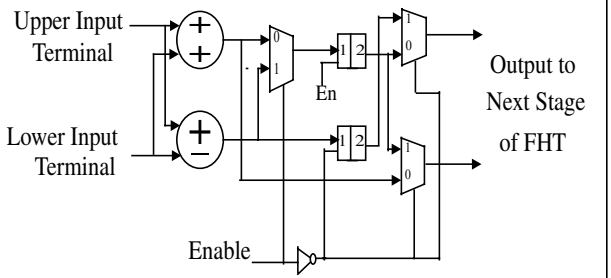

Figure 1: Individual Stage of FHT

Figure 2 shows the design for a FHT structure which is used for decoding a 256 chip Walsh-Hadamard sequence. The FHT structure shown is divided into different stages. If a block of N Walsh-Hadamard chips is to be processed then the upper input terminal receives N/2 input signal bits and the lower input terminal, the remaining N/2 signal bits. The upper and lower input terminal of the first stage receive signal bits from the buffer. The inputs to the FHT are applied non-sequentially. In a 256 chip FHT, during the first clock cycle the first Walsh-Hadamard chip "1" is input to the upper input terminal of the first stage and the Walsh-Hadamard chip "129" is input to the lower input terminal. In the next clock cycle, Walsh-Hadamard chips "2" and "130" arrive at upper and lower input terminals, then "3" and "131" and so on. The input signals from Walsh-Hadamard chips corresponding to "1" through "128" are applied to the upper input terminal and "129" through "256" are applied to the lower input terminal.

The correlation coefficients generated by each stage of the FHT which is not the last stage are called intermediate correlation coefficients. The memory implemented as shift registers stores the intermediate correlation results. The counter shown in Figure 2, is used for selecting each of the stages of the FHT. The bits of the counter are used as enable signals for each of the stages. The counter bit C0 is the LSB and C6 is the MSB. Counter bit C6 is alternately low for 64 clock cycles and then goes high for the next 64 clock cycles (i.e. 0000000..0111111,1000000..1111111). The bit C0 is alternately low and high for each clock cycle (i.e. 0000000,0000001,0000010,0000011,etc.). The number of bits in the counter depends on the number of stages which in turn depends on the length of Walsh-Hadamard sequence to be used. If there are N Walsh-Hadamard chips then the counter length must be $\log_2 N$ bits. The length of the shift register in each of the stages "s" of the design is given by the following relation $(N/4)/2^s$. For example, the length of the shift registers used in the first stage of the FHT is $(256/4)/2^0=64$. The length of registers used in the other stages can be calculated in a similar manner.

The upper shift registers in each of the stages are always enabled whereas the lower shift registers are enabled by the bits of the counter. The input vectors are given to the adder and subtractor which generate the correlation coefficients. The correlation coefficient or Hadamard code metrics which need to be generated is explained in Table 1 for a 16 chip input sequence. This operation is also called the butterfly operation. The butterfly operation is also used in other DSP applications such as in computing the Discrete Fourier Transform (DFT) using the Fast Fourier Transform (FFT) algorithm.

The multiplexers after the shift register in each stage of the FHT are configured to generate output signals corresponding to the upper and lower input terminal. In the last stage of the FHT, the outputs of these multiplexers are combined using an adder and a subtractor circuit. The output is then given to a comparator. The comparator selects the larger of the two code metrics. The larger metric corresponds to the Hadamard code which was transmitted and the Hadamard row is identified.

During clock cycles 0 through 63, bit C6 of the counter is 0, thus the input terminal "0" of the first multiplexer (Mux 1_1) in stage 1 is selected. The upper adder circuit in stage 1 generates outputs corresponding to the summation of the pairs of input Walsh-Hadamard chips applied during the first 64 clock cycles and the lower subtractor circuit generates signals corresponding to the difference of these pairs of input signals. The upper shift register is enabled to store the results of the addition and the lower shift register stores the difference of the first 64 pairs of input Walsh-Hadamard chips. After 64 clock cycles, bit C6 of the counter goes high and the lower shift register is disabled. The input terminals "0" of the outer multiplexers (Mux 1_2 and Mux 1_3) in stage 1 are selected. As bit C6 is high for the next 64 clock cycles, Mux 1_1 generates output signals corresponding to the next 64 Walsh-Hadamard chip pairs as received by the subtractor. The upper shift register in stage 1 remains enabled so as to accept the output signals from the subtractor. Meanwhile, the lower shift register sequentially outputs signals corresponding to Walsh-Hadamard chips "0" through "63" which it received during the first 64 clock cycles. Thus, during clock cycles 64 through 127, input signals corresponding to Walsh-Hadamard chips “0” through "63" arrive at the upper output terminal of stage 1

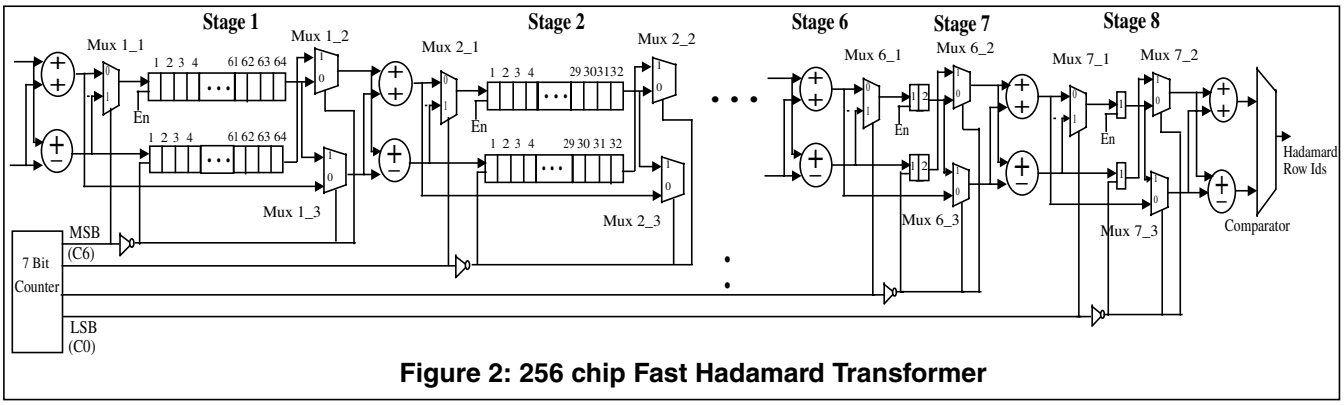

Figure 2: 256 chip Fast Hadamard Transformer

and input signals corresponding to Walsh-Hadamard chips "64" through "127" arrive at the lower output terminal. These signals are then given to the next stage of the FHT. Similar operations are performed in the subsequent stages of the FHT to generate the correlation coefficients. It is clear from the butterfly operation, that each subsequent stage of the FHT receives an input from the previous stage in half the number of clock cycles required for the previous stage. This is achieved by reducing the length of shift register in each subsequent stage of the FHT by a factor of two.

4.Application of FHT in WCDMA Cell Search

In an asynchronous CDMA system, the mobile station needs to achieve code, time and frequency synchronization with the base station before any communication with the base station can take place. This process of achieving synchronization with the base station is called cell search [6,7,8]. Cell search is performed in different types of scenarios: initial cell search which is performed when a mobile station is switched on and target cell search which is performed during idle and active modes during a call. In WCDMA systems, there are 512 downlink scrambling codes. To reduce the cell search time, the synchronization process is divided into different stages: (1) slot boundary detection, (2) code group and frame boundary identification, (3) scrambling code identification, (4) frequency synchronization, and, (5) cell identification. The last two stages are performed only during initial cell search.

Target cell search is used to find handover candidates during a call. In target cell search, the mobile station is already camped on a cell and receives a neighbor cell list from the network. This simplifies the cell search procedure, since the scrambling codes of the other cells are already known.

4.1 Synchronization Channels in Cell Search

Three synchronization channels are used in cell search as shown in Figure 3: the Primary Synchronization Channel (P-SCH), Secondary Synchronization channel (S-SCH) and the Common Pilot Channel (CPICH).

The P-SCH is used to carry code sequences of length 256

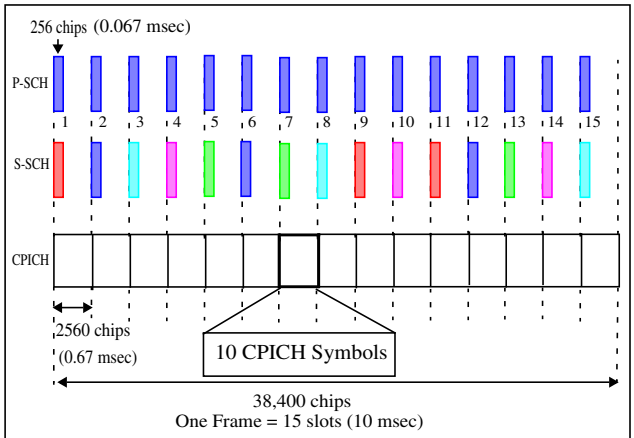

Figure 3: Synchronization Channels in Cell Search

chips transmitted time aligned with the slot boundary. The same code sequence is used by all the base stations. The S-SCH is used to carry different code sequence in each of the slots and the entire code sequence is repeated after every radio frame. A radio frame consists of 38,400 chips and is divided into 15 slots. Each slot is of 2,560 chips. The CPICH is used to carry the downlink common pilot symbols scrambled by the scrambling code of the base station. Each slot of this channel is divided into 10 symbols each of 256 chips.

4.2 Cell Search Algorithm

The process of achieving code and time synchronization in the cell search algorithm is divided into three stages (1) slot synchronization, (2) frame synchronization and code group identification, and, (3) scrambling code identification.

4.2.1 Stage 1: Slot Synchronization

During stage 1 of the cell search procedure the mobile

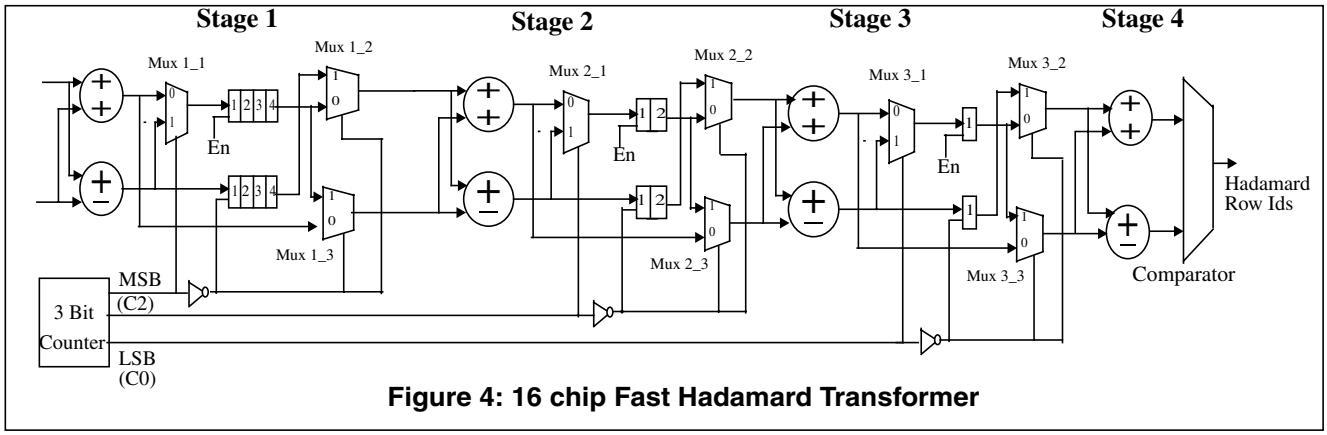

Figure 4: 16 chip Fast Hadamard Transformer

Table 1: Hadamard Code Metrics (Butterfly Operation)

Input	Stage 1	Stage 2	Stage 3	Stage 4
y1	y1+y2	(y1+y2)+(y3+y4)	((y1+y2)+(y3+y4))+ ((y5+y6)+(y7+y8))	((y1+y2)+(y3+y4))+((y5+y6)+(y7+y8))+ ((y9+y10)+(y11+y12))+((y13+y14)+(y15+y16))
y2	y1-y2	(y1+y2)-(y3+y4)	((y1+y2)+(y3+y4))- ((y5+y6)+(y7+y8))	((y1+y2)+(y3+y4))+((y5+y6)+(y7+y8))- ((y9+y10)+(y11+y12))+((y13+y14)+(y15+y16))
. . .				
y15	y15+y16	(y13-y14)+(y15-y16)	((y9-y10)-(y11-y12))+ ((y13-y14)+(y15-y16))	((y1-y2)-(y3-y4))-((y5-y6)-(y7-y8))+ ((y9-y10)-(y11-12))-((y13-y14)+(y15-y16))
y16	y15-y16	(y13-y14)-(y15-y16)	((y9-y10)-(y11-12))- ((y13-y14)+(y15-y16))	((y1-y2)-(y3-y4))-((y5-y6)-(y7-y8))- ((y9-y10)-(y11-12))-((y13-y14)+(y15-y16))

station uses the SCHs, Primary Synchronization Code (PSC) to acquire slot synchronization to a cell. This is typically done with a single filter matched to the PSC which is common to all cells. The slot timing of the cell can be obtained by detecting peak values in the matched filter output. The starting position of the synchronization code may be determined from observations over one slot duration. However, decisions based on observations over a single slot may be unreliable, when the signal-to-noise ratio (SNR) is low or if fading is severe. Reliable slot synchronization is required to minimize cell search time. In order to increase reliability, observations are made over multiple slots and the results are then combined. This ensures that the correct slot boundary is identified.

4.2.2 Stage 2: Frame Synchronization and Code Group Identification

During stage 2 of the cell search procedure, the mobile station uses the SCHs Secondary Synchronization Code (SSC) to achieve frame synchronization and identify the code group of the cell found in stage 1. This is done by correlating the received signal with all possible SSC sequences and identifying the maximum correlation value. Since the cyclic shifts of the sequences are unique, the code group as well as the frame synchronization is determined.

4.2.3 Stage 3: Scrambling Code Identification

During stage 3 of the cell search procedure, the mobile station determines the exact primary scrambling code used by the cell. The primary scrambling code is typically identified through symbol-by-symbol correlation over the CPICH with all codes within the code group identified in stage 2. In this stage, a threshold value is used to decide whether the code has been identified. The threshold value can be predetermined using a parameter called the probability of false alarm rate [1]. The hardware implementations of stage 1 and stage 3 of the cell search designs are discussed in [9]. In this paper we consider stage 2 of the cell search design which uses a reduced length FHT design shown in Figure 4, to identify the code group

4.3 WCDMA Secondary Synchronization Codes

The 64 secondary SCH sequences are constructed such that their cyclic shifts are unique, i.e., a non-zero cyclic shift less than 15 of any of the 64 sequences is not equiva-

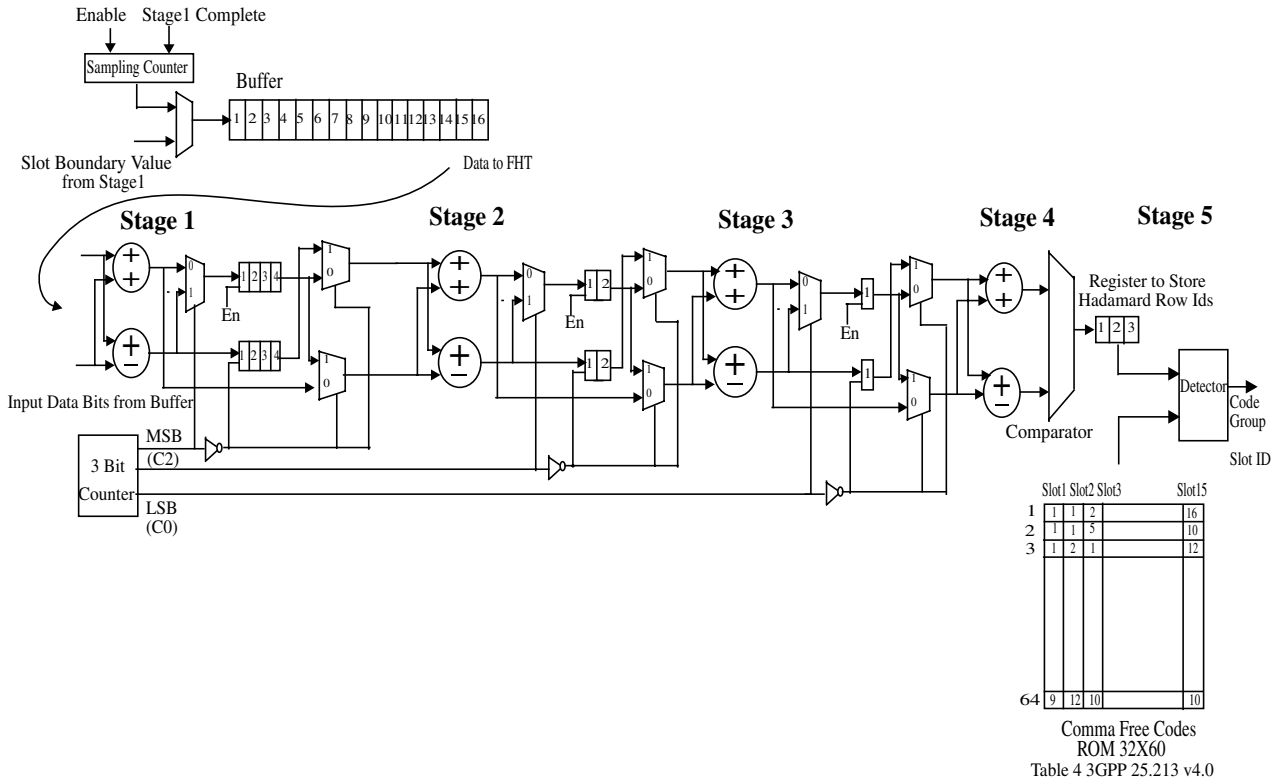

Figure 5: Stage 2 of Cell Search Design using a Fast Hadamard Transformer

Table 2: Allocation of Secondary Synchronization Codes used in Cell Search

Scrambling Code Group	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Group 0	1	1	2	8	9	10	15	8	10	16	2	7	15	7	16
Group 1	1	1	5	16	7	3	14	16	3	10	5	12	14	12	10
• • •															
Group 62	9	11	12	15	12	9	13	13	11	14	10	16	15	14	16
Group 63	9	12	10	15	13	14	9	14	15	11	11	13	12	16	10

lent to some cyclic shift of any other of the 64 sequences. Table 2 lists part of the sequences of SSCs used to encode the 64 different scrambling code groups.The 16 SSCs, ($C_{ssc,1}$,..,$C_{ssc,16}$), are complex-valued with identical real and imaginary components, and are constructed from position wise multiplication of a Hadamard sequence and a sequence z, defined as z=(b,b,b,-b,b,b,-b,-b, b,-b,b,-b,-b,-b,-b,-b), where b=(1,1,1,1,1,1,-1,-1,1,-1,1,-1,1,- 1,-1,1). The entries in Table 2, denote what SSC to use in the different slots for the different scrambling code groups, e.g. the entry "5" means that SSC, $C_{ssc,5}$ shall be used for the corresponding scrambling code group and slot. The k^{th} SSC, $C_{ssc,k}$ k=1,2,..,16 can be calculated using the following expression:

$C_{ssc,k}=(1+j)(H_m(0)z(0),H_m(1)z(1),..,H_m(255)z(255))$

where m=16(k-1) (2)

If the modulating sequence "z", is removed from equation (2), then the secondary code is same as the row of a Hadamard matrix. The value of "k" is obtained from Table 2 and varies from 1 to 16. Thus, there are 16 possible Hadamard sequences of length 256 chips.

4.4 Reduced Length FHT Design

If the 256X256 Hadamard matrix used to generate the secondary synchronization codes is observed carefully, then it is noticed that the 256 chip Walsh-Hadamard sequence can be identified by 16 chip sequences. Thus in a CDMA receiver, only the first 16 chips of the entire 256 chip Walsh-Hadamard sequence can be used. The reduced length sequence helps in reducing the hardware utilization.

Table 3: Hardware Comparison of 16 and 256 chip Fast Hadamard Transformer

FPGA XCV 1000E BG560 Speed Grade 6	Number of Slice Registers	Number of 4 Input LUTs	Equivalent Gate Count	Max. Frequency of Operation (Post Route Timing)
FHT 16 chips	71	173	1591	35.769 MHz
FHT 256 chips	1070	1370	17191	16.025 MHz

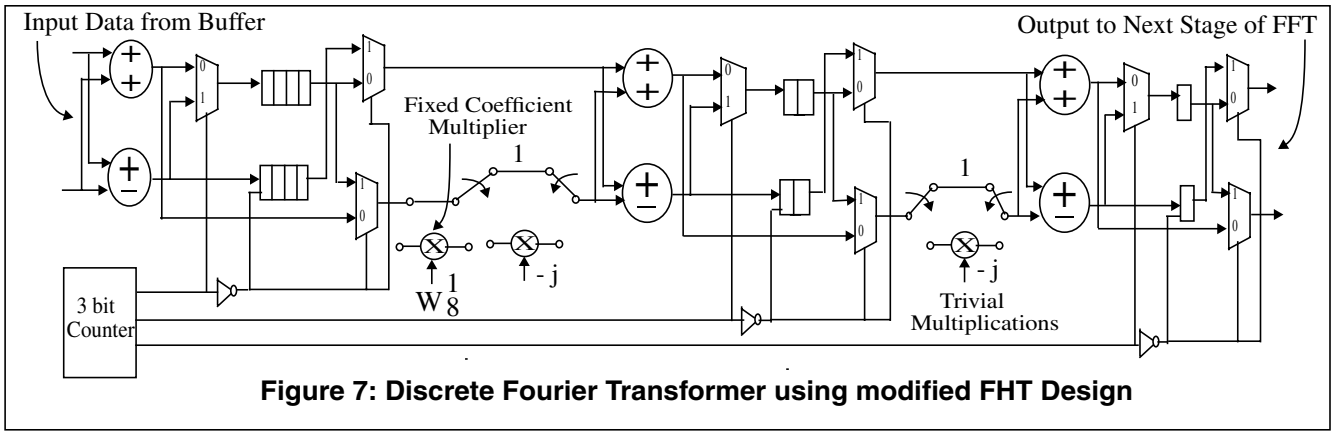

Figure 7: Discrete Fourier Transformer using modified FHT Design

The buffer which is used to store the input values will be reduced in length from 256 to 16 registers. The reduced length sequence will also reduce the detection time. Thus, the reduced length Walsh-Hadamard sequence helps in achieving faster decoding and reduced hardware circuitry as shown in Figure 4.

4.5 Cell Search Design

Figure 5 shows stage 2 of the cell search design. The inputs to the FHT are applied from the buffer according to the timing diagram shown in Figure 6. The FHT provides a very efficient means for decoding the Walsh-Hadamard codes. The FHT shown has an input sequence of length 16 chips. Accumulation over at least 3 slots is necessary to uniquely identify a code group in this design. These correspond to the 3 rows of the Hadamard matrix. Once the 3 Hadamard rows are identified then it is given to the detector, which finds the code group from the comma free table (Table 2) stored in a ROM. A 3-bit counter is used for selecting the stages as shown in Figure 5. Use of a counter to select each of the stages of the FHT leads to a reduction in hardware utilization. Once the metrics are generated then the largest metric is selected and the Hadamard row is decoded. The same process repeats for data collected from two more slots to completely detect the code group.

4.6 Re-using Hardware Modules for DFT

The hardware design for the reduced length FHT and the DFT are similar. In the DFT design, trivial multiplications and a fixed coefficient multiplier circuit are added to the FHT circuit. Thus, the same hardware circuit can be re-used for performing the FHT and the DFT as shown in Figure 7. This saves hardware resources in the cell search processor. The details of the DFT design are provided by the author in [5].

Butterfly Input								
Stage 1 Upper Input	1	2	3	4	5	6	7	8
Stage 1 Lower Input	9	10	11	12	13	14	15	16
Stage 2 Upper Input					1	2	3	4
Stage 2 Lower Input					5	6	7	8
Stage 3 Upper Input							1	2
Stage 3 Lower Input							3	4
Stage 4 Upper Input								1
Stage 4 Lower Input								2

Figure 6: Input Timing Diagram of 16 chip FHT

5.Experimental Method and Results

The designs were synthesized for a Xilinx Virtex-E XCV1000E FPGA [10] using the Xilinx Foundation ISE software. The same design constraints were used in the synthesis for both the cell search designs. From Table 3, we observe that the FHT design using 16 chips has a 90% lower equivalent gate count as compared to the FHT design using 256 chip input sequence and more than double the maximum frequency of operation.

6.Conclusions

The FHT design presented in this paper provides a hardware efficient circuitry for decoding the Walsh-Hadamard codes used in WCDMA cell search. Design schemes for reducing the input Walsh-Hadamard sequence length were also presented. The reduced length FHT design helps achieve 90% reduction in hardware resource and more than doubles the maximum frequency of operation. The significance of the design presented is that it can be easily modified for longer length sequences and the hardware circuitry can be re-used for performing DFT. This is beneficial for a cell search processor used in a mobile handset as it reduces the chip area and power utilization.

Further work is planned to use the modules already designed in a synchronization circuit for software defined radios. The reconfiguration of the circuit will be performed "on the fly" by passing different parameters to the hardware modules. Thus, the same circuitry can be used for different wireless specifications.

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