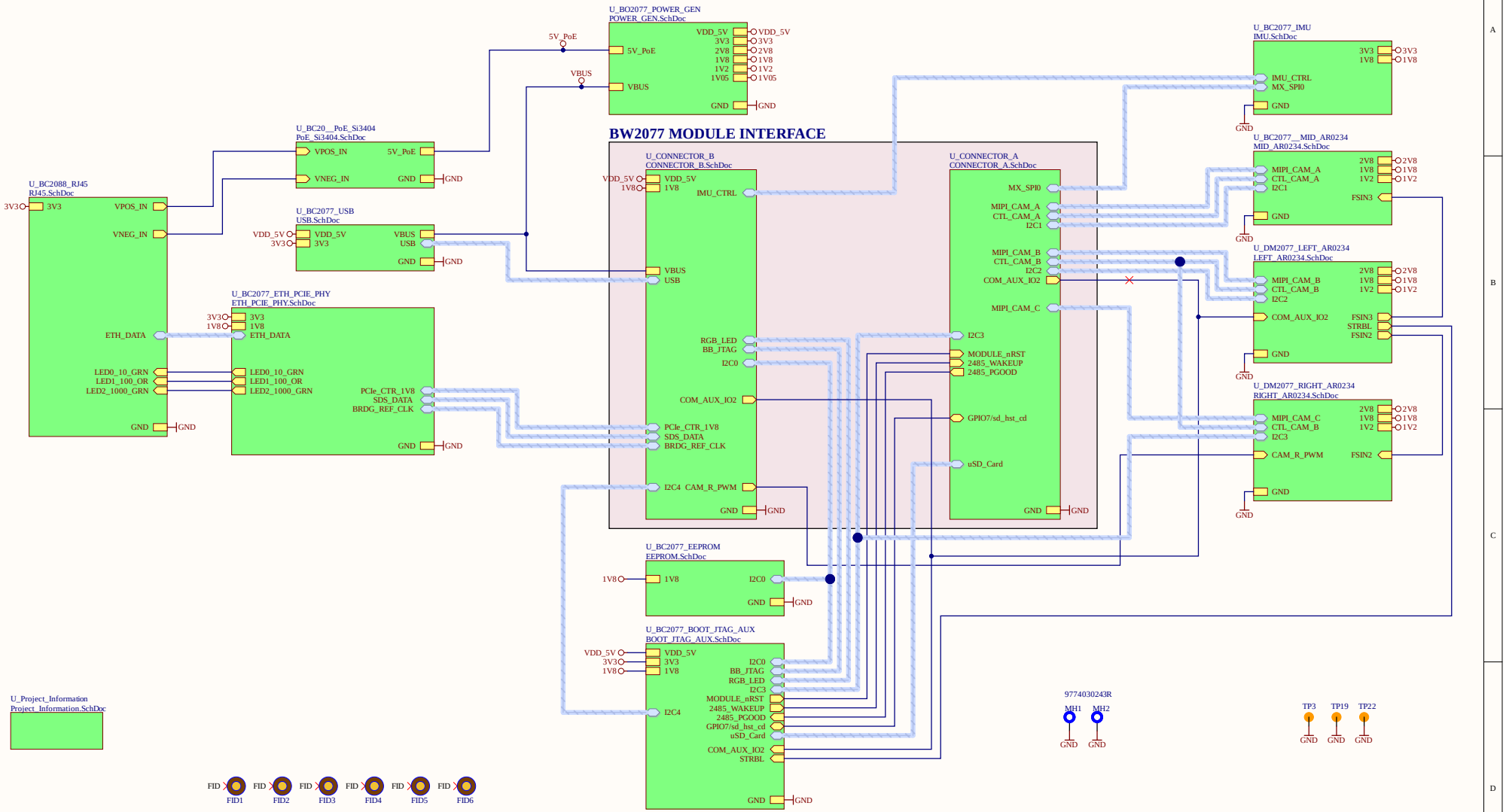
Project: ***BC2087***
Current Revision: ***R2M1E2***

BC2087 Revision History:

Date	Revision	Reason for Change	Changes Implemented
22/Aug/2022	Iniital Release -> R0M0E0		
17/01/2023	R0M0E0 -> R1M0E1	- Change the right camera to be connected to I2C3 not I2C0 as is at the moment. - Changed BNO INT and WAKE pins to IO42 and IO15 (MX) so that they are not on boot pins on KB. - PERST should be connected to IO - Right camera should have a seperate reset line - Boot resistor for KB in wrong configuration - Expose UART for KB debugging - No space for THT UART pins - FSYNC should be PWM capable	- Moved right camera to I2C3 - Changed pins to IO42 and IO15 (MX) - Changed PCIE_PERST to IO39 (MX) - Added right camera reset line to IO43 (MX) - Depupulated R45 - Added a header with I2C4/UART - Changed to SMD pins - Connected FSYNC to IO46 (MX) and IO14 (KB)

Title ***BC2087***			***Luxonis Holding*** ***1925 Harmony Park Drive*** ***Westminster, CO*** ***80234*** ***United States***	Cannot open file C:\Users\BrianLuxonis\
Size: Tabloid	Number:D2088000	Revision:R2M1E2		
Date: 26/04/2023 Time: 14:17:42	Sheet 1 of 12			
Drawn by: ***Boris Chou / Blaz Kvas***				



Title	BC2087		Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D2088000	Revision: R2M1E2	Cannot open file C:\Users\BrianLuxonis\
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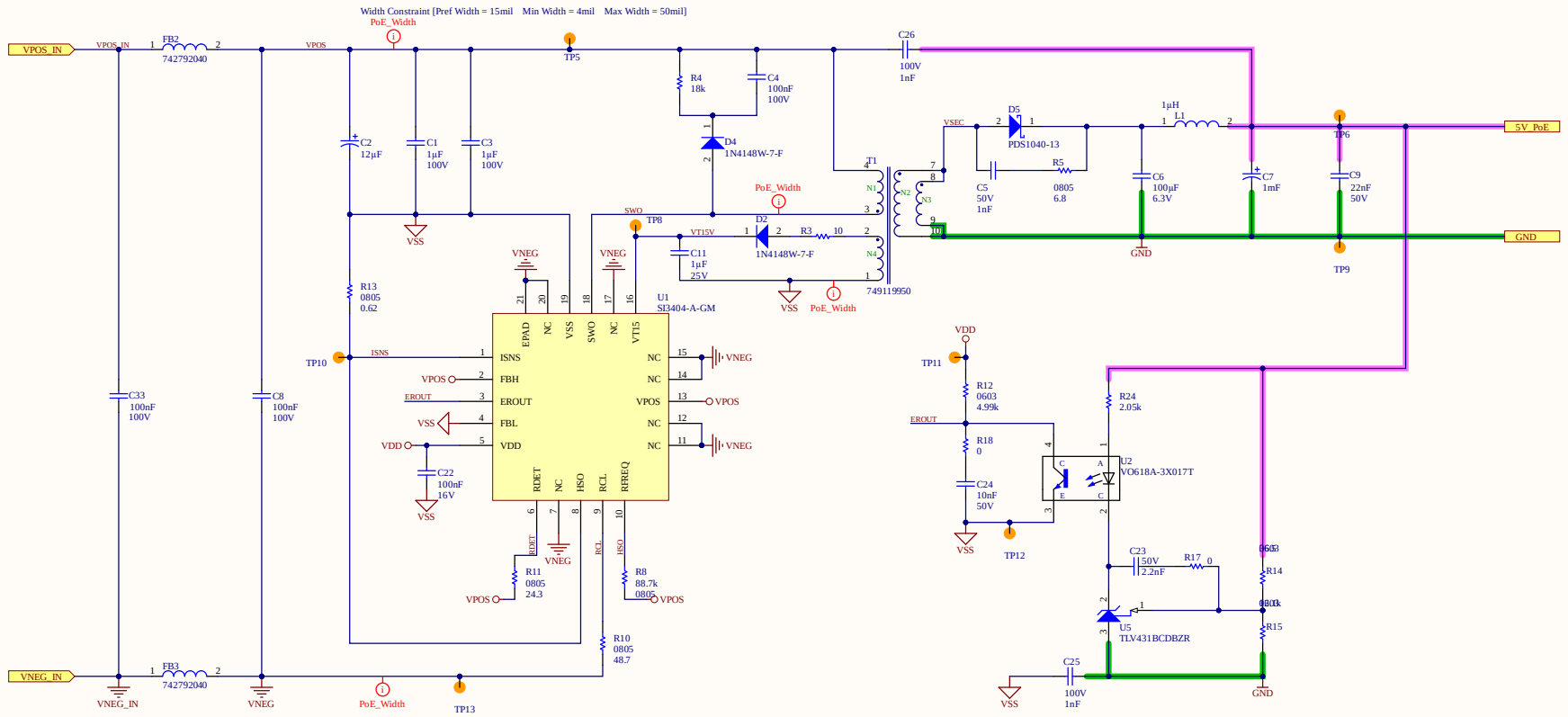

VNEG is a thermal plane as well as ESD and EMI. Use thermal vias to at least 1 inch square plane on backside.

Schematic based on the reference design for the SI3404 PoE.

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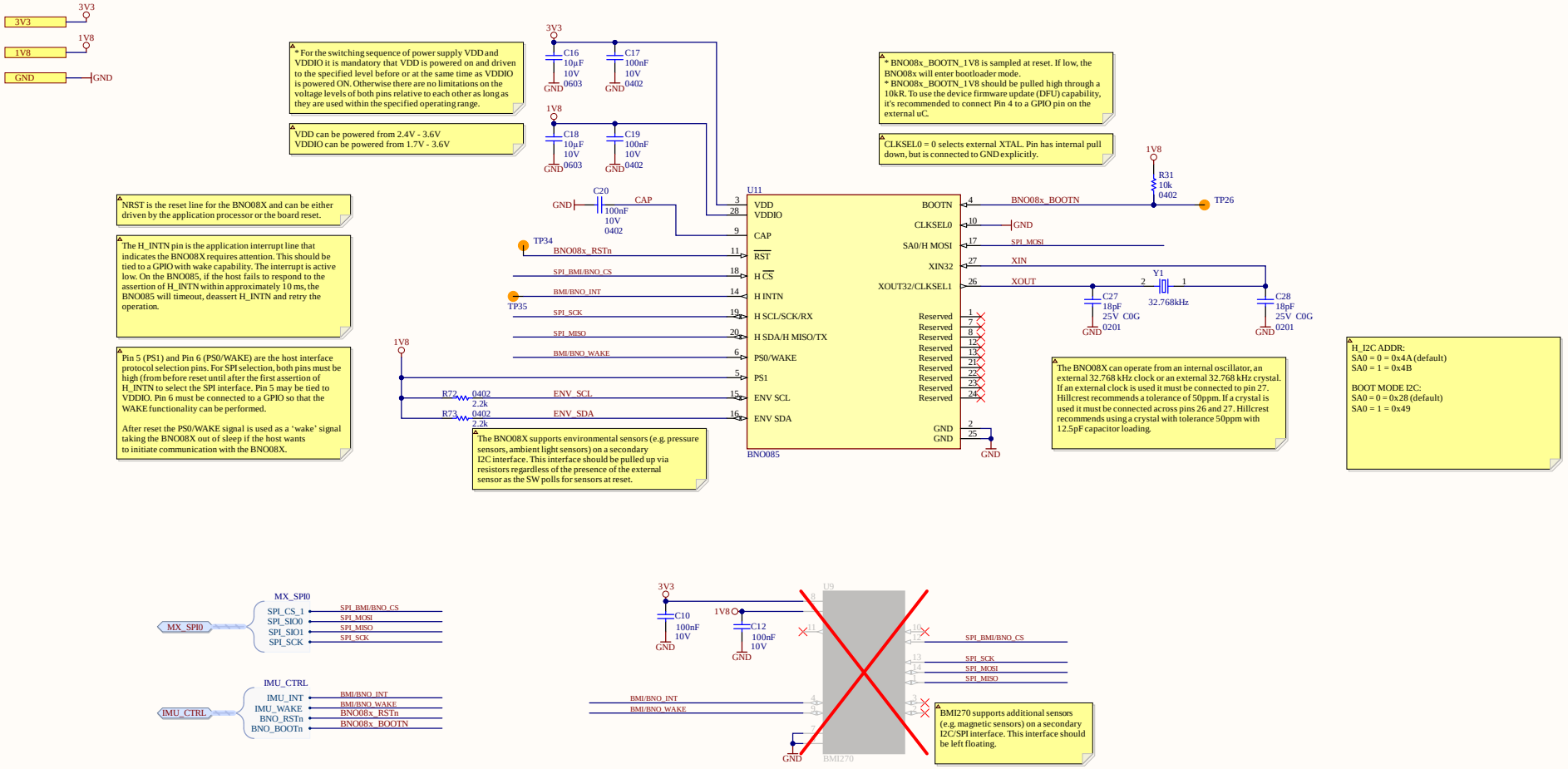

Sensor Orientation (gravity vector ↓)					upright	upsidedn
Output Signal X	0g / 0 LSB	1g / 8192 LSB	0g / 0 LSB	-1g / -8192 LSB	0g / 0 LSB	0g / 0 LSB
Output Signal Y	-1g / -8192 LSB	0g / 0 LSB	1g / 8192 LSB	0g / 0 LSB	0g / 0 LSB	0g / 0 LSB
Output Signal Z	0g / 0 LSB	0g / 0 LSB	0g / 0 LSB	0g / 0 LSB	1g / 8192 LSB	-1g / -8192 LSB

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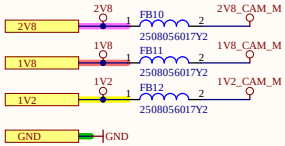
Place FBs and caps close to their associated camera connector.



Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.3	115mA
DOVDD	VIF	1.8V ± 0.1	13mA
DVDD	VDIG	1.2V ± 0.06	250mA

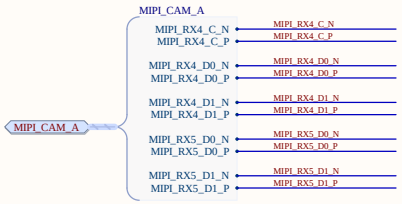
On the BW1097, the IMX378 camera module is hardwired into the "Cam-A" logical position. This means the logic which used to be required to support the module being plugged into different physical connectors (and different logical positions) is no longer needed and can be removed.

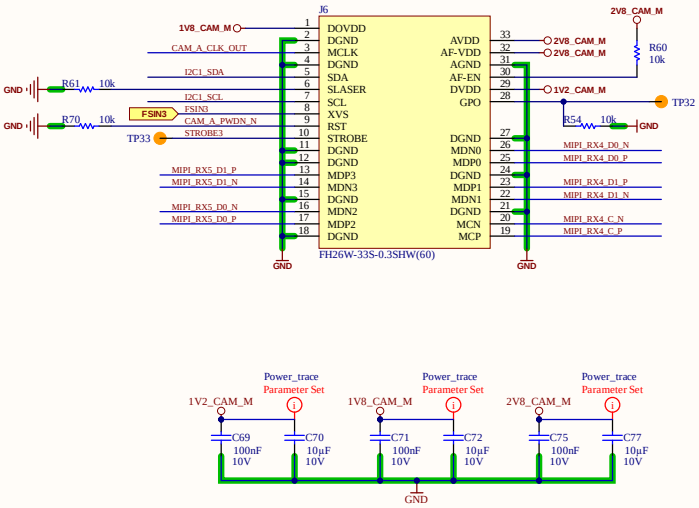
Note: It is still a limitation that the clock source for the cameras must be shared between CAMA/C and CAMB/D.

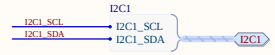
AR0234 MODULE CONNECTOR

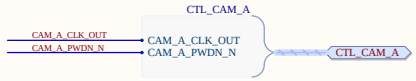
MODULE & SENSOR INFORMATION			
MODULE	TBD	I2C Clock Rate	400 kHz Max
SENSOR	AR0234CS 2.3 Mega pixel CMOS 1/2.6 inch	I2C Address (8 bits)	TBD (Sensor)
MAX RESOLUTION	1920x1200	Sensor Clock Input	6 - 54 MHz

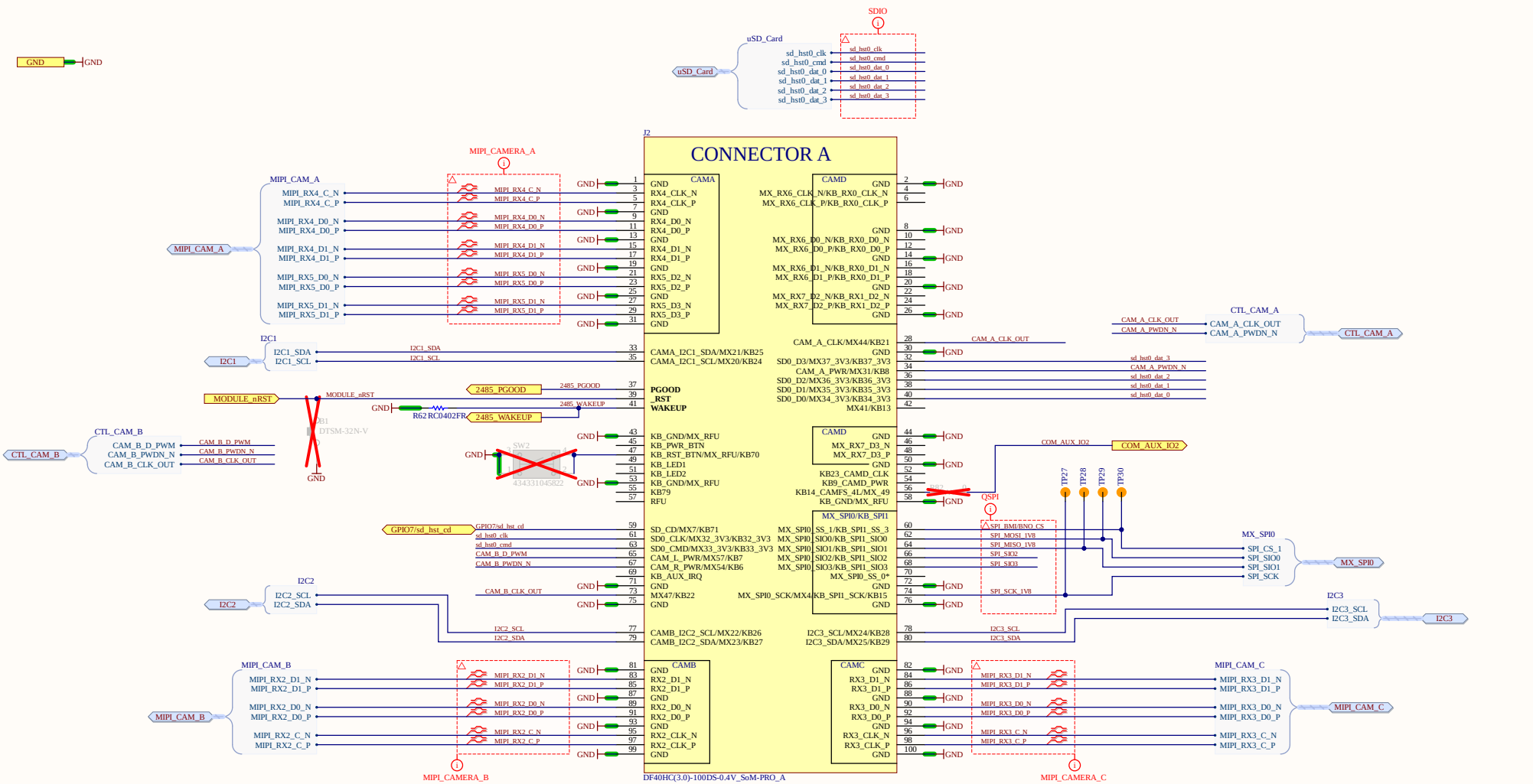
MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / lane










CONNECTOR A
J2
DF40HC(3.0)-100DS-0.4V_SoM-PRO_A
SDIO
uSD_Card
MIPI_CAMERA_A
MIPI_CAMERA_B
MIPI_CAMERA_C
MIPI_CAM_A
MIPI_CAM_B
MIPI_CAM_C
CTL_CAM_A
CTL_CAM_B
I2C1
I2C2
I2C3
QSPI
MX_SPI0
MODULE_nRST
2485_PGOOD
2485_WAKEUP
COM_AUX_IO2
GPIO7/sd_hst_cd
CAMA
CAMB
CAMC
CAMD
MX_SPI0/KB_SPI1
IMU SPI is length matched between connector and IMU. QSPI bus is length matched between connector and header pads.
Title BC2087
Size: Tabloid
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Drawn by: Boris Chou / Blaz Kvas
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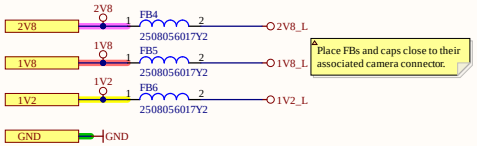

MODULE & SENSOR INFORMATION			
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Module	Sensor		
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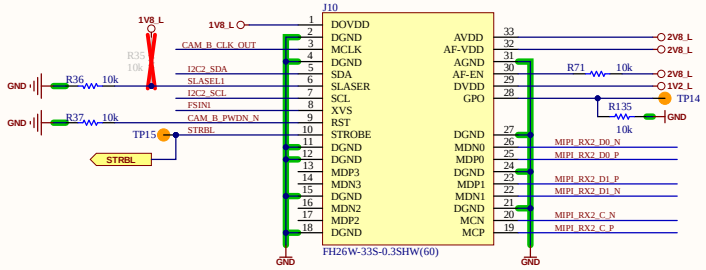
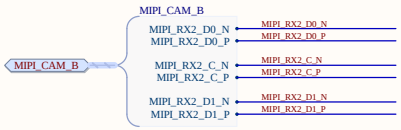
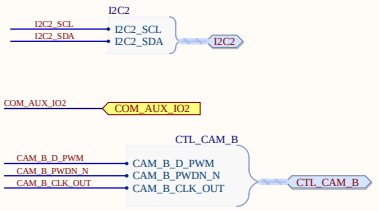
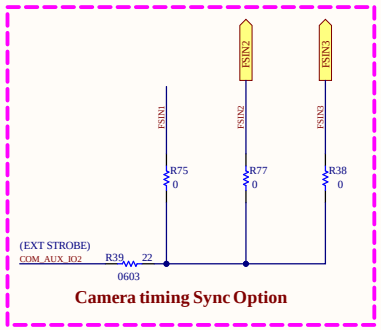
DOVDD	VIF	1.8V ± 0.1	13mA
DVDD	VDIG	1.2V ± 0.06	250mA

Mark "LEFT" on PCB
Place so that is the module's left camera.

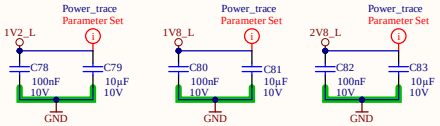








Need to check



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Size: Tabloid	Number: D2088000	Revision: R2M1E2	Cannot open file C:\Users\BrianLuxonis\
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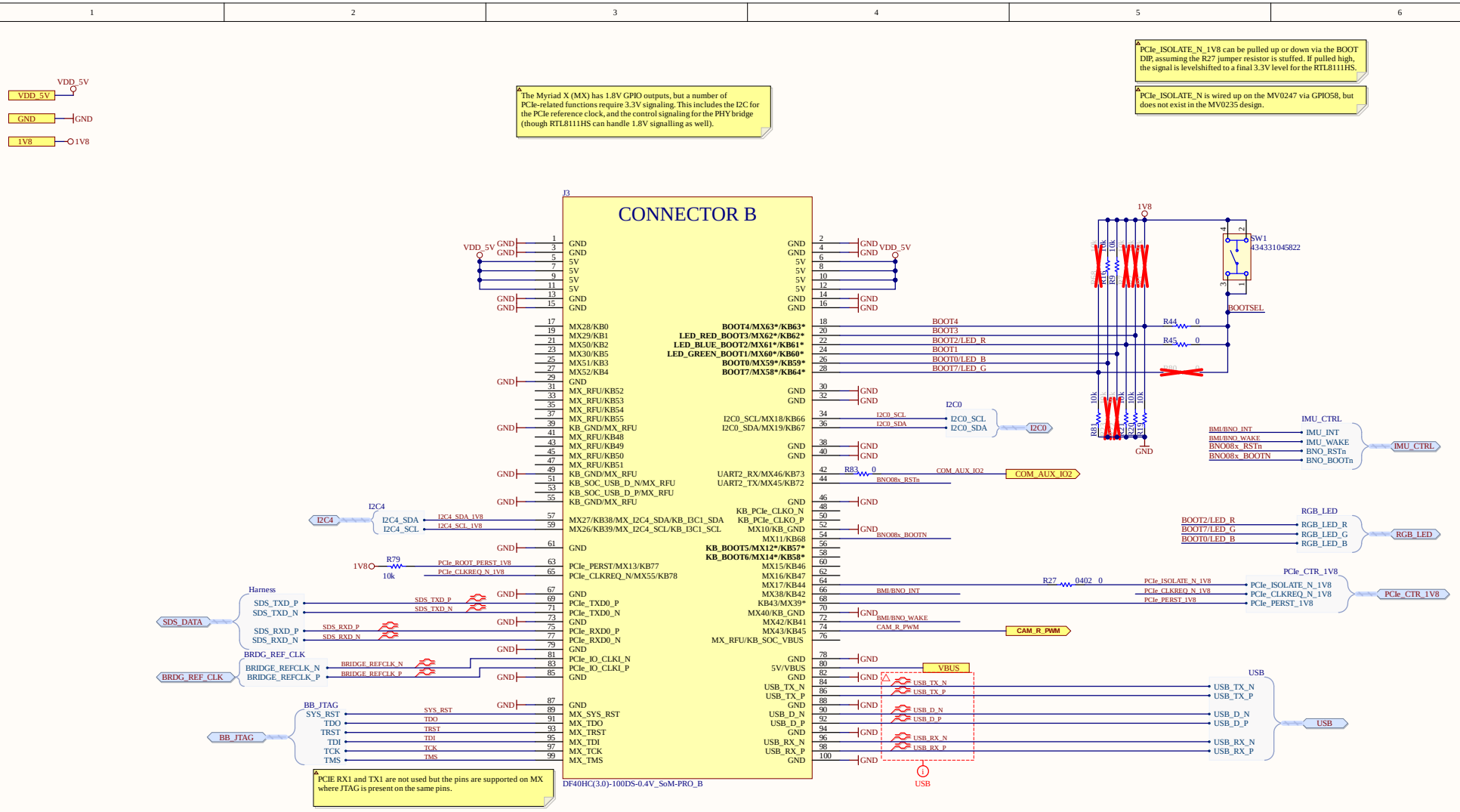
VDD_5V
GND
1V8
The Myriad X (MX) has 1.8V GPIO outputs, but a number of PCIe-related functions require 3.3V signaling. This includes the I2C for the PCIe reference clock, and the control signaling for the PHY bridge (though RTL8111HS can handle 1.8V signalling as well).
PCIe_ISOLATE_N_1V8 can be pulled up or down via the BOOT DIP, assuming the R27 jumper resistor is stuffed. If pulled high, the signal is levelshifted to a final 3.3V level for the RTL8111HS.
PCIe_ISOLATE_N is wired up on the MV0247 via GPIO58, but does not exist in the MV0235 design.
J3
CONNECTOR B
DF40HC(3.0)-100DS-0.4V_SoM-PRO_B
BOOT4/MX63*/KB63*
LED_RED_BOOT3/MX62*/KB62*
LED_BLUE_BOOT2/MX61*/KB61*
LED_GREEN_BOOT1/MX60*/KB60*
BOOT0/MX59*/KB59*
BOOT7/MX58*/KB64*
I2C0_SCL/MX18/KB66
I2C0_SDA/MX19/KB67
UART2_RX/MX46/KB73
UART2_TX/MX45/KB72
KB_PCIe_CLKO_P
KB_PCIe_CLKO_N
MX10/KB_GND
KB_BOOT5/MX12*/KB57*
KB_BOOT6/MX14*/KB58*
MX15/KB46
MX16/KB47
MX17/KB44
MX38/KB42
KB43/MX39*
MX40/KB_GND
MX42/KB41
MX43/KB45
MX_RFU/KB_SOC_VBUS
5V/VBUS
USB_TX_N
USB_TX_P
USB_D_N
USB_D_P
USB_RX_N
USB_RX_P
MX28/KB0
MX29/KB1
MX50/KB2
MX30/KB5
MX51/KB3
MX52/KB4
MX_RFU/KB52
MX_RFU/KB53
MX_RFU/KB54
MX_RFU/KB55
KB_GND/MX_RFU
MX_RFU/KB48
MX_RFU/KB49
MX_RFU/KB50
MX_RFU/KB51
KB_GND/MX_RFU
KB_SOC_USB_D_N/MX_RFU
KB_SOC_USB_D_P/MX_RFU
KB_GND/MX_RFU
MX27/KB38/MX_I2C4_SDA/KB_I3C1_SDA
MX26/KB39/MX_I2C4_SCL/KB_I3C1_SCL
PCIe_PERST/MX13/KB77
PCIe_CLKREQ_N/MX55/KB78
PCIe_TXD0_P
PCIe_TXD0_N
PCIe_RXD0_P
PCIe_RXD0_N
PCIe_IO_CLKI_N
PCIe_IO_CLKI_P
MX_SYS_RST
MX_TDO
MX_TRST
MX_TDI
MX_TCK
MX_TMS
PCIE RX1 and TX1 are not used but the pins are supported on MX where JTAG is present on the same pins.
SW1
434331045822
BOOTSEL
R44 0
R45 0
I2C0
I2C0_SCL
I2C0_SDA
IMU_CTRL
BMI/BNO_INT
BMI/BNO_WAKE
BNO08x_RSTn
BNO08x_BOOTn
R83 0
COM_AUX_IO2
RGB_LED
RGB_LED_R
RGB_LED_G
RGB_LED_B
R27 0402 0
PCIe_CTR_1V8
PCIe_ISOLATE_N_1V8
PCIe_CLKREQ_N_1V8
PCIe_PERST_1V8
CAM_R_PWM
R79 10k
PCIe_ROOT_PERST_1V8
Harness
SDS_DATA
SDS_TXD_P
SDS_TXD_N
SDS_RXD_P
SDS_RXD_N
BRDG_REF_CLK
BRIDGE_REFCLK_N
BRIDGE_REFCLK_P
BB_JTAG
SYS_RST
TDO
TRST
TDI
TCK
TMS
VBUS
USB
USB_TX_N
USB_TX_P
USB_D_N
USB_D_P
USB_RX_N
USB_RX_P
Title BC2087
Size: Tabloid
Number:D2088000
Revision:R2M1E2
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Sheet 6 of 12
Drawn by: Boris Chou / Blaz Kvas
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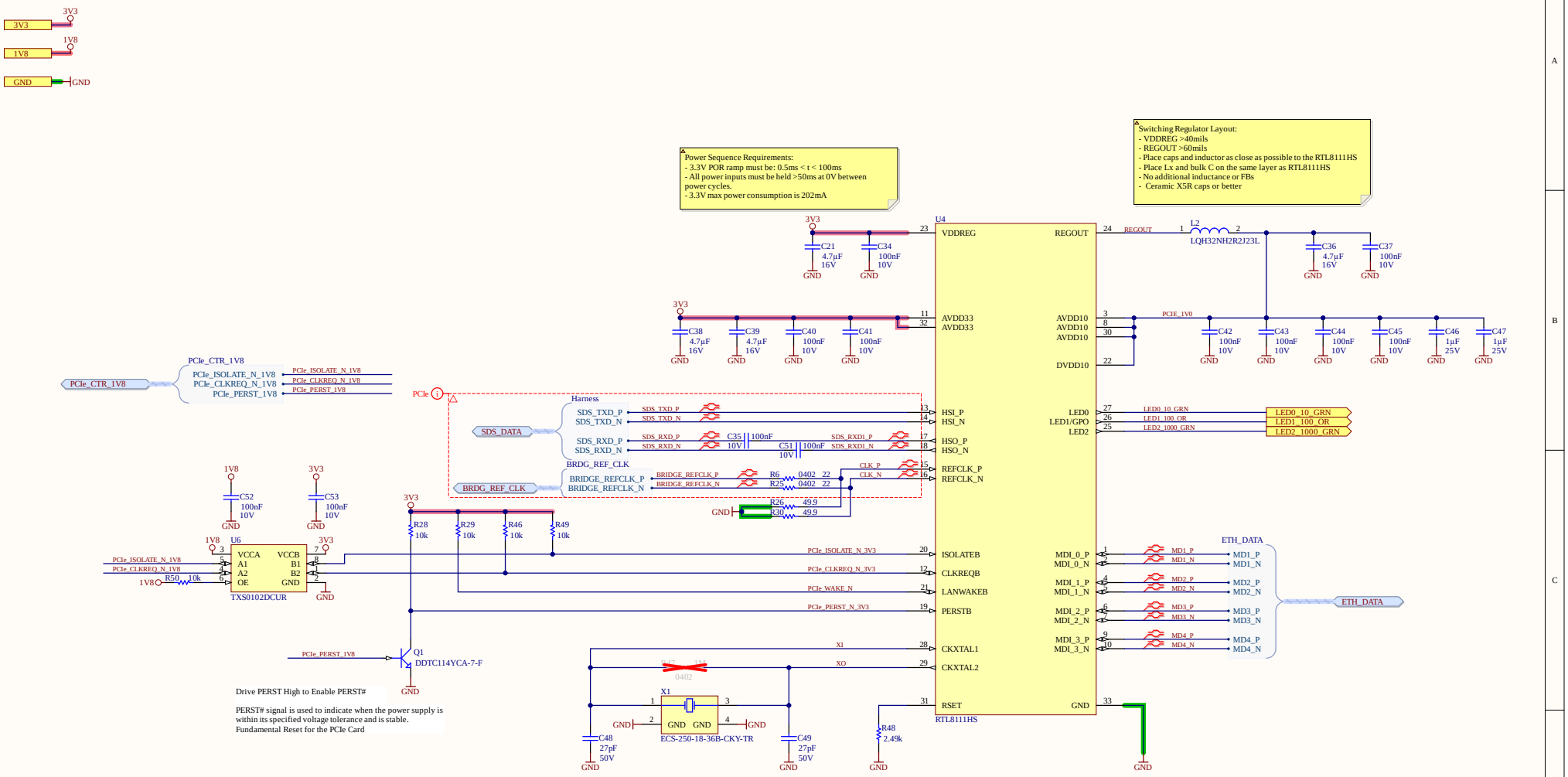
3V3
1V8
GND
Power Sequence Requirements:
- 3.3V POR ramp must be: 0.5ms < t < 100ms
- All power inputs must be held >50ms at 0V between power cycles.
- 3.3V max power consumption is 202mA
Switching Regulator Layout:
- VDDREG >40mils
- REGOUT >60mils
- Place caps and inductor as close as possible to the RTL8111HS
- Place Lx and bulk C on the same layer as RTL8111HS
- No additional inductance or FBs
- Ceramic X5R caps or better
U4
RTL8111HS
VDDREG
REGOUT
AVDD33
AVDD10
DVDD10
HSI_P
HSI_N
HSO_P
HSO_N
REFCLK_P
REFCLK_N
LED0
LED1/GPO
LED2
ISOLATEB
CLKREQB
LANWAKEB
PERSTB
CKXTAL1
CKXTAL2
RSET
MDI_0_P
MDI_0_N
MDI_1_P
MDI_1_N
MDI_2_P
MDI_2_N
MDI_3_P
MDI_3_N
L2
LQH32NH2R2J23L
PCIE_1V0
PCIe_CTR_1V8
PCIe_ISOLATE_N_1V8
PCIe_CLKREQ_N_1V8
PCIe_PERST_1V8
Harness
SDS_DATA
BRDG_REF_CLK
SDS_TXD_P
SDS_TXD_N
SDS_RXD_P
SDS_RXD_N
BRIDGE_REFCLK_P
BRIDGE_REFCLK_N
LED0_10_GRN
LED1_100_OR
LED2_1000_GRN
ETH_DATA
U6
TXS0102DCUR
Q1
DDTC114YCA-7-F
X1
ECS-250-18-36B-CKY-TR
Drive PERST High to Enable PERST#
PERST# signal is used to indicate when the power supply is within its specified voltage tolerance and is stable.
Fundamental Reset for the PCIe Card
Schematic based on the reference design from the MV0247 PoE AOB reference design, with checking against the Realtek RTL8111HS reference design, layout guide, and datasheet.
Title BC2087
Size: Tabloid
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Date: 26/04/2023
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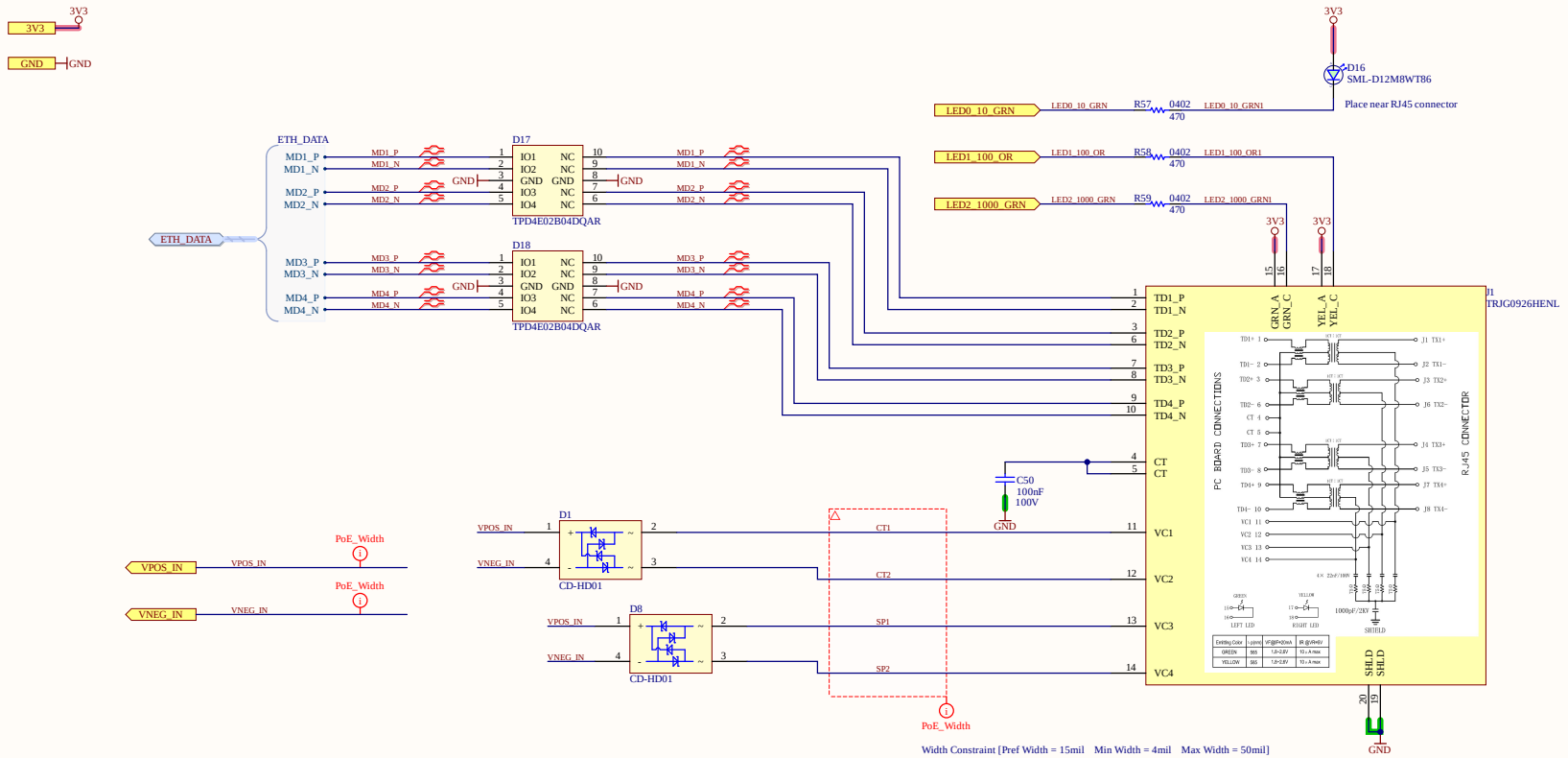

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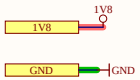

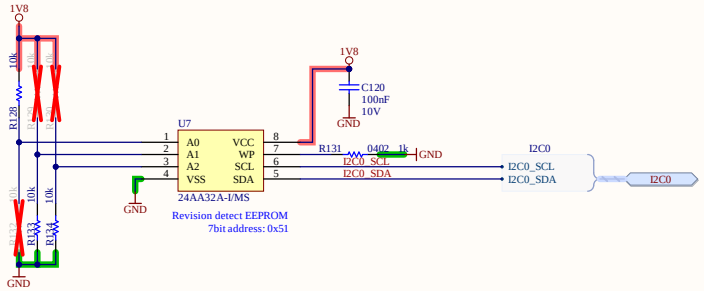

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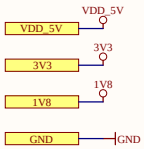
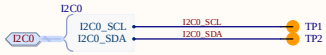
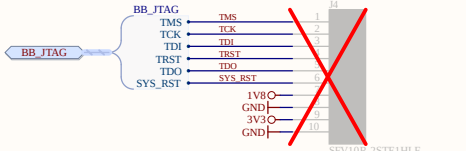
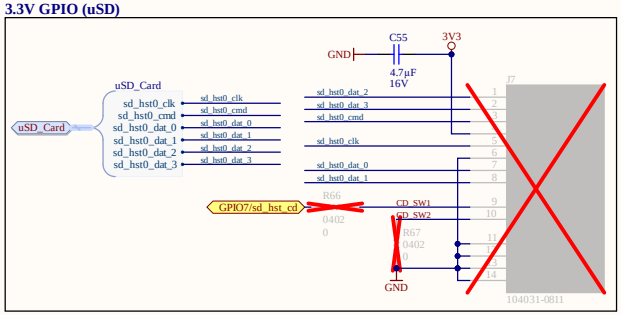




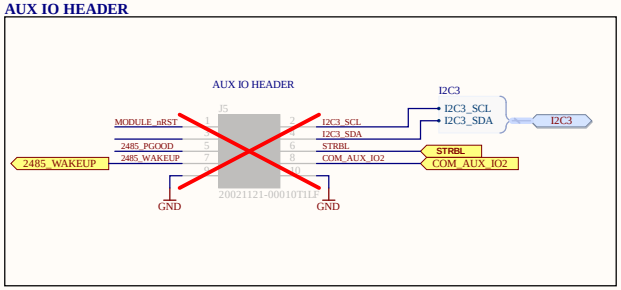
JTAG CONNECTOR



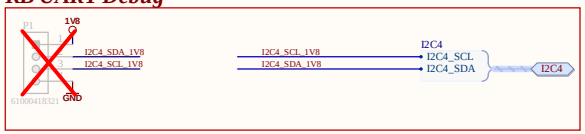
3.3V GPIO (uSD)



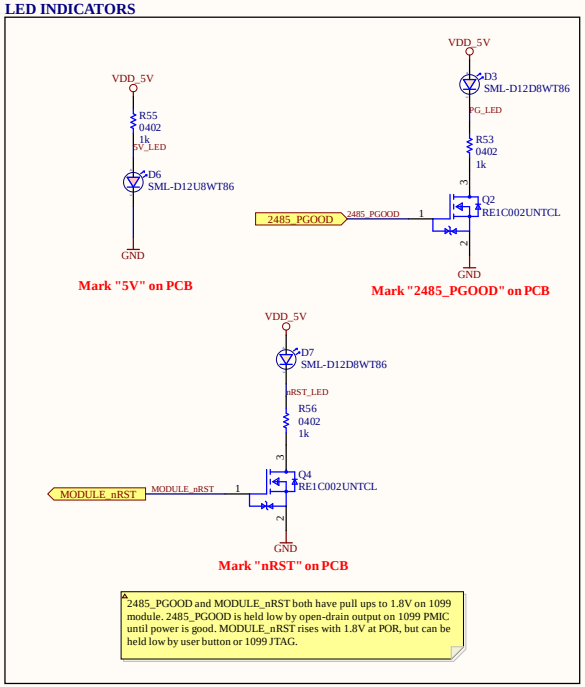
AUX IO HEADER

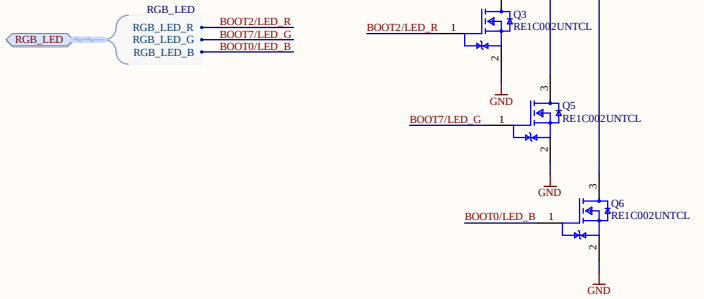


KB UART Debug



LED INDICATORS





Title **BC2087**			*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*
Size: Tabloid	Number: D2088000	Revision: R2M1E2	Cannot open file C:\Users\BrianLuxonis\
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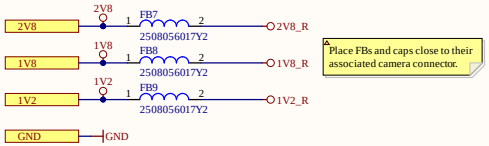
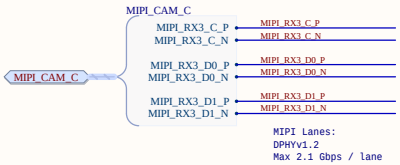
Drawn by: ***Boris Chou / Blaz Kvas***			

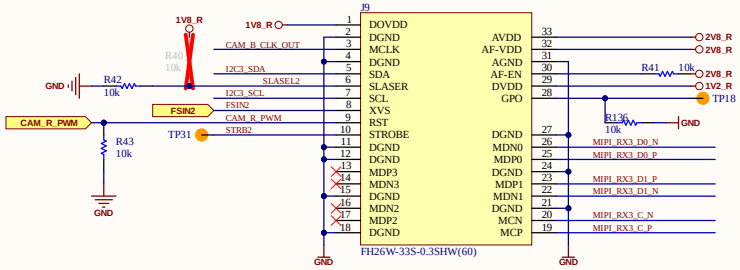


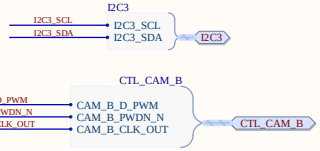
MODULE & SENSOR INFORMATION			
MODULE	TBD	I2C Clock Rate	400 kHz Max
SENSOR	AR0234CS 2.3 Mega pixel CMOS 1/2.6 inch	I2C Address (8 bits)	TBD (Sensor)
MAX RESOLUTION	1920x1200	Sensor Clock Input	6 - 54 MHz

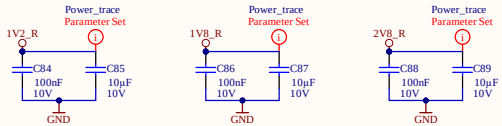
Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.3	115mA
DOVDD	VIF	1.8V ± 0.1	13mA
DVDD	VDIG	1.2V ± 0.06	250mA









Because the stereo pair of OV9282 modules hard wired to CAM_B (below) no additional reset cirucitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM. This also means that the signal CAM_AUX_IO1 is no longer required here, as that was only possible if the stereo pair were connected to CAM_C or CAM_D

OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to tl sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

CAMERA CONNECTOR RESET CONNECTION TABLE

CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM_1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM_2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

Title BC2087			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
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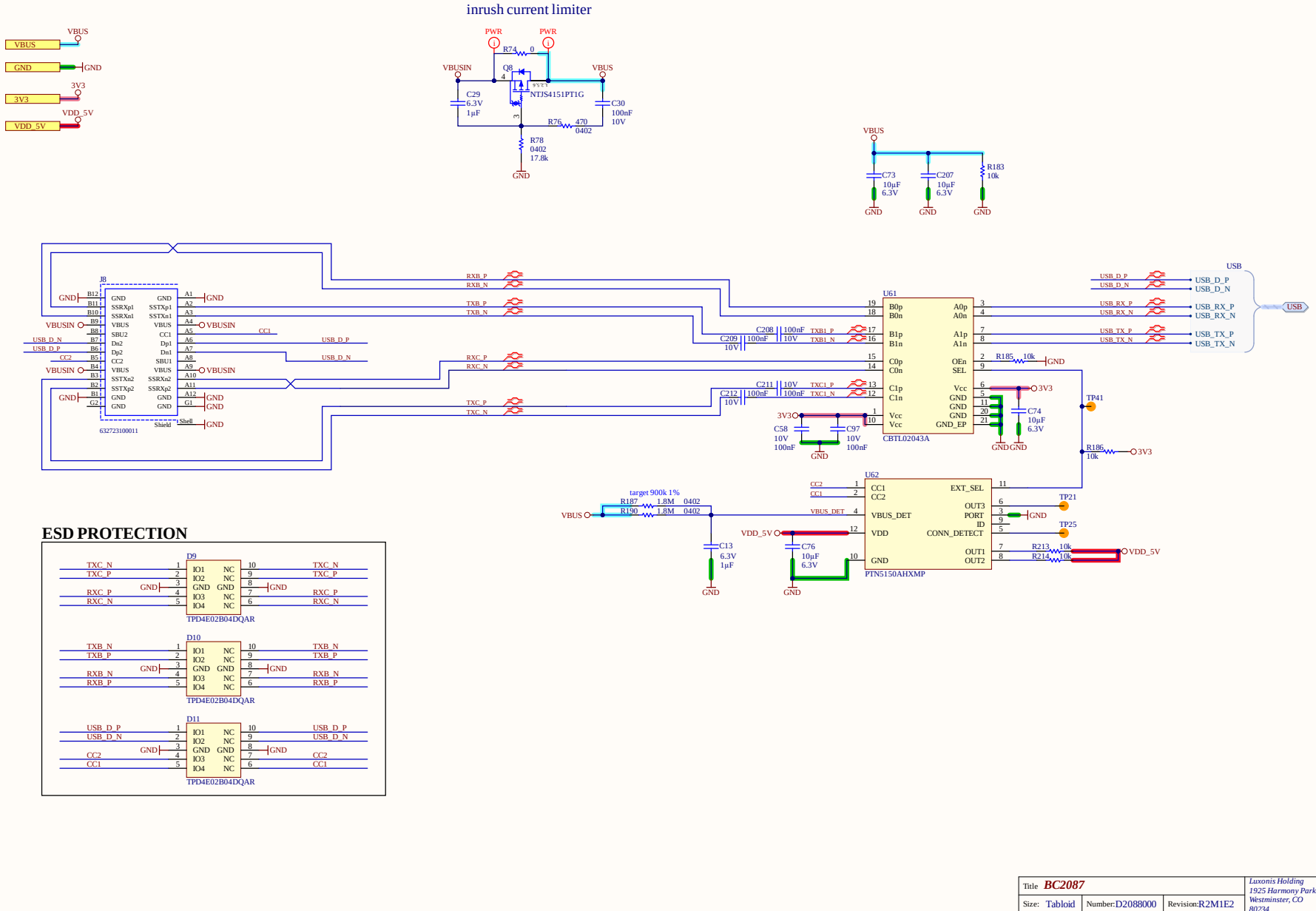

Title	BC2087		Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D2088000	Revision: R2M1E2	Cannot open file C:\Users\BrianLuxonis\
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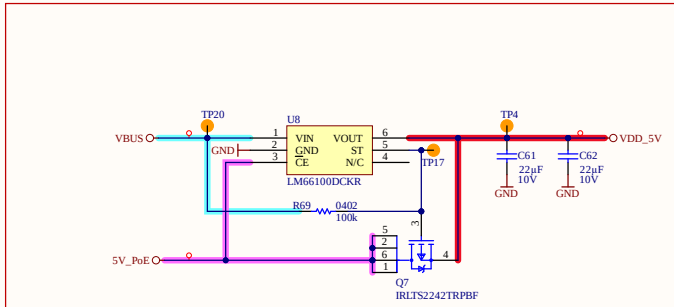
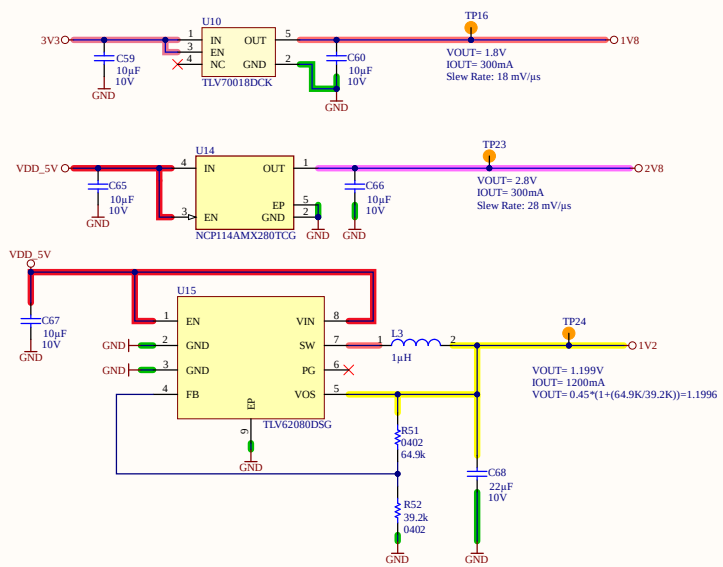
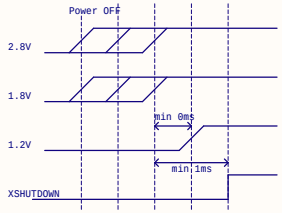
POWER INPUT



POWER SUPPLIES FOR CAMERA MODULES



AR0234 POWER REQUIREMENTS



Supply Information

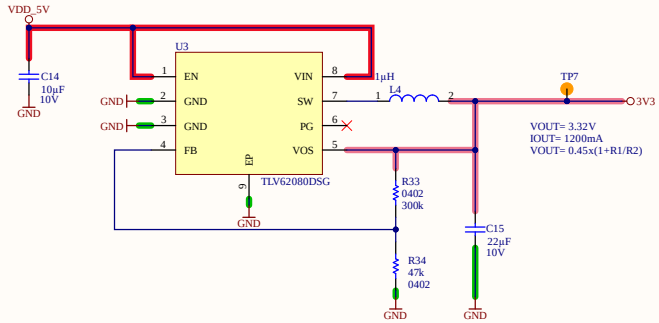
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

1. AVDD rising can occur before or after DOVDD rising as long as they are rising before XSHUTDOWN rising
2. XSHUTDOWN is pulled up after AVDD and DOVDD are stable
3. DVDD rises after DOVDD, but before XSHUTDOWN is pulled high

POWER SEQUENCING REQUIREMENTS:

The BW2099 module handles it's own power sequencing on-board. (TBC)

The camera modules have their own power sequencing requirements. The OV9282 have requirements for sequencing, and the IMX378 has a max slew rate requirement. See above.



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