Connector A

Dedicated pins		Alternate	Connected to	Main Function	Pin				Pin	Main Function	Connected to	Alternate		
	Power		PMK8550	PMK8550_PWM1	1				2	VCOIN_IN	PM8550			
	GND			GND	3				4	GND				
	Camera			GND	5				6	GND				
	System			GND	7				8	GND				
	SSC			3.8-5V	9				10	10				
	PCIE			3.8-5V	11				12	3.8-5V				
	USB			3.8-5V	13				14	3.8-5V				
	voltage level/protocol			3.8-5V	15				16	3.8-5V				
	Note			3.8-5V	17				18	3.8-5V				
	LL = Logic level			3.8-5V	19				20	3.8-5V				
	PU = pull up resistor			GND	21				22	GND				
	PS = Power Supply			GND	23				24	GND				
				GND	25				26	GND				
	QUP1_SE0_L1	GPIO_29	QCS8550	I2C/I3C_SCL	27	1V8 LL			1V8 LL	28	DEBUG_UART_TX	QCS8550	GPIO_26	QUP1_SE7_L2	UIM1_PRESENT
	QUP1_SE0_L0	GPIO_28	QCS8550	I2C/I3C_SDA	29	1V8 LL			1V8 LL	30	DEBUG_UART_RX	QCS8550	GPIO_27	QUP1_SE7_L3	UIM0_PRESENT
Connector PN: DF40C-100DP-0.4V(51)				GND	31				1V8 LL	32	PMK8550_PWM2				
Mates with: DF40HC(3.0)-100DS-0.4V			Sync Controller	EXT_STRB_CTR	33	1V8 LL			1V8 LL	34	FORCE_USB_BOOT	QCS8550	GPIO_43	QUP1_SE3_L3	
			Sync Controller	EXT_FSYNC	35	1V8 LL			Leave floating	36	PMIC_RB	QCS system			
				GND	37					38	GND				
			QCS8550	CSI5_LN0_P	39	MIPI D-PHY			Leave floating	40	KPD_PWR_N	PM8550			
			QCS8550	CSI5_LN0_N	41	MIPI D-PHY			1V8 JTAG interface	42	TDO	QCS8550			
				GND	43				1V8 JTAG interface	44	TRST	QCS8550			
			QCS8550	CSI5_LN1_P	45	MIPI D-PHY			1V8 JTAG interface	46	TDI	QCS8550			
			QCS8550	CSI5_LN1_N	47	MIPI D-PHY			1V8 JTAG interface	48	TCK	QCS8550			
				GND	49				1V8 JTAG interface	50	TMS	QCS8550			
			QCS8550	CSI5_CLK_P	51	MIPI D-PHY				52	GND				
			QCS8550	CSI5_CLK_N	53	MIPI D-PHY			Leave floating	54	KYPD_VOLN_N	PMK8550			
				GND	55				Leave floating	56	KYPD_VOLP_N	PMK8550			
			QCS8550	CSI5_LN2_P	57	MIPI D-PHY				58	GND				
			QCS8550	CSI5_LN2_N	59	MIPI D-PHY			1V8, SD 6.0 spec	60	SD_CARD_DET_N	QCS8550			
				GND	61				1V8, SD 6.0 spec	62	SDC2_CLK	QCS8550			
			QCS8550	CSI5_LN3_P	63	MIPI D-PHY			1V8, SD 6.0 spec	64	SDC2_CMD	QCS8550			
			QCS8550	CSI5_LN3_N	65	MIPI D-PHY			1V8, SD 6.0 spec	66	SDC2_DATA_1	QCS8550			
				GND	67				1V8, SD 6.0 spec	68	SDC2_DATA_1	QCS8550			
				GND	69				1V8, SD 6.0 spec	70	SDC2_DATA_2	QCS8550			
			QCS8550	DSI0_LN0_P	71	MIPI D-PHY			1V8, SD 6.0 spec	72	SDC2_DATA_3	QCS8550			
			QCS8550	DSI0_LN0_N	73	MIPI D-PHY				74	GND				
				GND	75				1V8 LL, L15B PS PU	76	SSC_I3C0_SCL	QCS8550	GPIO_189	SSC_QUP_SE0_L1	
			QCS8550	DSI0_LN1_P	77	MIPI D-PHY			1V8 LL, L15B PS PU	78	SSC_I3C0_SDA	QCS8550	GPIO_188	SSC_QUP_SE0_L0	
			QCS8550	DSI0_LN1_N	79	MIPI D-PHY			1V8 LL	80	SSC_UART_TX	QCS8550	GPIO_202	SSC_QUP_SE5_L2	
				GND	81				1V8 LL	82	SSC_UART_RX	QCS8550	GPIO_203	SSC_QUP_SE5_L3	
			QCS8550	DSI0_CLK_P	83	MIPI D-PHY			1V8 LL, L15B PS	84	SSC_IMU_SPI_MISO	QCS8550	GPIO_192	SSC_QUP_SE2_L0	
			QCS8550	DSI0_CLK_N	85	MIPI D-PHY			1V8 LL, L15B PS	86	SSC_IMU_SPI_MOSI	QCS8550	GPIO_193	SSC_QUP_SE2_L1	
				GND	87				1V8 LL, L15B PS	88	SSC_IMU_SPI_CLK	QCS8550	GPIO_194	SSC_QUP_SE2_L2	
			QCS8550	DSI0_LN2_P	89	MIPI D-PHY			1V8 LL, L15B PS	90	SSC_IMU_SPI_CS_N	QCS8550	GPIO_195	SSC_QUP_SE2_L3	
			QCS8550	DSI0_LN2_N	91	MIPI D-PHY			1V8 LL	92	AON_CAM_STANDBY_0	QCS8550	GPIO_206	SSC_QUP_SE7_L0	
				GND	93				1V8 LL	94	AON_CAM_STANDBY_1	QCS8550	GPIO_207	SSC_QUP_SE7_L1	
			QCS8550	DSI0_LN3_P	95	MIPI D-PHY				96	GND				
			QCS8550	DSI0_LN3_N	97	MIPI D-PHY			1V8 LL, L15B PS PU	98	CCI_I2C5_SCL	QCS8550	GPIO_1	QUP2_SE0_L1_MIRB	IBI_I3C_QUP2_SE0_SCL_MIRB
				GND	99				1V8 LL, L15B PS PU	100	CCI_I2C5_SDA	QCS8550	GPIO_0	QUP2_SE0_L0_MIRB	IBI_I3C_QUP2_SE0_SDA_MIRB

	QUP/I2CHUB/SSC Lane to function mapping								
	L0	L1	L2	L3	L4	L5			L6
(HS)-UART	CTS	RFR	TX	RX	–	–			–
I2C/I3C	SDA	SCL	–	–	–	–			–
SPI	MISO	MOS	SCLK	CS_0	CS_1	CS_2			CS_3

Connector B

Dedicated pins				Alternate	Connected to	Main Function	Pin			Pin	Main Function	Connected to	Alternate		
			Power		PM8850	LED_RGB_RED	1	Current source		2	GND				
			GND		PM8850	LED_RGB_GREEN	3	Current source	USB 3.0	4	USB0_SS_TX0_P	QCS8550			
			Camera		PM8850	LED_RGB_BLUE	5	Current source	USB 3.0	6	USB0_SS_TX0_N	QCS8550			
			System			GND	7			8	GND				
			SSC		QCS8550	PCIE1_QCS_RX0_P	9	PCIe GEN 4	USB 2.0	10	USB0_HS_D_P	QCS8550			
			PCIE		QCS8550	PCIE1_QCS_RX0_N	11	PCIe GEN 4	USB 2.0	12	USB0_HS_D_N	QCS8550			
			USB			GND	13			14	GND				
			PWM		QCS8550	PCIE1_QCS_RX1_P	15	PCIe GEN 4	USB 3.0	16	USB0_SS_RX0_P	QCS8550			
			voltage level/protocol		QCS8550	PCIE1_QCS_RX1_N	17	PCIe GEN 4	USB 3.0	18	USB0_SS_RX0_N	QCS8550			
			Note			GND	19			20	GND				
			LL = Logic level		QCS8550	PCIE1_QCS_REFCLK_P	21	PCIe GEN 4	USB 2.0	22	USB0_DP_AUX_P	QCS8550			
			PU = pull up resistor		QCS8550	PCIE1_QCS_REFCLK_N	23	PCIe GEN 4	USB 2.0	24	USB0_DP_AUX_N	QCS8550			
			PS = Power Supply			GND	25			26	GND				
			Connector PN: DF40C-100DP-0.4V(51)		QCS8550	PCIE1_QCS_TX0_N	27	PCIe GEN 4	1V8 LL, L15B PS PU	28	QUP1_SE1_L0	QCS8550	GPIO_32	SPI1_SE1_MISO	IBI_I3C_QUP1_SE1_SDA
			Mates with: DF40HC(3.0)-100DS-0.4V		QCS8550	PCIE1_QCS_TX0_P	29	PCIe GEN 4	1V8 LL, L15B PS PU	30	QUP1_SE1_L1	QCS8550	GPIO_33	SPI1_SE1_MOSI	IBI_I3C_QUP1_SE1_SCL
						GND	31		1V8 LL, L15B PS	32	QUP1_SE1_L2	QCS8550	GPIO_34	SPI1_SE1_SCLK	
					QCS8550	PCIE1_QCS_TX1_N	33	PCIe GEN 4	1V8 LL, L15B PS	34	QUP1_SE1_L3	QCS8550	GPIO_35	SPI1_SE1_CS	
					QCS8550	PCIE1_QCS_TX1_P	35	PCIe GEN 4		36	GND				
						GND	37		1V8, 1V8_STM	38	CSI4_STRB	Sync Controller			
	GP_MN	GRFC5_MIRB	QUP1_SE5_L1	GPIO_53	QCS8550	I2C1_SCL	39	1V8 LL	1V8, 1V8_STM	40	CSI2_3_STRB	Sync Controller			
		GRFC4_MIRB	QUP1_SE5_L0	GPIO_52	QCS8550	I2C1_SDA	41	1V8 LL	1V8, 1V8_STM	42	CSI0_1_STRB	Sync Controller			
						GND	43		1V8 LL	44	HIFI_DAC_I2S_MCLK	QCS8550			
	LPASS_1	SWR_TX_DATA0	LPI_I2S0_WS	GPIO_166	QCS8550	HIFI_DAC_I2S_WS / LPI_I2S0_WS	45	1V8 LL	1V8 LL	46	PoE_T2P	POE controller			
	LPASS_3	SWR_RX_CLK	LPI_I2S0_DATA1	GPIO_168	QCS8550	HIFI_DAC_I2S_DATA1 / LPI_I2S0_DATA1	47	1V8 LL	1V8, 1V8_STM	48	IR_LED_FAULT	Sync Controller			
	LPASS_2	SWR_TX_DATA1	LPI_I2S0_DATA0	GPIO_167	QCS8550	HIFI_DAC_I2S_DATA2 / LPI_I2S0_DATA0	49	1V8 LL	1V8, 1V8_STM	50	IR_EN/PWM	Sync Controller			
	LPASS_0	SWR_TX_CLK	LPI_I2S0_SCK	GPIO_165	QCS8550	HIFI_DAC_I2S_SCK / LPI_I2S0_SCK	51	1V8 LL	1V8, 1V8_STM	52	IR_ADIM/HD	Sync Controller			
	LPASS_4	SWR_RX_DATA0	LPI_I2S0_DATA2	GPIO_169	QCS8550	I2S1_DATA0 / LPI_I2S0_DATA2	53	1V8 LL	1V8 LL	54	I2S1_SCK	QCS8550	GPIO_121		
SWR_RX_DATA1	LPASS_5	EXT_MCLK1_C	LPI_I2S0_DATA3	GPIO_170	QCS8550	I2S1_DATA1 / LPI_I2S0_DATA3	55	1V8 LL	1V8 LL	56	I2S1_WS	QCS8550	GPIO_123		
						GND	57			58	GND				
					QCS8550	PCIE0_QCS_TX0_N	59	PCIe GEN 3	MIPI D-PHY	60	CSI1_LN1_P	QCS8550			
					QCS8550	PCIE0_QCS_TX0_P	61	PCIe GEN 3	MIPI D-PHY	62	CSI1_LN1_N	QCS8550			
						GND	63			64	GND				
					QCS8550	PCIE0_QCS_TX1_N	65	PCIe GEN 3	MIPI D-PHY	66	CSI1_LN0_P	QCS8550			
					QCS8550	PCIE0_QCS_TX1_P	67	PCIe GEN 3	MIPI D-PHY	68	CSI1_LN0_N	QCS8550			
						GND	69			70	GND				
					QCS8550	PCIE0_QCS_REFCLK_N	71	PCIe GEN 3	MIPI D-PHY	72	CSI1_CLK_P	QCS8550			
					QCS8550	PCIE0_QCS_REFCLK_P	73	PCIe GEN 3	MIPI D-PHY	74	CSI1_CLK_N	QCS8550			
						GND	75			76	GND				
					QCS8550	PCIE0_QCS_RX0_N	77	PCIe GEN 3	1V8 LL	78	IMU1_LSM_INT	QCS8550	GPIO_84		I2CHUB0_SE9_L0
					QCS8550	PCIE0_QCS_RX0_P	79	PCIe GEN 3	1V8 LL	80	IMU2_LSM_INT	QCS8550	GPIO_85		I2CHUB0_SE9_L1
						GND	81			82	GND				
					QCS8550	PCIE0_QCS_RX1_N	83	PCIe GEN 3	MIPI D-PHY	84	CSI0_CLK_P	QCS8550			
					QCS8550	PCIE0_QCS_RX1_P	85	PCIe GEN 3	MIPI D-PHY	86	CSI0_CLK_N	QCS8550			
						GND	87			88	GND				
					QCS8550	PCIE0_WAKE_N	89	PCIe GEN 3, 1V8 LL	MIPI D-PHY	90	CSI0_LN1_P	QCS8550			
					QCS8550	PCIE0_CLK_REQ_N	91	PCIe GEN 3, 1V8 LL	MIPI D-PHY	92	CSI0_LN1_N	QCS8550			
					QCS8550	PCIE0_RESET_N	93	PCIe GEN 3, 1V8 LL		94	GND				
					QCS8550	CCI_I2C0_SCL	95	1V8 LL, L15B PS PU	MIPI D-PHY	96	CSI0_LN0_P	QCS8550			
					QCS8550	CCI_I2C0_SDA	97	1V8 LL, L15B PS PU	MIPI D-PHY	98	CSI0_LN0_N	QCS8550			
						GND	99			100	GND				

	QUP/I2CHUB/SSC Lane to function mapping							
	L0	L1	L2	L3	L4		L5	L6
(HS)-UART	CTS	RFR	TX	RX	–		–	–
I2C/I3C	SDA	SCL	–	–	–		–	–
SPI	MISO	MOS	SCLK	CS_0	CS_1		CS_2	CS_3

Connector C

Dedicated pins	
	Power
	GND
	Camera
	System
	SSC
	PCIE
	USB
	PWM
	voltage level/protocol
	LL = Logic level
	PU = pull up resistor
	PS = Power Supply

Connector PN: DF40C-100DP-0.4V(51)

Mates with: DF40HC(3.0)-100DS-0.4V

Alternate	Connected to	Main Function	Pin				Pin	Main Function	Connected to	Alternate		
		GND	1				2	GND				
	PM8550	FLASH_LED_1_4	3	Current source			4	PG_3V3				
	PM8550	FLASH_LED_1_4	5	Current source			6	PG_1V8				
	PM8550	FLASH_LED_1_4	7	Current source			8	GND				
	PM8550	FLASH_LED_1_4	9	Current source		1V8 LL	10	SSC_I2C1_SDA	QCS8550	GPIO_190	SSC_2	SSC_QUP_SE1_L0
	PM8550	FLASH_LED_1_4	11	Current source		1V8 LL	12	SSC_12C1_SCL	QCS8550	GPIO_191	SSC_3	SSC_QUP_SE1_L1
	PM8550	FLASH_LED_1_4	13	Current source		1V8, 1V8_STM	14	VCSEL_EN/PWM	Sync Controller			
		GND	15			1V8, 1V8_STM	16	VCSEL_ADIM/HD	Sync Controller			
		GND	17			1V8, 1V8_STM	18	DOT_FAULT	Sync Controller			
		GND	19				20	GND				
	PM8550	REAR_TOF_THERM	21			MIPI D-PHY	22	CSI3_RESET_N	QCS8550			
	PM8550	CAM_FLASH_THERM	23			MIPI D-PHY	24	CSI2_RESET_N	QCS8550			
		GND	25			MIPI D-PHY	26	CSI4_AON_RESET_N	QCS8550			
	QCS8550	CSI4_LN0_P	27	MIPI D-PHY		MIPI D-PHY	28	CSI0_RESET_N	QCS8550			
	QCS8550	CSI4_LN0_N	29	MIPI D-PHY		MIPI D-PHY	30	CSI1_RESET_N	QCS8550			
		GND	31			MIPI D-PHY	32	CSI5_RESET_N	QCS8550			
	QCS8550	CSI4_LN1_P	33	MIPI D-PHY			34	GND				
	QCS8550	CSI4_LN1_N	35	MIPI D-PHY		MIPI D-PHY	36	CSI0_MCLK	QCS8550			
		GND	37			MIPI D-PHY	38	CSI4_AON_MCLK	QCS8550			
	QCS8550	CSI4_CLK_P	39	MIPI D-PHY		MIPI D-PHY	40	CSI1_MCLK	QCS8550			
	QCS8550	CSI4_CLK_N	41	MIPI D-PHY		MIPI D-PHY	42	CSI2_MCLK	QCS8550			
		GND	43			MIPI D-PHY	44	CSI3_MCLK	QCS8550			
	QCS8550	CSI4_LN2_P	45	MIPI D-PHY			46	GND				
	QCS8550	CSI4_LN2_N	47	MIPI D-PHY		1V8, 1V8_STM	48	CSI4_FS	Sync Controller			
		GND	49			1V8, 1V8_STM	50	CSI2_3_FS	Sync Controller			
	QCS8550	CSI4_LN3_P	51	MIPI D-PHY		1V8, 1V8_STM	52	CSI0_1_FS	Sync Controller			
	QCS8550	CSI4_LN3_N	53	MIPI D-PHY		PCIe GEN 4, 1V8 LL	54	PCIE1_WAKE_N	QCS8550			
		GND	55				56	GND				
	QCS8550	CCI_AON_I2C_SCL	57	1V8 LL, L15B PS PU		1V8, SD 6.0 spec	58	SDC4_SIO0_QSPI_SIO0	QCS8550	GPIO_89	QSPI_DATA[0]	
	QCS8550	CCI_AON_I2C_SDA	59	1V8 LL, L15B PS PU		1V8, SD 6.0 spec	60	SDC4_SIO1_QSPI_SIO1	QCS8550	GPIO_90	USB1_HS_AC_EN	
		GND	61			1V8, SD 6.0 spec	62	SDC4_SIO2_QSPI_SIO2	QCS8550	GPIO_48	USB_PHY_PS_MIRA	QUP1_SE6_L0
		GND	63			1V8, SD 6.0 spec	64	SDC4_SIO3_QSPI_SIO3	QCS8550	GPIO_49	QUP1_SE6_L1	
	QCS8550	CSI2_LN0_P	65	MIPI D-PHY		1V8, SD 6.0 spec	66	QSPI_CS_0	QCS8550	GPIO_91	QSPI_CS_N_0	
	QCS8550	CSI2_LN0_N	67	MIPI D-PHY		1V8, SD 6.0 spec	68	SDC4_CLK_QSPI_CLK	QCS8550	GPIO_50	QUP1_SE6_L2	
		GND	69			1V8, SD 6.0 spec	70	SDC4_CMD_QSPI_CS_1	QCS8550	GPIO_51	QUP1_SE6_L3	
	QCS8550	CSI2_LN1_P	71	MIPI D-PHY			72	GND				
	QCS8550	CSI2_LN1_N	73	MIPI D-PHY		PCIe GEN 4, 1V8 LL	74	PCIE1_RESET_N	QCS8550			
		GND	75			PCIe GEN 4, 1V8 LL	76	PCIE1_CLK_REQ_N	QCS8550			
	QCS8550	CSI2_CLK_P	77	MIPI D-PHY			78	GND				
	QCS8550	CSI2_CLK_N	79	MIPI D-PHY		1V8 LL	80	QUP2_SE6_L3	QCS8550	GPIO_79	SPI2_SE6_CS	QDSS_CTI_TRIG1_IN_MIRB
		GND	81			1V8 LL	82	QUP2_SE6_L2	QCS8550	GPIO_78	SPI2_SE6_SCLK	
	QCS8550	CSI3_CLK_P	83	MIPI D-PHY		1V8 LL	84	QUP2_SE6_L0	QCS8550	GPIO_76	SPI2_SE6_MISO	
	QCS8550	CSI3_CLK_N	85	MIPI D-PHY		1V8 LL	86	QUP2_SE6_L1	QCS8550	GPIO_77	SPI2_SE6_MOSI	
		GND	87				88	GND				
	QCS8550	CSI3_LN0_P	89	MIPI D-PHY		1V8 LL, L15B PS PU	90	I2C2_SDA	QCS8550	GPIO_20	GP_PDM_MIRB[2]	
	QCS8550	CSI3_LN0_N	91	MIPI D-PHY		1V8 LL, L15B PS PU	92	I2C2_SCL	QCS8550	GPIO_21	GP_PDM_MIRB[1]	
		GND	93				94	GND				
	QCS8550	CSI3_LN1_P	95	MIPI D-PHY		1V8 LL	96	CCI_I2C2_SCL	QCS8550			
	QCS8550	CSI3_LN1_N	97	MIPI D-PHY		1V8 LL	98	CCI_I2C2_SDA	QCS8550			
		GND	99				100	GND				

	QUP/I2CHUB/SSC Lane to function mapping									
	L0	L1	L2		L3		L4		L5	L6
(HS)-UART	CTS	RFR	TX		RX		–		–	–
I2C/I3C	SDA	SCL	–		–		–		–	–
SPI	MISO	MOSI	SCLK		CS_0		CS_1		CS_2	CS_3