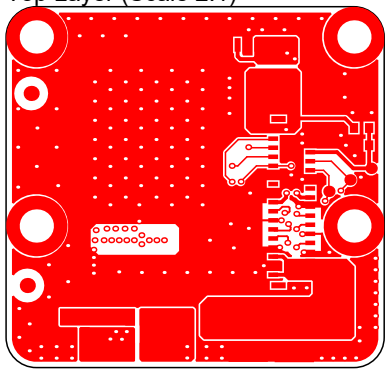
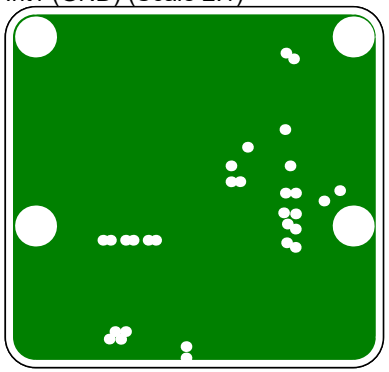
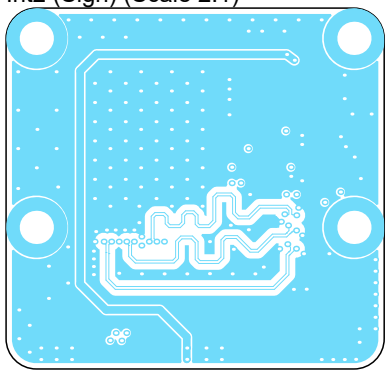
Top Layer (Scale 2:1)



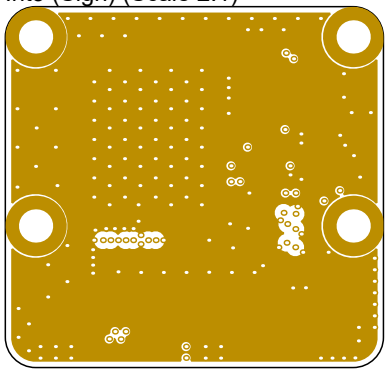
Int1 (GND) (Scale 2:1)



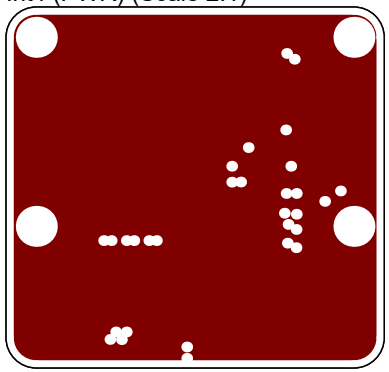
Int2 (Sign) (Scale 2:1)



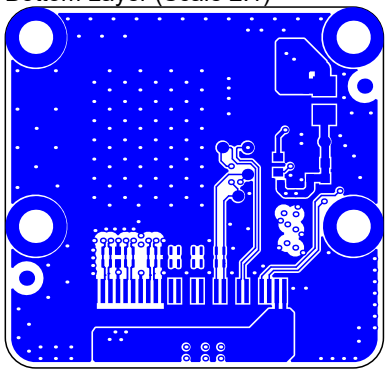
Int3 (Sign) (Scale 2:1)



Int4 (PWR) (Scale 2:1)



Bottom Layer (Scale 2:1)



FABRICATION NOTES:

Fabricate per IPC-6011 & IPC-6012 CLASS 2
Inspect per IPC-A-600 CLASS 2
Test per IPC-TM-650

*** PCB has 6 copper layers**
*** Copper thicknesses are finished and include base foil plus Cu plating on plated layers.**
*** PCB thickness: 63mil +/- 3mil**
*** Min. trace width/clearance: 0.1mm/0.1mm**
*** Min. hole drill/ring: 8mil/16mil**
*** Soldermask gang relief is allowed for pads in same footprint, if footprint is NSMD.**
*** Silkscreen, non-conductive epoxy ink, color: white**
*** Solder mask color: black**
*** Remove slikscreen as needed to prevent ink on any exposed copper**
*** Surface finish: ENIG**
*** Hole dimensions are finished size, +/-3mil**
*** Linear board dimension tolerance: +/-10mil**
*** Bow, twist, warp not to exceed 0.75% of greatest diagonal span**
*** PCB shall be UL Recognized printed wiring board (ZPMV2), minimum flammability rating 94V-0**
*** PCB shall be marked with fabricator company or trade name, UL mark, and date code using legend ink on secondary side**
*** All PCBs shall be electrically tested for opens and shorts per gerber. Test marking shall be marked on secondard side.**

Fabricator shall panelize the PCB using mouse bites and tab routing. V-scoring not allowed.

Controlled impedance differential pairs shall be within +/-10% for 100ohm targets, and +/-10% for 90ohm targets. See Sheet 3 for transmission line details and location of 90ohm differential pairs.

Title: ***EL0258***	LUXonis
Number: D0000999 Revision: R0M0 E1	
Date: 05/06/2023 Sheet: 1 of 3	PROPRIETARY AND CONFIDENTIAL
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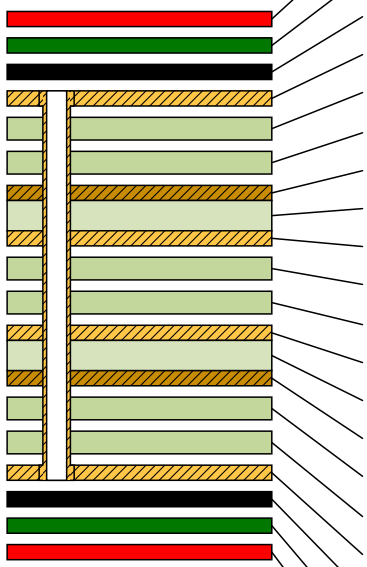
Layer Stack Legend



Layer	Thickness	Type	Gerber	Df	Dk
Top Overlay		Legend	GTO		
Top Solder	1.00mil(0.025mm)	Solder Mask	GTS	0,03	4
Top Surface Finish	0.79mil(0.020mm)	Surface Finish			
Top Layer	1.38mil(0.035mm)	Signal	GTL		
	2.80mil(0.071mm)	*Dielectric*		*0,02*	*4,1*
	2.80mil(0.071mm)	*Dielectric*		*0,02*	*4,1*
Int1 (GND)	1.38mil(0.035mm)	Internal Plane	GP1		
	18.00mil(0.457mm)	*Dielectric*		*0,02*	*4,7*
Int2 (Sign)	1.38mil(0.035mm)	Signal	G1		
	2.80mil(0.071mm)	*Dielectric*		*0,02*	*4,1*
	2.80mil(0.071mm)	*Dielectric*		*0,02*	*4,1*
Int3 (Sign)	1.38mil(0.035mm)	Signal	G2		
	18.00mil(0.457mm)	*Dielectric*		*0,02*	*4,7*
Int4 (PWR)	1.38mil(0.035mm)	Internal Plane	GP2		
	2.80mil(0.071mm)	*Dielectric*		*0,02*	*4,1*
	2.80mil(0.071mm)	*Dielectric*		*0,02*	*4,1*
Bottom Layer	1.38mil(0.035mm)	Signal	GBL		
Bottom Surface Finish	0.79mil(0.020mm)	Surface Finish			
Bottom Solder	1.00mil(0.025mm)	Solder Mask	GBS	0,03	4
Bottom Overlay		Legend	GBO		

Total thickness: 64.64mil(1.642mm)

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
◇	201	8.00mil(0.203mm)	Plated	
□	4	86.61mil(2.200mm)	Plated	
	205 Total			

Title: ***EL0258***	LUXonjs
Number: D0000999 Revision: R0M0 E1	
Date: 05/06/2023 Sheet: 2 of 3	PROPRIETARY AND CONFIDENTIAL
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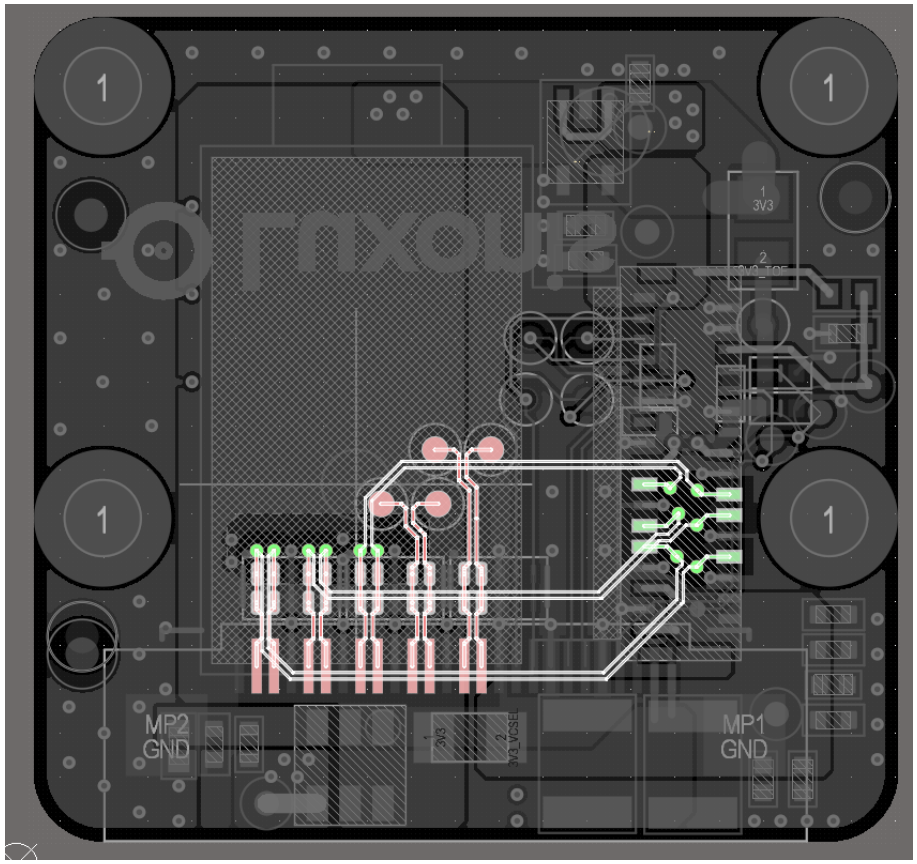

100 OHM (+/-10%) DIFF PAIRS

Transmission Line Structure Table

Impedance Id	Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Wide Trace Width	Narrow Trace Width	Gap	Reference layers	Target Tolerance
1	Edge-Coupled Coated Microstrip	100	100.03	Top Layer	0.12mm	0.12mm	0.13mm	Int1 (GND)	10%
2	Edge-Coupled Offset Stripline	100	100.02	Int2 (Sign)	0.06mm	0.06mm	0.13mm	Int1 (GND),Int3 (Sign)	10%
3	Edge-Coupled Offset Stripline	100	100.02	Int3 (Sign)	0.06mm	0.06mm	0.13mm	Int2 (Sign),Int4 (PWR)	10%
4	Edge-Coupled Coated Microstrip	100	100.03	Bottom Layer	0.12mm	0.12mm	0.13mm	Int4 (PWR)	10%

Title: ***EL0258***	LUXonjs
Number: D0000999 Revision: R0M0 E1	
Date: 05/06/2023 Sheet: 3 of 3	PROPRIETARY AND CONFIDENTIAL
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