Unifying FPGAs and SIMD Arrays

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Acknowledgments: Support for this research was provided in part by the Advanced Research Projects Agency under Office of Naval Research contracts ONR N00014-91-J-1698 and DABT63-92-C-0039. This material is based upon work supported under a National Science Foundation Graduate Fellowship. Any opinions, findings, conclusions or recommendations expressed in this publication are those of the author and do not necessarily reflect the views of the National Science Foundation.

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Outline

- Unified Computational Array Model
  - FPGAs
  - SIMD Arrays
- Hybrid Array
  - DPGA
  - Benefits
- Conclusions

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FPGA v/s SIMD Computation

- FPGA
  - Fixed Function in Time
  - Spatially Varying Computation
  - Bit-Parallel Computation
  - Build Computation Spatially
    - Low-latency
- SIMD Array
  - Operation Varies in Time
  - Homogenous Computation in Space
  - Bit-Serial Computation
  - Build Computation in Time
    - High Throughput on Homogeneous data

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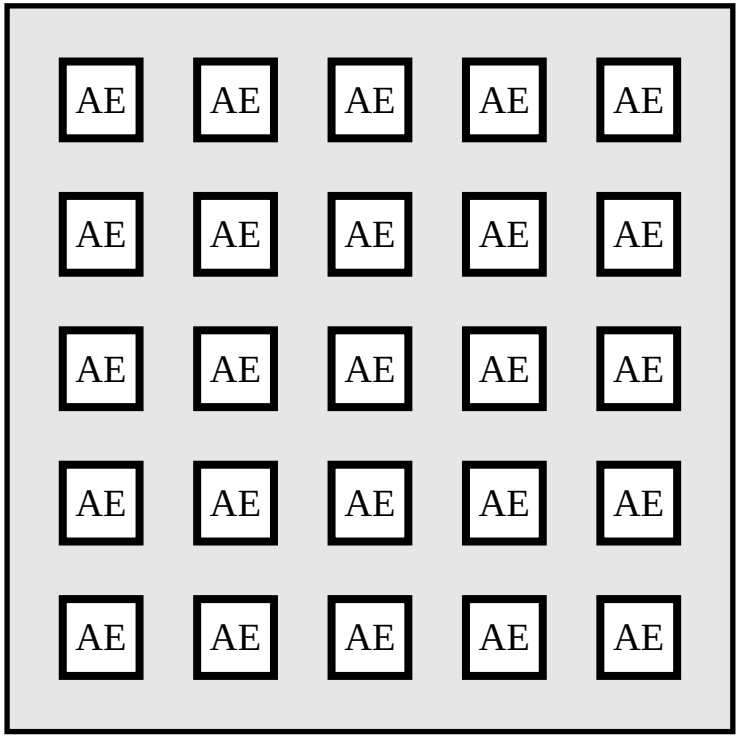
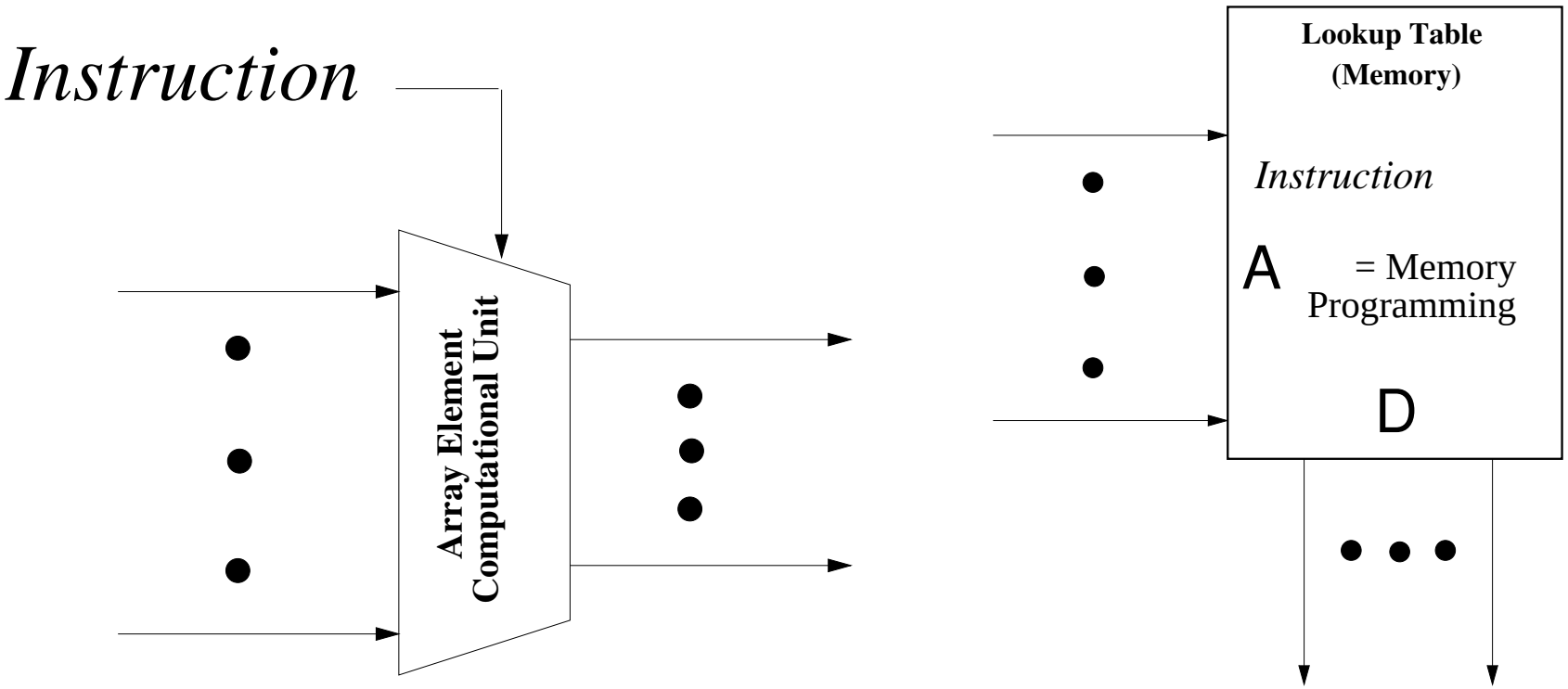
Unified Computational Array Model

- **Lattice of AEs**
  - **Computational Unit**
  - **Local State**
- **Interconnection resources**
- *Instruction* **controls**
  - **AE operation**
  - **Interconnect**
  - **State manipulation**



Unified Computational Array Model

(Computational Element)



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Unified Computational Array Model

(Instruction Distribution)

- **Ideal Model:** *Instruction*/**AE/cycle**

$$I_{BW} = \frac{P \cdot I_{size}}{t_{cycle}}$$

  - 100 AE's, $I_{size} = 6$, 10MHz $\Rightarrow$ 6Gbits/sec

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Unified Computational Array Model

(Weakening Instruction Distribution)

- **FPGA**
  - *Instruction*/**AE**
  - **uniform in time**
  - **Slow "programming" phase**
- **SIMD Array**
  - *Instruction*/**cycle**
  - **uniform in space**

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Dynamically Programmable Gate Arrays

(Hybrid Model)

- **Broadcast a** *Context Identifier*
- **Indirect** *Instruction* **Lookup**
- **Separate lookup programming for each AE**
- **Features:**
  - **Limited Instruction Bandwidth**
  - **Spatially and Temporally Varying Computation**

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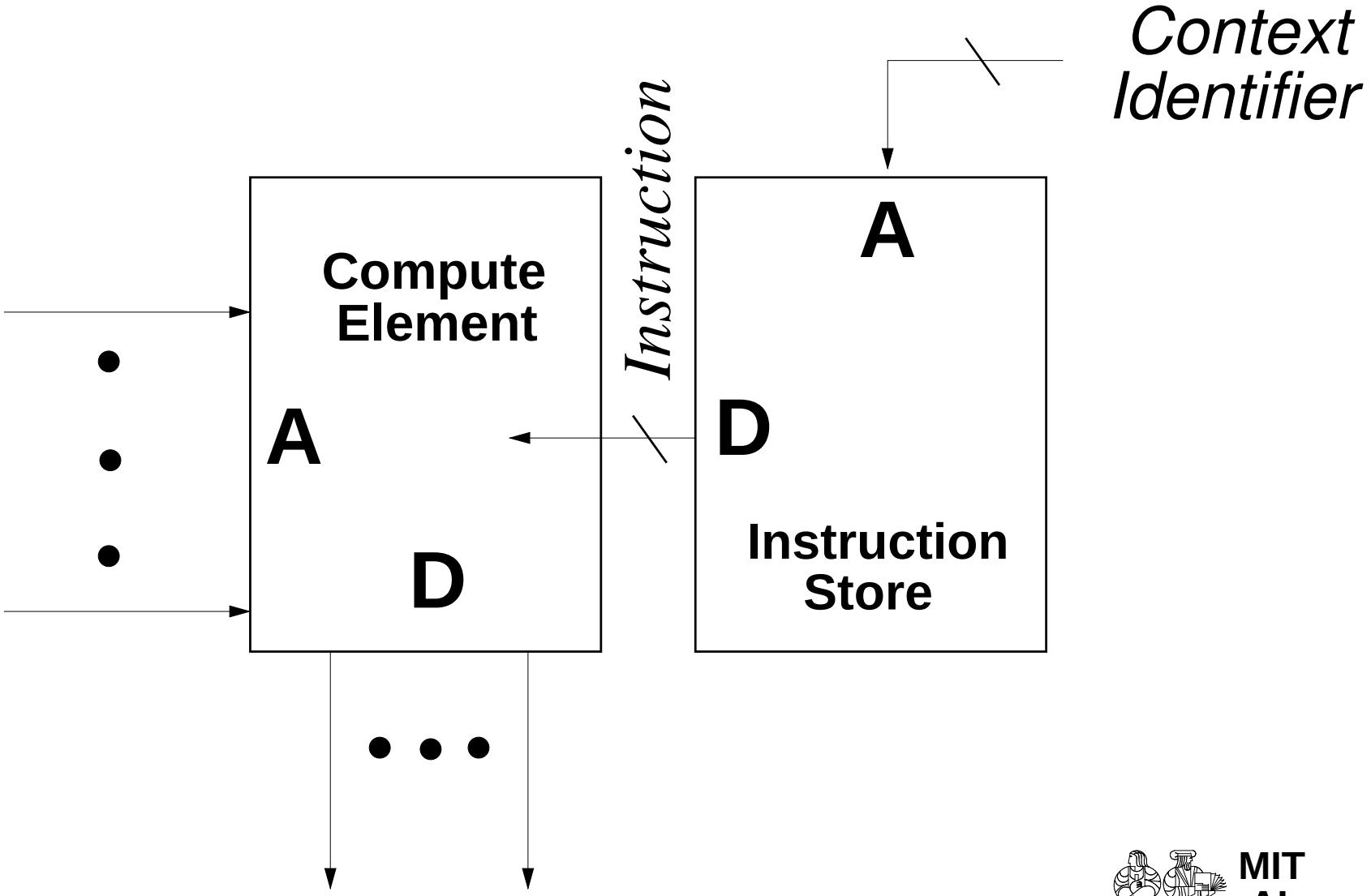
Dynamically Programmable Gate Arrays



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Dynamically Programmable Gate Arrays

(Application)

- Multi-stream SIMD
- Boundary condition handling
- Rapid context switch FPGA
- Time-slice computation
- Virtual Cells
- Processor Assisstance

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Conclusions

- Unified Computational Array Model
  - Bandwidth Limitation
  - FPGA and SIMD Arrays opposite extremes
- DPGA
  - Limited bandwidth requirements
  - Spatially and temporally varying computation
- Array implementation
  - Match array mirco-architecture to technology
  - Cross-fertilization between FPGA and SIMD designs
  - Avoid architectural extremes

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