ECE 10B Winter 2019

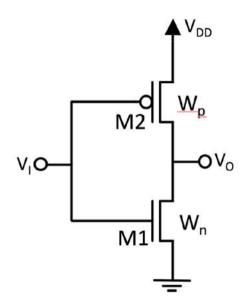
## UNIVERSITY OF CALIFORNIA, SANTA BARBARA

Department of Electrical and Computer Engineering

## Homework 1 – due January 18, 2018 by 5:00pm

NOTE: For all the problems here, and from now on, we'll use the common terminology for K. Namely, we'll use  $K_n = K_n$ ' (W/L) for n-MOSFETs and  $K_p = K_p$ '(W/L) for p-MOSFETs.  $K_n$ ' =  $\mu_n C_{ox}$  and  $K_p$ ' =  $\mu_p C_{ox}$ .

1) For the CMOS inverter circuit shown below, assume the following:  $K_n' = K_p'$ ,  $L_n = L_p = 1 \mu m$ , and  $/V_{TP}/=V_{TN} = V_T$ . Let's define the threshold as the point  $(v_I = V_{TH})$  in the  $v_O$  versus  $v_I$  transfer curve where  $v_O = V_{DD}/2$ .



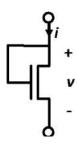
- a) Sketch the inverter transfer curve and mark the  $V_{TH}$  point.
- b) Find an expression for the inverter threshold voltage  $V_{TH}$  in terms of  $V_{DD}$ ,  $V_T$ ,  $W_n$  and  $W_p$ .
- c) If  $W_n = W_p$ , what is  $V_{TH}$ ? In what mode of operation are M1 and M2 when  $V_I = V_{TH}$ ?

d) Now assume  $V_{DD} = 5$ V. Fill in  $V_{TH}$  in the tables below for the cases when  $V_T = 0$ V and when  $V_T = 1$ V.

| $V_T = 0 V$ |   |   |    |  |  |
|-------------|---|---|----|--|--|
| $W_p$ $W_n$ | 1 | 4 | 16 |  |  |
| 1           |   |   |    |  |  |
| 4           |   |   |    |  |  |
| 16          |   |   |    |  |  |

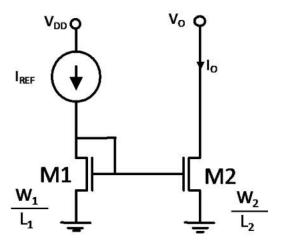
| $V_T = 1 V$ |   |   |    |  |  |
|-------------|---|---|----|--|--|
| $W_p$ $W_n$ | 1 | 4 | 16 |  |  |
| 1           |   |   |    |  |  |
| 4           |   |   |    |  |  |
| 16          |   |   |    |  |  |

2. The configuration shown below, an n-MOSFET with its drain and gate terminals connected together, is called a **diode-connected MOSFET**.



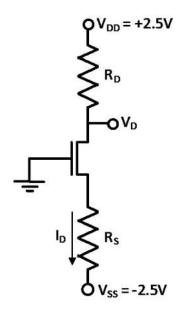
- a. In what mode does the MOSFET operate and why?
- b. Find the i-v characteristics of the two-terminal device in terms of the MOSFET parameters K and  $V_T$ .
- c. Plot the *i-v* characteristics if  $K = 1 \text{mA/V}^2$  and  $V_T = 1 \text{V}$  over the range of v = 0 to 5V (1V increments in voltage are sufficient)

3. Consider the circuit shown below. Assume that both of the transistors are matched, meaning: 1)  $K_n$  is the same for both devices M1 and M2, and is equal to  $1 \text{mA/V}^2$ ; 2)  $V_T = 0.5 \text{V}$  for both M1 and M2. Recall that  $K = K_n$  (W/L), where W is the length and L is the width of the MOSFET. Further assume that  $V_{DD} = 3 \text{V}$  and  $V_O$  is large enough that M2 operates in the saturation regime.



- a. In what mode does M1 operate and why?
- b. Find the relationship between  $I_O$  and  $I_{REF}$  in terms of the MOSFET parameters.
- c. Find  $V_{GS}$  if  $I_{REF} = 10$ mA,  $W_I = 10$ µm, and  $L_I = 1$ µm.
- d. Find  $I_O$  under the conditions in part (c) if  $W_2 = 20 \mu m$  and  $L_2 = 1 \mu m$ .
- e. What is the minimum value for  $V_O$  to ensure M2 is in saturation under the conditions of part (d)?

4. Determine the Values of  $R_D$  and  $R_S$  such that the circuit below operates at  $I_D=0.4$  mA and  $V_D=+0.5V$ . Assume  $V_T=0.7V$ ,  $K_n=100\mu\text{A}/\text{V}^2$ , L=1  $\mu\text{m}$ , and W=32  $\mu\text{m}$ .



5. Determine  $V_O$  in the circuit below in terms of the power supply voltages and MOSFET parameters  $(W_1, L_1, W_2, L_2, V_T)$ . You can assume that  $K_n$  is the same for both of the n-MOSFETs and that both M1 and M2 are biased in the saturation region.

