Schematic Driven Silicon Photonics Design (Invited)

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ABSTRACT

Electronic circuit designers commonly start their design process with a schematic, namely an abstract representation of the physical circuit. In integrated photonics on the other hand, it is very common for the design to begin at the physical component level. In order to build large integrated photonic systems, it is crucial to design using a schematic-driven approach. This includes simulations based on schematics, schematic-driven layout, layout versus schematic verification, and post-layout simulations.

This paper describes such a design framework implemented using Mentor Graphics and Lumerical Solutions design tools. In addition, we describe challenges in silicon photonics related to manufacturing, and how these can taken into account in simulations and how these impact circuit performance.

Keywords: silicon photonics design, photonic integrated circuits design, design methodologies, electronic design automation (EDA), manufacturing variability, corner analysis

1. INTRODUCTION

Efficient circuit simulations can be by achieved by using S-parameters directly. This is particularly simple for the optical transmission response of an optical circuit, built using components with known S-parameters. For time domain simulations, the circuit modelling tool internally needs to convert the S-parameters into a time-domain representation. In this section, we use the results of the FDTD simulations in a circuit simulation, using Lumerical INTERCONNECT.

2. FABRICATION VARIABILITY AND YIELD PREDICATION FOR SILICON PHOTONIC MZI SWITCHES

The high refractive index contrast of SOI permits sharp waveguide bends and ultrasmall device sizes, making it promissing for the development of dense integration of photonic components. However, silicon photonic devices face serious reliability challenges. Fabrication errors on either the waveguide linewidth or thickness might affact the propagation constant of light inside the waveguide, and, thus, degrade the performance of devices.

Yield simulation and prediction are critical for photonic devices. In semiconductor manufacturing community, corner analysis and simple Monte Carlo simulation are typically used to analyze fabrication variability, the former of which predicts the worst performance of devices; while the later of which assume a uniform process variation across a wafer. However, neither of them captures die-to-die, device-to-device, and intra-device correlated variations. Correlated yield analysis is driving more and more attention, and some statistical investigations regarding on-chip correlation[1,2] and uncertainty of devices[3] have been reported. In this work, we propose, for the first time, a correlated and physical layout dependent methodology for the yield analysis of on-chip photonic integrated circuits. From physical layout to Monte Carlo simulation, our methodology will provides an insight into the significance of compact layout for photonic designs, and offers a useful tool for post-layout verification and power trimming estimation.

Figure 1(a) shows the flow chart of our proposed methodology, and the procedures include:

- First, silicon photonic circuits and/or devices under test are layouted using Klayout,[4] an open-source graphic tool.

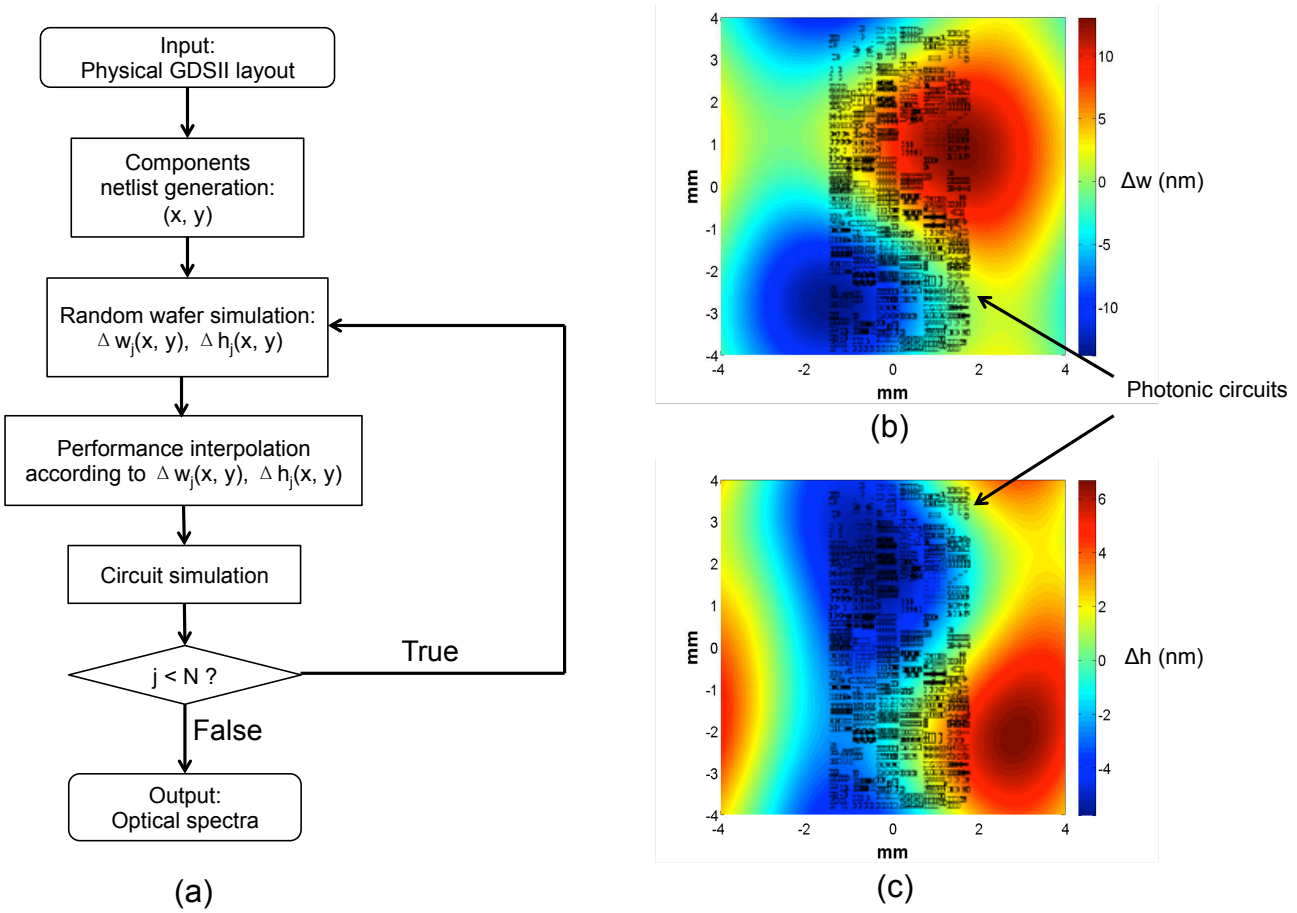

Figure 1: (a) Flow chart of the proposed methodology; (b) simulated waveguide linewidth deviations across a wafer; (c) simulated waveguide thickness deviations across a wafer.

- The netlist of the layout, which provides information about the primitive elements and the connections between the elements, are generated from Klayout and imported into Lumerical INTERCONNECT for circuit simulation.
- The third step is wafer simulation. In INTERCONNECT, silicon linewidth deviations, $\Delta w(x, y)$, and thickness deviations, $\Delta h(x, y)$, are simulated across the whole wafer, as demoed in Figs. 1(b) and 1(c), respectively. The simulated deviations are characterized by a sigma RMS amplitude and a correlation length, and both of them are based on experimental results.[1,2] In each run of the Monte Carlo simulation, different deviation maps will be generated.
- According to the spatial dependent linewidth and thickness deviations, the optical S-parameters of primitive elements and the optical propagation constants of connecting waveguides are interpolated in INTERCONNECT.
- Finally, the interpolated circuit will be simulated.

The scatter plot in Fig. 2 shows the simulated phase error of a balanced MZI versus the waveguide spacing between two phase arms, in a 248 nm CMOS compatible process. In the Monte Carlo simulations, the horizontal length of the phase arms, L, is 200 μm. The phase error is defined as the absolute optical phase difference between the two phase arms. Ideally, the phase error should be 0 when there is no fabrication variation. However, this figure clearly shows that the phase error of the MZI is approximately linearly proportional to the waveguide spacing, emphasizing the significance of very compact layout designs. Additionally, the simulated phase error can be used to estimate the trimming power of MZI based photonic switches.

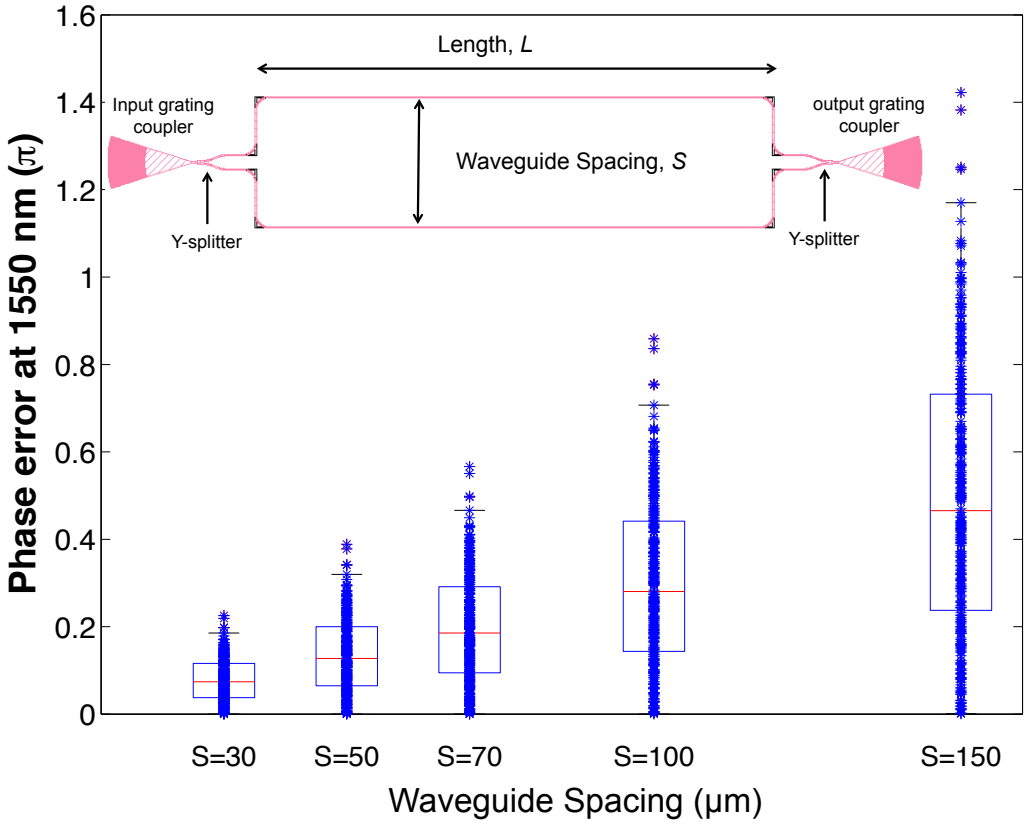

Figure 2: Scatter plot of phase error of a balanced MZI versus waveguide spacing.

3. CONCLUSION

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