Dongxu Lyu

Ph.D. student, Department of Micro/Nano Electronics, Shanghai Jiao Tong University

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Education

Shanghai Jiao Tong University — Shanghai, China
Ph.D. student in Department of Micro/Nano Electronics — *Sep. 2020 – Jun. 2025 (expected)*
Supervisor: Guanghui He

Shanghai Jiao Tong University — Shanghai, China
B.E. in Microelectronics Science and Engineering — *Sep. 2016 – Jun. 2020*
Supervisor: Guanghui He

Honors and Awards

1st Prize, China Postgraduate IC Innovation Competition	Association of Chinese Graduate Education	2021
Shanghai Outstanding Graduate	Shanghai City	2020
Departmental Excellent Undergraduate Thesis	Shanghai Jiao Tong University	2020
Guanghua Scholarship	Shanghai Jiao Tong University	2019

Professional Experience

Huixi Technology — Shanghai, China
Hardware & Toolchain Intern (Full-time) — *Mar. 2022 – Present*

- Build C/C++ behavior models for specialized NPU in Rhino Autonomous Driving Chip **independently**.
- Unit&Integration Test of NPU RTL design.
- NPU RTL design for matrix&vector units.

Selected Research Projects

Efficient Hardware Accelerators for AI Computing — *Jan. 2022 – Present*

- **First** grid-based feature learning network accelerator for large-scale point cloud processing.[C3,J2]
- Real-time 3D sparse convolution accelerator.[C4]
- 2D object detection accelerator.[C2]

Emerging Stochastic Computing Techniques for AI Computing — *Sep. 2021 – Jan. 2023*

- Sobol-based stochastic computing technology.[C1]

Efficient Massive MIMO Detectors for 5G/6G Communication — *Sep. 2019 – Sep. 2021*

- Tree-based soft-output MIMO detector.[J1]

Talks

Conference Presentation

- "FLNA: An Energy-Efficient Point Cloud Feature Learning Accelerator with Dataflow Decoupling", in *DAC'23*, Moscone Center West, San Francisco, CA, USA, July 12, 2023
- "SpOctA: A 3D Sparse Convolution Accelerator with Octree-Encoding-Based Map Search and Inherent Sparsity-Aware Processing", in *ICCAD'23*, Hyatt Soma Downtown, San Francisco, CA, USA, Octotor 31, 2023

Skills

Programming Languages: C/C++, Python, Go, MATLAB, Verilog/SystemVerilog

EDA Tools: Modelsim, VCS, DVE, Verdi, Synopsys Design Compiler, Synopsys IC Compiler, Xilinx Vivado Design Suite,

Publications

Conference

[C4] **Dongxu Lyu**, Zhenyu Li, Yuzhou Chen, Jinming Zhang, Ningyi Xu and Guanghui He, "SpOctA: A 3D Sparse Convolution Accelerator with Octree-Encoding-Based Map Search and Inherent Sparsity-Aware Processing," in *2023 42th IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Oct 29 - Nov 2, 2023

[C3] **Dongxu Lyu**, Zhenyu Li, Yuzhou Chen, Ningyi Xu and Guanghui He, "FLNA: An Energy-Efficient Point Cloud Feature Learning Accelerator with Dataflow Decoupling," in *2023 60th ACM/IEEE Design Automation Conference (DAC)*, Jul 9 - Jul 13, 2023

[C2] Yuzhou Chen, Jinming Zhang, **Dongxu Lyu**, Xi Yu and Guanghui He, "O^3NMS: An Out-Of-Order-Based Low-Latency Accelerator for Non-Maximum Suppression," in *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 21 - May 25, 2023

[C1] Aokun Hu, Wenjie Li, **Dongxu Lyu** and Guanghui He, "An Efficient Stochastic Convolution Accelerator based on Pseudo-Sobol Sequences," in *17th ACM International Symposium on Nanoscale Architectures (NANOARCH)*, Dec, 2022

Journal

[J2] **Dongxu Lyu**[‡], Zhenyu Li[‡], Yuzhou Chen, Weifeng He, Ningyi Xu and Guanghui He, "FLNA: Flexibly Accelerating Feature Learning Networks for Large-Scale Point Clouds with Efficient Dataflow Decoupling," **Minor Revision** in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Nov, 2023 ([‡]: equal contribution)

[J1] Zhuojun Liang, **Dongxu Lyu**, Chao Cui, Hai-Bao Chen, Weifeng He, Weiguang Sheng, Naifeng Jing, Zhigang Mao and Guanghui He, "A 3.85-Gb/s 8×8 Soft-Output MIMO Detector With Lattice-Reduction-Aided Channel Preprocessing," in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Nov, 2020