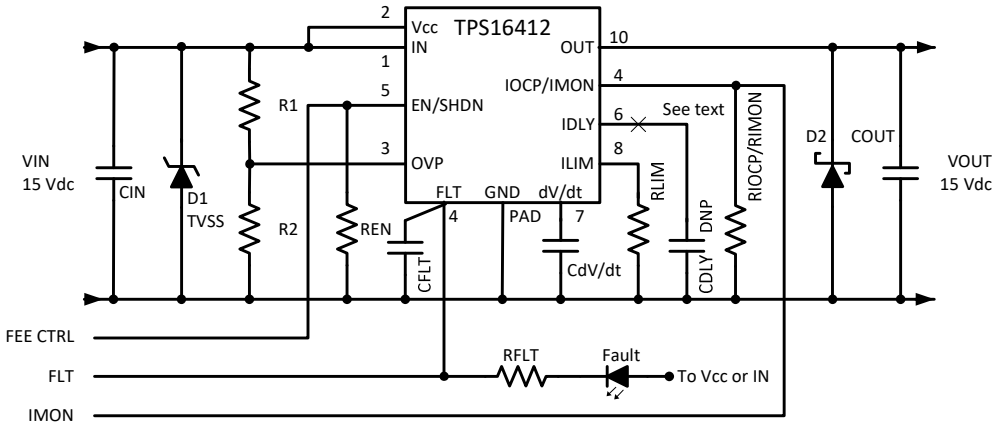
Application of the TI TPS16412 eFuse in the Rev. I ARX (includes Addendums 1 & 2)
Whitham D. Reeve

The TPS16412 is an integrated FET power management device and includes overvoltage protection, inrush control, current limiting, overcurrent protection, short-circuit protection and load current and fault monitoring. The device is supplied in the VSON or very-thin small-outline no-lead package. Device dimensions are 3 x 3 x 1 mm (LxWxH).

In the ARX application, the device provides FEE power feed and on/off switching control, overvoltage protection, current limiting, overcurrent protection and current and fault monitoring. Current limiting and overcurrent protection is used to prevent damage to the ARX and FEE bias-tee inductors from coaxial feedline faults that cause an overcurrent condition. The schematic and component values below (revised by Addendums 1 and 2) show the device configuration in the ARX. The components are described in the following sections along with calculations based on the methods described in the manufacturer's datasheet. A block diagram of the eFuse are shown at the end of this report.



Summary of components:

Component	Value	Remarks	
R1	1 Mohm, 1%	OCP voltage divider	
R2	68.1 kohm, 1%	OCP voltage divider	
REN	4.7 kohm, 1%	Enable pull-down	Addendum 1
CdVdt	0.68 µF, 50 V, 5%		
RLIM	27.4 kohm, 1%		Addendum 2
RIOCP	41.2 kohm, 1%		Addendum 2
RFLT	Depends on LED	LED current limit	
CDLY	Not used (see text)	Connect pin to GND or open	
CFLT	1 nF, 50 V		
D1	18 to 36 V	SMAJ-series	Littelfuse TVS
D2	60 V	B260A or B360A	Diodes, Inc. Schottky
COUT	10 µF + 0.1 µF	Both MLCC, Low ESR	
CIN	1 µF + 0.1 µF	Both MLCC	

Note 1: REN added by Addendum 2
Note 2: RLIM changed by Addendum 3 to increase the current limit to 360 mA
Note 3: RIOCP changed as a result of Addendum 2

The eFuse defines and monitors several currents: INRUSH < IOUT < ILIM ≤ IOCP ≤ IFast-trip ≤ ISCP, where INRUSH is the momentary current through the eFuse when it is turned on and it charges the capacitance on its output, IOUT is the load current, ILIM is the design current limit, IOCP is the design overcurrent protection threshold current that allows momentary overcurrent, IFast-trip is the fault current above the overcurrent protection threshold, and ISCP is the short-circuit protection current. The INRUSH, ILIM and IOCP are configurable. The IFasttrip is internally set to 1.9X IOCP and ISCP is internally set to 6.7 A. The IFast_trip and ISCP invoke delay timers that allow momentary currents such as those from motor starting and capacitor charging.

Enable and shutdown input: The EN/SHDN pin controls the eFuse. Setting this pin high turns on the device. Holding the EN/SHDN pin low for more than tLOW_SHDN (24 ms) puts the eFuse into low power shutdown mode in which internal device components are turned off. According to the datasheet (section 7.5), the thresholds are 1.2 V for the rising condition on the EN/SHDN pin and 0.59 V for the falling condition. The maximum allowed voltage on the EN/SHDN pin is 5.5 V.

Addendum 1 ~ eFuse Enable Pull-Down Resistor

The eFuse datasheet sect. 7.5 says the open circuit Enable voltage (VEN-Open) on pin 5 Enable is 4.9 V. This voltage is produced internally and will enable the eFuse when the pin sees an open circuit.

For each channel-pair, the Enable pin 5 on each eFuse is connected directly to P16 (polarization B) and P17 (polarization A) on the MAX7301 port expander. The MAX7301 powers up with P16 and P17 set as GPIO inputs (Table 4 of MAX7301 datasheet), and the input leakage current IIH and IIL is ±100 nA. This can be considered an open circuit in the context of the eFuse Enable input. Thus, the eFuse is enabled until the associated port expander port is configured as an output and pulled low. This can be fixed by using a pull-down resistor on the eFuse Enable pin 5.

The eFuse Enable pin leakage current IEN is –10 µA minimum, and the enable threshold voltage for a rising input VENR is 1.2 V and for a falling input VENF is 0.59 V. Thus, it is necessary to ensure that the voltage drop across the pull-down resistor is << 0.59 V, say, for example, 0.59 V/10 = 0.06 V.

The combined current through the pull-down resistor is –10 µA ± 0.1 µA = –9 to –10.1 µA. To limit the voltage drop to the example 0.06 V, the pull-down resistor resistance range is (0.06 V)/(–9 to –10.1 µA) = 6 667 to 5 941 ohms. Lower resistance values would provide lower voltages.

For example, a 4.7 kohm pull-down resistor would limit the voltage drop to (–9 to –10.1 µA) x 4.7k = 0.042 to 0.048 V. A 4.7 kohm resistor is chosen for this application.

IN to OUT resistance: According to the datasheet (section 7.5), the resistance RON across the IN and OUT pins when the device is turned on can be as low as 96 mohm at low temperatures to as high as 215 mohm at 85 °C. A typical value is 153 mohm. With 240 mA FEE operating current, the typical voltage drop across the eFuse is 37 mV and the maximum voltage drop is 52 mV.

Overvoltage protection: The overvoltage protection thresholds are adjusted by connecting the OVP pin through a resistive voltage divider R1 and R2 to the input voltage IN pin. The overvoltage protection function may be disabled by connecting the OVP pin to GND.

The eFuse turns off the internal FET and pulls the FLT pin low if the voltage on the OVP pin rises above the threshold voltage VOVPR. If the voltage on the OVP pin subsequently falls below OVPF, the internal FET is turned on and the FLT pin is pulled high through a pull-up resistor.

According to the datasheet (section 9.5), the pull-up resistor should limit the current to 3 mA on the FLT pin. Therefore, for a 15 V supply voltage, the RFLT should be > 5 kohms; the suggested value for the ARX application is at least 10 kohms. The FLT pin may be pulled high through a low-current fault indicating LED and appropriate current limiting/pull-up resistor.

The rising overvoltage protection VOVPR and falling overvoltage protection OVPF thresholds are set according to the datasheet (section 9.2.2.1) by

$$OVPR = VOVPR \cdot \frac{R1 + R2}{R2} \text{ ohms} \quad (1)$$

$$OVPF = VOVPF \cdot \frac{R1 + R2}{R2} \text{ ohms} \quad (2)$$

Only the rising overvoltage protection function is used in the ARX application. The rising overvoltage protection threshold setpoint OVPR is set below the FEE voltage regulator maximum voltage (26 V continuous and 60 V for 100 ms transients) or eFuse device maximum voltage (40 V), whichever is lower. In this application, OVPR = 24 V to be conservative. According to the datasheet (section 7.5), the OVP pin voltage for the rising condition VOVPR = 1.48 to 1.58 V (minimum, maximum) and for the falling condition OVPF = 1.34 to 1.46 V (minimum, maximum).

Only the rising condition is considered. Solving equation (1) for R2 gives

$$R2 = \frac{VOVPR \cdot R1}{\left(OVPR - VOVPR\right)} \text{ ohms} \quad (3)$$

In this application, R1 is set to 1M ohms. Substituting OVPR (24 V), R1 (1 Mohm) and typical VOVPR (1.53 V) gives

$$R2 = \frac{VOVPR \cdot R1}{\left(OVPR - VOVPR\right)} = \frac{1.53 \cdot 1M}{\left(24 - 1.53\right)} = 68.1 \text{ kohms} \quad (4)$$

The nearest 1% resistor value is 68.1 kohms.

For VOVPR minimum and maximum datasheet values of 1.48 and 1.58 V, the rising overvoltage protection setpoints are

$$OVPR(\text{min}) = VOVPR(\text{min}) \cdot \frac{R1 + R2}{R2} = 1.48 \cdot \frac{1M + 68.1k}{68.1k} = 23.2 \text{ V} \quad (5)$$

$$OVPR(\text{max}) = VOVPR(\text{max}) \cdot \frac{R1 + R2}{R2} = 1.58 \cdot \frac{1M + 68.1k}{68.1k} = 24.8 \text{ V} \quad (6)$$

Output slew rate and inrush current control (dV/dt): The inrush current through the eFuse when it turns on is directly proportional to the load capacitance COUT and rising voltage slew rate SR. According to the datasheet (section 8.3.3), the slew rate is

$$SR(V/s) = \frac{IINRUSH(A)}{COUT(F)} \text{ V/s} \quad (7)$$

Alternatively,

$$IINRUSH(A) = SR(V/s) \cdot COUT(F) \text{ A} \quad (8)$$

There is an advantage to slowing the voltage slew rate at the v1.8 FEE to reduce damaging transients on the MCL GALI-6+ output stage amplifier during voltage ramp-up. Mini-Circuits recommends 100 ms ramp-up time. For a 100 ms ramp time, the slew rate would be 15 V/100 ms = 150 V/s. The slew rate is configured as described later. Assuming COUT is 10 µF, the inrush current IINRUSH would be

$$IINRUSH(A) = SR(V/s) \cdot COUT(F) = 150 \cdot 10 \cdot 10^{-6} = 1.5 \cdot 10^{-3} \text{ A} = 1.5 \text{ mA} \quad (9)$$

The average power dissipation PDINRUSH inside the eFuse during inrush may be calculated from

$$PDINRUSH(W) = \frac{IINRUSH(A) \cdot VIN(V)}{2} \text{ W} \quad (10)$$

In the ARX application

$$PDINRUSH(W) = \frac{IINRUSH(A) \cdot VIN(V)}{2} = \frac{1.5 \cdot 10^{-3} \cdot 15}{2} = 0.011 \text{ W} \quad (11)$$

For a given power dissipation, the thermal shutdown time of the eFuse must be greater than the ramp-up time to avoid startup problems. The datasheet (section 7.7, figures 7.14 and 7.15) provides plots of thermal shutdown time vs power dissipation for VIN = 12 V and 24 V. The maximum scale for time to shutdown on both plots is 200 ms and the curves are very steep at power dissipation values below 1 W, thus it cannot be reliably determined from the plots if the shutdown time is greater than the ramp-up time. This operational aspect might be determined from the TPS16412 Evaluation Module, and it may be necessary to reduce the ramp-up time from 100 ms to a lower value. In any case, the eFuse protects itself from over-temperature as discussed later.

A capacitor CdVdt may be connected to the dVdt pin to set the voltage slew rate and control the inrush current when the eFuse is turned on. The fastest slew rate is attained by leaving the dVdt pin open but the fastest slew rate value is not given in the datasheet.

Assuming the 100 ms ramp-up time and associated inrush current are suitable from a thermal standpoint, the following calculations may be made. According to the datasheet (section 8.3.3), the capacitance CdVdt in terms of the dV/dt charging current IdVdt and the dVdt Gain GdVdt is calculated from

$$CdVdt(F) = \frac{IdVdt(A) \cdot GdVdt}{SR(V/s)} \text{ F} \quad (12)$$

The recommended range of CdVdt is 10 nF to 5 µF. The datasheet (section 7.5) provides values for IdVdt and GdVdt. Typical IdVdt = 2 µA and GdVdt = 50 V/V. If the slew rate is 150 V/s, as previously used, then

$$CdVdt(F) = \frac{IdVdt(A) \cdot GdVdt}{SR(V/s)} = \frac{2 \cdot 10^{-6} \cdot 50}{150} = 0.67 \cdot 10^{-6} \text{ F} = 0.67 \text{ µF} \quad (13)$$

The nearest 5% standard ceramic capacitor value is 0.68 µF.

Active current limiting: The eFuse responds to overcurrent conditions by actively limiting the current when an overload occurs. The device first provides a blanking time configured by a capacitor on the IDLY pin. During the blanking time, the device can provide a current up to overcurrent protection setpoint IOCP. At the end of the blanking time, the eFuse limits current to the current limit threshold ILIM. The blanking time allows the eFuse to ride through motor starting currents or large filter capacitor charging currents. The blanking time delay and IOCP are discussed in the next section.

The current limit setting for the ARX is based on the current carrying capabilities of the bias-tee inductors in the ARX and FEE. The specified ARX inductor (Coilcraft 1205POC-103) can handle approximately 0.5 A for a 40 °C temperature rise above 85 °C ambient and the FEE inductor (Coilcraft 1008PS-472) can handle approximately 1.4 A for a 40 °C temperature rise above 85 °C ambient. The FEE normal operating current is about 240 mA for V2.0 & V2.1 FEE and about 250 mA for V1.8 FEE.

ILIM is set by connecting a resistor RLIM from the ILIM pin to GND. The current limiting accuracy is given in the datasheet (section 3) as ±6%. According to the datasheet (section 8.3.4), RILIM is calculated from

$$RLIM = \frac{0.984 \cdot 10k}{ILIM(A)} \text{ kohms} \quad (14)$$

The recommended range of RLIM is 5.1 to 348 kohms.

Addendum 2 ~ Current Limit Adjustment

An eFuse current limit of 360 mA (240 mA + 50%) is used, in which case

$$RLIM = \frac{0.984 \cdot 10k}{ILIM(A)} = \frac{0.984 \cdot 10k}{0.360} = 27.3 \text{ kohms} \quad (15)$$

The nearest 1% resistor value above 27.3 kohms is 27.4 kohms.

Note: The 2-channel prototype ARX board originally used 32.4 kohms to set the current limit to 300 mA, but this was deemed too close to the nominal load current. As a result of this change, the Overcurrent Protection had to be adjusted upward as described below.

Overcurrent protection and blanking time for transient loads: The overcurrent protection setpoint current IOCP must be higher than the current limit ILIM discussed in the previous section by at least 10% margin (this margin is not specified in the datasheet and was provided by a TI applications engineer on the TI Forum). It is controlled by delay timers. When the load current rises above ILIM due to a momentary or continuous overload, the eFuse provides current up to the overcurrent protection setpoint IOCP for the duration of the configurable tIDLY timer

(default 6.5 ms) and then reduces the current to ILIM for a maximum duration of the tLIM_DUR timer (default 2X tIDLY = 13 ms). These timers allow the device to ride through momentary transients. The tIDLY timer is configurable as described below but it is not used in the ARX application.

The overcurrent protection setpoint IOCP is configured by connecting a resistor RICOP from the IOCP/IMON pin to GND. According to the datasheet (section 8.3.6), the resistor value is calculated from

$$RIOCP = \frac{2.25A}{IOCP(A)} \cdot 7.32k \text{ ohms} \quad (16)$$

The recommended range of RIOCP is 6.34 to 80.6 kohms. If IOCP is set to 400 mA (current limit of 360 mA plus 10%), then

$$RIOCP = \frac{2.25A}{IOCP(A)} \cdot 7.32k = \frac{2.25A}{0.400} \cdot 7.32k = 41.2k \text{ ohms} \quad (17)$$

The nearest 1% resistor value is 41.2 kohms.

The blanking time for overload and overcurrent events is configured by connecting a capacitor between the IDLY pin and GND. According to the datasheet (section 8.3.6), the tIDLY, or blanking time IDLY, is

$$IDLY = \frac{6.5ms}{12nF} \cdot CDLY(nF) \text{ ms} \quad (18)$$

The recommended range of CDLY is 0.012 to 10 µF. If the IDLY pin is left open or connected to GND, the eFuse disables the blanking time and goes directly to current limiting. The blanking time is not required in the ARX application, so the IDLY pin should be connected to GND or not connected. If connected to ground, a zero ohm resistor may be used so that it can be replaced with a capacitor if a need for CDLY is found in the future.

Fast trip and short circuit protection: According to the datasheet (section 8.3.7), if the output current reaches the short circuit current ISCP level, an output short circuit is detected, and the eFuse turns off the internal FET after a short circuit protection delay tSCP_dly (280 ms). To prevent false tripping during low level input transients, the eFuse uses a fast-trip comparator to turn off the internal FET if the output current exceeds Ifast-trip (1.9 x IOCP).

Analog load current monitor on the IOCP/IMON pin: The eFuse provides an output load monitor current on the IOCP/IMON pin that is proportional to the internal FET current. The resistor RIOCP placed from the IOCP/IMON pin to GND converts the current to a voltage that may be sensed by the ARX control system. According to the datasheet (section 8.3.8), the output current IOUT is calculated from the value of resistor RIOCP (RIMON), the voltage VIMON across the resistor, the IMON/IOUT gain GIMON and IMON offset current OSIMON from

$$IOUT = \frac{VIMON - (OSIMON \cdot RIMON)}{GIMON \cdot RIMON} \text{ A} \quad (19)$$

Note that RIMON in this equation is the same resistor RIOCP determined in the previous section. The values of the gain GIMON range from 45 to 55 µA/A (50 µA/A typical) and the values of the IMON offset current OSIMON

range from –0.8 to +0.8 µA (0.05 µA typical). For the RIMON determined in the previous section (47.5 kohm), the typical offset voltage is 2.4 mV.

Addendum 3 ~ Load Current Monitoring

The gain of the eFuse load current monitor in the Rev. I ARX configuration is nominally 50 µA/A, which with the revised RIMON resistor value is equivalent to approximately 2 V/A compared to 10 V/A for the Rev. H current monitor. The gain is determined by the internal configuration of the eFuse as well as the external resistor RIMON. Thus, for example, for a load current of 250 mA, the output voltage from the eFuse is approximately 0.5 V compared to 2.5 V for the Rev. H current monitor. See the document *Evaluation of the TI TPS16412 eFuse for Use in the Rev. I ARX* for measurements and a plot.

The eFuse load current output has a small offset voltage. The calculated offset voltage from the eFuse is a couple mV, approximately equivalent to the error in the Rev. H shunt resistor. In the Rev. H ARX, the equivalent resistance is 0.099 ohms instead of 0.1 ohms because the Rev. H ARX has a 10 ohm resistor is parallel with the 0.1 ohm load shunt resistor.

IN-to-OUT short circuit detection: According to the datasheet (section 8.3.9), if the eFuse detects a resistance less than RSHORT (30 mohm) across the IN and OUT pins, it pulls the FLT pin low. At startup, the eFuse watches for a short across the IN and OUT pins and, if none exists, continues normal startup. After startup the device watches at regular (unspecified) intervals and if a short is detected, the FLT pin is pulled low after a delay tIN_OUT_Short_Detect (135 ms). After a short is detected, the eFuse is latched off. It may be reset by toggling the EN/SHDN pin or the Vcc supply. The EN/SHDN pin must be kept low for at least tLOW_SHDN (24 ms).

Thermal shutdown and overtemperature protection: The eFuse uses automatic shutdown to protect from high internal junction temperatures. The TPS 16412 eFuse does not latch off during thermal shutdown but apparently waits indefinitely for the temperature to lower. It automatically resets when the temperature decreases below a threshold.

According to the datasheet (section 8.3.10), during current limiting, the internal FET power dissipation is (VIN – VOUT) x IOUT, which will cause the junction temperature to increase. If the device junction temperature reaches TTSD (155 °C), the internal FET is turned off. The eFuse will wait for the temperature to go below TTSD – TTSD-hyst, where TTSD-hyst = 12 °C, and the device restarts after a delay tRETRY (8 x tIDLY where the default tIDLY = 6.5 ms). Note that tIDLY may be increased by connecting capacitor CDLY as discussed above, but this is not used in the ARX application.

Application: The eFuse has a relatively large thermal pad underneath that must be connected to GND. The pad is the primary thermal conductive path from the internal FET junction through the PCB to ambient air, so the GND should have as large an area as possible.

The input decoupling capacitor CIN should be ceramic and greater than 10 nF. Transient protection is needed on the input and output of the eFuse to protect it from overvoltages due to inductive kickback when the device interrupts the current during short circuit or overload conditions or when the board is disconnected and reconnected.

According to the datasheet (section 9.5.1), the transient voltage at the eFuse input is estimated from

$$VSPIKE(ABSOLUTE) = VIN + \left(ILOAD \cdot \sqrt{LIN/CIN} \right) \quad (20)$$

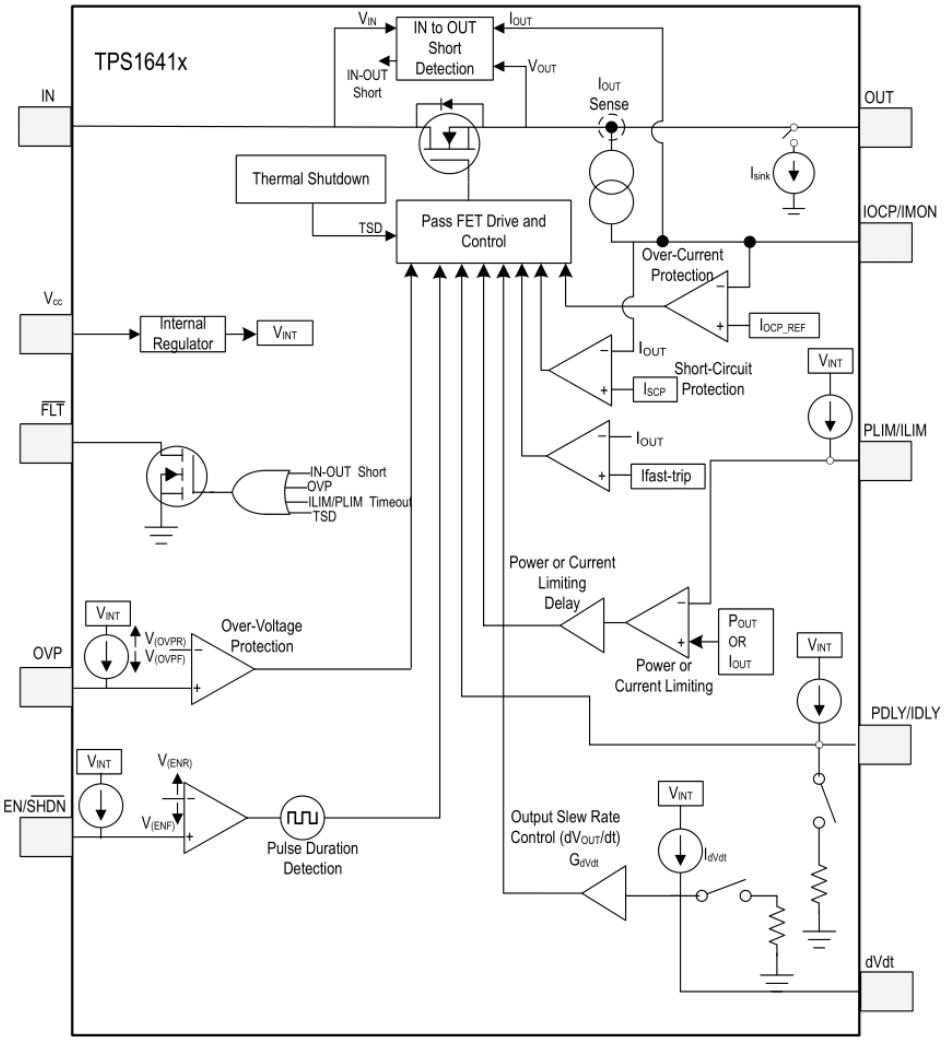
where VIN is the input supply voltage, ILOAD is the load current, LIN is the inductance looking into the source and CIN is the capacitance at the device input. Rather than attempt calculation of the peak spike voltages that might exist in the ARX, a TVSS D1 is placed across the input and a Schottky diode D2 is placed across the output. The eFuse IN pin is rated to 40 V and the Vcc pin is rated to 60 V. The eFuse OUT pin has an absolute maximum voltage rating of –1 V for negative transients.

In the ARX application, the IN and Vcc pins are tied together so a unidirectional TVS diode on the input should be rated no higher than 36 V (40 V – 10%) and no lower than 18.0 V (15 V + 20%). The percentages shown here are not adjusted for TVS diode tolerance. Suitable devices are the Littelfuse SMAJ-series TVS diodes. A Schottky diode is used on the output. A suitable device is rated 60 V such as the Diodes, Inc. B260A (2 A) or B360A (3 A). The protection devices on the input and output should be located as close as possible to the IN and OUT pins they are designed to protect.

The input power supply decoupling capacitor CIN should be placed as close as possible to the IN and GND terminals of the eFuse, and high current carrying power paths must be as short as possible and sized to carry at least twice the full load current (preferably twice the limiting current). The GND terminal must be tied to the PCB ground plane at the eFuse terminal. According to the datasheet (section 9.5.1), the capacitor COUT should be low ESR and larger than 1 µF (previous calculations assumed 10 µF).

The resistors and capacitors used to control the eFuse must be located close to their respective pins with the other ends connected with the shortest possible trace lengths to reduce parasitic effects on the current limit and overvoltage response. The datasheet (Figure 9-11) shows a layout example. Based on comments posted by a TI applications engineer in the TI forum, the FLT pin may be vulnerable to stray coupling to the OVP pin depending on the PCB trace layout so provision should be made for a small capacitor CFLT from the FLT pin to GND to slow down the FLT ramp rate. The recommended capacitor value is 1 nF (this capacitor is not shown in the datasheet but is a known fix for a stray coupling problem on the TPS16412 Evaluation Module).

TPS16412 block diagram:



Document Information

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- 0.1 (1st draft completed 08 Apr 2023)
- 0.2 (Component summary, 11 Apr 2023)
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