RF Switch & Digital Step Attenuator Evaluation

Whitham D. Reeve

This document provides analyses of the RF switches and digital step attenuators used in the existing Rev. G and H ARX and proposed for use in the Rev. I ARX. Refer to the Rev. I ARX System Block Diagram in the Reports folder. Also included is a brief summary of how the RF switches were found and analyzed.

RF switch: The Rev. G ARX used the Macom MASWSS-0115 SPDT reflective switch for the split and reduced bandwidth filters and the Hittite (ADI) HMC245QS16E SP3T absorptive switch for the 3 and 10 MHz HPF. The Rev. H ARX used the Peregrine Semiconductor (pSemi) PE42422 SPDT switch for both the HPF and LPF.

The Rev. I ARX is proposed to use the Analog Devices HMC-194A SPDT and P-Semi PE42540 SP4T switches. See table below for a comparison. The proposed Rev. I switches are shown shaded.

ARX Revision	**Rev. I**	**Rev. I**	**Rev. G**	**Rev. G**	**Rev. H**
Type	**SPDT**	**SP4T**	**SPDT**	**SP3T**	**SPDT**
Parameter	**HMC 194A**	**PE42540**	**MASWSS-0115**	**HMC245QS16E**	**PE42422**
Voltage (V)	3.3 V	3.3 V	3 V	5 V	2.3 – 5 V
Freq Low (MHz)	dc	10 Hz	dc	dc	dc
Freq Hi (MHz)	3 GHz	8 GHz	3 GHz	3.5 GHz	6 GHz
IL (dB)	0.5/0.9 max	0.80/1.1 max	0.25/0.40 max	0.70/1.0 max	0.23 typ
ISO (dB)	50 min/55	45/40 min	20 min	46/40 min	68 typ
RL (dB)	26 typ	23 typ	20 typ	23 typ	33 typ
1 dB (dBm)	24 min28 typ	33/31 min	21/25 typ	29/26 min	33 typ
IP2 (dBm)	N/A	100 typ	90 typ	N/A	96/105 typ
IP3 (dBm)	40 min/53 typ	58 typ	45 typ	48/44 min	75/81 typ
Cost (100 pc)	$3.28	$9.35	$1.10	$7.19	$1.61

An important concern is the switch performance under high power conditions including the 1 dB compression and 2nd and 3rd order intercept points. The proposed HMC-194A SPDT LPF switches are located prior to any amplification so are subject only to relatively low RF levels. The 1 dB compression point at the output of the 1st stage amplifier is +18 dBm. With an amplifier gain of 25 dB, the input would be –7 dBm for 1 dB compression. The HMC-194A SPDT switch has a minimum margin of 31 dB above this level. The GALI-74+ amplifier used in all three stages has IP3 of +38 dBm (IP2 is not specified for this amplifier). Since the amplifier IP3 is at least 2 dB lower than switch IP3, the amplifier IP3 controls.

The proposed PE42540 SP4T HPF switches are located after the 1st amplifier stage and between the 2nd digital step attenuator and the 2nd amplifier stage. Assuming the attenuator is set to 0 dB, the output of the 1st amplifier stage will be +18 dBm at its 1 dB compression point. The PE42540 SP4T switch has a minimum1 dB compression point of 31 dB, in which case the margin is 13 dB. As with IP3 above, the amplifier IP3 controls.

The relatively high gain of the receiver stages and the ability to control the attenuation in 0.5 dB steps with the digital step attenuators reduces the effects of the switch insertion losses. The cascade of two SPDT and two SP4T switches will have a maximum insertion loss of 4.0 dB.

Another important consideration is isolation between poles of the switches. High isolation is considered desirable to minimize interaction between the filters. The minimum isolation of the selected switches is 40 dB for the PE42540 and 50 dB for the HMC-194A. Return losses of the proposed switches are above 20 dB. The proposed switches are compatible with the Rev. I ARX 3.3 V bus voltage.

The total cost of a set of SPDT and SP4T switches (HMC-194A and PE42540), 2 of each switch in each ARX channel, in 100 pc quantity is $25.26.

Analyses of the RF switches proceeded as follows: The websites of the known RF switch manufacturers were searched for suitable products. The manufacturers were Analog Devices (Hittite), Macom, Mini-Circuits, and pSemi (Perregrine Semiconductor). Other manufacturers were found on distributor websites (Mouser and Digi-Key) but none met the basic requirements.

The basic requirements, in order of search filtering, were low frequency (0 to 3 MHz), operating and control voltage (3 V single supply voltage), and minimum isolation (≥ 30 dB). Some switches have a recommended supply or control voltage of 3.3 V, and I assume this can be accommodated by increasing the 3 V bus to 3.3 V. Many switches were found that require a 5 V single supply voltage, dual supply voltages (+ and -) or a negative single supply voltage, but these all were rejected. Switch packaging or parameters not shown on the spreadsheet were not used in the searches.

After filtering the results for the basic requirements, the insertion loss, cost and other parameters were tabulated. Approximately 16 SPDT switches and 4 SP4T switches were found by this method. With some exceptions, the datasheets generally specified the isolation parameter at frequencies ≥ 1 GHz or from 0 to 1 GHZ or 0 to 2.5 GHz and not specifically at the lower frequencies of interest (< 100 MHz).

The isolation vs frequency plots for some switches with isolation < 30 dB also were viewed. Some switches in this category had much higher isolation at the lower frequencies but most plots showed little detail or were useless below 500 MHz. Also, these plots were typical and not minimum.

The difference between typical and minimum is on the order of 10 dB, more or less, but this can vary with the manufacturer and product. This means that the switch isolation at the frequencies of interest becomes somewhat subjective and generally best verified by a manufacturer's evaluation module or board. However, due to cost, availability and the time required to design and perform evaluation tests, I did not do this for any of the RF switches.

Addendum added 30 Jan 2024 for RF switch modifications:
The filter output switches are rotated 180° with respect to the input switches on the PCB. To prevent crossing the filter RF traces and having to use vias, the ports to which the filters are connected on the output are not one-to-one; that is, the filter on RF1 on the input switch is not connected through a filter to RF1 on the output switch. Instead, the filter on RF1 on the input switch is connected through a filter to RF2 on the output switch, and so on. This required changes in the truth tables for the output switch shown below.

SPDT RF Switch ADI HMC194A Logic

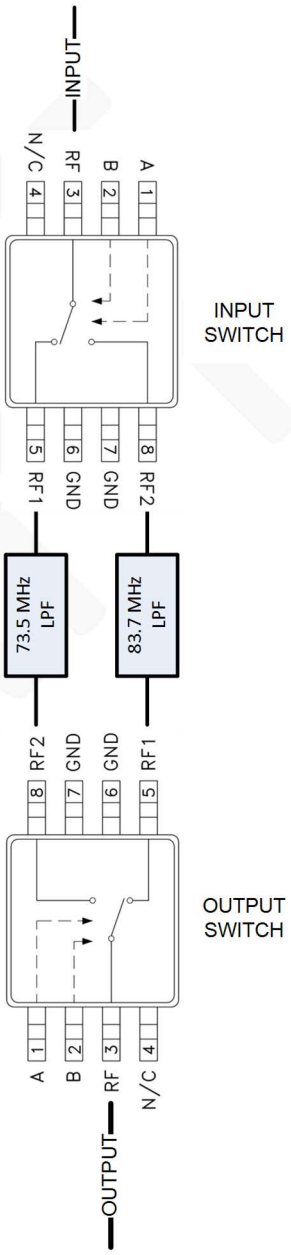
Table 1 ~ Original logic:

Direction	A B	Switch
IN 73.5 MHz	0 1	RF1 – IN
OUT 73.5 MHz	0 1	RF1 – OUT
IN 83.7 MHz	1 0	RF2 – IN
OUT 83.7 MHz	1 0	RF2 – OUT

Table 2 ~ Inverted logic:

A & B reversed on output switch

Direction	A B (orig)	Switch
IN 73.5 MHz	0 1 (0 1)	RF1 – IN
OUT 73.5 MHz	1 0 (0 1)	RF2 – OUT
IN 83.7 MHz	1 0 (1 0)	RF2 – IN
OUT 83.7 MHz	0 1 (1 0)	RF1 – OUT



SP4T RF Switch P-Semi 42540 Logic

Table 1 ~ Original logic:

Direction	V1 V2	Switch
IN 3 MHz	0 0	RF1 – IN
OUT 3 MHz	0 0	RF1 – OUT
IN 10 MHz	1 0	RF2 – IN
OUT 10 MHz	1 0	RF2 – OUT
IN 20 MHz	0 1	RF3 – IN
OUT 20 MHz	0 1	RF3 – OUT
IN 30 MHz	1 1	RF4 – IN
OUT 30 MHz	1 1	RF4 – OUT

Table 2 ~ Inverted logic:
V1 inverted on output switch

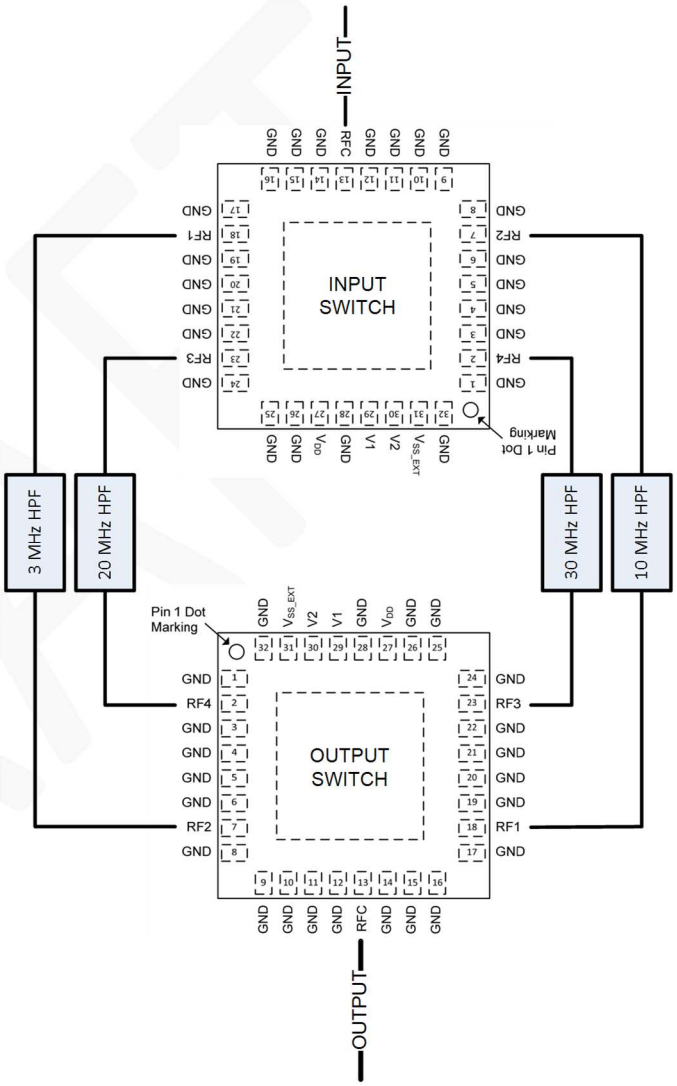
Direction	V1 V2 (orig)	Switch
IN 3 MHz	0 0 (0 0)	RF1 – IN
OUT 3 MHz	1 0 (0 0)	RF2 – OUT
IN 10 MHz	1 0 (1 0)	RF2 – IN
OUT 10 MHz	0 0 (1 0)	RF1 – OUT
IN 20 MHz	0 1 (0 1)	RF3 – IN
OUT 20 MHz	1 1 (0 1)	RF4 – OUT
IN 30 MHz	1 1 (1 1)	RF4 – IN
OUT 30 MHz	0 1 (1 1)	RF3 – OUT

Table 3 ~ Inverted logic:
V2 inverted on output switch only

Direction	V1 V2 (orig)	Switch
IN 3 MHz	0 0 (0 0)	RF1 – IN
OUT 3 MHz	0 1 (0 0)	RF3 – OUT
IN 10 MHz	0 1 (0 1)	RF3 – IN
OUT 10 MHz	0 0 (0 1)	RF1 – OUT
IN 20 MHz	1 0 (1 0)	RF2 – IN
OUT 20 MHz	1 1 (1 0)	RF4 – OUT
IN 30 MHz	1 1 (1 1)	RF4 – IN
OUT 30 MHz	1 0 (1 1)	RF2 - OUT

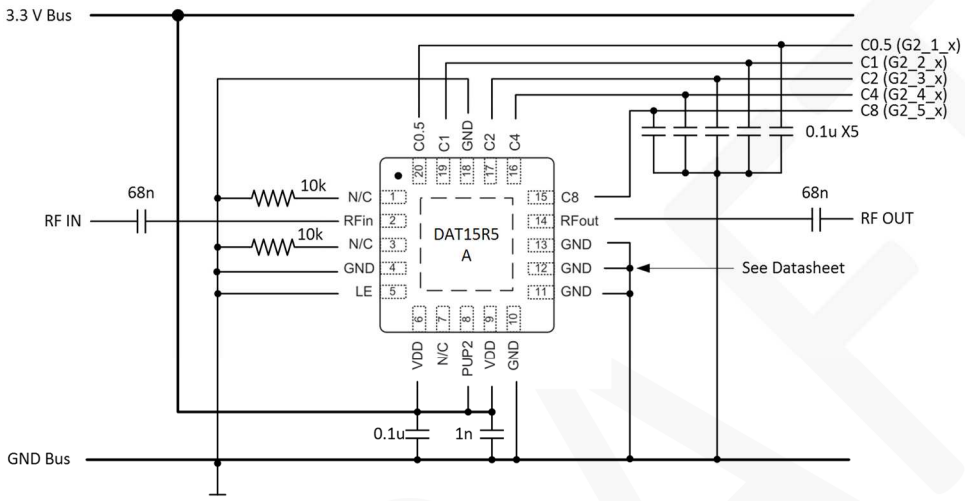
Table 4 ~ Inverted logic:
V1 & V2 inverted on output switch

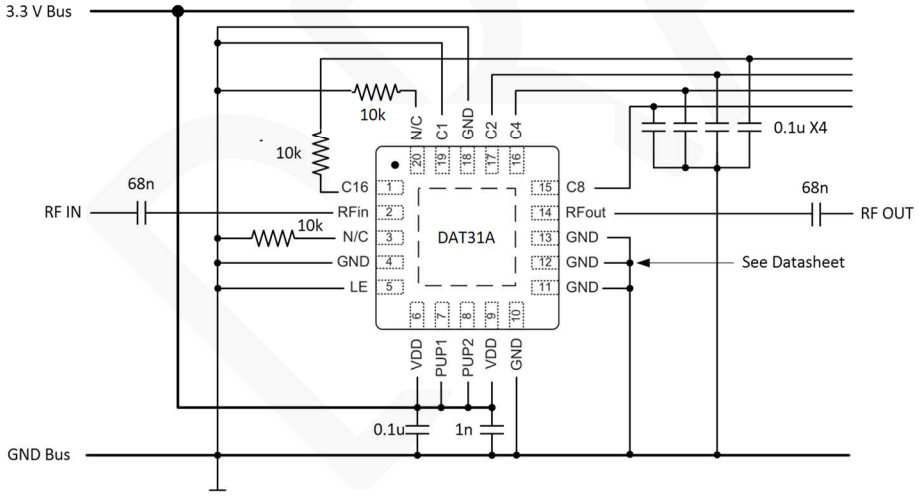
Direction	V1 V2 (orig)	Switch
IN 3 MHz	0 0 (0 0)	RF1 – IN
OUT 3 MHz	1 1 (0 0)	RF4 – OUT
IN 10 MHz	0 1 (0 1)	RF3 – IN
OUT 10 MHz	1 0 (0 1)	RF2 – OUT
IN 20 MHz	1 0 (1 0)	RF2 – IN
OUT 20 MHz	0 1 (1 0)	RF3 – OUT
IN 30 MHz	1 1 (1 1)	RF4 – IN
OUT 30 MHz	0 0 (1 1)	RF1 – OUT



Digital step attenuator: The Rev. G ARX used the Mini-Circuits (MCL) DAT-31A-PP+, 5 bit, 0 – 31 dB attenuators but only 4 bits were used for control, giving a 2 dB resolution. The Rev. H ARX used the Hittite HMC472ALP4E, 6 bit, 0 – 31.5 dB attenuators. The Rev. I ARX will use the DAT-31A-PP+, 5 bit, 0 – 31 dB attenuator for positions AT1 and AT2 and the DAT-15R5A-PP+, 5 bit, 0 – 15.5 dB attenuator for the third position AT3. AT1 and AT2 will continue using 4 bits for control, while AT3 will use all 5 bits for control, the latter providing 0.5 dB resolution. The MCL DAT-series attenuators are well proven in the Rev. G ARX and no special analysis is undertaken here.

Wiring and connection considerations taken from the MCL datasheets are shown below.





Document Information

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0.1 (Minor edits for clarity, 24 Apr 2023)
0.2 (Updated SPDT to HMC-194A and SP4T to PE42540, added attenuator schematics, 29 Sep 2023)
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