Logic & Monitoring Components Evaluation

This document provides analyses of the logic components used in the existing Rev. G and H ARX and proposed for use in the Rev. I ARX. Refer to the Rev. I ARX block diagram for reference (see Reports folder).

Logic components: Because of the need for compatibility with the existing control system and associated software, the control logic for the Rev. I ARX is almost identical to that used in the Rev. G ARX. The Rev. H logic is considerably different but does include useful monitoring functions, which are adopted as described in the next section below.

The Rev. G ARX uses the 4-wire Serial Peripheral Interface (SPI) to control eight 20-port I/O expander integrated circuits (IC, MAX7301) through a buffer/driver IC (74LVC16244A). Each I/O expander controls the two polarizations A and B of an antenna stand, thus controlling 16 receiver channels on each ARX PCB. This basic configuration is adopted without change.

The Rev. G ARX used only 18 of the 20 ports on the I/O expander. These unused ports are used in the Rev. I ARX to add some control functionality, specifically 0.5 dB attenuator resolution (attenuator AT3 only) and an ARX board identification LED. The latter provides a flashing LED that may be used to identify the ARX board associated with a certain antenna stand or other function common to a single ARX PCB.

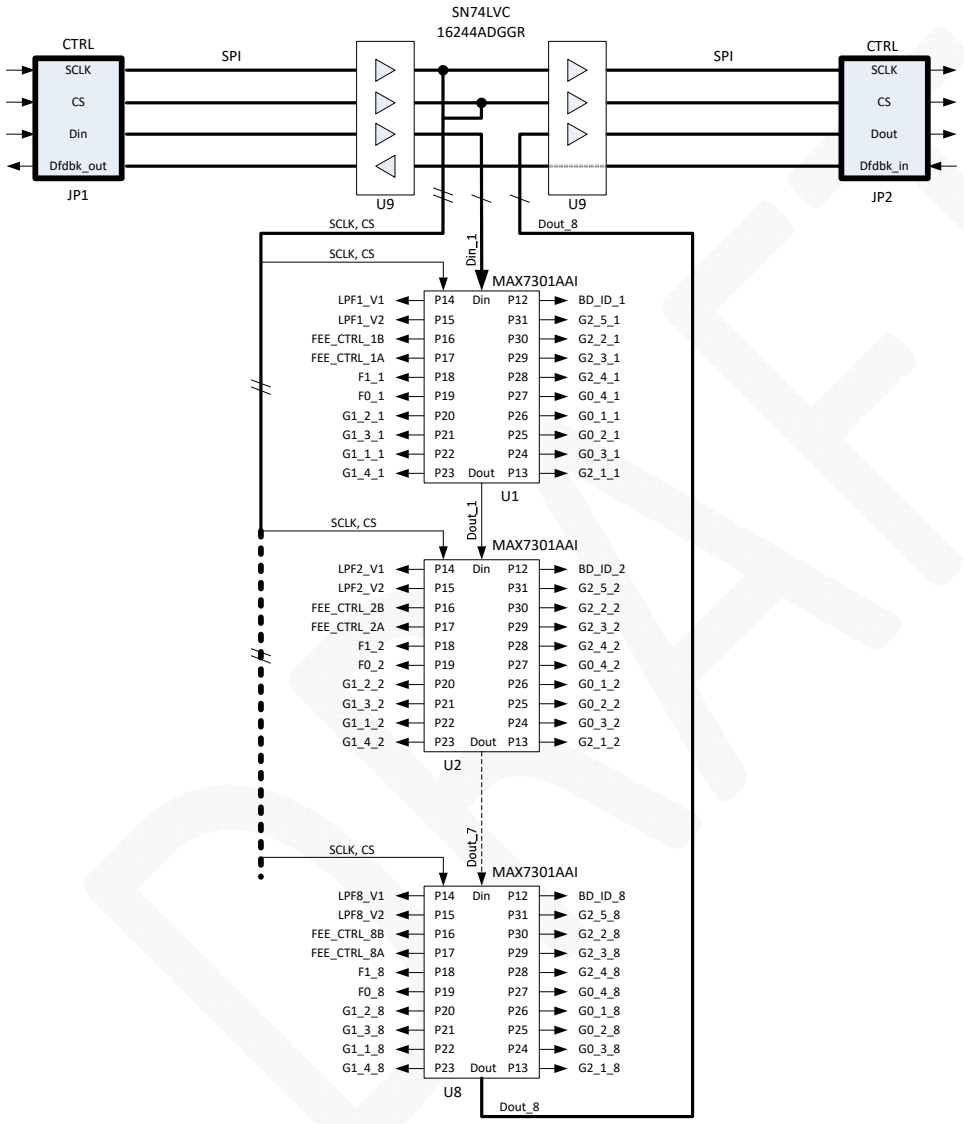
All switches and attenuators, except the HPF filter bank switches, are controlled by a dedicated port on the I/O expander. The HPF filter bank switches use four control pins, one for each position of the SP4T switch, so a 74LVC139 dual 2-4 line decoder is used to derive the four control lines from 2 control bits. Each decoder IC controls two channels.

The port assignments on the first I/O expander in the Rev. I ARX are shown in the table below (note that the ports/pins on the 20-port I/O expander are designated P12 – P31). The assignments are incremented for each additional I/O expander.

Pin	Assignment	Function
P12	BD_ID_1	Board Identification
P13	G2_1_1	Gain Cont. Atten. AT3 C0.5
P14	LPF1_V1	SPDT Pin 1
P15	LPF1_V2	SPDT Pin 2
P16	FEE_CTRL_1B	FEE Pwr Cont. 1B
P17	FEE_CTRL_1A	FEE Pwr Cont. 1A
P18	F1_1	SP4T Bin. Dec. Pin 1
P19	F0_1	SP4T Bin. Dec. Pin 2
P20	G1_2_1	Gain Cont. Atten. AT2 C4
P21	G1_3_1	Gain Cont. Atten. AT2 C8
P22	G1_1_1	Gain Cont. Atten. AT2 C2
P23	G1_4_1	Gain Cont. Atten. AT2 C16
P24	G0_3_1	Gain Cont. Atten. AT1 C8
P25	G0_2_1	Gain Cont. Atten. AT1 C4
P26	G0_1_1	Gain Cont. Atten. AT1 C2

P27	G0_4_1	Gain Cont. Atten. AT1 C16
P28	G2_4_1	Gain Cont. Atten. AT3 C4
P29	G2_3_1	Gain Cont. Atten. AT3 C2
P30	G2_2_1	Gain Cont. Atten. AT3 C1
P31	G2_5_1	Gain Cont. Atten. AT3 C8

The block diagram below shows the SPI and I/O expander hierarchy for the Rev. I ARX.



Truth tables:

TPS16412 : FEE power controller

Table 1. Truth Table : Positive logic: 0 = 0 V; 1 = +3 V

State	On	Off
Control	1	0

DAT-31A-PP+ : Attenuator

Truth Table : Positive logic: 0 = 0 V; 1 = +3 V

Attenuation	C16	C8	C4	C2	C1
Reference	0	0	0	0	0
1 (dB)	0	0	0	0	1
2 (dB)	0	0	0	1	0
4 (dB)	0	0	1	0	0
8 (dB)	0	1	0	0	0
16 (dB)	1	0	0	0	0
31 (dB)	1	1	1	1	1

Note: Not all 32 possible combinations of C1 - C16 are shown in table

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DAT-15R5A-PP+ : Attenuator:

Truth Table : Positive logic: 0 = 0 V; 1 = +3 V

Attenuation	C8	C4	C2	C1	C0.5
Reference	0	0	0	0	0
0.5 (dB)	0	0	0	0	1
1 (dB)	0	0	0	1	0
2 (dB)	0	0	1	0	0
4 (dB)	0	1	0	0	0
8 (dB)	1	0	0	0	0
15.5 (dB)	1	1	1	1	1

Note: Not all 32 possible combinations of C0.5 - C8 are shown in table

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HMC194A : SPDT RF switch for LPF:

Truth Table : Positive logic: 0 = 0 V; 1 = +3 V

Control		RF Path	
A	B	RF – RF1	RF – RF2
0	1	ON	OFF
1	0	OFF	ON
		70 MHz	80 MHz

PE42540 : SP4T RF switch for HPF:

Truth Table : Positive logic: 0 = 0 V; 1 = +3 V

Control		RF Path			
V1	V2	RF – RF1	RF – RF2	RF – RF3	RF – RF4
0	0	ON	OFF	OFF	OFF
1	0	OFF	ON	OFF	OFF
0	1	OFF	OFF	ON	OFF
1	1	OFF	OFF	OFF	ON
		3 MHz	10 MHz	20 MHz	30 MHz

Document Information

Author: Whitham D. Reeve

Revisions: 0.0 (Original draft started, 23 Apr 2023)
0.1 (Updated Rev. H control, 25 Apr 2023)
0.2 (Added truth tables, 29 Apr 2023)
0.3 (Updated monitoring for board temperature, 30 Apr 2023)
0.4 (Truth table check, 19 May 2023)
0.5 (Removed system block diagram, moved Monitoring section to a separate document, 29 Sep 2023)

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