Comparison of ARX Rev. H and Rev. G and I Impedance Matching Networks

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Comparisons: The "Impedance Matching at ARX Coax Inputs" report from CIT for the Rev. H ARX discusses the attempts to optimize the matching of the receiver RF input circuits to the outside plant. It appears there are several important differences between the resulting Rev. H RF input design and the Rev. G and I designs with respect to impedance matching. The designs are compared below as determined from the report and Rev. H ARX schematic. Some aspects of the Rev. H ARX schematic differ from the report, so the information below may not be complete.

1. The Rev. H ARX uses an "isolated" ground for RF circuitry, which is separate from the power and logic ground, whereas the Rev. G and I use a single ground for all circuitry. The "isolated" ground in the Rev. H ARX is tied to the power and logic ground through a 6.8 uH inductor (L18) in parallel with a diode (D4). The characteristics of the inductor and diode and the effects a “split” ground has on the RF input are unknown. Also, the PCB stackup, which defines the layer characteristics of the 4-layer PCB, of the Rev. H ARX is unknown so it is not known if or how ground impedances are controlled. It also is unknown what the physical separation of the two grounds is or how they are configured (except that they are bonded by the inductor/diode as mentioned).

2. The Rev. H bias-tee that couples power to the FEE uses a 10 uH inductor (L1) with 26 MHz self-resonant frequency (SRF) whereas Rev. G uses a 4.7 uH inductor with 90 MHz SRF and Rev. I uses a 10 uH inductor with 165 MHz SRF. The SRF is the frequency where the inductive reactance equals the capacitive reactance of the device. Above the SRF, the device has a capacitive characteristic. In the ARX applications, the bias-tee inductor is a shunt impedance across the RF input. One of the goals of a bias-tee is to make the shunt impedance as high as possible while considering complexity, parts availability and cost. In the Rev. H ARX, the shunt impedance decreases above 26 MHz whereas in the Rev. G and I, the shunt impedance increases with frequency up to 90 MHz (Rev. G) and 165 MHz (Rev. I). A decreasing shunt impedance can complicate impedance matching.

3. The Rev. H ARX RF input has provisions for either coaxial or fiber optic cable feed from the FEE. A 0 ohm resistor (R1 or R2) is used to select one or the other. The Rev. G and I use only a coaxial cable feed. The added circuitry in the Rev. H ARX has an unknown effect on RF performance but the assumption is that the effect is not important.

4. The Rev. H has a transient voltage suppressor (called zener diode D1 in the report) across the input for ESD protection. The initial TVS in the Rev. H ARX had 5 pF maximum shunt capacitance (according to the report) and thus it affected the RF input path impedance matching particularly at higher frequencies. A 5 pF capacitor has 354 ohms reactance at 90 MHz (this would be in parallel with the 50 ohm system impedance). This TVS was replaced with a different part having 0.6 pF *typical* shunt capacitance. The Rev. G uses a transient surge suppressor ON Semi SL15T1G. The Rev. I uses a BAV99LT1G dual switching diode similar to that used in the V2.0 FEE; this device has 1.5 pF maximum capacitance, or 1179 ohms shunt reactance at 90 MHz. The reactance of a capacitor increases with decreasing frequency. An ideal protection device would have 0 capacitance and infinite shunt reactance at all frequencies.

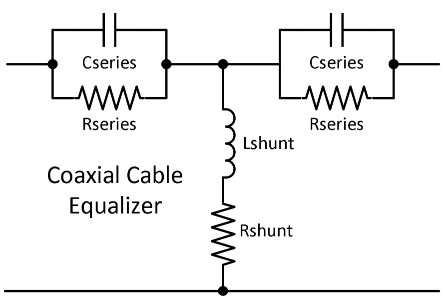
5. The Rev. H ARX has a digital step attenuator after the bias-tee inductor. The attenuator "ACG" (ac ground) pins are connected to the PCB "isolated" ground through capacitors. The initial capacitor values were too small and

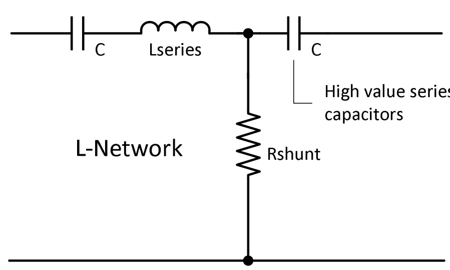
later increased to 0.1 µF to improve the low frequency impedance matching. The combined effects of the ACG capacitors and "isolated" ground are unknown.

6. The Rev. H ARX uses an optional impedance matching network that, according to the report, improved overall impedance matching. The network consists of a 15 nH series inductor (2300 MHz SRF and 300 mA maximum rated current) and a 510 ohm shunt resistor. To limit heat dissipation, the resistor is dc isolated from the bias-tee circuits by 0.1 µF series capacitors on each side of its shunt connection. Ideal 0.1 µF dc isolation capacitors have 0.53 ohms series reactance at 3 MHz. Nothing is known about the characteristics of these capacitors at VHF or about the inductance change of the series inductor when the FEE operating current (about 250 mA) is 83% of the inductor's rated current (300 mA).

<u>ARX Rev. I RF Input</u>: The Rev. I RF input will have optional circuitry, in the form of PCB SMD pads, for an impedance matching network but its exact form needs to be determined by additional work. The CIT report cited above has some outside plant measurements that may be useful. The return loss of the FEE output is quite good (> 20 dB from about 10 to 90 MHz), indicating a good match to the 50 ohm system impedance, so it probably can be assumed that the outside plant and cable entrance panel are the main source of impedance variations.

Impedance matching possibilities are a coaxial cable equalizer network or a simple L-network, the latter is similar to the Rev. H. design (see basic schematics below). It may be possible to layout the PCB to accommodate either network and the SMD pads can be populated as required, but any unused SMD pads will add capacitance to the RF path, which is known to be detrimental to impedance matching at VHF. Any network on the input will be a compromise because of the widely varying cable lengths involved in the LWA.





The cable equalizer is not actually an impedance matching network but is designed to provide decreasing loss with increasing frequency, opposite of a coaxial cable. An L-network made from a series inductor and shunt resistor, as in the Rev. H design, compensates for capacitive reactance in the outside plant and reduces the real part of the impedance (according to the report).

The L-network is the preferred impedance matching method. It is shown in the above schematic with the inductor inside the isolation of high-value coupling capacitors to eliminate inductance changes with FEE load current.

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