ARX Power Evaluation

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This document provides analyses of the voltage regulating components used in the existing Rev. G and H ARX and those proposed for use in the Rev. I ARX. It includes thermal and heat dissipation calculations, a power system block diagram and description of the power supply input protection circuits proposed for the Rev. I ARX.

ARX Input and Bus Voltages:

The Rev. G ARX used 8 Vdc to power all on-board components through separate 3, 5 and 7 V voltage regulators and 15 Vdc to power the Front End Electronics. The 3 and 5 V circuits powered the logic and RF switching circuits and the 7 V circuit powered the GALI-74+ amplifiers. The Rev. H ARX used 5 Vdc for all on-board components including the ABA-54563-BLKG amplifiers and 15 Vdc for the FEE.

To avoid replacing expensive power supplies and maintain compatibility with the existing stations that use the Rev. G ARX, the 8 V and 15 V input voltage buses are unchanged in the Rev. I ARX. To improve the operating margin, the 8 V power supplies are adjusted to 8.8 V for both the Rev. G and Rev. I ARX (but still referred to as the 8 V bus). Additional changes recommended to improve the operating margin are described later.

The 5 V bus is not required in the Rev. I ARX PCB, and the 8 V input to the PCB is stepped down by a linear voltage regulator to 3.3 V for the logic, RF switching and monitoring circuits and to 7.0 V for the amplifiers. Although the amplifier voltage in the Rev. I ARX is the same as the Rev. G ARX, the voltage regulation in Rev. I in combination with the higher input voltage provides overall higher operating margin for the amplifiers.

Altitude Derating:

Thermal and power dissipation calculations are used to determine if a device is able to meet specific application conditions without overheating. In the case of the LWA installations in New Mexico and elsewhere, it is necessary to evaluate the heat dissipation at high altitudes because the thinner air at high altitudes reduces the ability of electronic devices to dissipate heat. The operating altitude of the LWAs in New Mexico is on the order of 7000 ft (2100 m) and the Rev. I ARX will be deployed at sites with altitudes as high as 10 000 ft (3000 m).

Altitude meter	Altitude feet	Derating factor
0	0	1.00
500	1640	0.97
100	3280	0.94
1500	4920	0.91
2000	6560	0.89
2500	8200	0.86
3000	9840	0.83
3500	11480	0.81
4000	13120	0.78

The derating factor for high altitudes is discussed in a Texas Instruments application note (see References) but altitudes only to 8350 ft are listed. However, the TI derating factors are comparable at most altitudes to those given in a design note from Flex Power Modules (FPM) for forced air cooling (see table). The FPM data extends to 13 120 ft.

Note that the FPM derating factors are the inverse of the derating factors used in the calculations. The TI factor for 2100 m (7000 ft) altitude is 1.17 and higher than the (interpolated)

FPM factor for the same altitude, so the TI factor is used for that altitude. The FPM factor is used for 3000 m (9840 ft) altitude and is (1/0.83 =) 1.20.

Thermal Control on a PCB: The thermal calculations described below are based on standard PCB dimensions and layer configurations and using the PCB itself as a heatsink. No external heatsinks are used on the power management devices. To ensure the actual ARX PCB is adequate as a heatsink, the following recommendations from a Texas Instrument Tech-Days presentation (*You Think LDOs are Simple?*, see References) are implemented:

- ✓ Use as much metal (copper) as possible in the areas around the device, on the same layer and the layers below it;
- ✓ The more thermal vias the better for spreading the heat between the different layers;
- ✓ Place the largest possible array of thermal vias in the thermal pad to maximize the amount of heat that can be transferred from the device to the internal and bottom layers;
- ✓ A 6x6 via array allows the internal layers to dissipate heat almost as well as the top layer which may be crowded with other components;
- ✓ Make vias as small as possible to decrease the amount of open space in the via hole;
- ✓ If the power pad is too small to place many vias, then placing extra vias as close as possible to the power pad is still helpful.

Logic and Control Power Bus:

Voltage: All logic and control devices are selected to operate at 3.3 V.

3.3 V Bus Load: The load on the 3.3 V bus consists of the following integrated circuits; all loads are estimated:

Type	Qty per PCB	Unit load (mA)	Total load per PCB (mA)
DAT-31A-PP+ digital step attenuator	16 x 2 = 32	0.230	7.36
DAT-15R5A-PP+ digital step attenuator	16 x 1 = 16	0.230	3.68
MAX7301AAI I/O expander	16 x 1/2 = 8	0.270	2.16
74LVC16244ADGGR buffer/driver	16 x 1/16 = 1	24	24.0
HMC194A LPF switch	16 x 2 = 32	0.05	1.60
PE42540 HPF switch	16 x 2 = 32	0.160	5.12
Diagnostics microprocessor	1	?	25 (guess)
Diagnostics support ICs	?	?	5 (guess)
AD8361 RF power detector	16	1.1	17.6
		Total	91.64

The 3.3 V bus design load of 92 mA is increased to 200 mA to account for the uncertainty in the diagnostic components and to provide some margin. The performance requirements in terms of line and load regulation and dropout voltage for the 3.3 V voltage regulator are not critical.

Voltage Regulator Device 3.3 V Bus: The Texas Instruments TLV1117 LDO regulator with fixed 3.3 V output (TLV1117-33xxx) was evaluated to power the 3.3 V bus but its thermal characteristics turned out to be unsuitable for the load conditions. The Rohm BDxxC0A-C series was then evaluated and the BD33C0AFP with fixed 3.3 V output and TO252-3 package was selected. The maximum recommended input voltage is 26.5 V, maximum

output current is 1 A and maximum dropout voltage is 0.5 V. In the ARX application, the input voltage is 8.8 V and load current is estimated 200 mA maximum (see above).

3.3 V Bus Thermal Calculations: The estimated thermal performance is based on the junction-to-air (also referred to as junction-to-ambient) thermal resistance $R_{\theta JA}$. According to the datasheet, $R_{\theta JA}$ = 23 °C/W for the TO252-3 package. The maximum allowable junction temperature is 125 °C, and the quiescent current (called circuit current in the Rohm datasheet, see References) for the BD33C0AFP can be as high as 2.5 mA.

The power that can be dissipated P_d by the device must be ≥ the power consumed P_c by the device. The power consumed is

$$P_c = (V_{IN} - V_{OUT}) \cdot I_{OUT} + V_{IN} \cdot I_q$$

where V_{IN} and V_{OUT} are the input and output voltages (V), I_{OUT} is the load current (A) and I_q is the voltage regulator quiescent current (A). For the BD33C0AFP in this application, V_{IN} = 8.8 V, V_{OUT} = 3.3 V, I_q = 2.5 mA, and

$$P_c = (V_{IN} - V_{OUT}) \cdot I_{OUT} + (V_{IN} \cdot I_q) = (8.8 - 3.3) \cdot 0.2 + (8.8 \cdot 0.0025) = 1.12 \text{ W}$$

The maximum power dissipation at sea level is

$$P_d = \frac{T_J - T_a}{R_{\theta JA}}$$

where T_J is the junction temperature (125 °C) and T_a is the ambient temperature. Assuming an operational maximum ambient temperature of 85 °C, the maximum power dissipation at sea level is

$$P_d = \frac{T_J - T_a}{R_{\theta JA}} = \frac{125 - 85}{23} = 1.74 \text{ W}$$

The maximum power dissipation at sea level is reduced by the factors 1.17 and 1.20 for 2100 and 3000 m altitudes, respectively. With these factors, the maximum power dissipation P_d = 1.74/1.17 = 1.49 W at 2100 m altitude and P_d = 1.74/1.20 = 1.45 W at 3000 m altitude. Therefore, $P_d > P_c$ (1.12 W) and, under the stated conditions, the BD33C0AFP device meets the thermal requirements.

Equivalent Series Resistance for 3.3 V Regulator Input and Output Capacitors: The datasheet for the BC33C0AFP regulator recommends X5R or X7R dielectrics when ceramic capacitors are used on the output and that the ESR be controlled on both the input and output capacitors. These input and output capacitor values and series resistors for ESR are To Be Determined. See Operation Note 15 in the datasheet and Rohm application note *BAxxCC0 Series Circuit Using a Ceramic Output Capacitor* listed in the References.

Amplifier Power Bus:

Voltage: As discussed below, the voltage regulators for 7.0 V amplifier power bus in the Rev. G ARX had no margin. The Rev. I ARX uses the same amplifiers. Each receiver channel uses three amplifiers, and each amplifier presents a nominal load of 80 mA giving a total load of 240 mA in each receiver channel. The Rev. G ARX PCB

used two LM1084 voltage regulators, and the load was split with 8 receiver channels on each regulator. Thus, the design load on each Rev. G voltage regulator was 8 x 0.24 A = 1.92 A.

Rev. G ARX PCB Power Dissipation: Neglecting the 3.3 V and 5.0 V loads and only considering the 7.0 V amplifier loads:

The total amplifier load current on each Rev. G PCB is 2 x 1.92 A = 3.84 A. The total power consumed by the amplifiers including bias resistors is 7.0 V x 3.84 A = 26.9 W.

Each voltage regulator has a quiescent current of 10 mA. Power losses in the two voltage regulators assuming 8.0 V input and 7.0 V output are (1.0 V x 3.84 A) + (1.0 V x 0.01 A x 2) = 3.86 W.

The total power input per PCB is 26.9 W + 3.9 W = 30.8 W, and the total input current is 30.8 W/8.0 V = 3.85 A/PCB.

8.0 V Input Bus Voltage Drop: Per Zoom meeting of 5 Sep 2023, the ARX power cables are 12 or 14 AWG (not sure which), lengths are approx. 5 ft and each cable serves 4 ARX PCBs. Therefore, the load per power wiring circuit cable is 4 PCBs x 3.85 A/PCB = 15.4 A. This value does not include current to the 3.3 and 5.0 V circuits on the Rev. G ARX PCB.

The power wiring is assumed to be tinned 19 strand/27 AWG, 14 AWG copper or tinned 19 strand/25 AWG, 12 AWG copper. Looking first at 14 AWG as worst-case:

The dc resistance at 20 °C for tinned, 19 strand/27 AWG, 14 AWG copper wire is 3.05 ohms/1000 ft. The loop length is 10 ft, giving a loop resistance of 0.0305 ohms. The voltage drop in the power wiring at 20 °C is 15.4 A x 0.0305 ohms = 0.47 V. Since the station runs hotter than 20 °C, the wire resistance will be somewhat higher, and the voltage drop also will be somewhat higher. Assuming the wire temperature is 40 °C (104 °F), the resistance will be 0.0329 and the voltage drop will be 15.4 A x 0.0329 ohms = 0.51 V. For reference, the calculation of copper wire resistance as a function of temperature is:

$$R_T = R_{ref} \cdot \left[1 + \alpha \cdot \left(T - T_{ref} \right) \right]$$

where R_T is the wire resistance at any temperature T, R_{Ref} is the resistance at the reference temperature T_{Ref}, and α is the temperature coefficient of resistance. For copper, α = 0.004 / °C at practical operating temperatures. T_{Ref} is given in copper wire properties tables (usually 20 °C) along with R_{Ref}.

Considering power wiring voltage drop at the assumed 40 °C operating temperatures, the input voltage to the Rev. G PCBs is not 8.0 V but closer to 7.5 V. The typical dropout voltage of the LM1084 is 1.0 V and can be as high as 1.5 V. Thus, with 8.0 V input voltage, the voltage regulators under worst-case conditions deliver around 6 V, which is considerably lower than the Rev. G design voltage of 7.0 V at the amplifier bias circuits. If the 3.3 V and 5.0 V loads are taken into account, the situation is worse because of the additional voltage drop in the power wiring circuit cables due to those load currents.

Increasing Power Wiring Size to 12 AWG: The dc resistance at 20 °C for tinned 19 strand/25 AWG, 12 AWG copper wire is 1.87 ohms/1000 ft and at 40 °C is 2.0196 ohms/1000 ft. The loop resistance for 10 ft loop length is 0.0187 and 0.020196 ohms, respectively. The voltage drop for a 15.4 A load is 15.4 A x 0.0187 ohms = 0.29 V at 20 °C and 15.4 A x 0.020196 = 0.31 V at 40 °C. Although the voltage drop is lower, the LM1084 voltage regulators are still starved in terms of input voltage as shown below.

ARX Rev. I Scenario 1 – Linear Technology LM1084 LDO Voltage Regulator: If the power supply output voltage is 8.0 V, then, as shown above, the voltage at the PCB with 14 AWG power wiring is 8.0 V – 0.51 V = 7.5 V and with 12 AWG power wiring is 8.0 V – 0.31 V = 7.7 V, both at 40 °C. The LM1084 regulator has a maximum 1.5 V dropout voltage under all conditions. For the worst-case with 14 AWG wiring, the LM1084 output will be 7.5 V – 1.5 V = 6.0 V, and with 12 AWG wiring will be 7.7 V – 1.5 V = 6.2 V. Both voltages are far below the required minimum recommended amplifier operating voltage of 7.0 V (see R BIAS table on pg 3 of Mini-Circuits GALI-74+ datasheet).

If the power supply voltage is increased to 8.8 V, the voltage at the PCB with 14 AWG power wiring will be 8.8 V – 0.51 V = 8.3 V and with 12 AWG power wiring is 8.8 V – 0.31 V = 8.5 V, both at 40 °C. For the worst-case with 14 AWG wiring, the LM1084 output will be 8.3 V – 1.5 V = 6.8 V and with 12 AWG wiring will be 8.5 V – 1.5 V = 7.0 V. Even with the elevated input voltage, the 14 AWG power wiring does not meet the design goal of 7.0 V at the amplifiers, whereas the 12 AWG wiring provides the needed voltage but has no margin.

ARX Rev. I Scenario 2 – Rohm BDxxC0Axx LDO Voltage Regulator: The Rohm BDxxC0AFP LDO voltage regulator datasheet specifies a maximum dropout voltage of 0.5 V but recommends an operating input voltage of V_{Out} + 1 V (see Recommended Operating Conditions on pg 7/43 of datasheet). If the power supply voltage is increased to 8.8 V, the voltage at the PCB with 14 AWG power wiring will be 8.8 V – 0.51 V = 8.3 V and with 12 AWG power wiring will be 8.8 V – 0.31 V = 8.5 V, both at 40 °C.

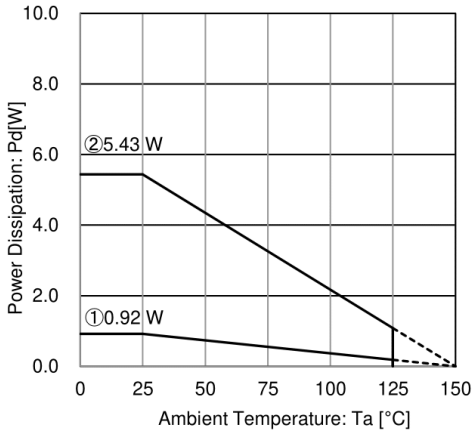
If the LDO output voltage (and the amplifier operating voltage) is supposed to be 8.0 V, the input must be at least 9.0 V, which is not achievable with nominal 8 V power supplies having ±10% adjustment range. However, by reducing the LDO output voltage (and amplifier operating voltage) to 7.0 V, the LDO requires 8.0 V input voltage. This is achievable and provides at least some margin under relatively high temperature conditions (40 °C) with 14 AWG power wiring. Using 12 AWG power wiring, the margin is increased by 0.2 V.

This scenario has been selected and further supported by the following thermal calculations. As mentioned above, the lowest recommended operating voltage for the amplifiers is 7.0 V, which requires an adjustable LDO voltage regulator because 7.0 V is not a standard fixed regulator output voltage. Therefore, for this application, the adjustable BD00C0AWFP in the TO252-5 package will be used.

Thermal Calculations for Rohm BDxxC0A Regulator: As discussed above, the operating altitude of the LWAs in New Mexico is on the order of 7000 ft (2100 m) and future LWAs will be deployed near 10 000 ft (3000 m). At higher altitudes, it is necessary to derate the voltage regulator junction-to-ambient thermal resistance θ_{JA} values determined at sea level (derating makes θ_{JA} values larger and is equivalent to reducing the allowable power

dissipation). The discussion below first calculates sea level conditions and then applies the derating for operation at 7000 ft and 10 000 ft altitudes.

The thermal calculations assume a 4-layer FR4 PCB with two signal and two power (2s2p) layers, TO252-5 package (condition 2 in the plots from the datasheet figure 74 below) and sea level. For these conditions, junction-to-ambient thermal resistance θ_{JA} = 23 °C/W. The maximum device current is 1 A and its maximum dropout voltage is given as 0.5 V but, as mentioned above, Rohm recommends that the device input voltage exceeds the desired output voltage by at least 1 V.



Each Rohm LDO voltage regulator will supply two receiver channels. Each channel contains three amplifiers, giving a total of six amplifiers per voltage regulator. Therefore, the operating current of each LDO will be 6 amplifiers x 0.08 A/amplifier = 0.48 A, rounded to 0.5 A to provide some margin.

The allowable power dissipated P_d must be ≥ the power consumed P_c by the voltage regulator The power consumed is

$$P_c = (V_{IN} - V_{OUT}) \cdot I_{OUT} + V_{IN} \cdot I_q \text{ W}$$

where V_{IN} and V_{OUT} are the input and output voltages (V), I_{OUT} is the load current (A) and I_q is the voltage regulator quiescent (or circuit) current (A). Assuming the BD00C0AWFP is used in this application:

14 AWG power wiring at 40 °C: V_{IN} = 8.3 V, V_{OUT} = 7.0 V, input-output differential = 1.3 V, I_{OUT} =0.5 A, and I_q = 2.5 mA:

$$P_c = (V_{IN} - V_{OUT}) \cdot I_{OUT} + (V_{IN} \cdot I_q) = (8.3 - 7.0) \cdot 0.5 + (8.3 \cdot 0.0025) = 0.671 \text{ W}$$

12 AWG power wiring at 40 °C: V_{IN} = 8.5 V, V_{OUT} = 7.0 V, input-output differential = 1.5 V, I_{OUT} =0.5 A and I_q = 2.5 mA:

$$P_c = (V_{IN} - V_{OUT}) \cdot I_{OUT} + (V_{IN} \cdot I_q) = (8.5 - 7.0) \cdot 0.5 + (8.5 \cdot 0.0025) = 0.771 \text{ W}$$

The maximum power dissipation P_d at sea level is

$$P_d = \left[\frac{(T_J - T_a)}{R_{\theta JA}} \right] \text{W}$$

where T_J is the junction temperature and T_a is the ambient temperature. Assuming a maximum ambient temperature of 85 °C, the maximum power dissipation at sea level is

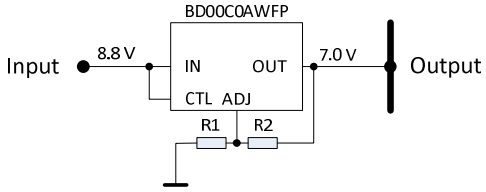
$$P_d = \left[\frac{(125°C - 85°C)}{23} \right] = 1.74 \text{ W}$$

The maximum power dissipation at sea level is reduced by the factors 1.17 and 1.20 for 2100 and 3000 m altitudes, respectively. With these factors, the maximum power dissipation is P_d = 1.74 W/1.17 = 1.49 W at 2100 m altitude and P_d = 1.74 W/1.20 = 1.45 W at 3000 m altitude. Therefore, $P_d > P_c$ (0.671W for 14 AWG wiring and

0.771 W for 12 AWG wiring) and, under the stated conditions, the BD00C0AWFP device meets the thermal requirements.

Equivalent Series Resistance for 7.0 V Regulator Input and Output Capacitors: The datasheet for the BC00C0AWFP regulator recommends X5R or X7R dielectrics when ceramic capacitors are used on the output and that the equivalent series resistance (ESR) be controlled on both the input and output capacitors. These input and output capacitor values and series resistors for ESR are To Be Determined. See *Operation Note 15* in the datasheet and Rohm application note *BAxxCC0 Series Circuit Using a Ceramic Output Capacitor* listed in the References.

Resistive Voltage Divider for Rohm Variable Voltage Regulators: To set the output voltage, the ADJ pin of the BC00C0AWFP voltage regulators is connected to the resistive voltage divider shown below. The designations R1 and R2 are the same as used in the device datasheet.



Output voltage Vout ≈ ADJ × (R1+R2) / R1, where ADJ is the Adjust Terminal Voltage (reference voltage) and R1 and R2 are the voltage divider resistances. According to the datasheet, the ADJ pin, or reference voltage, is typically 0.75 V but can vary from 0.742 to 0.758 V. To limit offset voltage due to the ADJ pin current, the recommended range for R1 is 5k to 10k. Rearranging the output voltage equation for R2 gives R2 = [(Vout x R1) / ADJ] – R1.

For 7.0 V output, the Rohm application note (*Table of resistance for output voltage setting on linear regulator ICs*, see References), Table 1, shows R1 = 8.2k and R2 = 68k. These values assume ADJ = 0.75 V and do not account for possible variations in the ADJ pin voltage. The goal of this design is to not let the amplifier bias voltage go below 7.0 V. If the ADJ pin voltage is worst-case (ADJ = 0.742 V), then R2 = 69.1k. The nearest standard 1% value in size 0805 is 69.8k. However, this does not account for the R1 and R2 resistor tolerances (±1%) and ADJ pin voltage variation.

For worst-case calculations, the nominal value of R1 is assumed to be 8200 ohms (for example, Bourns p/n CR0805-FX-8201ELF). R1 can vary ±82 ohms from 8118 to 8282 ohms due to its tolerance. The worst-case in terms of maintaining at least 7.0 V output voltage is a high value for R1 and a low value for ADJ. For this situation, R2 must be ≥ 69.85k, which is not a standard value. The nearest standard 1% value higher than 69.85k is 71.5k (for example, Bourns p/n CR0805-FX-7152ELF). R2 can vary ±715 ohms from 70 785 to 72 215 ohms due to its tolerance.

The lowest regulator output voltage occurs when R1 is highest, R2 is lowest and ADJ is lowest; in this case, Vout = 7.08 V, which meets the design goal stated above. The highest regulator output voltage occurs when R1 is lowest, R2 is highest and ADJ is highest; in this case, Vout = 7.5 V. When all values are nominal, the regulator output voltage is 7.35 V. All voltages are acceptable for biasing the GALI-74+ amplifiers when it is set for a bias voltage of 7.0 V.

Note: Changes in the voltage divider resistances due to temperature variations are assumed to be smaller than variations due to tolerances. Also, an LDO output voltage = 7.35 V is higher than the nominal output of 7.0 V and implies lower available input margin (the input would have to be 0.35 V higher for 7.35 V output than for 7.0 V

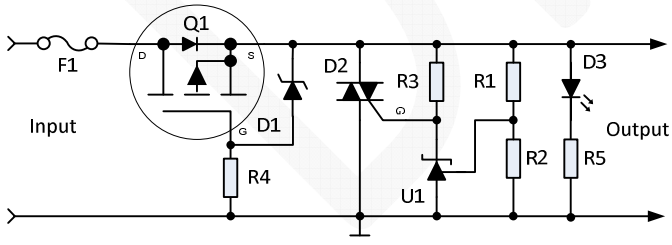
output under worst-case conditions). Although the Rohm datasheet specifies a maximum dropout of 0.5 V, it recommends that the input exceed the output by 1 V, and the 1 V value was used in all the previous voltage drop calculations. Thus, the needed margin is intact with the datasheet maximum dropout voltage.

Voltage Regulator Locations on PCB: It is desirable to locate the 7.0 V voltage regulators so that their power is dissipated uniformly across the PCB. The power dissipation of the eight voltage regulators will be nearly equal, differing mainly due to component tolerances. The goal is to reduce the differences in channel gain due to temperature differentials between receiver channels. This might be achieved by locating each voltage regulator at the top of the PCB directly in line with the two receiver channels it serves.

Increasing the Operating Margin: Upgrading the power wiring from 14 AWG to 12 AWG is recommended to improve the voltage regulator margins. Another improvement is to install remote voltage sensing (also called 4-wire sensing) on the 8 V power supply. The power supply is Artysen model IVS1-5I0-2I0-60-A and, when used with remote voltage sensing, it is able to compensate up to 0.5 V voltage drop in the wiring between the power supply output terminals and load terminals. The load voltage would be sensed, and regulated, at the end of the daisy-chained 8 V power wiring where the sense leads would be connected. Although not analyzed as part of the ARX power evaluation, the 15 V bus also may benefit from remote voltage sensing. This power supply is the Artysen model IVS1-5N0-3N0-60-A.

Input Voltage Protection:

The 8 V and 15 V inputs on the ARX PCB are each equipped with the reverse polarity and overvoltage crowbar circuit shown below. The body diode in MOSFET Q1, Zener diode D1 and R4 provide the reverse polarity guard function. During normal operation, the body diode of the MOSFET is forward-biased and conducts for a very short time until the MOSFET turns on when the gate voltage is pulled below the source voltage. D1 limits the gate-source voltage to a safe value to prevent damage to the MOSFET and R4 limits the current in D1. If the input polarity is reversed, the gate-source voltage is positive with respect to the input and the MOSFET turns off, protecting the downstream circuits from a negative voltage. The MOSFET has very low drain-source resistance when turned on, which provides very low voltage drop across it during normal operation.



R1 and R2 form a voltage divider to set the voltage of the programmable reference U1 to the desired crowbar trip voltage. The intrinsic reference voltage of U1 is 2.5 V. The trip voltage setting for the 8.8 V input is 12 V and for the 15 V input is 20 V. Below the crowbar trip voltage only a very small leakage current flows through R3, producing negligible voltage drop. The gate of Triac D2 is at the bus voltage and remains off. When the input voltage rises to the point where the voltage across R1 increases to 2.5 V (U1 reference voltage), U1 conducts and draws current through R3, which results in a voltage drop and reduced voltage at the gate of D2. When the voltage drop reaches nominal 1 V, Triac D2 turns on and latches and shorts the positive bus to ground. The resulting short circuit current flows through fuse F1, MOSFET Q1 and Triac D2 to ground and opens the fuse.

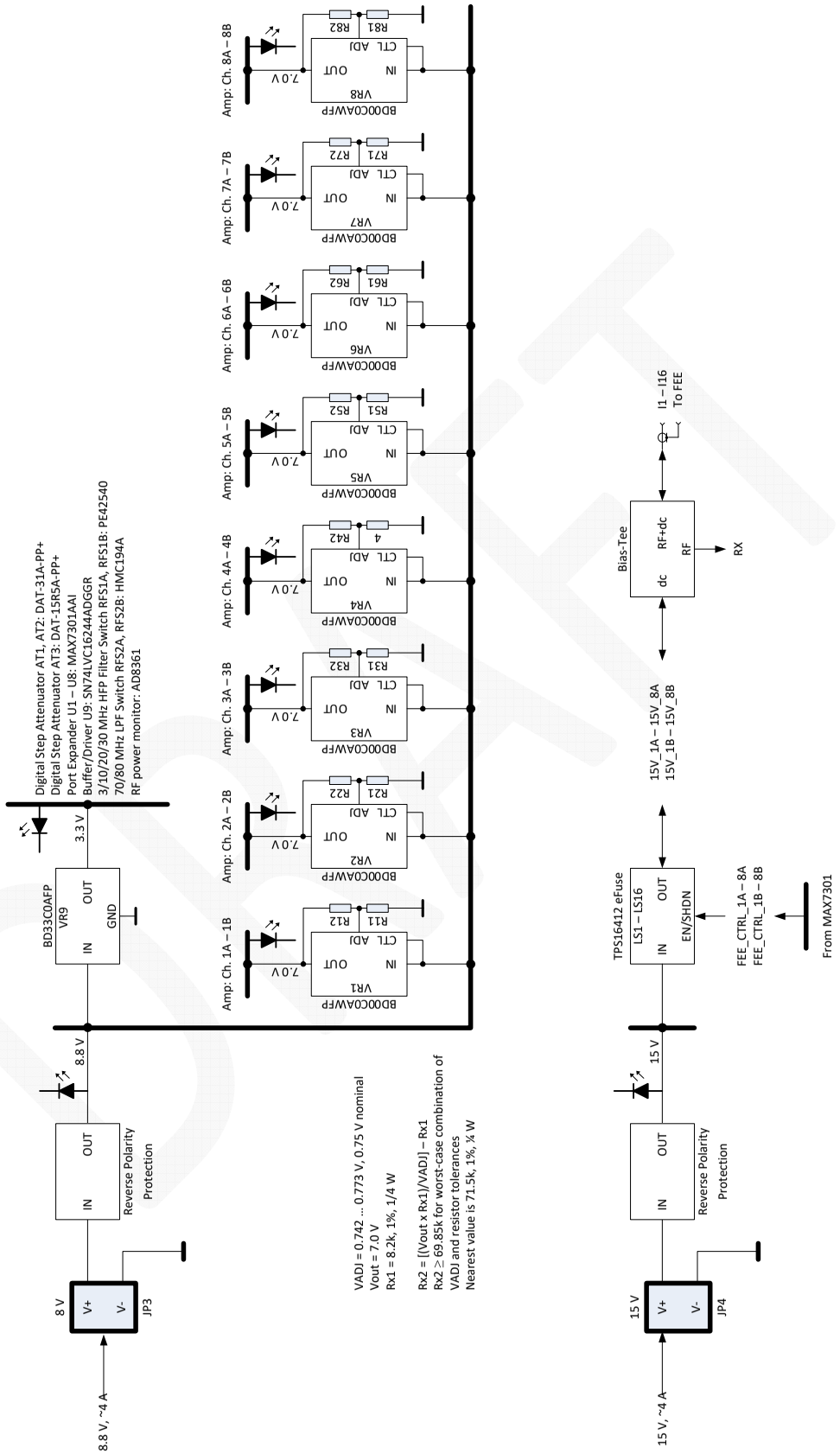
The programmable reference U1 output voltage (at U1 cathode) is

$$V_{Out} = V_{Ref} \cdot \left(1 + \frac{R1}{R2}\right) - I_{Ref} \cdot R1$$

where V_{Out} is the programmable reference output voltage, V_{Ref} is the device reference voltage (2.5 V) and I_{Ref} is the device leakage current (I_{Ref} < 4 µA). For most applications, I_{Ref} is assumed to be zero. R3 is set so that the current into D2 is limited to no more than 5 to 10 mA. The sum of R1 + R2 is in the range of 10 to 15 kOhm or to provide a current on the order of 1 mA. The fuse F1 current rating is 125 to 150% of the nominal load current to prevent nuisance opening. As previously discussed, the nominal load current on the 3.3 V bus is 0.2 A and on the 8 V bus is 8 voltage regulators x 0.5 A/voltage regulator = 4 A. Component values are shown in the table below (blank fields are To Be Determined for each voltage bus, 8 and 15 V).

Designation	**Device**	**8 V Bus**	**15 V Bus**	**Remarks**
F1	Fuse			ATM-series, automotive blade fuse
Q1	P-Channel MOSFET	BSC030P03NS3GAUMA1	BSC030P03NS3GAUMA1	30 V, 100 A, 3 mOhm
D1	Zener diode			
D2	Triac	T3035H-6G	T3035H-6G	D-PAK, 30 A, 35 mA max
D3	LED			Low current
U1	Programmable Ref.	TL431DBZ	TL431DBZ	SOT-23
R1	Resistor			
R2	Resistor			
R3	Resistor			
R4	Resistor			
R5	Resistor			

Power System Block Diagram:



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Document Information

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- 0.0 (Original draft started, 24 Apr 2023)
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- 0.2 (Revised calcs for TO-252-3 voltage regulator, 02 May 2023)
- 0.3 (Completed 1st draft, 03 May 2023)
- 0.4 (Revised 8.0 V bus thermal analysis for 85 °C and 2100 m altitude, 29 Aug 2023)
- 0.5 (Added power block diagram, 3000 m altitude and packaging, 30 Aug 2023)
- 0.6 (Added 3.3 V bus thermal analysis, 03 Sep 2023)
- 0.7 (Added PCB heat dissipation, 04 Sep 2023)
- 0.8 (Replaced most of the section on amplifier bus voltage, 15 Sep 2023)
- 0.9 (Edits and added variable LDO voltage divider resistors, 16 Sep 2023)
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- 1.1 (12 AWG wiring upgrade, remote voltage sensing and LDO location, 19 Sep 2023)
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