Interface Control Document

For: Digital Signal Processing Subsystem (DP)

Status: Version O
2012-10-31

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System Engineering Approval	**Date**
	YYYY-MM-DD
System Architecture Approval	**Date**
	YYYY-MM-DD

Change Record

Version	Date	Affected Section(s)	Reason/Initiation/Remarks
A	2008-12-23	All	Initial Template Draft
B	2009-2-13	All	Draft for PDR Release
C	2009-2-20	1.4, 3.3, 4.6, 6	All references to 256 inputs were replaced with 260 inputs to accommodate the extra 4 inputs of outlier antennas. References updated.
D	2009-2-25	1.3, 2, 4.4, 4.5, 4.6, 4.7, 6	All references to UT replaced with "station time." "MIB Entries" table added. "Suggested Interval" and "Conversion Factor" rows removed from command descriptions. SET_TBW_TRIGGER_TIME and SET_TBW_BITS replaced by SET_TBW_CONFIG. References updated.
E	2009-4-1	2, 4, 5	Extensive changes to Sections 2 and 4. "DP MIB Entries" table modified and expanded. New Section 5.
F	2009-4-6	4.2.2, 4.3.3.6	Increased maximum value of TBW_SAMPLES. Minor changes to CLK and CLK_VAL.
G	2009-4-7	4.2.2, 5.3	Updated Table of Contents. Added T_NOM MIB entries for each DRX_ID. Fixed Figure 4- TBW Output Format.
H	2009-12-21	4.2.2, 4.3.3.2, 4.3.3.4, 4.3.3.6	NUM_STANDS changed to uint16. TBN_BW may have values 1-7. For 520 antennas, number of bytes in BAM command is 3120. CLK_SET_TIME changed to uint32.
I	2010-8-18	Figure 2, Figure 3, Figure 4, 4.3.3.6	DRX, TBN, TBW Output Format figures updated. CLK command no longer necessary. DP will use NTP instead.
J	2010-11-11	4.3.3.2, 5, 5.1, 5.2, 5.3, A.3	TBN_GAIN has a valid range of 0-30. DRX, TBN, and TBW data is signed numbers in two's complement format. DRX, TBN, and TBW time stamps are all with respect to 1970 January 1 00:00 UTC. TBN packets will contain 512 samples. Change DRX Filter 5 from 4,000,000 Hz to 4,900,000 Hz.

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Version	Date	Affected Section(s)	Reason/Initiation/Remarks
K	2011-1-28	2.3, 3.3.3, 4.3.3.2, 4.3.3.3, 5.1, 5.3	Improved description of stand to board mapping in new Table 1. 10 MHz signal rms voltage modified. Correction to TBN_BW math. DRX_BW is unit8. Changes to definition of DRX output format. Improved definition of DRX Time field.
L	2011-5-2	2.3, Figure 1, Table 4, 4.1.1, 4.3.2, 4.3.3.2, 4.3.3.3, 4.3.3.4, 4.3.3.5	Replaced Figure 1- Rack Layout with Figure 1- Board Numbering. Updated T_NOM, ANT_SAT, and BOARD_STAT in Table 4. TBW_STATUS has only two possible values: idle or busy. Added detail about INI command and initialization time. Added detail about DP SUMMARY MIB value if board is missing or calibration delays are not within valid range. Added detail about configuration file. The DP can accept a maximum number of 80 control commands per slot from MCS. Clarification of TBN_GAIN. DRX_GAIN valid range is 0-15. Explicitly stated maximum coarse delay for BAM command. Additional information added about default filter coefficients and reference to BFU0001.
M	2011-5-18	3.1, 4.3.1, 5.1, 7	Removed reference to old Rack Layout diagram. Replaced reference to “DP Error Code Definitions” with explicit information about DP SUMMARY value of ERROR. Replaced TBN_ID reference to Figure 2 with Table 7. Clarified “DP Board Status Specification” reference.

Version	Date	Affected Section(s)	Reason/Initiation/Remarks
N	2011-12-16	4.2, 4.3, 5.1, 5.2	Updated the TBN and DRX frame formats to include the tuning words. Added STP command. Added new MIB entries to describe the current state of the DP system. Updated the TBN command to describe timing limits imposed by the NCO synchronization. Expanded the INI discussion to include how calibration failure affects the transient buffer and beamformer subsystems differently. Added list of command exit codes and subsystem status codes. Clarified the "status/flags" field of the DRX data frame. Check consistency to command arguments.
O	2012-10-31	4.3.3.2	Changed the TBN tuning range to 5 to 93 MHz.

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1 DESCRIPTION

1.1 Purpose

The purpose of this document is to define the interface between the Digital Signal Processing (DP) subsystem and all other subsystems of a Long Wavelength Array (LWA) station. The DP subsystem described here is used to digitize the output of the Analog Receiver (ARX) using the digitizer (DIG), control the wideband and narrowband transient buffers (TBW and TBN, respectively), form beams in the desired direction using each beam forming unit (BFU), and output data for use by other subsystems using each digital receiver (DRX).

1.2 Scope

This document contains lists of software monitor and control points and hardware connections available in the DP subsystem. This document is limited in scope to the interface between the DP subsystem and all other subsystems at a single LWA station.

1.3 Related Documents and Drawings

- MCS Common ICD [1]
- ASP ICD [9]
- Preliminary Design of the Timebase and Clock Distribution (TCD) Subsystem for the LWA [6]
- LWA-1 Data Aggregation & Communications (DAC) Capabilities [8]

1.4 Applicable Documents and Drawings

- Preliminary Design of LWA DP Subsystem [7]
- LWA Station Architecture, Ver. 1.4 [3]
- LWA Memo 154: Preliminary Design for the Digital Processing Subsystem of a Long Wavelength Array Station [4]
- LWA Memo 151: LWA Signal Delays and Time Tagging [5]

1.5 Order of precedence

In the event of conflict between the text of this document and applicable documents, the applicable documents shall take precedence unless explicitly mentioned in this document.

2 ABBREVIATIONS AND ACRONYMS

ARX	Analog Receiver
ASP	Analog Signal Processor
ATCA	Advanced Telecom Computing Architecture
BFU	Beam Forming Unit
DAC	Data Aggregation and Communication

DIG	Digitizer
DP	Digital Signal Processing
DRX	Digital Receiver
LSB	Least Significant Bit
LWA	Long Wavelength Array
MIB	Management Information Base
MCS	Monitor and Control System
MSB	Most Significant Bit
MSPS	Mega-Samples Per Second
TBN	Transient Narrowband Buffer
TBW	Transient Wideband Buffer
TCD	Timebase and Clock Distribution
U	Rack Units (1.75 inches)

2.1 Command Parameter Types

uint8	unsigned integer, 8 bits
sint8	signed integer, 8 bits
uint16	unsigned integer, 16 bits
sint16	signed integer, 16 bits
uint32	unsigned integer, 32 bits
sint32	signed integer, 32 bits
float32	single precision IEEE-754 standard float, big endian
float64	double precision IEEE-754 standard float, big endian

2.2 Fixed Point Number Notation

Fixed point numbers with n total bits and m bits to the right of binary point will be represented as n.m.

Example 1: 16 bit signed, 15 bits after the binary point: (16.15)
Represent -0.25 as 1.110 000000000000 binary

Example 2: 16 bit unsigned number, 8 bits after binary point: (16.8)
Represent 6.125 as 00000110.00100000 binary

Example 3: 16 bit signed, 15 bits after binary point: (16.15)
Represent 0.625 as 0.101000000000000 binary

2.3 Channel and Board Numbering

Stands are numbered s=1…260. Stand s includes channels 2*(s-1)+1 (X polarization) and 2*(s-1)+2 (Y polarization) and therefore channels are numbered c=1…2*520. Boards are numbered b=1…28 where boards 1 and 15 are DP2s and all other boards are DP1s. Stands to board mapping is shown in Table 1. Beams 1 and 2 are output by board 1 and beams 3 and 4 are output by board 15.

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Table 1: Stand to Board Mapping

Stands	Board	Stands	Board
1-10	2	131-140	16
11-20	3	141-150	17
21-30	4	151-160	18
31-40	5	161-170	19
41-50	6	171-180	20
51-60	7	181-190	21
61-70	8	191-200	22
71-80	9	201-210	23
81-90	10	211-220	24
91-100	11	221-230	25
101-110	12	231-240	26
111-120	13	241-250	27
121-130	14	251-260	28

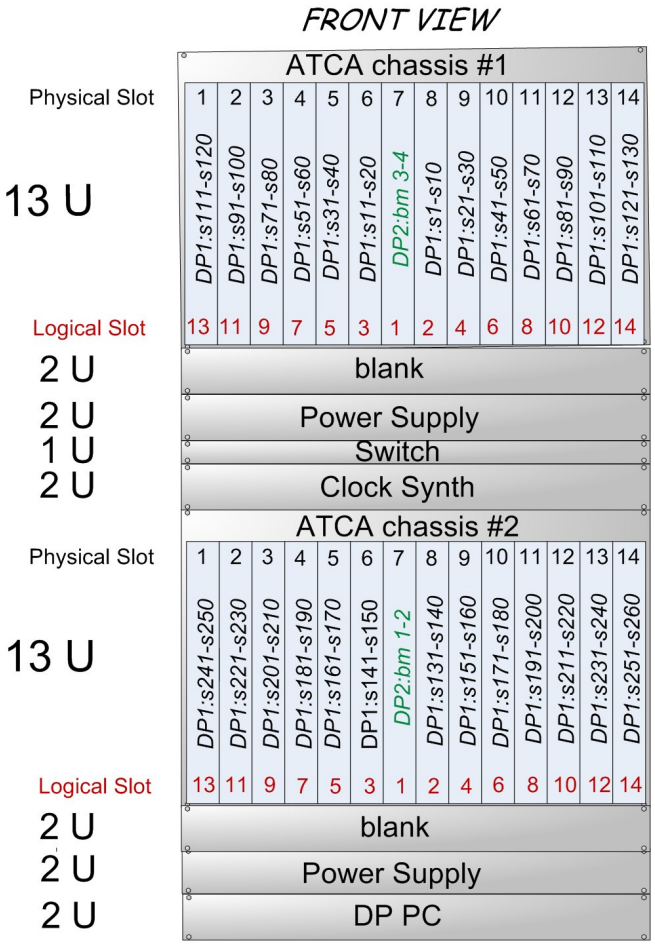

Figure 1: Board Numbering

2.4 Fixed Parameters

Table 2 describes several fixed parameters, the symbols which represent them elsewhere in the document, and their actual values.

Table 2: DP Fixed Parameters

Parameter	Symbol	Value
Signal sampling frequency	f_s	196.0 MHz
Slot Duration (see section 4.3.2)	T	1.0 sec
Sub-slot Duration (see section 4.3.2)	T_2	0.010 sec
Maximum UDP packet size	N_MAX_{UDP}	8192 bytes

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3 PHYSICAL SYSTEM INTERFACES

3.1 Mechanical Interface

The DP subsystem rack will consist of two ATCA chassis, two power supply units, a clock synthesizer, a TBN/TBW switch, and a DP subsystem computer. The total maximum height of the rack is 40 U or 70 inches. The width of the rack is 19 inches.

3.2 Electrical Power Interface

Maximum electrical power usage by the DP will not exceed 4.2 kW. The type of power connectors and type of power required by the DP is 120 VAC and 240 VAC.

3.3 Electronic Interface

3.3.1 List of Connectors

The connections between the DP subsystem and all other subsystems are listed in the table below.

Table 3: List of Connectors

Subsystem	No. of connectors	Type of connector
ASP	130	RJ-45
TCD	1	RJ-45
MCS	1	RJ-45
DAC	4	CX4
DAC	1	CX4

3.3.2 Analog Signal Processor (ASP) Electrical Interface

The connection between the ASP subsystem and the DP subsystem (more specifically, the DIG) will consist of 130 Category 7 (ISO/IEC 11801, class F) cables. Each cable includes 4 individually shielded twisted copper wire pairs which will be used for differential signals from both polarizations of 2 stands. Shielded RJ-45 connectors will be used for each cable. Shielded RJ-45 bulkheads will be used to feed through rack walls.

The impedance of the twisted pairs is 100 Ω. Each differential pair will be terminated in 100 Ω ±1%. The signal level on each differential pair for full scale analog to digital converter (ADC) range will be ±0.71 volts. Absolute maximum signal level will be limited to ±4.0 volts peak.

3.3.3 Timebase and Clock Distribution (TCD) Electrical Interface

The connection between the TCD subsystem and the DP subsystem will consist of 1 Category 7 cable. This cable has 4 individually shielded twisted pairs, 2 of which will be used. Two signals will be sent from the TCD to the DP, a 10 MHz reference and a 1 PPS. The 10 MHz will be considered to be the primary timing reference.

The 10 MHz signal will be a sinusoid with level = 0.707 volts rms across the differential pair.

The 1 PPS signal will have high and low logic levels > 1 μsec long. The rising edge of this signal as registered by the next positive going zero crossing of the 10 MHz will be considered to be the 1 PPS reference time. The setup time of the 1 PPS rising edge with respect to the positive going zero crossing of the 10 MHz will be >10 nsec and the hold time will be >10 nsec. The logic levels of the 1 PPS signal will be LVPECL.

3.3.4 Monitor and Control System (MCS) Electrical Interface

The connection between the Monitor and Control subsystem (MCS) and the DP subsystem will consist of a single 1000BASE-T (full-duplex gigabit Ethernet) connection over Category 6 cable, as specified in the MCS Common ICD [1].

3.3.5 Data Aggregation and Communication (DAC) Electrical Interface

The connection between the Data Aggregation and Communication (DAC) subsystem and the DP subsystem will consist of 4 10GBASE-CX4 (full-duplex 10-gigabit Ethernet) connections for the DRX data and 1 10GBASE-CX4 (full-duplex 10-gigabit Ethernet) connection for the TBN/TBW data.

4 MONITOR/CONTROL INTERFACE

4.1 Overview

The interface between the DP subsystem and the MCS consists entirely of communication between the MCS station computer (or set of computers) and the DP subsystem control computer. This communication will take place via an Ethernet local area private network.

The DP system will be expected to understand and implement low-level commands. The DP system will send monitoring information to MCS only in response to specific requests. Nothing will be sent automatically or spontaneously, even if an error condition is detected.

4.1.1 MCS Interface

Message formats and protocols will conform to the specifications in the MCS Common ICD [1]. Binary DATA field numbers larger than 1 byte are set Most Significant Byte first (big endian). All structures are packed.

The configuration file is located at /lwa/software/defaults.cfg on the DP subsystem control computer. Each line is a whitespace delimited tag/value pair. Tags are case-insensitive.

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4.1.2 Timing

Time will be partitioned into slots of length T, where T is listed in Table 2. Slot boundaries correspond to station time second boundaries. For example, the first slot of the day is from station time (hh:mm:ss) 00:00:00 to 00:00:01. The DP will implement control commands intended for slot N during slot N-1. Therefore, control commands intended for slot N must be received and accepted by the DP subsystem during slot N-2. Slot boundaries are always tied to the slowest distributed hardware timing signal (currently 1 PPS). The slot period T is constrained always to be a rational fraction n/d of the timing signal period, and furthermore every d-th slot boundary must coincide exactly with a specific phase of the timing signal (like its rising edge).

Slots are divided into sub-slots of length T_2, where T_2 is listed in Table 2. Thus, the sub-slots shall be numbered from 0 to 99, with sub-slot 0 at the beginning of the slot. This value of T_2 meets the desired station timing requirement for Minimum Observation Duration [10]. Many commands sent from MCS to the subsystem must specify the sub-slot at which the command shall take effect. The minimum observation length is therefore equal to T_2. The TBW trigger time parameter is independent of T and TBW data capture need not begin on a sub-slot boundary.

4.2 Monitor (RPT) Responses

4.2.1 General Considerations

Monitor data shall be polled by the MCS according to the protocol specified in the MCS Common ICD [1]. Monitor commands are lower priority than control commands and a response can be expected within 3 seconds. The value returned is the one in effect at the time of the response, except as noted. It should be noted that DP-MCS does not currently support branching in MIB indices.

4.2.2 MIB Entries

Table 4: DP MIB Entries

Index	Label	Description	Type	Bytes
2	TBW_STATUS	0 = TBW is idle 4 = TBW is currently recording data or reading out previously recorded data.	uint8	1
3	NUM_TBN_BITS	Number of bits used by TBNs. In the current design, the value of this entry is always 16 (8 bits each for I and Q).	uint8	1
4.1	NUM_DRX_TUNINGS	Number of DRX Tunings. In the current design, the value of this entry is always 2.	uint8	1
4.2	NUM_BEAMS	Number of beams. In the current design, the value of this entry is always 4.	uint8	1
4.3	NUM_STANDS	Number of stands. Typical value is 260.	uint16	2

Index	Label	Description	Type	Bytes
4.4	NUM_BOARDS	Number of boards. Typical value is 28.	uint8	1
4.5	BEAM_FIR_COEFFS	A number between 1 and 32. The actual number of FIR coefficients implemented in hardware. In the current design, the value of this entry is always 28.	uint8	1
4.6	T_NOM	T_{nom} = L from LWA Memo 151 [5], in units of samples at f_s for each BEAM_ID.		
4.6.1	T_NOM1	T_{nom} = L from LWA Memo 151 [5], in units of samples at f_s for BEAM 1.	uint16	2
…				
4.6.4	T_NOM4	T_{nom} = L from LWA Memo 151 [5], in units of samples at f_s for BEAM 4.	uint16	2
5	FIR			
5.1	FIR1	FIR coefficients for the channel specified by FIR_CHAN_INDEX for BEAM1. Format is sint16 coefficients(16,32). The first index is the fractional delay in units of 1/16 sample. The second index is the coefficient number within one filter.	sint16	1024
5.2	FIR2	Same as FIR1 for BEAM2	sint16	1024
5.3	FIR3	Same as FIR1 BEAM3	sint16	1024
5.4	FIR4	Same as FIR1 for BEAM4	sint16	1024
5.5	FIR_CHAN_INDEX	Index to the channel whose filter table is given in 5.1-5.4. Valid values are 1-520. After reading, this value is incremented by one and after 520, this value returns to 1. See Section 2.3 for channel numbering.	uint16	2
6	CLK_VAL	Time at the beginning of the slot immediately preceding receipt of the RPT command, in milliseconds past station time midnight.	uint32	4
7.1	ANT1_STAT	Antenna statistics for Antenna 1		
7.1.1	ANT1_RMS	Root mean square (rms) – This value represents the square root of the mean of the total input power, rms(samples[1:STAT_SAMP_SIZE]) for Antenna 1. This value is dimensionless.	float32	4

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Index	Label	Description	Type	Bytes
7.1.2	ANT1_DCOFFSET	DC Offset – This value represents sum(samples[1:STAT_SAMP_SIZE])/STAT_SAMP_SIZE for Antenna 1.	float32	4
7.1.3	ANT1_SAT	Saturation Count – This value represents in number of A/B saturation events (+/-2,047) seen in samples[1:STAT_SAM_SIZE].	uint32	4
7.1.4	ANT1_PEAK	Peak Count – This value represents the peak A/D value seen in STAT_SAMP_SIZE samples used to compute the antenna statistics. This entry is available for all 520 antennas under the appropriate labels.	uint32	4
7.2	ANT2_STAT	Same as ANT1_STAT for Antenna 2		
7.2.1	ANT2_RMS	Same as ANT1_RMS for Antenna 2	float32	4
7.2.2	ANT2_DCOFFSET	Same as ANT1_OFFSET for Antenna 2	float32	4
7.2.3	ANT2_SAT	Same as ANT1_SAT for Antenna 2	uint32	4
7.2.4	ANT2_PEAK	Same as ANT1_PEAK for Antenna 2	uint32	4
…				
7.52	ANT520_STAT	Same as ANT1_STAT for Antenna 520		
7.520.1	ANT520_RMS	Same as ANT1_RMS for Antenna 520	float32	4
7.520.2	ANT520_DCOFFSET	Same as ANT1_OFFSET for Antenna 520	float32	4
7.520.3	ANT520_SAT	Same as ANT1_SAT for Antenna 520	uint32	4
7.520.4	ANT520_PEAK	Same as ANT1_PEAK for Antenna 520	uint32	4
7.521	STAT_SAMP_SIZE	The number of samples used to calculate Antenna stats. Typical value is 10,000.	uint32	4
8	BOARD_STAT	Board Status Information		
8.1	BOARD1_INFO	Information on Board 1		

Index	Label	Description	Type	Bytes
8.1.1	BOARD1_STAT	Board 1 Status describes the board status, including information about power supply voltages, chip temperatures, and Xilinx DCM locks. A complete specification of the format of this field is given in the DP Board Status Specification [13]. Boards 1-13 are DP1 #1-#13 in chassis 1. Board 14 is DP2 #1 in chassis 1. Boards 15-27 are DP1 #14-26 in chassis 2. Board 28 is DP2 #2 in chassis 2. This entry is available for all 28 boards under the appropriate labels.	uint32	4
8.1.2	BOARD1_TEMP_MIN	Minimum FPGA die temperature in Celsius on Board 1. For boards which have been shutdown due to too high of FPGA temperatures, this will be -1.	float32	4
8.1.3	BOARD1_TEMP_MAX	Maximum FPGA die temperature in Celsius on Board 1. For boards which have been shutdown due to too high of FPGA temperatures, this will be -1.	float32	4
8.1.4	BOARD1_TEMP_AVG	Average FPGA die temperature in Celsius on Board 1. For boards which have been shutdown due to too high of FPGA temperatures, this will be -1.	float32	4
8.1.5	BOARD1_FIRMWARE	Firmware version loaded on Board 1 during the INI process.	char	256
8.1.6	BOARD1_HOSTNAME	Host name of Board 1 that is used to communicate with the board.	char	256
8.2	BOARD2_INFO	Information on Board 2		
8.2.1	BOARD2_STAT	Same as BOARD1_STAT for Board 2	uint32	4
8.2.2	BOARD2_TEMP_MIN	Same as BOARD1_TEMP_MIN for Board 2	float32	4
8.2.3	BOARD2_TEMP_MAX	Same as BOARD1_TEMP_MAX for Board 2	float32	4
8.2.4	BOARD2_TEMP_AVG	Same as BOARD1_TEMP_AVG for Board 2	float32	4
8.2.5	BOARD2_FIRMWARE	Same as BOARD1_FIRMWARE for Board 2	char	256

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Index	Label	Description	Type	Bytes
8.2.6	BOARD2_HOSTNAME	Same as BOARD1_HOSTNAME for Board 2	char	256
…				
8.28	BOARD28_INFO	Information on Board 28		
8.28.1	BOARD28_STAT	Same as BOARD1_STAT for Board 28	uint32	4
8.28.2	BOARD28_TEMP_MIN	Same as BOARD1_TEMP_MIN for Board 28	float32	4
8.28.3	BOARD28_TEMP_MAX	Same as BOARD1_TEMP_MAX for Board 28	float32	4
8.28.4	BOARD28_TEMP_AVG	Same as BOARD1_TEMP_AVG for Board 28	float32	4
8.28.5	BOARD28_FIRMWARE	Same as BOARD1_FIRMWARE for Board 28	char	256
8.28.6	BOARD28_HOSTNAME	Same as BOARD1_HOSTNAME for Board 28	char	256
9	CMD_STAT	Command Status Information for all control commands scheduled for execution in the slot immediately preceding the time that the RPT command was received. This information will be returned in a data structure with the following format: uint32 slot_time; uint16 num_commands; uint32 reference[num_commands]; uint8 completionCode[num_commands]; *slot_time* is in seconds past station time midnight. *num_commands* is an integer describing the number of commands whose status is reported in this message. *reference* is an array that describes the reference number associated with the control command from MCS [1]. *completionCode* is an array that describes the completion status of each command, where 0 = OK, and values > 0 indicate an error and the corresponding error code. The error codes are listed in Table 10.	uint32, uint16, uint32, uint8	up to 606
10	TBN_CONFIG	Current TBN configuration		
10.1	TBN_CONFIG_FR	Current TBN tuning frequency in Hz. This entry is	float32	4

Index	Label	Description	Type	Bytes
	EQ	only valid if TBN is running.		
10.2	TBN_CONFIG_FILTER	Current TBN filter mode. This entry is only valid if TBN is running.	uint16	2
10.3	TBN_CONFIG_GAIN	Current TBN gain. This entry is only valid if TBN is running.	uint16	2
11	DRX_CONFIG	Current DRX configuration.		
11.1	DRX_CONFIG_1	Current DRX configuration for beam 1. This entry is available for all NUM_BEAMS under the appropriate labels.		
11.1.1	DRX_CONFIG_1_1	Current DRX configuration for beam 1, tuning 1. This entry is available for all NUM_DRX_TUNINGS under the appropriate labels.		
11.1.1.1	DRX_CONFIG_1_1_FREQ	Current DRX tuning frequency in Hz for beam 1, tuning 1. This entry is only valid if DRX is running on beam 1, tuning 1.	float32	4
11.1.1.2	DRX_CONFIG_1_1_FILTER	Current DRX filter mode for beam 1, tuning 1. This entry is only valid if DRX is running on beam 1, tuning 1.	uint16	2
11.1.1.3	DRX_CONFIG_1_1_GAIN	Current DRX gain for beam 1, tuning 1. This entry is only valid if DRX is running on beam 1, tuning 1.	uint16	2
11.1.2	DRX_CONFIG_1_2	Current DRX configuration for beam 1, tuning 2.		
11.1.2.1	DRX_CONFIG_1_2_FREQ	Current DRX tuning frequency in Hz for beam 1, tuning 2. This entry is only valid if DRX is running on beam 1, tuning 2.	float32	4
11.1.2.2	DRX_CONFIG_1_2_FILTER	Current DRX filter mode for beam 1, tuning 2. This entry is only valid if DRX is running on beam 1, tuning 2.	uint16	2
11.1.2.3	DRX_CONFIG_1_2_GAIN	Current DRX gain for beam 1, tuning 2. This entry is only valid if DRX is running on beam 1, tuning 2.	uint16	2
11.2	DRX_CONFIG_2	Same as DRX_CONFIG_1 for Beam 2		
11.2.1	DRX_CONFIG_2_1	Same as DRX_CONFIG_1_1 for Beam 2, tuning 1.		
11.2.1.1	DRX_CONFIG_2_1_FREQ	Same as DRX_CONFIG_1_1_FREQ for Beam 2, tuning 1.	float32	4
11.2.1.2	DRX_CONFIG_2_1_FILTER	Same as DRX_CONFIG_1_1_FILTER for Beam 2, tuning 1.	uint16	2

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Index	Label	Description	Type	Bytes
11.2.1.3	DRX_CONFIG_2_1_GAIN	Same as DRX_CONFIG_1_1_GAIN for Beam 2, tuning 1.	uint16	2
11.2.2	DRX_CONFIG_2_2	Same as DRX_CONFIG_1_2 for Beam 2, tuning 2.		
11.2.2.1	DRX_CONFIG_2_2_FREQ	Same as DRX_CONFIG_1_2_FREQ for Beam 2, tuning 2.	float32	4
11.2.2.2	DRX_CONFIG_2_2_FILTER	Same as DRX_CONFIG_1_2_FILTER for Beam 2, tuning 2.	uint16	2
11.2.2.3	DRX_CONFIG_2_2_GAIN	Same as DRX_CONFIG_1_2_GAIN for Beam 2, tuning 2.	uint16	2
…				
11.4	DRX_CONFIG_4	Same as DRX_CONFIG_1 for Beam 4		
11.4.1	DRX_CONFIG_4_1	Same as DRX_CONFIG_1_1 for Beam 4, tuning 1.		
11.4.1.1	DRX_CONFIG_4_1_FREQ	Same as DRX_CONFIG_1_1_FREQ for Beam 4, tuning 1.	float32	4
11.4.1.2	DRX_CONFIG_4_1_FILTER	Same as DRX_CONFIG_1_1_FILTER for Beam 4, tuning 1.	uint16	2
11.4.1.3	DRX_CONFIG_4_1_GAIN	Same as DRX_CONFIG_1_1_GAIN for Beam 4, tuning 1.	uint16	2
11.4.2	DRX_CONFIG_4_2	Same as DRX_CONFIG_1_2 for Beam 4, tuning 2.		
11.4.2.1	DRX_CONFIG_4_2_FREQ	Same as DRX_CONFIG_1_2_FREQ for Beam 4, tuning 2.	float32	4
11.4.2.2	DRX_CONFIG_4_2_FILTER	Same as DRX_CONFIG_1_2_FILTER for Beam 4, tuning 2.	uint16	2
11.4.2.3	DRX_CONFIG_4_2_GAIN	Same as DRX_CONFIG_1_2_GAIN for Beam 4, tuning 2.	uint16	2

4.2.3 Examples

As an example, consider a monitor “RPT” command that requests the current value of NUM_BOARDS. Please note that single quotes (‘) are used in lieu of spaces for clarity and “@” is used to represent a byte of raw binary data.
MCS sends the message
DP_MCSRPT”””1591”10’54848’12345678’NUM_BOARDS
which is interpreted as follows:

- DESTINATION is “ DP”
- SENDER is MCS
- TYPE = “RPT”

- REFERENCE = 1591
- DATALEN = 10
- MJD = 54848
- MPM = 12345678
- DATA = “NUM_BOARDS”

DP responds
MCSDP_RPT”””1591”’9’54848’12345695’A’NORMAL@
which is interpreted as follows:

- DESTINATION is the MCS
- SENDER is “ DP“
- TYPE = “RPT”
- REFERENCE = 1591
- DATALEN = 1
- MJD = 54848
- MPM = 12345695

DATA = 1 byte of uint8 data representing the number of boards in the system (nominally 28).

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4.3 Control Commands

4.3.1 General Considerations

Control data shall be transmitted by the MCS according to the protocol specified in the MCS Common ICD [1]. Control commands are summarized in Table 5. Each command name will, by definition, be the message TYPE [1] used in communication with the MCS. The third column of Table 5 shows whether each command is time-specific and, if so, which command parameter indicates the time at which the command will be executed. See Section 4.3.3 for further explanation of time-specific commands.

Upon receipt of a control command, the DP will send a response within 3 seconds. In its response, the DP indicates whether the command was accepted or rejected by sending A (accepted command) or R (rejected command), followed by MIB index 1.1 (SUMMARY). In the event that a command is rejected, the comment field of the response will include an error code, as specified in Appendix B, Table 9, terminated by an exclamation point and a human-readable error message that elaborates on the reason the command was rejected. This error message is also copied to the MIB index 1.3 (LASTLOG).

If multiple control commands of the same type and sub-slot are received in the same slot, the *last* command received will be the one executed by DP.

All data fields are binary and all multi-byte numbers are transmitted big-endian.

Table 5: Summary of Control Commands

Command Name	Description	Time-Specific
TBW	Configuration of TBWs	yes, TBW_TRIGGER_TIME
TBN	Configuration of TBNs	yes, sub_slot
DRX	Configuration of DRXs	yes, sub_slot
BAM	Configuration of beams	yes, sub_slot
FST	Set-up of FIR filter coefficients table	no
INI	Initialization of the DP subsystem	no
STP	Stop the current TBN process	no
SHT	Shutdown/Reset of the DP subsystem	no

The DP has a variety of WARNING and ERROR conditions that are actively monitored. In the event that one of the conditions enumerated in Appendix B, Table 10 is detected, the MIB index 1.2 (INFO) is set with elaboration on the reason for the condition. The structure of the INFO index will be a list of space-separated MIB labels related to the condition terminated by an exclamation mark, a subsystem status code, as specified in

Appendix B, Table 10, terminated by an exclamation mark, and a human-readable error message. For example, if a brownout causes one of the two DP chassis to restart, the subsystem summary will be set to ERROR and INFO will read:

> NUM_BOARDS! 0x04! Boards missing due to FPGAs not being programmed – Found only 14 boards due to unprogrammed FPGAs, need 28

It should be noted that a WARNING condition will be automatically cleared when the condition leading to the warning no longer exists. An ERROR condition can only be cleared through external actions, i.e., issuing a SHT command followed by an INI and/or power cycling the DP chassis.

4.3.2 Limit on Command Rate

The DP will accept a maximum number of 80 control commands per slot from MCS. This limit applies to the total number of all types of control commands sent from MCS to DP, including commands that control beams and commands that control the TBNs and TBWs.

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4.3.3 Control Commands in Detail

4.3.3.1 TBW

Description	This command sets up configuration of all Wideband Transient Buffers (TBW). A TBW command always kills the currently running TBN command (see section 4.3.3.2) before execution. After the TBW command as finished reading out (approximately 3 minutes, 40 seconds), TBN is restarted at the start of the next slot if it was previously running before TBW was issued.
Arguments	The DATA portion of this message is structured as follows: uint8 TBW_BITS; sint32 TBW_TRIG_TIME; sint32 TBW_SAMPLES; TBW_BITS- At 2x12 bits per sample using a sampling rate of f_s = 196 MHz, the 32 MB RAM can record 61 msec of data. LSB = 0 means 12 bits LSB = 1 means 4 bits If the number of bits per sample is less than the full 12 bits per sample, then the data is truncated or rounded to the specified number of bits. TBW_TRIG_TIME- The trigger time utilizes units of samples from the start of the slot. Once the trigger time occurs, the TBWs will begin acquiring data. Note that if this command is received in slot N, the trigger time is assumed to occur in slot N+2. TBW_SAMPLES- This argument specifies the number of samples to read out. The maximum value of this argument is 12,000,000 for 12-bit samples and 36,000,000 for 4-bit samples.

4.3.3.2 TBN

Description	This command sets up configuration of the Narrowband Transient Buffers (TBN). The TBN processes are set up to run continuously. Note: The current implementation of TBN synchronizes the NCOs with 1 PPS. This leads to a 3 to 5 second delay between issuing the TBN command and when the TBN packets begin to be output. Thus, setting a non-zero sub-slot has the same effect as a sub-slot of zero.

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Arguments	The DATA portion of this message is structured as follows: float32 TBN_FREQ; sint16 TBN_BW; sint16 TBN_GAIN; uint8 sub_slot; Each output sample is rounded to NUM_TBN_BITS, which in the current design is 16 (8 bits each, I and Q). NUM_TBN_BITS is MIB entry 3. TBN_FREQ- This argument specifies the center frequency of the TBNs, in units of Hz. The valid range is 5-93 * 10^6 Hz. The frequency specified by the user will be rounded to the nearest multiple of $f_s / 2^{32}$, which is approximately 0.046 Hz. TBN_BW- This argument specifies a filter number, 1-7, which indicates the desired Nyquist sample rate of TBNs. TBN filter numbers are defined in Appendix A, Table 6. The maximum data rate supported for each TBN is 16 bits * 100 kHz = 1.6 Mbps. There are 20 TBNs on each DP1 board, resulting in a maximum data rate of 20 * 1.6 = 32 Mbps per DP1 board. TBN_GAIN- This argument specifies which bits are sent to the output. Valid values are 0-30. Given a value, x, the output will be divided by 2^x by trimming bit 0 (msb) through bit x-1, and then reduced to 8 bits by rounding off bit x+8 through bit 37. If overflow or underflow occurs, values are clipped to 127 or -127. sub_slot- This argument specifies the sub-slot number at the start of which the command shall take effect. Value may range from 0 to 99, where sub_slot=0 right at the beginning of the slot.

4.3.3.3 DRX

Description	This command sets up configuration of the specified DRX.
Arguments	The DATA portion of this message is structured as follows: uint8 DRX_BEAM; uint8 DRX_TUNING; float32 DRX_FREQ; uint8 DRX_BW; sint16 DRX_GAIN; uint8 sub_slot; DRX_BEAM- This argument specifies the DRX Beam which will be changed. Valid values are 1 to NUM_BEAMS. DRX_TUNING- This argument specifies the DRX tuning which will be changed. Valid values range from 1 to NUM_DRX_TUNINGS. Together, DRX_BEAM and DRX_TUNING specify a unique DRX ID, as shown in Appendix A, Table 7. DRX_FREQ- This argument specifies the center frequency of the DRX specified by DRX_BEAM and DRX_TUNING, in units of Hz. Valid range is 10-88 * 10^6 Hz. The frequency specified by the user will be rounded to the nearest multiple of $f_s/2^{32}$, which is approximately 0.046 Hz. DRX_BW- This argument specifies a filter number, 1-7, which indicates the sample rate of the DRX specified by DRX_BEAM and DRX_TUNING. DRX filter numbers are defined in Appendix A, Table 8. DRX_GAIN- This argument specifies an adjustable gain to compensate for bandwidth reduction. Valid values are 0-15. Given a value, x, the output will be divided by 2^x and then rounded to 4 bits. If overflow or underflow occurs, the output is 0x7 or 0x9, respectively. sub_slot- This argument specifies the sub-slot number at the start of which the command shall take effect. Value may range from 0 to 99, where sub_slot=0 right at the beginning of the slot.

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4.3.3.4 BAM

Description	This command sets up configuration of a beam. This command allows specification of delay and gain for each of the 520 signals in the specified beam. The delay parameters specify the coarse and fine delay for each polarization of the 260 stands. The gain parameters specify the 4 elements of the 2-by-2 matrix multiplication utilized for gain and polarization adjustments for each of the 260 stands. The total bytes need to specify both delay and gain is 2*520 + 2*260*2*2 = 3120 bytes.

Arguments	The DATA portion of this message is structured as follows: sint16 BEAM_ID; uint16 BEAM_DELAY[520]; sint16 BEAM_GAIN[260][2][2]; uint8 sub_slot; BEAM_ID- This argument specifies the beam which will be changed. Valid values are 1 to 4. BEAM_DELAY- This argument specifies the coarse and fine delay for the beam specified by BEAM_ID for 2 polarizations and 260 stands. Each 16-bit fixed point number is in units of samples at f_s, with format 16.12. The 4 bits after the binary point represent the fractional delay and the other 10 bits represent the coarse delay. The maximum coarse delay length is therefore 1023. For example, a fine delay value of 0001 (binary) specifies 1/16 of a sample, a fine delay of 0010 (binary) specifies 1/8 of a sample, etc. See Section 2.3 for channel numbering. BEAM_GAIN- This argument specifies the elements of the 2x2 matrix multiplications utilized for gain and polarization adjustments. For each of the 260 stands, 4 16-bit fixed point numbers must be specified, with format 16.1. The order of these values will be xx (x component of beam x), xy (x component of beam y), yx (y component of beam x), yy (y component of beam y). xy=yx=0 specifies no polarization correction. The determinant of this matrix should be >0.25 to avoid loss of precision. All 4 numbers may be set to zero to turn off a particular stand. sub_slot- This argument specifies the sub-slot number at the start of which the command shall take effect. Value may range from 0 to 99, where sub_slot=0 starting right at the beginning of the slot.

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4.3.3.5 FST

Description	This command sets up the table of FIR coefficients. This command will be used to configure one of the (260 stands x 2 filters each) 520 filters or all at once. Assuming N coefficients per filter and 16 table entries, N x 16 coefficients will need to be specified.
Arguments	The DATA portion of this message is structured as follows: sint16 INDEX; sint16 COEFF_DATA[16][32]; The filter whose coefficients are COEFF_DATA[i][ ] is used when the fine delay is i/16 sample. Valid values of INDEX are -1 to 520. If INDEX = -1, it specifies that the 520 channels are loaded with separate coefficient tables contained in the default filter table file, which is internal to DP. These are the values loaded at startup, so that they will be in effect if not FST command has been received. In this case, the rest of the data field is ignored. The default coefficients are documented in BFU0001. The default filter coefficients are normalized, with a DC gain of 1. If INDEX = 0, it specifies that each of the 520 channels shall be loaded with the same coefficient table, as given in the COEFF_DATA table. Otherwise, only the table for the channel number equal to INDEX is changed. See Section 2.3 for channel numbering. The COEFF_DATA table is fixed to 16*32 short (16-bit) words in size. Each of the sixteen entries in the table has space for up to 32 coefficients, but values beyond BEAM_FIR_COEFFS will be ignored. Unused coefficients must be padded with data to maintain table structure. An upper bound for completion of the FST command is 5 seconds.

4.3.3.6 INI

Description	This command initializes the DP subsystem using configuration information from a stored file. This command is intended to put the DP in the same state as it would be at power-up, prior to receiving any control commands. The INI command, defined in the MCS Common ICD [1], cleans up all DP processes, parses the configuration file, reloads DP1 firmware to DP1 boards, reloads DP2 firmware to DP2 boards, launches all DP processes, and re-calibrates. The INI command can be expected to complete within 1.5 minute. If any of the 28 boards does not respond to The DP subsystem control computer, the DP SUMMARY MIB entry will have a value of ERROR. If calibration delay values are not within the valid range, the DP SUMMARY MIB entry will have a value of ERROR and the error condition will be set in INFO. During the INI process, the transient buffer and beamformer subsystems are treated as independent. Specifically, if calibration of the beamformer delay fails, the transient buffer subsystem will still be available. Thus, control command of TBN and TBW will be accepted but command of BAM, FST, and DRX will be rejected until the beamformer subsystem has been successfully calibrated. Note: It is possible for an INI to end without performing a successful calibration of the beam former delay. It may be necessary to run INI multiple times before the beamformer is calibrated.
Arguments	The DATA field will be empty.

4.3.3.7 STP

Description	Stops the currently running TBN or beamformer process on DP. In the case of TBN, this command cleans up all TBN processes and clears the MIB entries that store the current TBN configuration. In the case of the beamformer, this command sets the gains for all antennas in the adder chain to zero.

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Arguments	The STP command accepts six arguments in the DATA field: 1) TBN – To stop the TBN processes, 2) TBW – To stop the TBW processes, 3) BEAM1 – To zero the adder chain for beam 1, 4) BEAM2 – To zero the adder chain for beam 2, 5) BEAM3 – To zero the adder chain for beam 3, and 6) BEAM4 – To zero the adder chain for beam 4.

4.3.3.8 SHT

Description	Issues a shutdown or reset to the DP. This command cleans up all DP processes and unloads the firmware on all boards, putting the system in a low power state.
Arguments	This command is specified completely in Section 5 of the MCS Common ICD [1].

4.3.4 Command Examples

As an example, consider a control command that sets parameters for the TBW command. Please note that single quotes (‘) are used in lieu of spaces for clarity and “@” is used to represent a byte of raw binary data.

MCS sends the message
DP_MCSTBW’’’’1592’’’9’54831’123451234’@@@@@@@@@
which is interpreted as follows:

- DESTINATION is “ DP”
- SENDER is MCS
- TYPE = “TBW”
- REFERENCE = 1592
- DATALEN= 9
- MJD = 54831
- MPM = 123451234
- DATA = 9 bytes of data specifying TBW_BITS, TBW_TRIG_TIME and TBW_SAMPLES

DP responds
MCSDP_TBW’’’’1592’’’8’54831’123451255’A’NORMAL
which is interpreted as follows:

- DESTINATION is the MCS
- SENDER is “ DP“

- TYPE = “TBW”
- REFERENCE = 1592
- MJD = 54831
- MPM = 123451255

The data field is:
A = Command was accepted
NORMAL = DP MIB index 1.1 entry indicating SUMMARY = NORMAL

Repointing a beam may require adjustment of gain, delay, dispersion, DRX center frequency, and/or DRX bandwidth. Gain, delay, and dispersion are controlled by the BAM command. DRX center frequency and bandwidth are controlled by the DRX command. Therefore repointing a beam requires at most a BAM and a DRX command.

5 OUTPUT INTERFACES

The DP will output data three types of data over two types of interfaces:

1. DRX data on 4 (one for each beam) 10 Gb Ethernet connections
2. TBN data on 1 10 Gb Ethernet connection
3. TBW data on the same 10 Gb Ethernet connection

All types of data will be sent to the Data Aggregation and Communication (DAC) Subsystem (or MCS-DR). All types of data will include IPv4 [11], UDP [11], and Data Frame headers. The Mark5C specification [2] is a starting point for the Data Payload output format for the DRX, TBN and TBW data. Customizations to the Mark5C format were made for the LWA data structures. While future compatibility with Mark5C recorders is a desire, it is not a requirement in this specification and is not guaranteed.

Data is always pushed out (and cannot be turned on or off). No commands or acknowledgments are expected from DAC (or MCS-DR).

All data values are signed numbers in two’s complement format.

5.1 DRX Output Interface

Figure 2 describes the LWA DRX Output Format.

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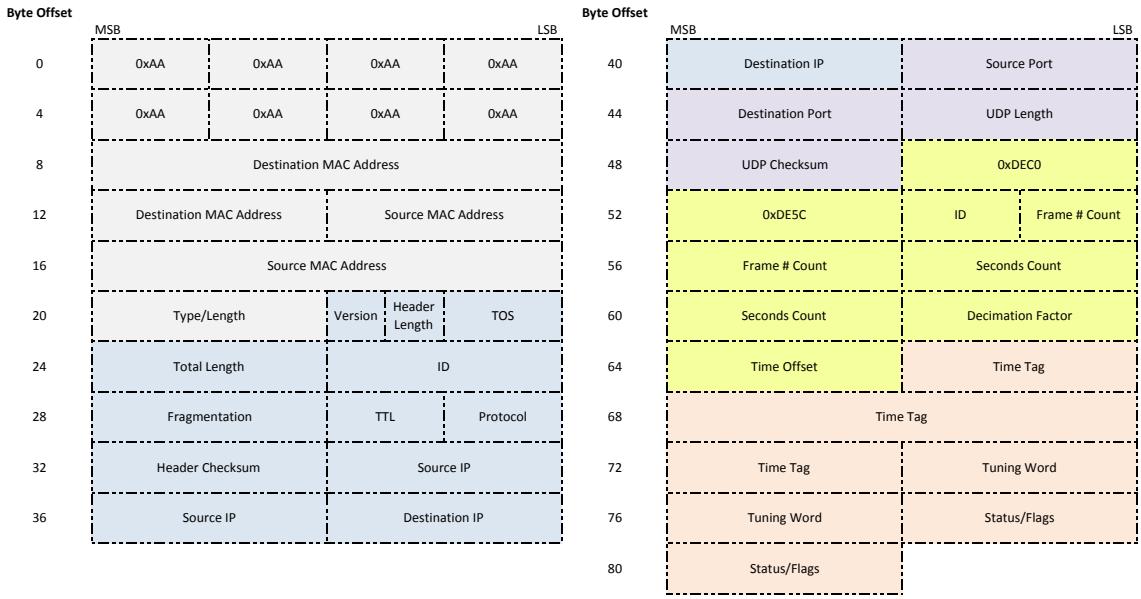

Figure 2: DRX Output Format

The DRX Output will utilize Ethernet (shown in gray), IP [11] (shown in blue), UDP [12] (shown in purple), and Mark 5C [2] (shown in yellow) headers. The Data Payload size is fixed (4156 bytes) and fits within an Ethernet jumbo packet. Each data frame will contain data of one polarization (X or Y), one DRX tuning, and 4096 samples. The Mark 5C header will include an ID field that identifies which polarization and tuning is associated with the data, as described in Table 7.

The Mark 5C header will include Frame Count and Seconds Count fields for compatibility purposes but both of these fields will always be set to zero. The Data Frame header will include a Decimation Factor field that describes the decimation factor used in producing the output data. The output sample rate is f_s/Decimation Factor. The Data Frame header will also include a Time Offset field that provides the known time offset (T_{nom} in LWA Memo 151 [5]), in units of $1/f_s$ since the beginning of the second. The Data Frame will include a Time field (t_1 in LWA Memo 151 [5]) in units of $1/f_s$ since 1970 January 1 00:00 UTC. For the *i*-th sample of the frame, the time at that sample is related to the frame time tag through:

$$t_i = \text{time} + (i-1) \times \text{DecimationFactor} \div f_s$$

The Data Frame will also include a tuning word, a unsigned 32-bit integer, which specifies the central tuning of the DRX data. This tuning word, w, can be converted to a frequency in Hz via:

$$f = \frac{w}{2^{32}} f_s,$$

where f_s is defined in Table 2. The status/flags field in the Data Frame is currently unimplemented in the DRX firmware and is set to zero for all frames.

Each sample is 8 bits total (4 bits I and 4 bits Q). Therefore 4096 samples require 4096 bytes. Inside each 32-bit word, the data will be arranged in the following order (from MSB to LSB):

I0 (bits 31-28), Q0 (bits 27-24), I1 (bits 23-20), Q1 (bits 19-16),
I2 (bits 15-12), Q2 (bits 11-8), I3 (bits 7-4), Q3 (bits 3-0).

The numbers in paraphrases are the bits within each sample such that 0 is the LSB.

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5.2 TBN Output Interface

TBN data will be 16 bits (8 bits each of I and Q). Figure 3 describes the LWA TBN Output Format.

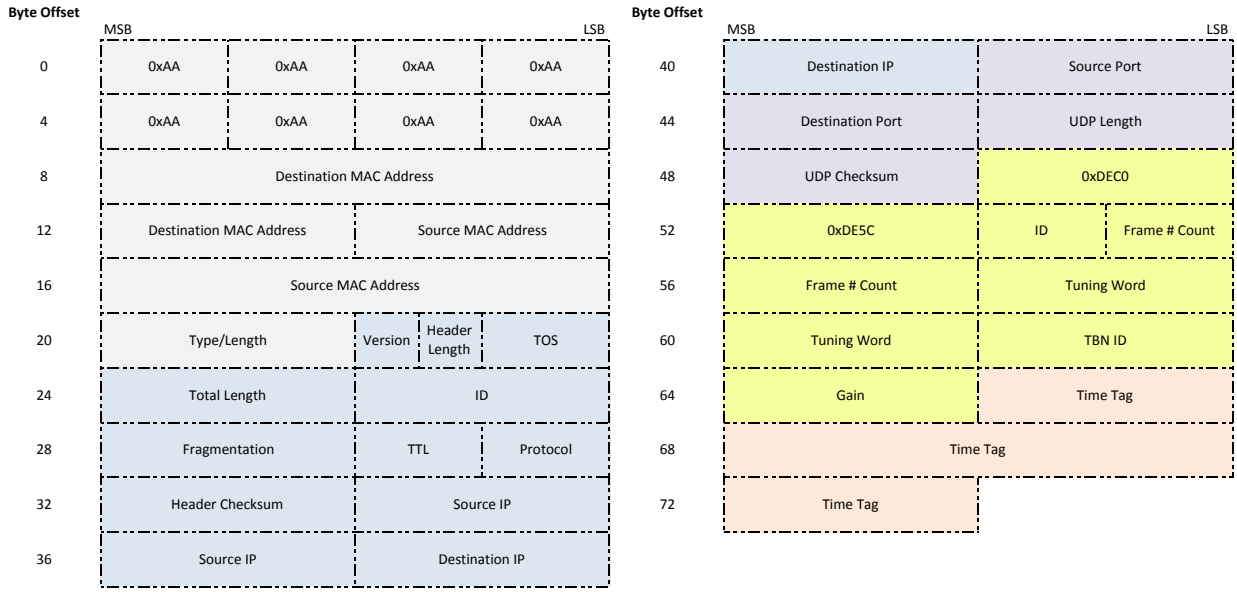

Figure 3: TBN Output Format

The TBN Output will utilize Ethernet (shown in gray), IP [11] (shown in blue), UDP [12] (shown in purple), and Mark 5C [2] (shown in yellow) headers. The Data Payload size is fixed (1076 bytes) and fits within a standard Ethernet packet. A Data Frame will contain 512 samples or 1024 bytes of complex data (I and Q) from a particular stand (of 260) of one polarization (X or Y). The Mark 5C header includes an ID field, but it is not sufficient to specify the data's stand, polarization, and other identifying information. This field will be included for Mark 5C compatibility but will always be set to zero. Instead, the Data Frame header will include a TBN_ID field that identifies which stand and polarization are associated with the data. See Section 2.3 for channel numbering. The MSB of TBN_ID will be 0, to indicate TBN data. The Data Frame will also include a tuning word, a unsigned 32-bit integer, which specifies the central tuning of the TBN data. This tuning word can be converted to a frequency in Hz via:

$$f = \frac{w}{2^{32}} f_s,$$

where f_s is defined in Table 2.

The Data Frame will include a Time Tag field that provides total number of samples at f_s since 1970 January 1 00:00 UTC. Inside each 32-bit word, the data will be arranged in the following order (from MSB to LSB):

I0 (byte3), Q0 (byte2), I1 (byte1), Q1 (byte0).

5.3 TBW Output Interface

TBW data will be 12 or 4 bits for each of two polarizations, for a total of either 24 or 8 bits per sample, respectively. Figure 4 describes the LWA TBW Output Format.

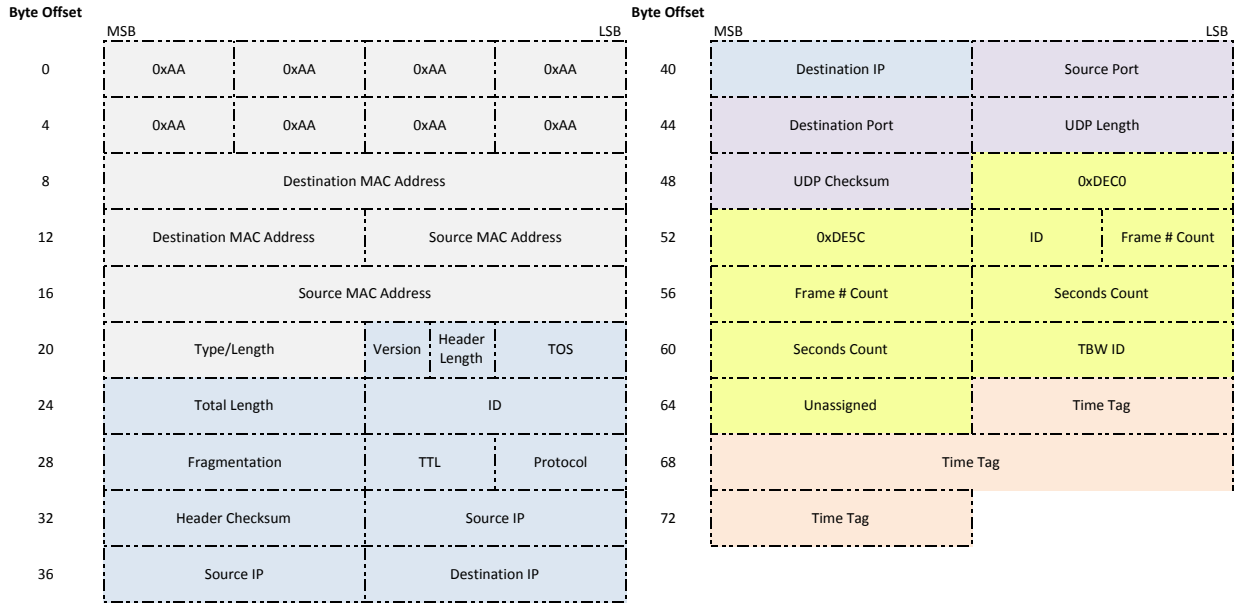

Figure 4: TBW Output Format

The TBW Output will utilize Ethernet (shown in gray), IP [11] (shown in blue), UDP [12] (shown in purple), and Mark 5C [2] (shown in yellow) headers.

The Data Payload size is fixed (1252 bytes) and fits within a standard Ethernet packet. A Data Frame will contain real data from a particular stand (of 260) and both polarizations (X and Y). If the data is 12 bit, each Data Frame will contain 400 samples or 1200 bytes. If the data is 4 bit, each Data Frame will contain 1200 samples or 1200 bytes. The Mark 5C header includes an ID field, but it is not sufficient to specify the data's stand and other identifying information. This field will be included for Mark 5C compatibility but will always be set to zero. Instead, the Data Frame header will include a TBW_ID field that identifies which stand is associated with the data. See Section 2.3 for stand numbering. The MSB of TBW_ID will be 1, to indicate TBW data. The next most significant bit will be 0 for 12 bit data and 1 for 4 bit data. The Data Frame will include a Time Tag field that provides the effective sampling time of the first sample of data (X0 and Y0), in total number of samples at f_s since 1970 January 1 00:00 UTC.

The data is packed binary, big-endian. Inside each 32 bit word, the data will be arranged in the following order:

X0, Y0, X1, Y1…

For example, the first 3 bytes consist of:

X0(11:4), [X0(3:0) Y0(11:8)], Y0(7:0)

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for 12-bit samples and:

[X0(3:0) Y0(3:0)], [X1(3:0) Y1(3:0)], [X2(3:0) Y2(3:0)]

for 4-bit samples. The brackets indicate a single byte and the number in parentheses are the bits within each sample such that 0 is the LSB.

The instantaneous transfer rate for TBW data will be less than 100 MB/s.

6 SAFETY INTERFACE

The DP has no safety issues requiring monitoring. No action of the monitor and control system can cause incorrect or dangerous conditions in the DP.

7 REFERENCES

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[6] J. Craig, "Preliminary Design of the Timebase and Clock Distribution (TCD) Subsystem for the LWA." February 16, 2009.

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[11] Postel, J. B., ed. "Internet Protocol," RFC 791. September, 1981.

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[13] M. Soriano and G. Crichton. “LWA Engineering Memo DP0015: DP Board Status Specification.” April 13, 2011.

[14] T. Clarke, “LWA Memo 159: Scientific Requirements for the Long Wavelength Array.” February 24, 2009.

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APPENDIX A

A.1 TBN Filter Codes

Table 6: TBN Filter Codes

Filter Number	Sample Rate (Hz)
1	1000
2	3125
3	6250
4	12500
5	25000
6	50000
7	100000

A.2 DRX_ID Numbering

Table 7: DRX_ID Numbering

DRX_BEAM	DRX_TUNING	Polarization	DRX_ID
1	1	X	9
1	1	Y	137
1	2	X	17
1	2	Y	145
2	1	X	10
2	1	Y	138
2	2	X	18
2	2	Y	146
3	1	X	11
3	1	Y	139
3	2	X	19
3	2	Y	147
4	1	X	12
4	1	Y	140
4	2	X	20
4	2	Y	148

DRX Numbering is as follows: DRX_ID is an unsigned 8-bit integer. Bits 0-2 are used to represent DRX_BEAM, bits 3-5 are used to represent DRX_TUNING, bit 6 is reserved for future use, and bit 7 is used to represent polarization.

A.3 DRX Filter Codes

Table 8: DRX Filter Codes

Filter Number	Sample Rate (Hz)
1	250000
2	500000
3	1000000
4	2000000
5	4900000
6	9800000
7	19600000

Note that sample rates are all f_s/n, where n is an integer. Therefore a sample rate of exactly 8 MHz (the required maximum instantaneous bandwidth [14]) is not possible. However, sample rates exceeding this requirement are provided.

Appendix B

B.1 Command Exit Codes

Table 9: Command Exit Codes

Exit Code	Meaning
0x00	Command accepted/processed without error
0x01	Invalid frequency
0x02	Invalid bandwidth
0x03	Invalid gain
0x04	Invalid sub-slot
0x05	Invalid beam
0x06	Invalid tuning
0x07	Invalid number of TBW data bits
0x08	Invalid TBW trigger time
0x09	Invalid TBW sample size
0x0A	Invalid arguments to command
0x0B	Other error running command
0x0C	Blocking operation in progress
0x0D	Beamformer sub-subsystem is not ready
0x0E	Transient buffer sub-subsystem is not ready
0x0F	Subsystem needs to be initialized

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B.2 Subsystem Status Codes

Table 10: Subsystem Status Codes

Status Code	Meaning
0x00	Subsystem is operating normally
0x01	Multiple board temperature warnings[1]
0x02	Boards missing during initialization
0x03	Boards missing due to thermal shutdown
0x04	Boards missing due to FPGAs not being programmed
0x05	Boards missing due to communication problems
0x06	Beamformer calibration failed
0x07	Beamformer calibration lost
0x08	Board-level shutdown failed
0x09	Board-level startup failed
0x0A	DRX time not updating correctly

[1] This is a WARNING rather than an ERROR condition.