instr	reg_dst	alu_src	alu_op	mem_to_reg	reg_write	mem_write	branch	beq	j_en	j_dest	jal
addi	0	1	add	0	1	0	0	x	0	x	0
addiu	0	1	addu	0	1	0	0	x	0	x	0
ori	0	1	or	0	1	0	0	x	0	x	0
lui	0	1	add	0	1	0	0	x	0	x	0
lw	0	1	add	1	1	0	0	x	0	x	0
sw	x	1	add	x	0	1	0	x	0	x	0
addu	1	0	addu	0	1	0	0	x	0	x	0
subu	1	0	subu	0	1	0	0	x	0	x	0
sltu	1	0	sltu	0	1	0	0	x	0	x	0
or	1	0	or	0	1	0	0	x	0	x	0
sll	1	0	sll	0	1	0	0	x	0	x	0
jal	x	x	x	0	0	0	0	x	1	0	1
slt	1	0	slt	0	1	0	0	x	0	x	0
bne	x	0	subu	0	0	0	1	0	0	x	0
beq	x	0	subu	0	0	0	1	1	0	x	0
jr	x	x	x	0	0	0	0	x	0	1	0
j	x	x	x	0	0	0	0	x	1	0	0