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White Paper

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DDR3 Routing Topology

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DDR3- Introduction

Double data rate three (DDR3) is a type of dynamic random-access memory (DRAM) released in June of 2007 as the successor to DDR2. DDR3 chips have bus clock speed of 400 MHz up to 1066 MHz, range in size from 1 to 24 GB, and consume nearly 30% less power than their predecessors. DDR3 SDRAM is neither forward nor backward compatible with any earlier type of random-access memory (RAM) because of different signaling voltages, timings, and other factors.

Comparison

The primary benefit of DDR3 SDRAM over its immediate predecessor, DDR2 SDRAM, is its ability to transfer data at twice the rate (eight times the speed of its internal memory arrays), enabling higher bandwidth or peak data rates. With two transfers per cycle of a quadrupled clock signal, a 64-bit wide DDR3 module may achieve a transfer rate of up to 64 times the memory clock speed megahertz (MHz) in megabytes per second (MB/s). With data being transferred 64 bits at a time per memory module, DDR3 SDRAM gives a transfer rate of (memory clock rate) × 4 (for bus clock multiplier) × 2 (for data rate) × 64 (number of bits transferred) / 8 (number of bits/byte). Thus with a memory clock frequency of 100 MHz, DDR3 SDRAM gives a maximum transfer rate of 6400 MB/s.

DDR SDRAM Standard	Internal rate (MHz)	Bus clock (MHz)	Prefetch	Data rate (MT/s)	Transfer rate (GB/s)	Voltage (V)
SDRAM	100-166	100-166	1n	100-166	0.8-1.3	3.3
DDR	133-200	133-200	2n	266-400	2.1-3.2	2.5/2.6
DDR2	133-200	266-400	4n	533-800	4.2-6.4	1.8
DDR3	133-200	533-800	8n	1066-1600	8.5-14.9	1.35/1.5
DDR4	133-200	1066-1600	8n	2133-3200	17-21.3	1.2

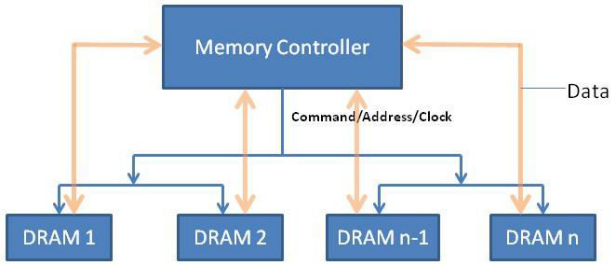
Table 1: Comparison

DDR3 Routing Topology Type:

T- Topology
Fly By Topology

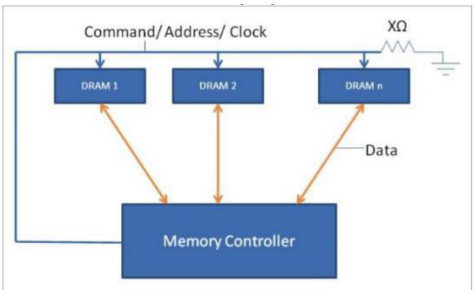
T- Topology

In T-Topology for connecting memory controller and DDR memory modules in which the command/Address/Clock signals are routed to each memory module in a branched fashion. T Topology adopted for DDR2 couldn't support higher signaling rates and more number of memory modules due to capacitive loading. In a T-topology, the signals are routed to a central node before routing them to individual memory modules, thus limiting the potential variability of trace lengths to shorter paths. But higher signaling rates couldn't be reliably supported over this topology due to multiple stubs and increase in capacitive load seen by the signals when increasing memory capacity.



Fly –By- Topology

JEDEC introduces fly-by- topology in the DDR3 specification for the differential clock, address, command and control signals.
The fly-by daisy chain topology increases the complexity of the data path and controller design to achieve levelling, but also greatly improves performance and eases board layout.
The advantage of fly-by- topology is that it supports higher frequency operation, reduces the quantity and length of stubs and consequently improves signal integrity and timing on heavily loaded signals.



Fly –By- Vs T- Topology

JEDEC Introduce Fly-By Topology in the DDR3 Specification for the Different Clock, Address, Command and Control Signals. Fly-by used in DDR3. This topology is more advance compared to Conventional T. Instead of mechanical line balancing, it uses automated signal time delay. DDR3 chip has an automatic leveling circuit for calibration and to memorize the calibration data. In simple, it has moved to some automated process that is better than DDR2.

The Advantages of fly-By topology is that it supports higher-frequency operation, reduces the quantity and length of the stubs and consequently improves signal integrity and timing on heavily loaded signals. Fly by topology also reduces simultaneous switching noise by deliberately causing flight- time skew, between the address group and the point to point topology signals, of the data groups. To account for this skew, the DDR3/4 Controller supports write leveling.

The double T- topology was used for DDR2 and had a downside in that the impedance discontinuities, due to branching along the traces, caused obvious margin losses. T-Topology also tends to have overshoot, while the levels for the fly-by are terminated and therefore do not reach the full swing voltage rails. Also, the length of the stubs has an effect on the maximum bandwidth of the transmission line.

DDR3 Signal Group

The DDR Memory signals can be divided into the following signal groups for the purpose of the design guide:

- Data
- Address/Command/Control
- Clocks

Layout Order for the DDR Signal Groups

To help ensure that the DDR interface is properly optimized, the following sequence is recommended for routing the DDR memory channel:

- Power (VTT island with termination resistors, VREF)
- Pin swapping within resistor networks
- Route data
- Route address/command
- Route control
- Route clocks

The data group is listed before the command, address, and control group because it operates at twice the clock speed and its signal integrity is of higher concern. In addition, the data group constitutes the largest portion of the memory bus and consists of the majority of the trace matching requirements, those of the data lanes.

The address/command, control, and the data groups all have a relationship to the routed clock. Therefore, the effective clock lengths used in the system must satisfy multiple relationships

Trace Length Matching Requirement

Clock signals

- Clocks must maintain a length matching between clock pairs of ±5 ps or approximately ± 25 mils (0.635 mm).
- Differential clocks need to maintain length matching between positive and negative signals of ±2 ps or approximately ± 10 mils (0.254 mm), routed in parallel.

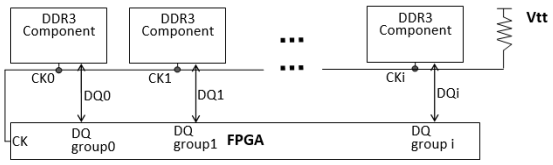
Address and Command signals

- Route all addresses and commands to match the clock signals to within ±25 ps or approximately ± 125 mil (± 3.175 mm) to each discrete memory component.

DQ/DQS/DM

- All signals within a given byte-lane group must be matched in length with a maximum deviation of ±10 ps or approximately ± 50 mils (± 1.27 mm).
- Ensure all signals within a given byte lane group are routed on the same layer to avoid layer to layer transmission velocity differences, which otherwise increase the skew within the group.
- DQ, DQS, DM signal don’t need to be “in order”, meaning it’s not required that

signals in group 1 arrive later than group 0, group 2 later than group 1 and so on.



(CKi – CK) = CLK signal propagation delay to device i

DQSi = DQ/DQS signals propagation delay for group i

DQS to clock

Timing between DQS and clock signal on each device is dynamically calibrated if leveling is enabled. To meet tDQSS, make sure the following layout rules are followed:

- Clock signal propagation delay is no shorter than propagation delay of DQS signal at every device; in fig above, it means:

(CKi – CK) – DQSi > 0 (0 =< i < number of components – 1)

- Total skew of CLK and DQS signal between groups is less than one clock cycle

(CKi – CK + DQSi)max – (CKi – CK + DQSi)min < 1 * Tck

These rules are to ensure during write leveling calibration we can put delay on the DQS signal to align DQS and clock, and to make sure skew is too large for the leveling circuit's capability

General Routing Guidelines

Route using 45° angles and *not* 90° corners. Do not route critical signals across split planes. Route over appropriate VCC and ground planes. Avoid routing memory signals closer than 25-mil (0.635 mm) to the memory clocks. Keep the signal routing layers close to ground and power planes. All specified delay matching requirements include PCB trace delays, different layer propagation velocity variance, and crosstalk. To minimize PCB layer propagation variance, it is recommended that signals from the same net group always be routed on the same layer.

Clock Routing Guidelines

Route clocks on inner layers with outer-layer run lengths held to under 500 mils (12.7 mm).

- 10-mil spacing for parallel runs < 0.5 inches (2× trace-to-plane distance)
- 15-mil spacing for parallel runs between 0.5 and 1.0 inches (3× trace-to-plane distance)
- 20-mil spacing for parallel runs between 1 and 6 inches (4× trace-to-plane distance)

The space between differential pairs must be at least 2× the trace width of the differential pair to minimize loss and maximize interconnect density. For example, differential clocks must be routed differentially (5 mil trace width, 10-15 mil space on centers, and equal in length to signals in the Address/Command Group). Take care with the via pattern used for clock traces. To avoid transmission-line-to-via mismatches, it is recommended that your clock via pattern be a Ground-Signal-Signal-Ground (GSSG) topology (via topology: GND | CLKP | CLKN | GND).

Address and Command Routing Guidelines

Similar to the clock signals in DDR3 SDRAM, address and command signals are routed in a daisy chain topology from the first SDRAM to the last SDRAM. Ensure that each net maintains the same consecutive order. Unbuffered DIMMs are more susceptible to crosstalk and are generally noisier than buffered DIMMs. Route the address and command signals of unbuffered DIMMs on a different layer than DQ and DM, and with greater spacing. Do not route differential clock and clock enable signals close to address signals.

Spacing rules for address and command and CLK signals

- 4 mils for parallel runs < 0.1 inch (approximately 1× spacing relative to plane distance)
- 10 mils for parallel runs < 0.5 inch (approximately 2× spacing relative to plane distance)
- 15 mils for parallel runs between 0.5 and 1.0 inches (approximately 3× spacing relative to plane distance)

- 20 mils for parallel runs between 1.0 and 6.0 inches (approximately 4× spacing relative to plane distance)

DQ, DQS, and DM Routing Guidelines

Maintain all other signals to a spacing that is based on its parallelism with other nets:

- 5 mils for parallel runs < 0.5 inches (approximately 1× spacing relative to plane distance)
- 10 mils for parallel runs between 0.5 and 1.0 inches (approximately 2× spacing relative to plane distance)
- 15 mils for parallel runs between 1.0 and 6.0 inches (approximately 3× spacing relative to plane distance)

DDR3 Design Guidelines-Critical Constraints:

- Clock nets, DQ (data) and DQS (strobes) are routed differentially.4.5” max length +/- 25MIL
- Net length from driver to first DIMM or chip-between 2 to 3” max depending on load.
- Net length between DIMM’s or chips-0.5”
- Net length from last DIMM or chip to the VTT Termination-0.2” to 0.55”
- All DSQ/DQ (data and data strobe) should be minimized to reduce the skew within groups (or lanes) and across group.
- Skew between address nets should be 200MIL. Address and command nets are daisy chained and with VTT pull-up for the termination.
- Zo for DDR3 is 50 ohm. Zdiff is 100 ohm.

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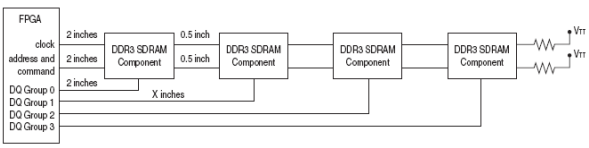

DDR3 topology using levelling

Conclusion:

JEDEC introduced fly-by topology in the DDR3 specification for the differential clock, address, command and control signals.

- The advantage of fly-by topology is that it supports higher-frequency operation, reduce the quantity and length of stubs and improves signal integrity and timing.
- T-topology can be challenging to route, particularly double T-topology with four back-to-back SDRAMs, but it can be advantageous when using multi-die packages with high capacitance loads.
- Excessive ring-back is often present in the first few nodes of the daisy chain.
- With conventional T-topology, the trace stub is lengthened with an increase in number of memory device loads.
- The clock trace should be routed to a longer delay than the strobe traces per byte lane.

About the Company

Founded in 2009, Logic Fruit Technologies has a highly experienced management team, which is backed by a talented and committed engineering team. Almost all the employees are hand-picked from IITs and NITs.

The company is leading its way into the next generation High Speed Serial Protocols (3 Gbps and above) like PCIe, Fibre Channel, USB, 3G-4G wireless protocols, HDMI and so on. The company has worked closely with reputed high tech companies like Agilent Technologies.

The company has gained a high reputation in market in such a short span due to its innovative outsourcing model, uncompromised quality of work and deep domain knowledge. The main goal of the company is to minimize client’s overhead and it works on the simple motto “Outsource and Forget”. It has a track record of always exceeding the client’s expectations.

For further information, check the website

www.logic-fruit.com.