

# KSZ9131RNX Ref. Design

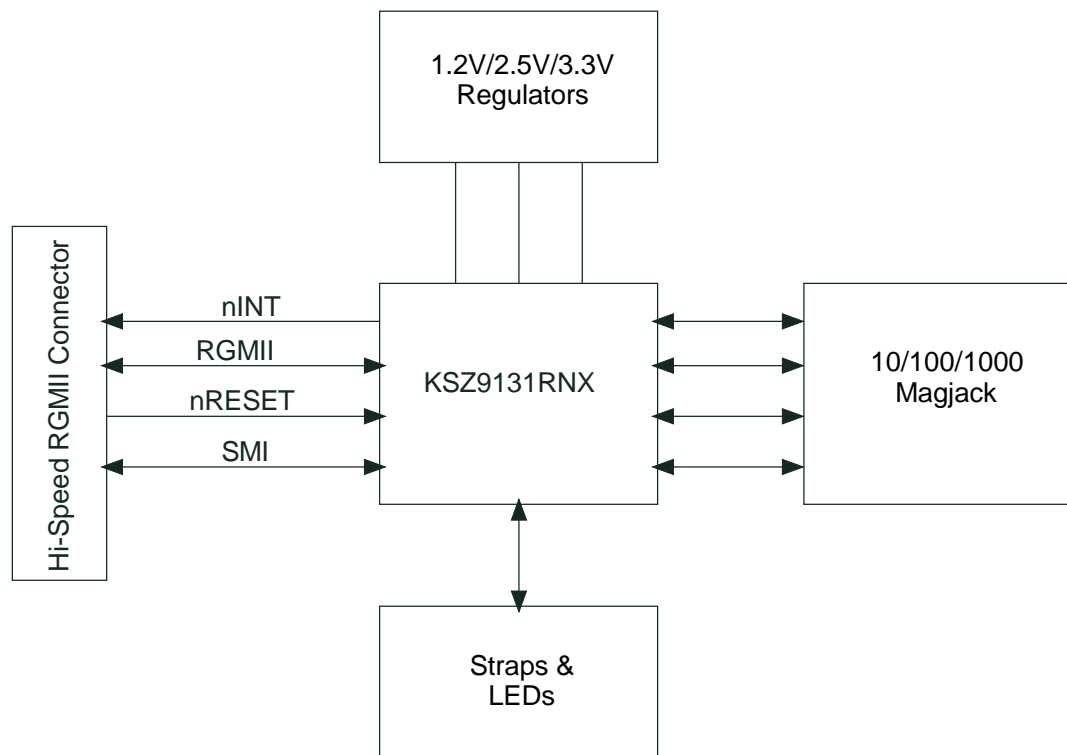
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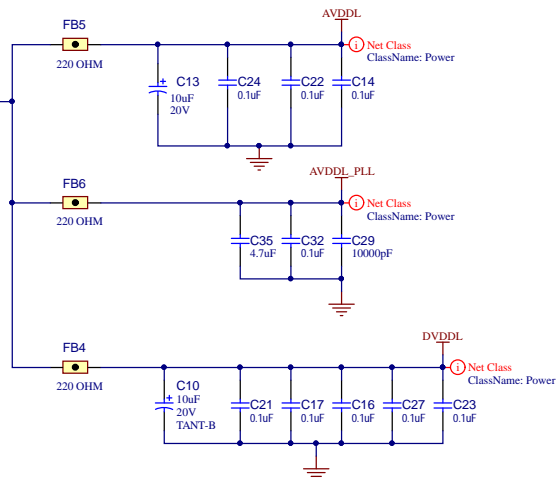
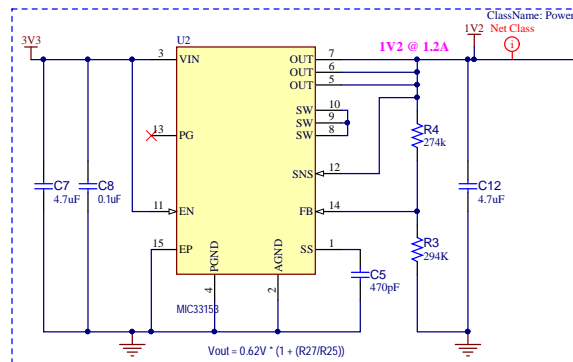
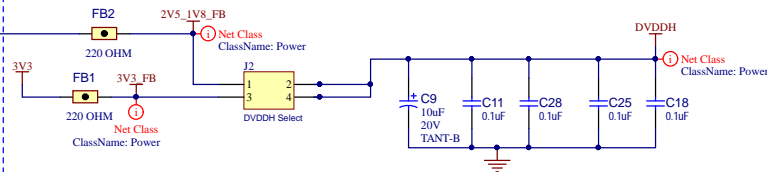
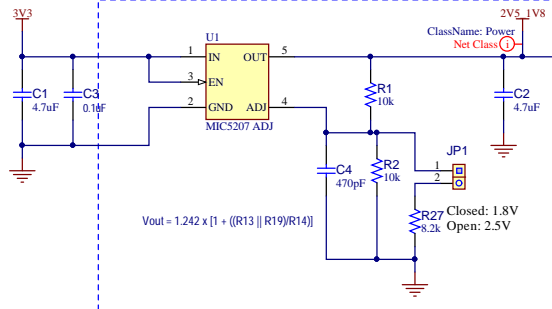
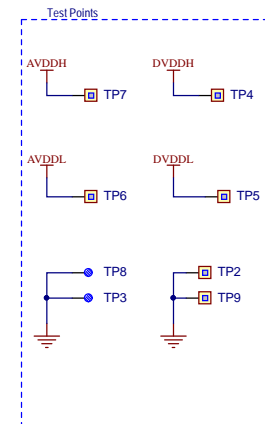
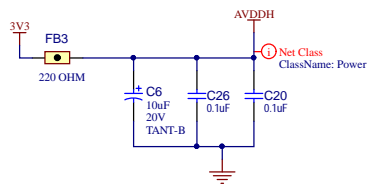
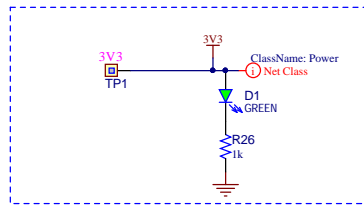
Sheet	Description
1	Title Page
2	KSZ9131RNX Power
3	KSZ9131RNX
4	KSZ9131RNX Hi-Speed RGMII Interface



## Revision History

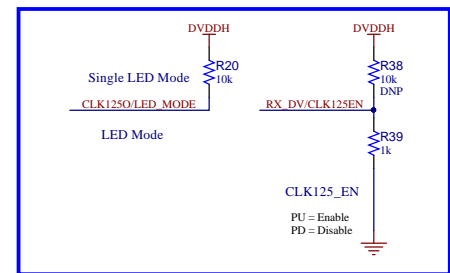
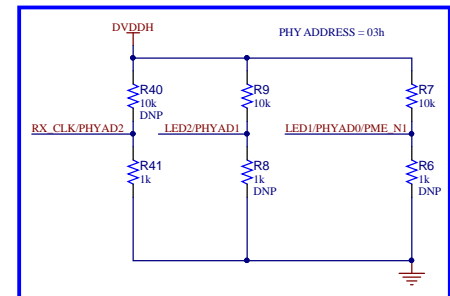
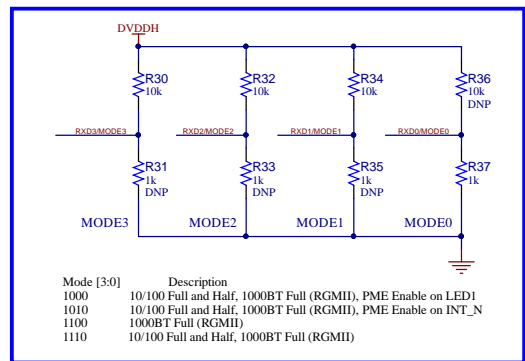
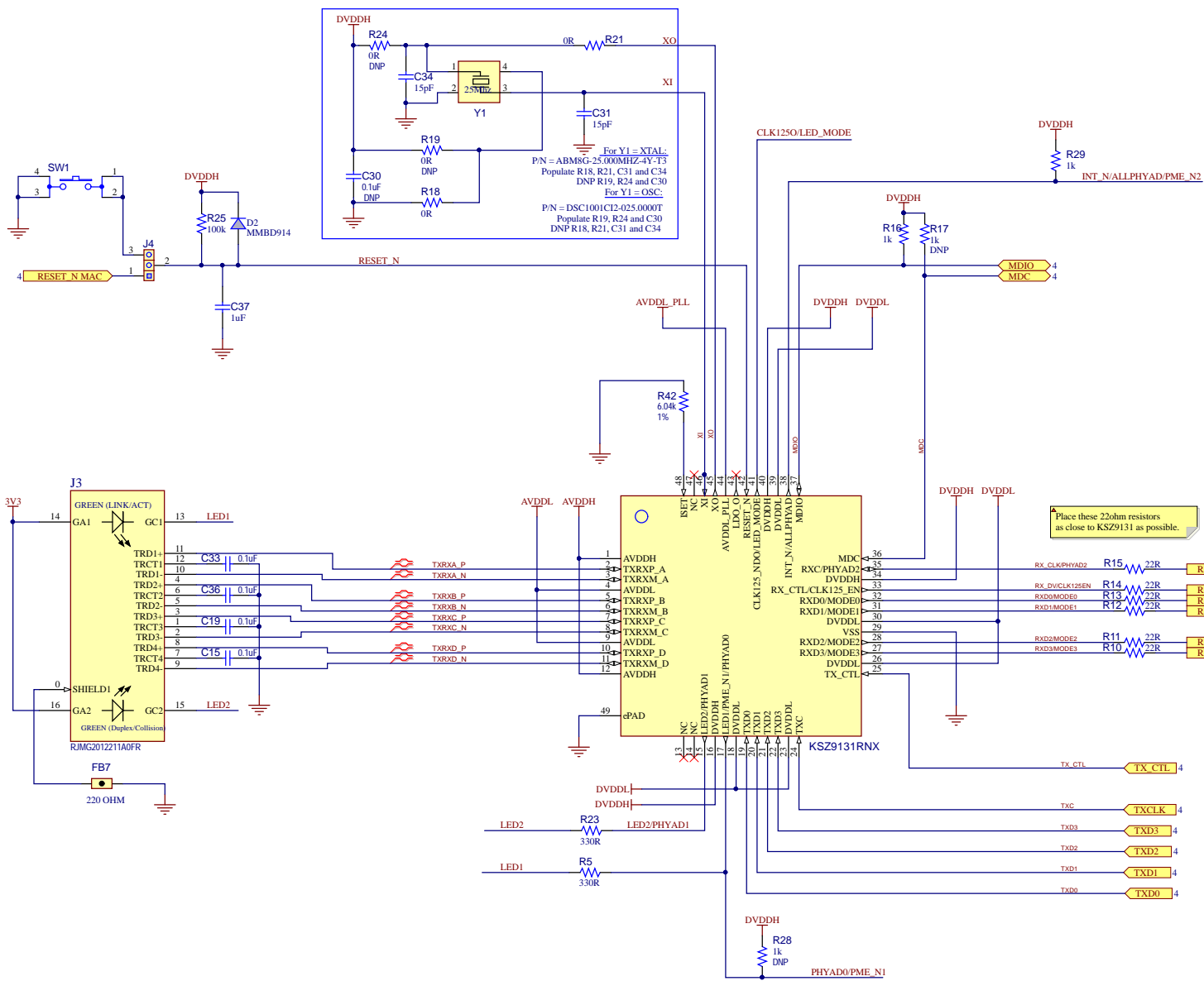
Revision	Date	Revision Summary	Author
1	1/3/2020	Initial release of design	J. MacKay

## Notes





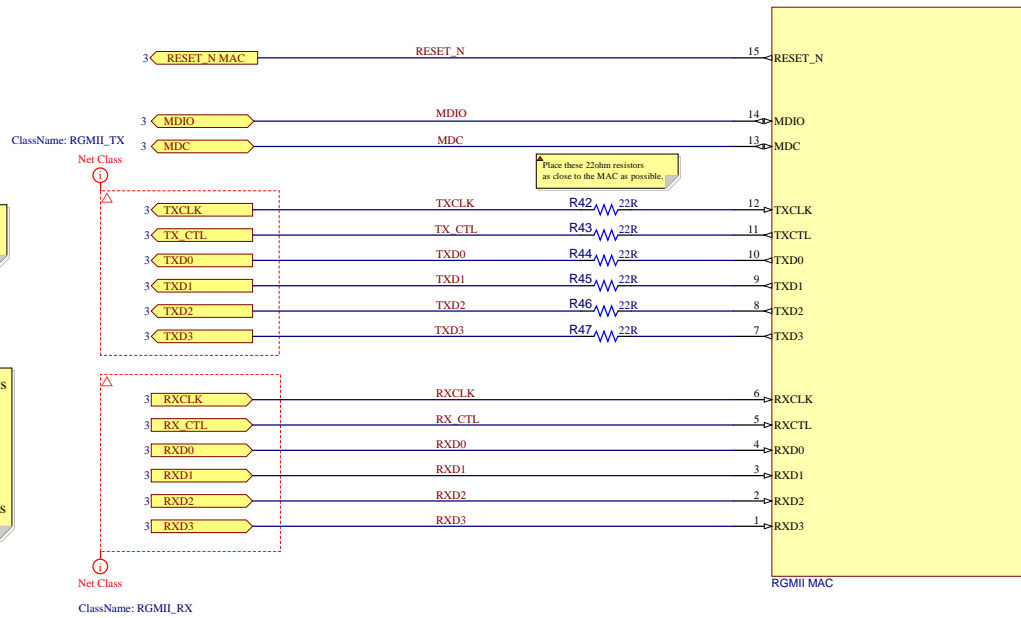
 <b>MICROCHIP</b>		Microchip Technology, Inc. USB/Network Group - UNG <a href="http://www.Microchip.com">www.Microchip.com</a>	Designed with  <a href="http://Altium.com">Altium.com</a>	
Description: <b>KSZ9131RNX Reference Design</b>		Variant: <b>[No Variations]</b>		
Page Title: *				
Project Name: <b>KSZ9131RNX Ref. Design</b>		PN: <b>KSZ9131RNX</b>		
Size: B	Date: <b>1/3/2020</b>	Designer: <b>J. MacKay</b>	Sheet 2 of 4	Rev 1



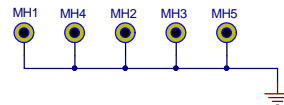
PCB Layout Constraint: The RGMII TXCLK – TX signals must be trace length matched from DUT to RGMII MAC to within 50 mils.



PCB Layout Constraint: The RGMII RX signals must be trace length matched from DUT to RGMII MAC to within 50 mils.

In addition to this, RXCLK must be either longer than the RX signals to add delay or the delay (1.2 ns-1.5 ns) must be added on the RGMII MAC. The KSZ9131RNX also provides pad skew values to adjust the delays if needed.



MTHOLE 4-40 120DL 220PAD



 <b>MICROCHIP</b>		Microchip Technology, Inc. USB/Network Group - UNG www.Microchip.com	Designed with  <b>Altium</b> Altium.com
Description: <b>KSZ9131RNX Reference Design</b>		Variant: <b>[No Variations]</b>	
Page Title: *			
Project Name: <b>KSZ9131RNX Ref. Design</b>		PN: <b>KSZ9131RNX</b>	
Size: B	Date: <b>1/3/2020</b>	Designer: <b>J. MacKay</b>	Sheet 4 of 4 Rev 1