

Shenzhen Rongpin Electronic Technology Co., Ltd.

SPECIFICATION

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	approve	review	examine	prepared by
sign				

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Chapter 1 Product Overview

1.1 Scope of application

- .Industrial control (power, assembly line automation)
- .Smart home (gateway, control panel)
- .Human-computer interaction, automatic vending machines, smart express cabinets
- .Smart hardware

1.2 Product Overview

The core board adopts Allwinner T113 dual-core CortexTM-A7 CPU, equipped with Linux system

System, A35 main frequency 1G, built-in 128M DDR3 memory, standard 4GB eMMC memory

storage. T113-S3 supports full format decoding, such as H.265, H.264, MPEG-1/2/4, JPEG, VC1, etc. A separate hardware encoder can encode in JPEG or MJPEG.

Integrates multiple adc/DACs and I2S/PCM/DMIC/OWA audio interface, supports RGB

The display screen, the core board leads to all functions, supports Ethernet, USB, serial port, is your human-machine

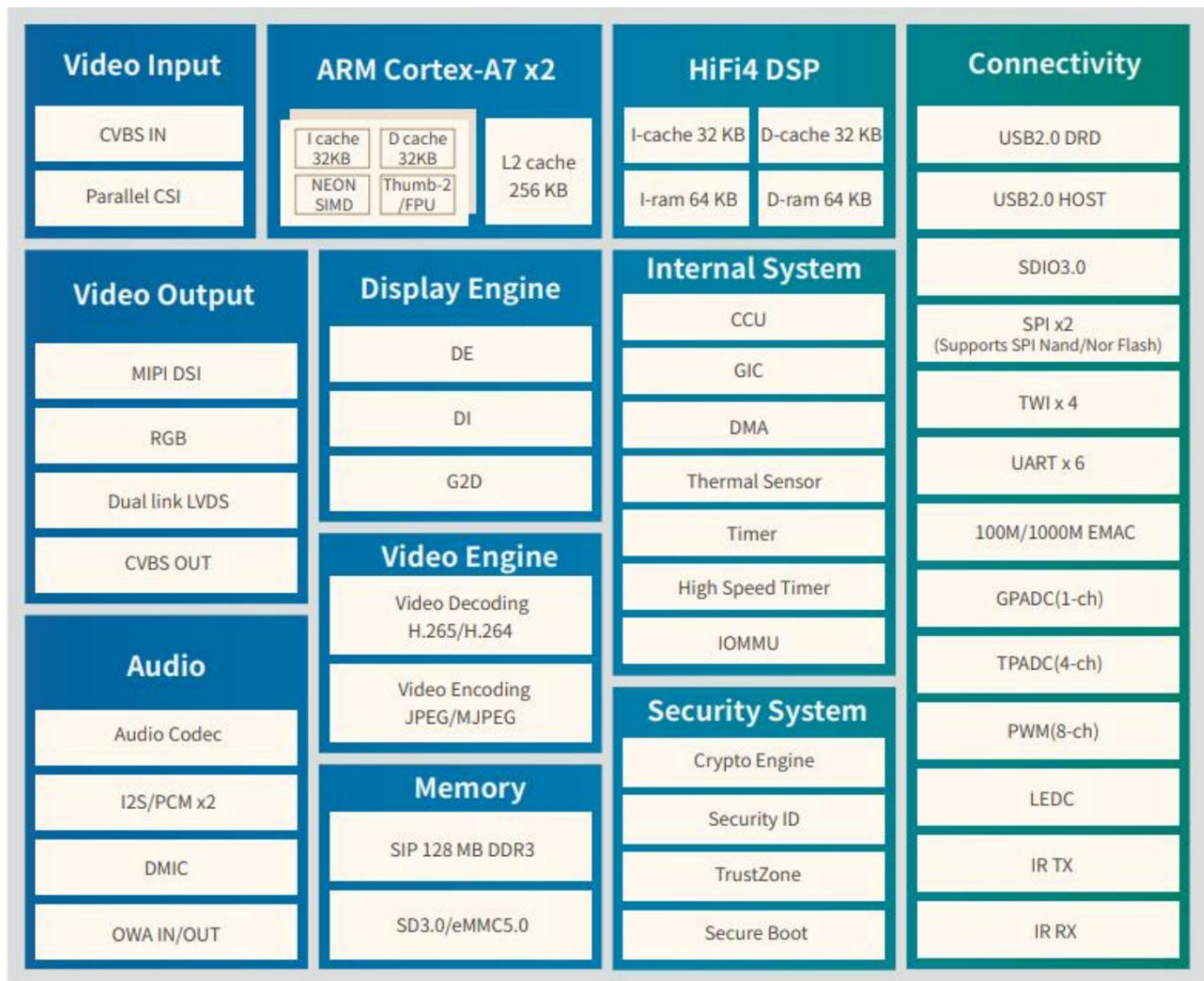
The best choice for interactive and industrial control projects.

1.3 Product Features

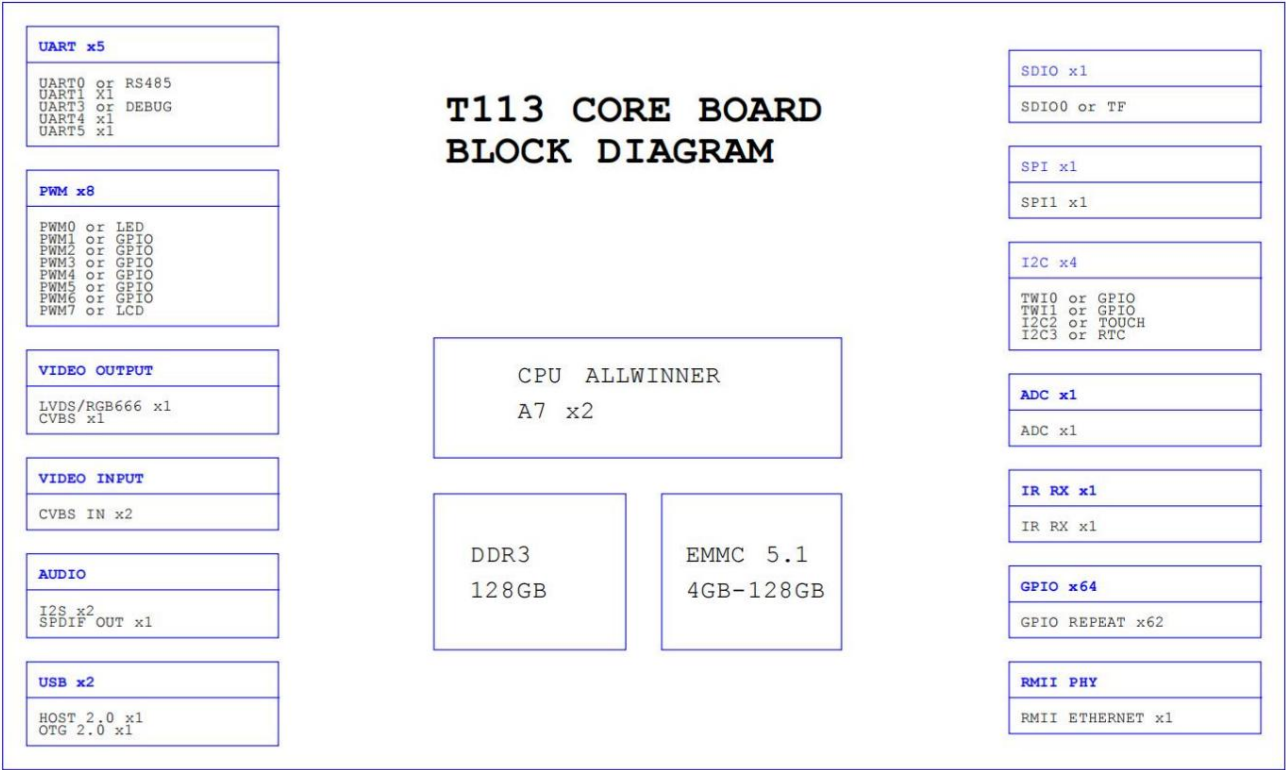
- Stamp hole core board, the size is 40mmx30mmx3mm, leading to all functions
- Support 1 channel CVBS output, 2 channels CVBS input.
- Support Linux system customization, provide system call interface API reference code, perfect support

Client upper layer application APP development and SDK.

1.4 Main chip block diagram



1.5 Core board block diagram

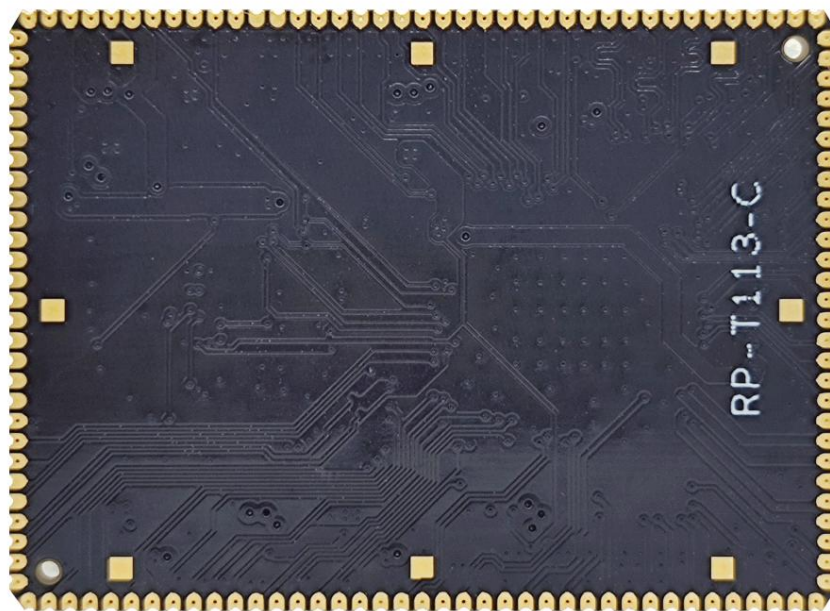


1.6 Appearance

front



reverse side



With shield



1.7 Function and Driver Support List

RP-T113 function and driver support list	
	buildroot Linux4.4.143
hardware function	
RGB interface	ÿ
USB	ÿ
GPIOs	ÿ
ADC button	ÿ
RTL8723 WIFI	ÿ
RTL8723BT4.2	ÿ
Ethernet 10M/100M/1000M	ÿ
earphone	ÿ
line out	ÿ
serial port	ÿ
RTC	ÿ
I2S_4ch input	
USB2.0	ÿ
CAN	ÿ
RS485	ÿ
bus driver	
ADC driver	ÿ
PWM driver	ÿ
SDIO driver	ÿ
GPIO driver	ÿ
USB driver	ÿ
can driver	ÿ
i2s driver	ÿ
i2c driver	ÿ
spi driver	ÿ

Chapter 2 List of Basic Functions

Main hardware indicators	
size	40mm length*30mm width*3mm height
connection method	stamp hole
CPU	AIWINNER RPT113 Dual Core ARM CortexTM-A7 CPU
Memory	Built-in 128MB DDR3
memory	EMMC 5.1 standard 4GB optional 8G/16G/32G
power management	discrete design
Operating Voltage	3.4-5.5V
support system	Linux5.4 QT5.12.5
Operating temperature	-25 to +85 degrees
life	Continuous operating life of more than 5 years

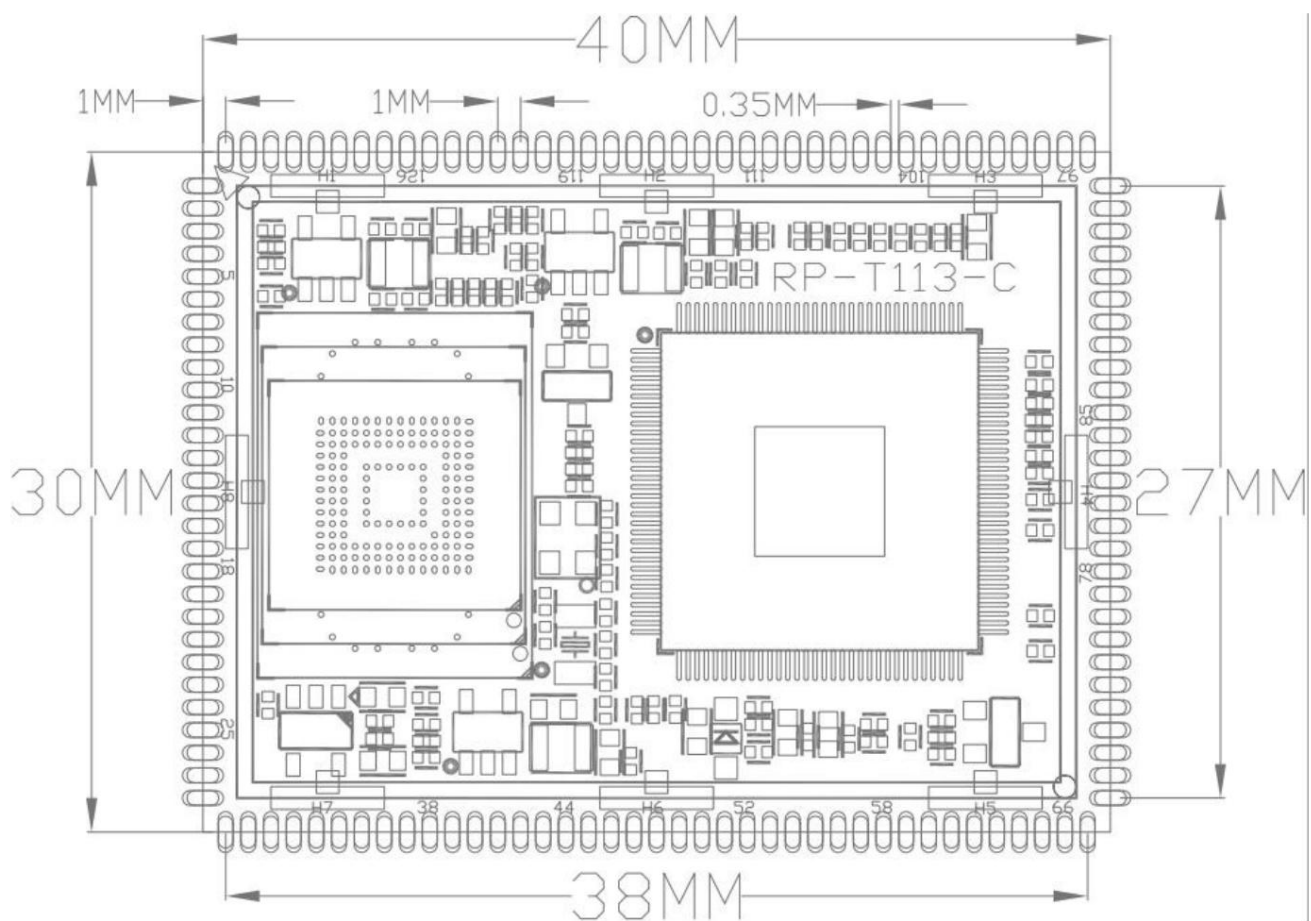
Core board common interface	
RGB	RGB666 output up to 720P
LVDS	Support single 6/8 LVDS output up to 1280x800
ethernet	Support Ethernet 100M RMII interface
CVBS input	Support two CVBS analog camera input
CVBS output	Support one CVBS output
I2S	Two I2S, one 8-channel/one 2-channel
voice	Support 1 left and right channel output
SDIO	Support one SDIO 3.0 interface
USB 2.0	1 independent USB 2.0
UART	5 serial ports
SPI	1 way SPI
I2C	4-way I2C
PWM	8-way PWM
ADC	1 channel analog ADC input interface
GPIOs	Multiplexable GPIO up to 62
upgrade	Support USB/TF card local upgrade

Chapter 3 PCB Dimensions and Interface Definition

front

PCB: 4-layer board

Size: 40mm*30mm*3mm



0mm*30mm*3mm

Chapter 4 Definition of Core Board Interface

Pin name	default function	I/O voltage configuration	configurable state can be reused for other functions	
1	GND			grounding
2	SDC0-DET	VCC-PF 3V3 I/O PF6	SPDIF_OUT/IR_RX/I2S2_MCLK/PWM5/PF_EINT6	
3	SDC0-D1	VCC-PF 3V3 I/O PF0	SDC0_D1/JTAG_MS/R_TAG_MS/I2S2_DOUT1/I2S2_DIN0/PF_EINT0	
4	SDC0-D0	VCC-PF 3V3 I/O PF1	SDC0_D0/JTAG_DI/R_TAG_DI/I2S2_DOUT0/I2S2_DIN1/PF_EINT1	
5	SDC0-CLK	VCC-PF 3V3 I/O PF2	SDC0_CLK/UART0_TX/TWI0_SCK/LED0/SPDIF_IN/PF_EINT2	
6	SDC0-CMD	VCC-PF 3V3 I/O PF3	SDC0_CMD/JTAG_DO/R_TAG_DO/I2S2_BCLK/PF_EINT3	
7	SDC0-D3	VCC-PF 3V3 I/O PF4	SDC0_D3/UART0_RX/TWI0_SDA/PWM6/IR_TX/PF_EINT4	
8	SDC0-D2	VCC-PF 3V3 I/O PF5	SDC0_D2/JTAG_CK/R_TAG_CK/I2S2_LRCK/PF_EINT5	
9	GND			grounding
10				no function
11				no function
12				no function
13				no function
14				no function
15				no function
16				no function
17				no function
18				no function
19				no function
20				no function
				no function
				no function
				no function
				no function
25				no function
26				no function
27	GND			grounding
28	VSYS	3V4-5V5 input		Main power input 3.4V-5.5V
29	GND			grounding
30	VCC-3V3	3V3	output	3.3V output 500mA
31	GND			grounding
32	VCC-1V8	1V8	output	1.8V output 80mA
33	GND			grounding
34	AVCC	1V8	output	1.8V output 100mA
35	EMMC_KEY	1V8-3V3 input		upgrade button

36	POWER_EN	3V4-5V5 input		boot enable
37	KEY_RST	3v3	enter	reset button
38	AP-CK24M-OUT	1V8	output	24M clock output
39	GND			grounding
40				no function
41				no function
42	PE13	VCC-PE 3V3 I/O	PE13/TWI2_SDA/PWM5/I2S0_DOUT0/I2S0_DIN1/DMIC_DATA3/RGMII_RXD2/PE_EINT13	
43	PE12	VCC-PE 3V3 I/O	PE12/TWI2_SCK/NCS0_FIELD/I2S0_DOUT2/I2S0_DIN2/RGMII_TXD3/PE_EINT12	
44	RXD1	VCC-PE 3V3 I/O	PE11/NCSI0_D7/UART1_RX/I2S0_DOUT3/I2S0_DIN3/JTAG_CK/RGMII_TXD2/PE_EINT11	
45	TXD1	VCC-PE 3V3 I/O	PE10/NCSI0_D6/UART1_TX/PWM4/IR_RX/JTAG_DO/EPHY_25M/PE_EINT10	
46	RXD3	VCC-PE 3V3 I/O	PE9/NCSI0_D5/UART1_CTS/PWM3/UART3_RX/JTAG_DI/MDIO/PE_EINT9	
47	TXD3	VCC-PE 3V3 I/O	PE8/NCSI0_D4/UART1_RTS/PWM2/UART3_TX/JTAG_MS/MDC/PE_EINT8	
48	RXD5	VCC-PE 3V3 input and output		PE7/NCSI0_D3/UART5_RX/TWI3_SDA/SPDIF_OUT/D_JTAG_CK/R_JTAG_CK/RGMII_CLKIN/RMII_RXER/PE_EINT7
49	TXD5	VCC-PE 3V3 input and output		PE6/NCSI0_D2/UART5_TX/TWI3_SCK/SPDIF_IN/D_JTAG_DO/R_JTAG_DO/RGMII_TXCTRL/RMII_TXEN/PE_EINT6
50	RXD4	VCC-PE 3V3 input and output		PE5/NCSI0_D1/UART4_RX/TWI2_SDA/LEDC_DO/D_JTAG_DI/R_JTAG_DI/RGMII_TXD1/RMII_TXD1/PE_EINT5
51	TXD4	VCC-PE 3V3 input and output		PE4/NCSI0_D0/UART4_TX/TWI2_SCK/CLK_FANOUT2/D_JTAG_MS/R_JTAG_MS/RGMII_TXD0/RMII_TXD0/PE_EINT4
52	RXD0	VCC-PE 3V3 input and output		PE3/NCSI0_MCLK/UART2_RX/TWI0_SDA/CLK_FANOUT1/UART0_RX/RGMII_TXCK/RMII_TXCK/PE_EINT3
53	TXD0	VCC-PE 3V3 input and output		PE2/NCSI0_PCLK/UART2_TX/TWI0_SCK/CLK_FANOUT0/UART0_TX/RGMII_RXD1/RMII_RXD1/PE_EINT2
54	PE1	VCC-PE 3V3 I/O	PE1/NCSI0_VSYNC/UART2_CTS/TWI1_SDA/LCD0_VSYNC/RGMII_RXD0/RMII_RXD0/PE_EINT1	
55	PE0	VCC-PE 3V3 input and output		PE0/NCSI0_HSYNC/UART2_RTS/TWI1_SCK/LCD0_HSYNC/RGMII_RXCTRL/RMII_CRS_DV/PE_EINT0
56	GND		Input and output ground	
57	LVDS0-V0P	VCC-PD 3V3 I/O	PD0/LCD0_D2/LVDS0_V0P/DSI_D0P/TWI0_SCK/PD_EINT0	
58	LVDS0-V0N	VCC-PD 3V3 I/O	PD1/LCD0_D3/LVDS0_V0N/DSI_D0N/UART2_TX/PD_EINT1	
59	LVDS0-V1P	VCC-PD 3V3 I/O	PD2/LCD0_D4/LVDS0_V1P/DSI_D1P/UART2_RX/PD_EINT2	
60	LVDS0-V1N	VCC-PD 3V3 I/O	PD3/LCD0_D5/LVDS0_V1N/DSI_D1N/UART2_RTS/PD_EINT3	
61	LVDS0-V2P	VCC-PD 3V3 I/O	PD4/LCD0_D6/LVDS0_V2P/DSI_CK/PD_EINT4	
62	LVDS0-V2N	VCC-PD 3V3 I/O	PD5/LCD0_D7/LVDS0_V2N/DSI_CKN/UART5_TX/PD_EINT5	
63	LVDS0-CKP	VCC-PD 3V3 I/O	PD6/LCD0_D10/LVDS0_CK/DSI_D2P/UART5_RX/PD_EINT6	
64	LVDS0-CKN	VCC-PD 3V3 I/O	PD7/LCD0_D11/LVDS0_CKN/DSI_D2N/UART4_TX/PD_EINT7	
65	LVDS0-V3P	VCC-PD 3V3 I/O	PD8/LCD0_D12/LVDS0_V3P/DSI_D3P/UART4_RX/PD_EINT8	
66	LVDS0-V3N	VCC-PD 3V3 I/O	PD9/LCD0_D13/LVDS0_V3N/DSI_D3N/PWM6/PD_EINT9	
67	SPI1_CS	VCC-PD 3V3 I/O	PD10/LCD0_D14/LVDS0_V0P/SPI1_CS/DBI_CSX/UART3_TX/PD_EINT10	
68	SPI1_CLK	VCC-PD 3V3 I/O	PD11/LCD0_D15/LVDS0_V0N/SPI1_CLK/DBI_SCLK/UART3_RX/PD_EINT11	
69	SPI1_MOSI	VCC-PD 3V3 I/O	PD12/LCD0_D18/LVDS0_V1P/SPI1_MOSI/DBI_SDO/TWI0_SDA/PD_EINT12	

70	SPI1_MISO	VCC-PD 3V3 I/O PD13/LCD0_D19/LVDS1	V1N/SPI1_MISO/DBI_SDI/DBI_TE/DBI_DCX/UART3_RTS/PD_EINT13
71	USB_DET	VCC-PD 3V3 I/O PD14/LCD0_D20/LVDS1	V2P/SPI1_HOLD/DBI_DCX/DBI_WRX/UART3_CTS/PD_EINT14
72	PD15	VCC-PD 3V3 I/O PD15/LCD0_D21/LVDS1	V2N/SPI1_WP/DBI_TE/IR_RX/PD_EINT15
73	PWM0	VCC-PD 3V3 I/O PD16/LCD0_D22/LVDS1	CKP/DMIC_DATA3/PWM0/PD_EINT16
74	PD17	VCC-PD 3V3 I/O PD17/LCD0_D23/LVDS1	CKN/DMIC_DATA2/PWM1/PD_EINT17
75	PD18	VCC-PD 3V3 I/O PD18/LCD0_CLK/LVDS1	V3P/DMIC_DATA1/PWM2/PD_EINT18
76	PD19	VCC-PD 3V3 I/O PD19/LCD0_DE/LVDS1	V3N/DMIC_DATA0/PWM3/PD_EINT19
77	TWI2_SCL	VCC-PD 3V3 I/O PD20/LCD0_HSYNC/TWI2_SCK/DMIC_CLK/PWM4/PD_EINT20	
78	TWI2_SDA	VCC-PD 3V3 I/O PD21/LCD0_VSYNC/TWI2_SDA/UART1_TX/PWM5/PD_EINT21	
79	PWM7	VCC-PD 3V3 I/O PD22/SPDIF_OUT/IR_RX/UART1_RX/PWM7/PD_EINT22	
80	GND		grounding
81	TWI3_SDA	VCC-PB 3V3 I/O PB7/LCD0_D17/I2S2_MCLK/TWI3_SDA/IR_RX/LCD0_D23/UART3_RX/CPUBIST1/PB_EINT7	
82	TWI3_SCL	VCC-PB 3V3 I/O PB6/LCD0_D16/I2S2_LRCK/TWI3_SCK/PWM1/LCD0_D22/UART3_TX/CPUBIST0/PB_EINT6	
83	CAN1-RX	VCC-PB 3V3 I/O PB5/LCD0_D9/I2S2_BCLK/TWI1_SDA/PWM0/LCD0_D21/UART5_RX/CAN1-RX0/PB_EINT5	
84	CAN1-TX	VCC-PB 3V3 input and output	PB4/LCD0_D8/I2S2_DOUT0/TWI1_SCK/I2S2_DIN1/LCD0_D20/UART5_TX/CAN1-TX0/PB_EINT4
85	CAN0-RX	VCC-PB 3V3 input and output	PB3/LCD0_D1/I2S2_DOUT1/TWI0_SCK/I2S2_DIN0/LCD0_D19/UART4_RX/CAN0-RX0/PB_EINT3
86	CAN0-TX	VCC-PB 3V3 input and output	PB2/LCD0_D0/I2S2_DOUT2/TWI0_SDA/I2S2_DIN2/LCD0_D18/UART4_TX/CAN0-TX0/PB_EINT2
87	GND		grounding
88	MICIN3N		enter Mic input negative
89	MICIN3P		enter Mic input positive
90	GND		grounding
91	FMINL		enter Voice into L
92	FMINR		enter Speech into R
93	GND		grounding
94	LINE INL		enter Voice into L
95	LINEINR		enter Speech into R
96	HPOUTFB		enter Headphone ground
97	HPOUTL		earphone left
98	HPOUTR		headphone right
99	GND		grounding
100	GPADC0	1V8	enter Analog ADC input
101	TP-X1		enter Resistive touch screen X1
102	TP-X2		enter Resistive touch screen X2
103	TP-Y1		enter Resistive touch screen Y1
104	TP-Y2		enter Resistive touch screen Y2
105	GND		grounding
106	TV-IN1		enter CVBS input 1



RONGPIN

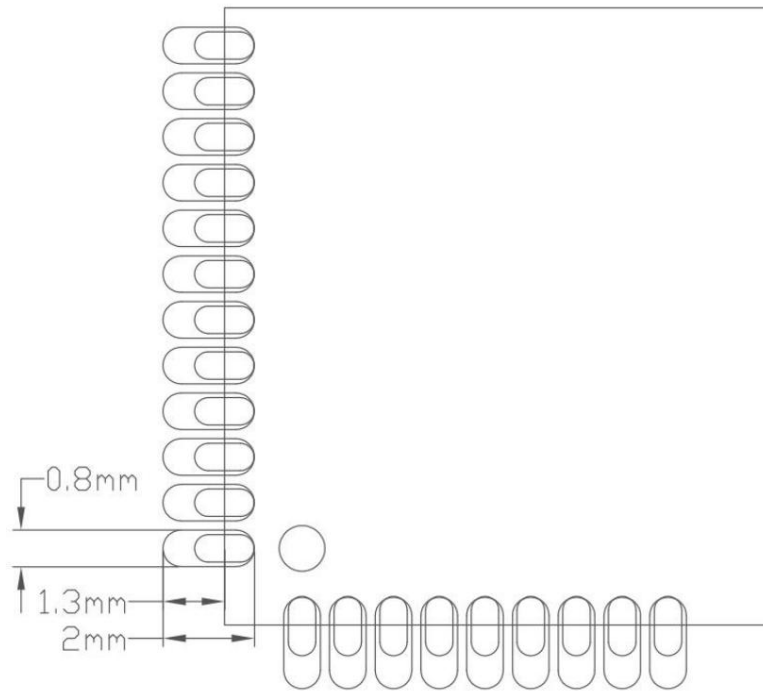
107	GND			grounding
108	TV-IN0		enter	CVBS input 0
109	GND			grounding
110	TV-OUT		output	CVBS output
111	GND			grounding
112	USB1-DP			USB1-DP
113	USB1-DM			USB1-DM
114	GND			GND
115	USB0-DM			OTG-DM
116	USB0-DP			OTG-DP
117	GND			grounding
118	RMII-MDIO	VCC-PG 3V3 I/O PG15/I2S1_DOUT0/TWI2_SDA/MDIO/I2S1_DIN1/SPI0_HOLD/UART1_CTS/PG_EINT15		
119	RMII-MDC	VCC-PG 3V3 I/O PG14/I2S1_DIN0/TWI2_SCK/MDC/I2S1_DOUT1/SPI0_WP/UART1_RTS/PG_EINT14		
120	RMII-RXER	VCC-PG 3V3 input and output		PG13/I2S1_BCLK/TWI0_SDA/RGMII_CLKIN/RMII_RXER/PWM2/LEDC_DO/UART1_RX/PG_EINT13
121	RMII-CRS-RXDV	VCC-PG 3V3 I/O PG0/SDC1_CLK/UART3_TX/RGMII_RXCTRL/RMII_CRS_DV/PWM7/PG_EINT0		
122	RMII-RXD0	VCC-PG 3V3 I/O PG1/SDC1_CMD/UART3_RX/RGMII_RXD0/RMII_RXD0/PWM6/PG_EINT1		
123	RMII-RXD1	VCC-PG 3V3 I/O PG2/SDC1_D0/UART3_RTS/RGMII_RXD1/RMII_RXD1/UART4_TX/PG_EINT2		
124	RMII-RXCK	VCC-PG 3V3 I/O PG10/PWM3/TWI3_SCK/RGMII_RXCK/CLK_FANOUT0/IR_RX/PG_EINT10		
125	RMII-TXCK	VCC-PG 3V3 I/O PG3/SDC1_D1/UART3_CTS/RGMII_TXCK/RMII_TXCK/UART4_RX/PG_EINT3		
126	RMII-TXD0	VCC-PG 3V3 I/O PG4/SDC1_D2/UART5_TX/RGMII_TXD0/RMII_TXD0/PWM5/PG_EINT4		
127	RMII-TXD1	VCC-PG 3V3 I/O PG5/SDC1_D3/UART5_RX/RGMII_TXD1/RMII_TXD1/PWM4/PG_EINT5		
128	RMII-TXEN	VCC-PG 3V3 input and output		PG12/I2S1_LRCK/TWI0_SCK/RGMII_TXCTRL/RMII_TXEN/CLK_FANOUT2/PWM0/UART1_TX/PG_EINT12
129	EPHY_25M	VCC-PG 3V3 I/O PG11/I2S1_MCLK/TWI3_SDA/EPHY_25M/CLK_FANOUT1/TCON_TRIG/PG_EINT11		
130	RMII-RESET	VCC-PG 3V3 I/O PG9/UART1_CTS/TWI1_SDA/RGMII_RXD3/UART3_RX/PG_EINT9		
131	PG8	VCC-PG 3V3 I/O PG8/UART1_RTS/TWI1_SCK/RGMII_RXD2/UART3_TX/PG_EINT8		
132	PG7	VCC-PG 3V3 I/O PG7/UART1_RX/TWI2_SDA/RGMII_TXD3/SPDIF_IN/PG_EINT7		
133	PG6	VCC-PG 3V3 I/O PG6/UART1_TX/TWI2_SCK/RGMII_TXD2/PWM1/PG_EINT6		
134	GND			grounding

Chapter 5 Current Parameter Table

Current parameter table

project		the smallest	typical	maximum
Power parameters	Voltage	3.4V	5V	5.5V
	ripple	--	50mV	
	RTC (HYM8563)	0.3uA	0.9uA	1.2uA
With backplane current test	Boot current	14mA	55mA	76mA
	Desktop Quiescent Current		38mA	
environment	Relative humidity	--	65%	75%
	Operating temperature	-25°C	--	85°C
	storage temperature	-40°C	-0°C	100°C

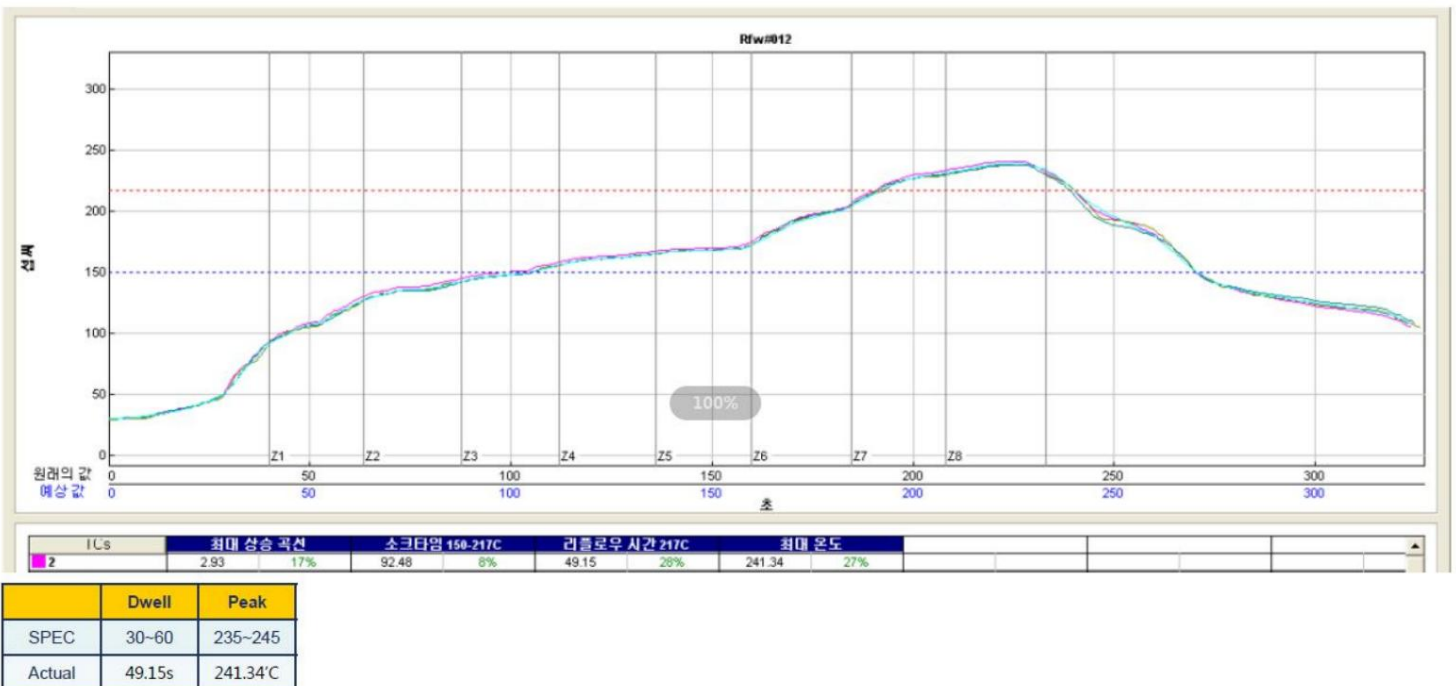
Chapter 6 Description of Stencil Opening Process



开钢网焊盘尺寸 $2\text{mm} \times 0.8\text{mm}$
增加爬锡量，保障焊接品质

Chapter 7 Core Board Secondary Welding Curve

Reflow Profile



Chapter 8 Precautions for Assembly and Use

Please pay attention to the following items for surface mount installation.

First, the production should try to filter out SMT patches. Electric soldering irons are prone to static electricity and may damage the pins of the core board.

Second, the mounting position should pay attention to the polarity.

The stencil mounted on the core board needs to refer to the stencil description in Chapter 6 above to increase the amount of tin climbing.