RL78/I1C

METER HARDWARE DESIGN GUIDE

(BASED ON 1 PHASE METER)

12TH APR 2023

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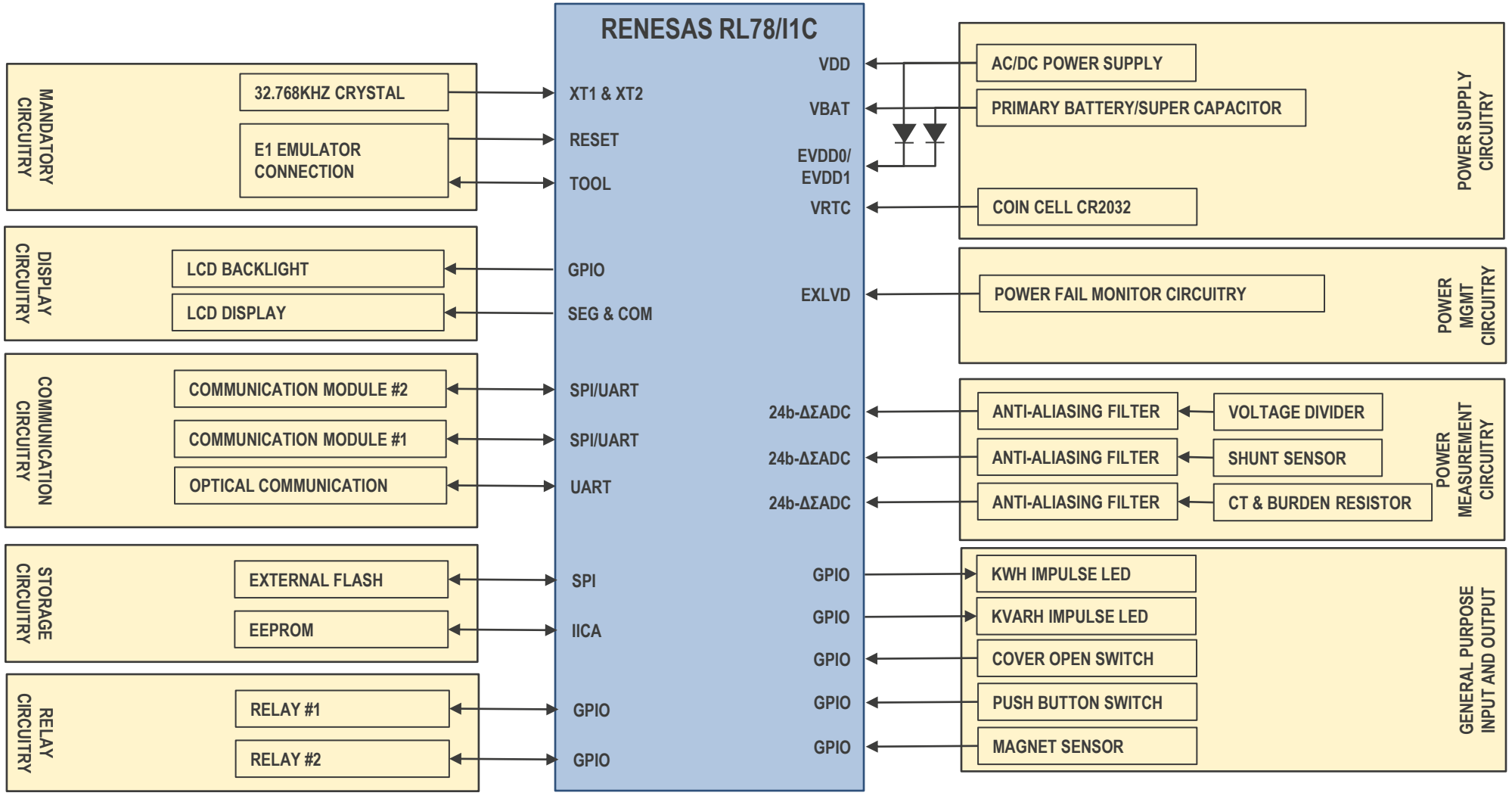
AGENDA

RL78/I1C SINGLE PHASE HARDWARE DESIGN

BLOCK DIAGRAM



RL78/I1C MANDATORY HARDWARE CONNECTION

POWER SUPPLY CONNECTION

RL78/I1C has 4 types Power Supply Inputs

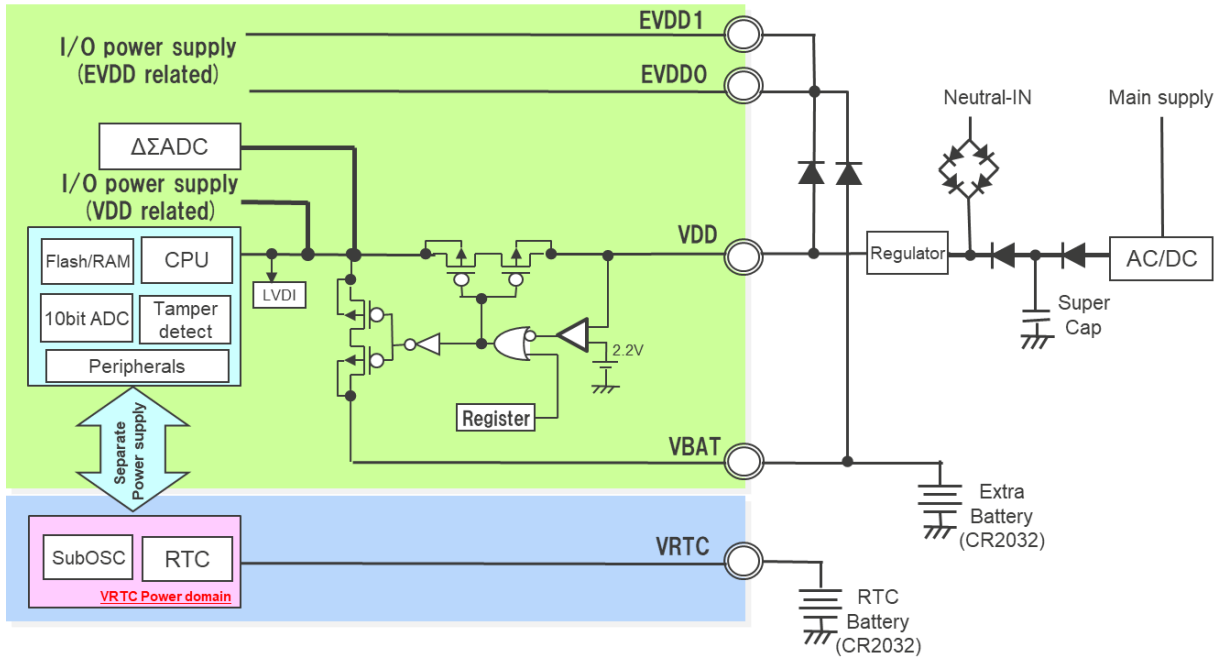
a. VDD :
- Power Supply to MCU core and peripherals (except RTC)
- Supply Range from 1.9V to 5.5V (LS Mode)

b. EVDD0/EVDD1 :
- Power Supply to GPIO (except Port 2 and Port 15)
- Supply Range from 1.9V to 5.5V

c. VBAT:
- Backup Power Supply to MCU core and peripherals (except RTC)
- Supply Range from 1.9V to 5.5V (LS Mode)

d. VRTC :
- Independent Power Supply for RTC and 32.768kHz Crystal (Sub-clock)
- Supply Range from 1.6V to 5.5V

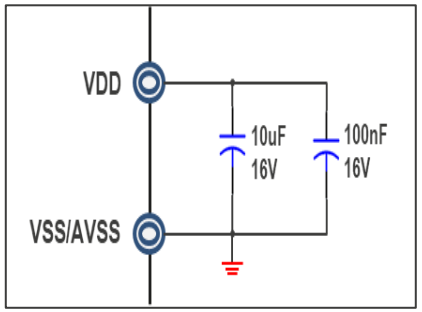
e. VSS/AVSS :
- MCU Reference Ground and ΔΣ-ADC Ground



MANDATORY CONNECTION IN VDD DOMIAN

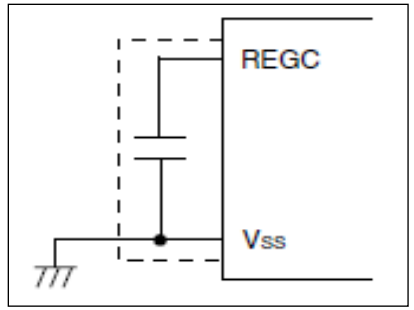
POWER SUPPLY CONNECTION

1. For Power Supply, recommended connection of **10uF + 0.1uF** as stabilization capacitance between VDD to VSS/AVSS as stabilization capacitance.



2. RL78/I1C contains a circuit for operating the device with a constant voltage. In order to stabilize the **regulator output voltage**, connect the REGC pin to VSS via a **capacitor 0.47 to 1uF**. Also, use a capacitor with good characteristic as it is used to stabilized internal voltage. Recommendation is to use capacitor **type X7R**.

3. RL78/I1C has a battery backup internal switching function. This monitors the supply voltage of VDD pin, and switches to **VBAT supply** pin when voltage at VDD pin falls below the **detection threshold (~2.2V)** at maximum **response time of 500us**. If the this function is not used, please connect VBAT pin to VSS.



When VBAT supply is used during ΔΣ-ADC, please make sure the backup battery has at least the capacitance of 10uF + 0.1uF

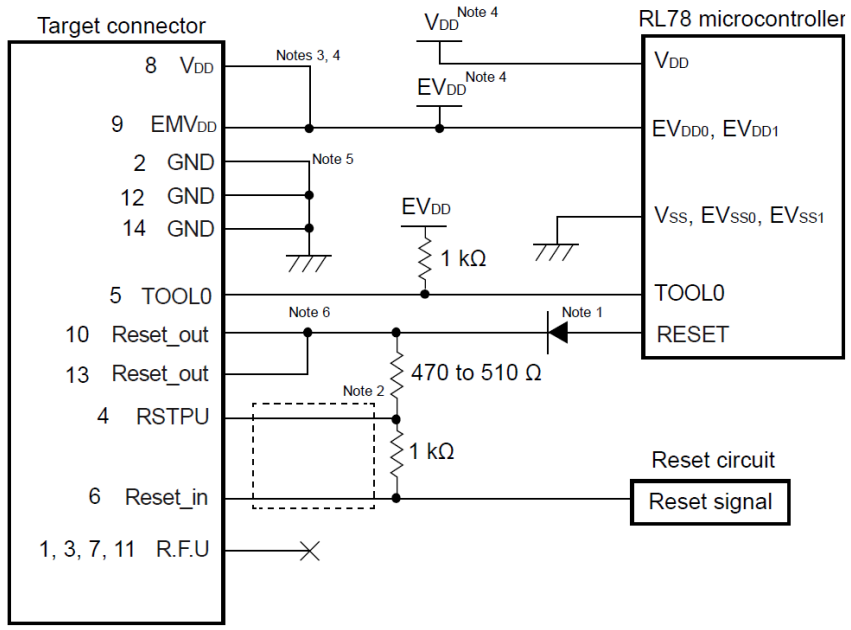
4. EVDD0/EVDD1 must be connected to VDD. If GPIO (except port 2, port 15 and P137) is using during VBAT supply, EVDD0/EVDD1 shall be connect to VBAT also to avoid potential voltage difference.

MANDATORY CONNECTION IN VDD DOMIAN

E1/E2LITE EMULATOR CONNECTION

RL78/I1C can be programmed and debugged via E1 and E2 Lite Emulator. 4 signals shown below are to be connected to Emulator for Flash programming and debugging purpose.

1. VDD/EVDD
   - ❑ Normally connected to Emulator pin 8 & 9
2. RESET
   - ❑ Do not connect pull up resistor to RESET pin as there is internal pull up resistor from internal VDD (VDD/VBAT). Diode connection is recommended to avoid voltage potential difference and only allowing RESET pin to be pulled low
3. TOOL0
   - ❑ Pull-up resistor of 1K to 3.9K is required.
4. GND
   - ❑ Normally connected to Emulator pin 2, 12 & 14



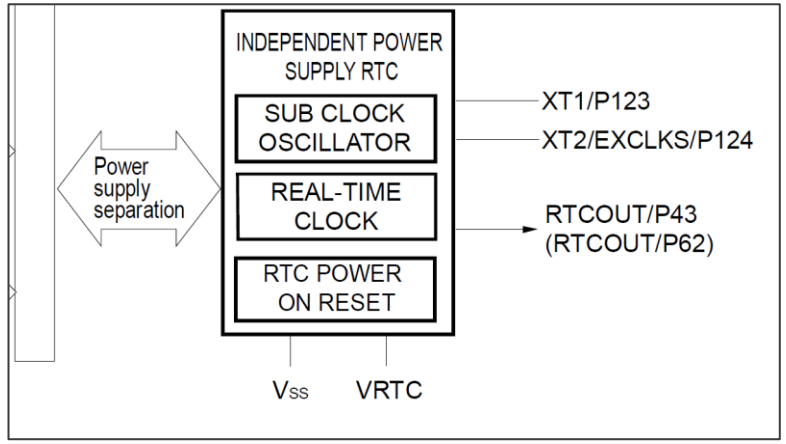
Please refer details to RL78/I1C UM r01uh0587ej0210-rl78i1c.pdf Chapter 37.1

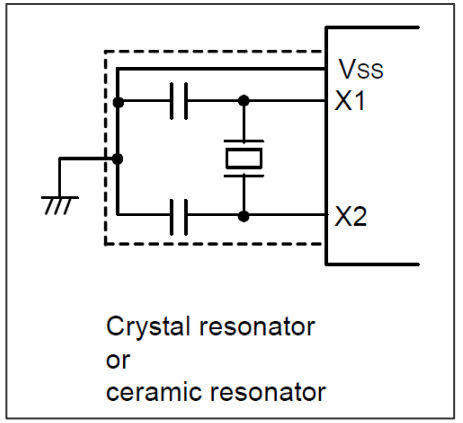
MANDATORY CONNECTION IN RTC DOMAIN

POWER SUPPLY AND CRYSTAL CONNECTION

Independent Power Supply RTC domain is powered by VRTC. It only has 3 elements, which is

1. Sub-clock Oscillator
   - Normally connected to 32.768kHz crystal to XT1 and XT2.
2. Real Time Clock
   - RTCOUT only has output due to limitation of GPIO as P43 and P62 is supply by EVDD
3. RTC Power On Reset
   - Power on reset will clear to 0 once voltage level of VRTC < 1.6V.



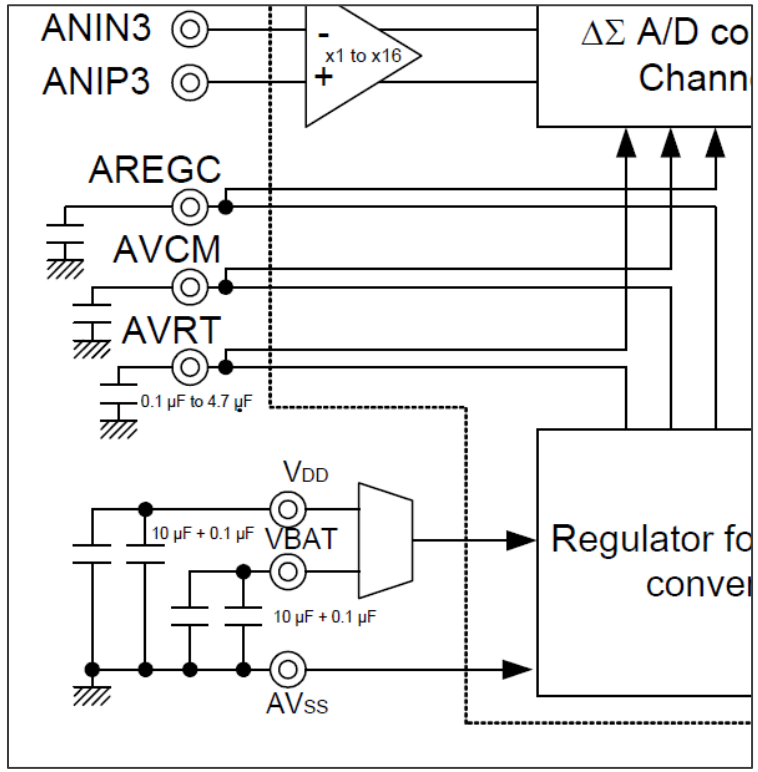


RL78/I1C POWER MEASUREMENT DESIGN

MANDATORY CONNECTION IN ΔΣ-ADC

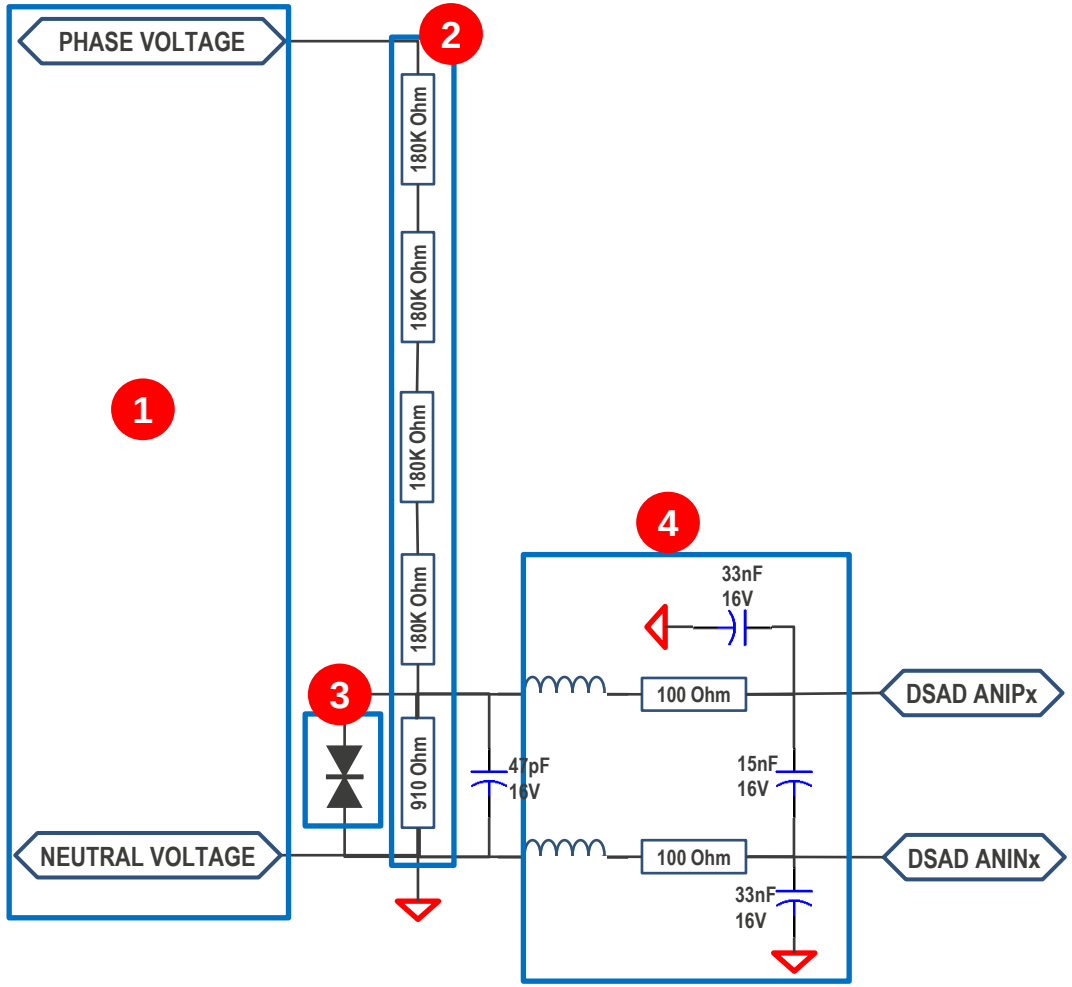
POWER SUPPLY AND VOLTAGE REFERENCE

1. For **Analog Power Supply**, since it is connected internally to internal VDD. Please connect capacitors of **10 µF + 0.1 µF** as stabilization capacitance between the VDD/VBAT and AVSS pins as shown in diagram.
2. Recommended connection of pins of AVRT, AVCM and AREGC are just connecting AV_{SS} via capacitor **470nF** type X7R.
3. Recommendation of Vss and AVss to be split by 0R Resistor or Inductor (depend on noise level)



MANDATORY CONNECTION IN ΔΣ-ADC

VOLTAGE MEASUREMENTS CIRCUITRY

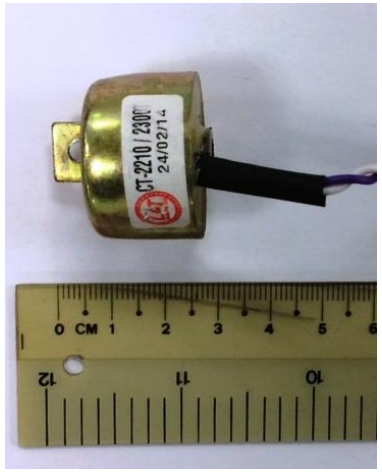


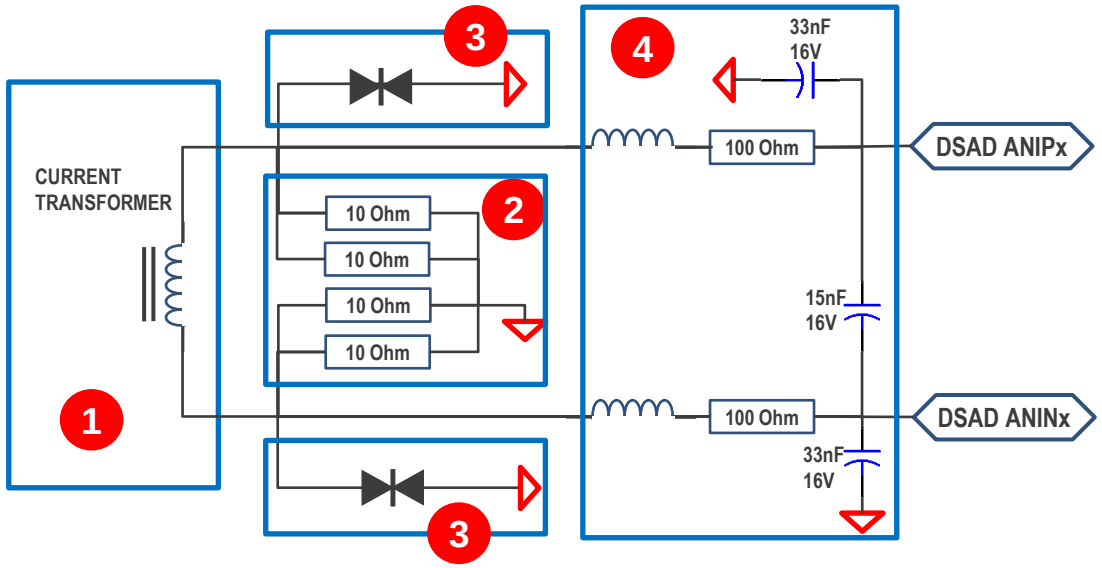
Voltage Measurement on RL78/I1C consist of 4 parts

1. Voltage Input
   - Voltage measurement input, normally direct from meter terminal supply. Range from 85VAC to 285Vac
2. Voltage Divider
   - To step down the voltage level from AC power supply to the range of measurements, maximum ± 0.5V
3. ESD Protection
   - ESD protection to ensure the input signal not exceeded 0.5V
4. Anti-aliasing Filter
   - Anti-aliasing filter is a LPF which include the impedance matching for the DSAD.

MANDATORY CONNECTION IN ΔΣ-ADC

CURRENT MEASUREMENT CIRCUITRY – CURRENT TRANSFORMER



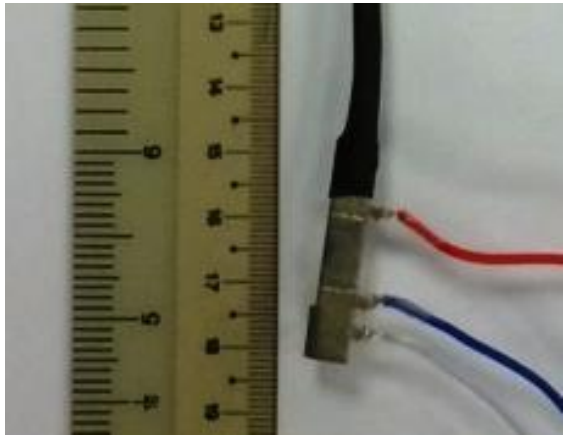


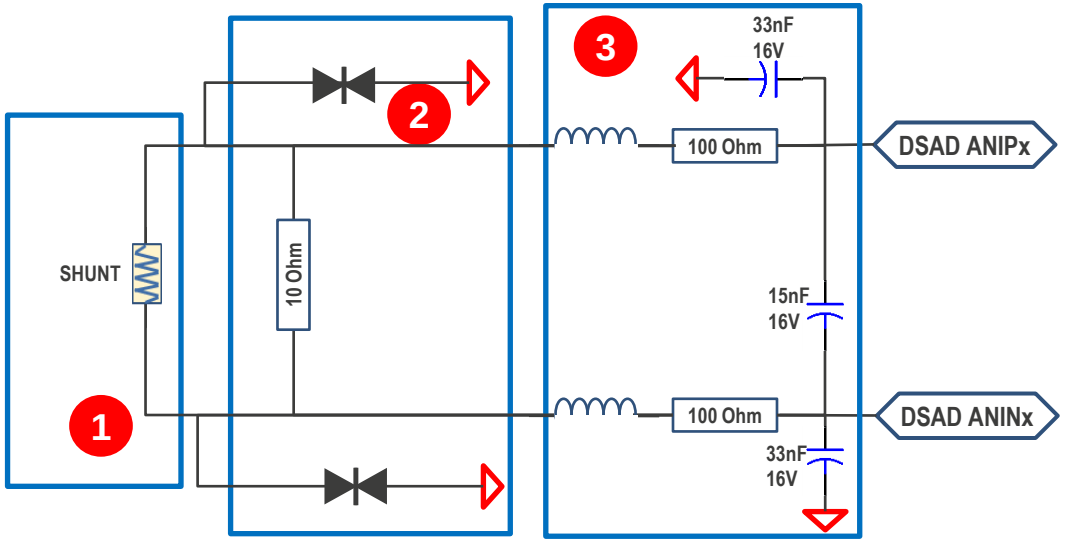
Current Measurement on RL78/I1C consist of 4 parts:

1. Current Sensor
   - Current sensor which here refer to current transformer, which steps down the current depends of the dynamic range of measurements. For 60A max meter, normally uses 3000:1 ratio CT.
2. Burden Resistance
   - Resistance uses to convert current measured to representing voltage level. Selection of resistors depends on dynamic range, which Vmax = 0.5V
3. ESD Protection
   - ESD protection to ensure the input signal not exceeded 0.5V
4. Anti-aliasing Filter
   - Anti-aliasing filter is a LPF which include the impedance matching for the DSAD.

MANDATORY CONNECTION IN ΔΣ-ADC

CURRENT MEASUREMENT CIRCUITRY – SHUNT





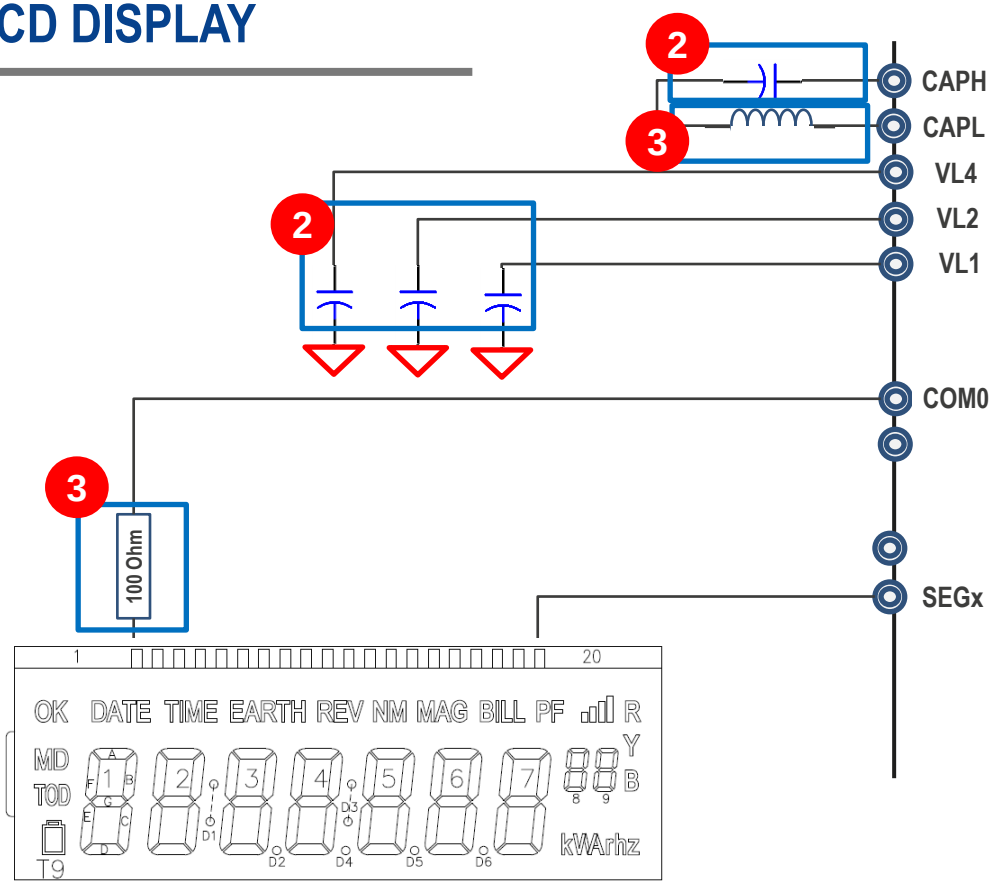
Current Measurement on RL78/I1C consist of 4 parts:

1. Current Sensor
   - Current sensor which here refer to shunt, which directly convert the current flow through it to representing voltage level.
   - Value of shunt depends on current measurements dynamic range. For < 100A measurements, 220 micro-ohms shunt is selected.
2. ESD Protection
   - ESD protection to ensure the input signal not exceeded 0.5V
3. Anti-aliasing Filter
   - Anti-aliasing filter is a LPF which include the impedance matching for the DSAD.

RL78/I1C PERIPHERAL DESIGN

MANDATORY PERIPHERAL DESIGN

LCD DISPLAY



PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
COM1								COM1	REV	1A	2A	3A	4A	5A	6A	7A	8A	9A	T10	T8
COM2							COM2		EARTH	1B	2B	3B	4B	5B	6B	7B	8B	9B	T11	T7
COM3						COM3			TIME	1F	2F	3F	4F	5F	6F	7F	8F	9F	T12	T6
COM4					COM4				DATE	1G	2G	3G	4G	5G	6G	7G	8G	9G	T13	T5
COM5				COM5					OK	1C	2C	3C	4C	5C	6C	7C	8C	9C	R	T4
COM6			COM6						MD	1E	2E	3E	4E	5E	6E	7E	8E	9E	Y	T3
COM7		COM7							TOD	1D	2D	3D	4D	5D	6D	7D	8D	9D	B	T2
COM8	COM8								T9	D4	D1	D2	D3	D5	D6	NM	MAG	BILL	PF	T1

Example given for the Display design as below LCD specification

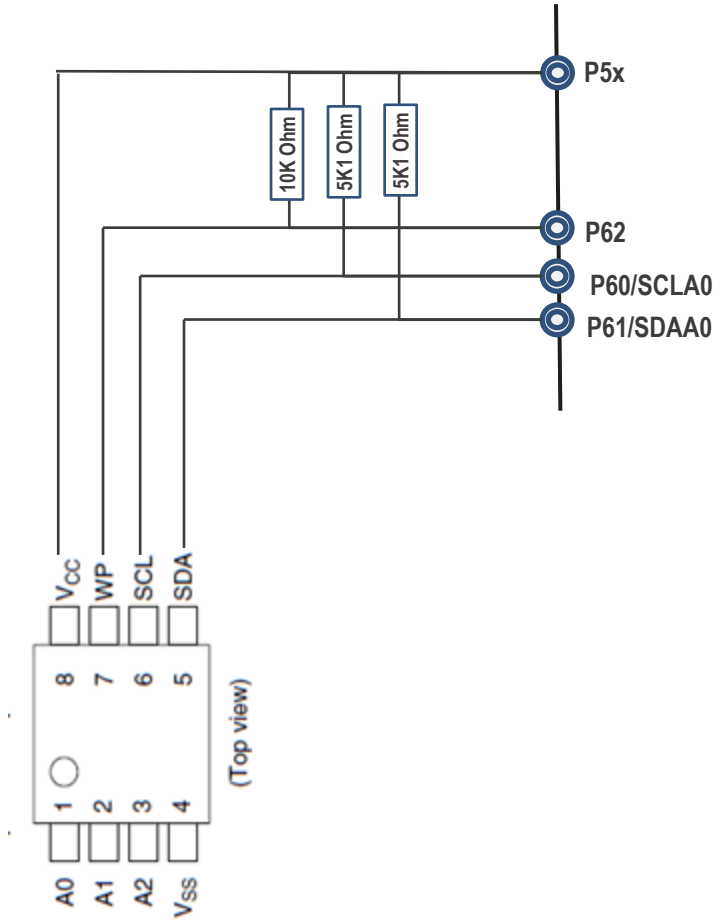
- ❑ 3.0V 64Hz, 1/8 duty, 1/3 bias, 96 segment

Hardware design recommendation as below:

1. Uses RL78/I1C LCD driver voltage generator – Internal Voltage Boosting method to ensure constant LCD contrast regardless of Internal VDD voltage fluctuation
2. Mandatory connection of capacitors 470nF capacitors to VL1, VL2, VL3 and between CAPH and CAPL
3. For better EMC immunity,
   - ❑ Connect ferrite bead between CAPL and 470nF capacitor
   - ❑ Connect damping resistor to all COMs pin only of LCD.

MANDATORY PERIPHERAL DESIGN

STORAGE – EEPROM



RL78/I1C has a master IIC channel which can connect multiple devices

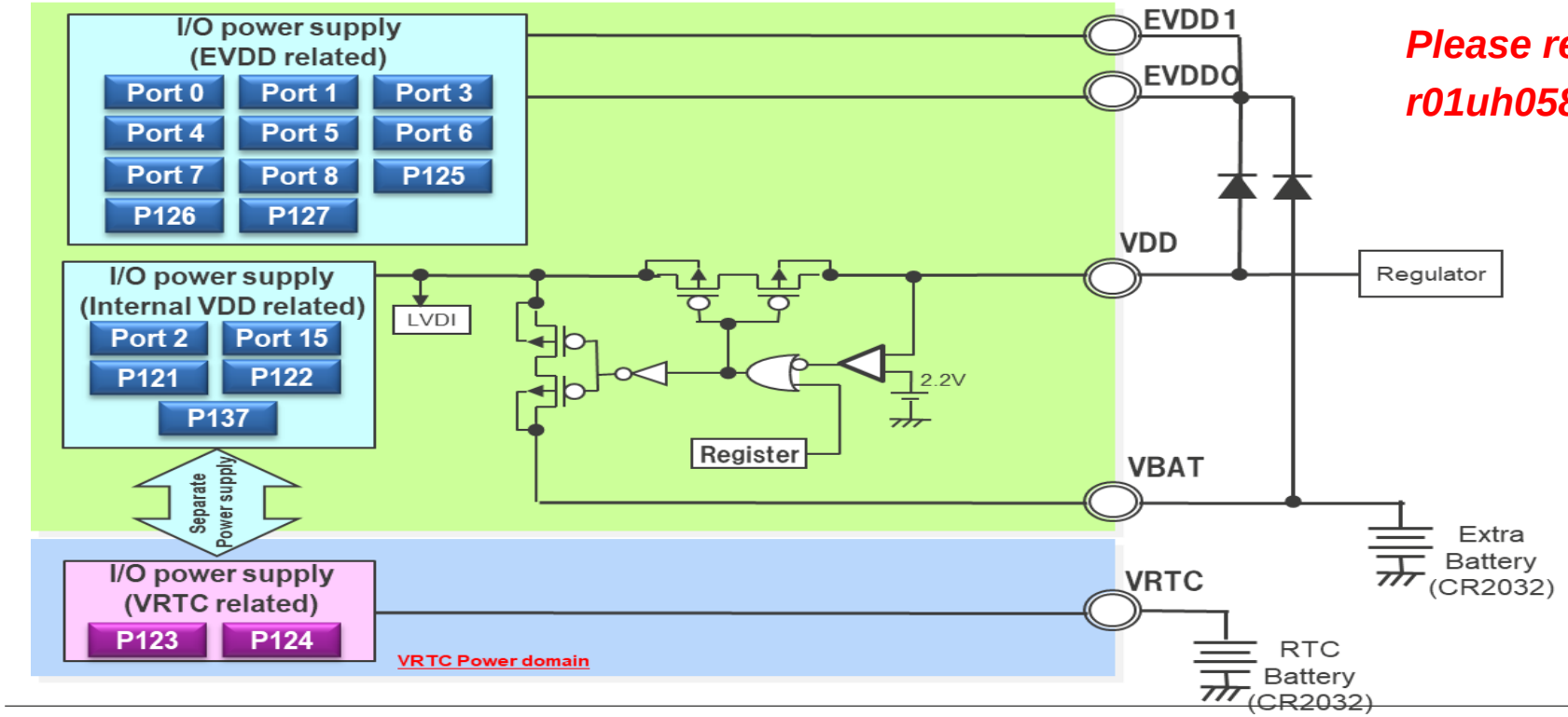
1. If power up EEPROM by Port power, please select port 1, 3, 5, 7, 8 for better pin configuration
2. All Port 6 pin need pull-up as internally it is an open drain GPIO. This include master IICA pin

PRECAUTION ON GPIO

POWER SOURCE FOR GPIO

Please take note of the power source which supplies each port and pin as shown.

Power Supply	Corresponding Pins
EV_{DD}	Port pins other than P20 to P23, P121 to P124, P137 and P150 to P152[Note 1]
V_{DD} or VBAT[Notes 2, 3]	• P20 to P23, P121, P122, P137, and P150 to P152 • RTCIC0 to RTCIC2 • $\overline{\text{RESET}}$, REGC • ANIP0 to ANIP2, ANIN0 to ANIN2
VRTC	P123, P124



Please refer details to RL78/I1C UM r01uh0587ej0210-rl78i1c.pdf Chapter 2.1

PRECAUTION ON GPIO

CURRENT LIMITS

Please take note of total pin current limitation.

When GPIO duty is more than 70%, please use the below to re-calculate the current limit. (n = to desire duty)

Total output current of pins = (IOH × 0.7)/(n × 0.01)

(T_A = –40 to +85°C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}[Note 4] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P02 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P57, P70 to P77, P80 to P85, P125 to P127	1.9 V ≤ EV_{DD} ≤ 5.5 V			–10.0[Note 2]	mA
		Total of P02 to P07, P40 to P43 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV_{DD} ≤ 5.5 V			–55.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–10.0	mA
			1.9 V ≤ EV_{DD} < 2.7 V			–5.0	mA
			1.7 V ≤ EV_{DD} < 1.9 V			–2.5	mA
		Total of P10 to P17, P30 to P37, P50 to P57, P70 to P77, P80 to P85, P125 to P127 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV_{DD} ≤ 5.5 V			–80.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–19.0	mA
			1.9 V ≤ EV_{DD} < 2.7 V			–10.0	mA
			1.7 V ≤ EV_{DD} < 1.9 V			–5.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])				–100.0	mA
	I_{OH2}	Per pin for P20 to P25, P150 to P152	1.7 V ≤ V_{DD}[Note 4] ≤ 5.5 V			–0.1[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	1.7 V ≤ V_{DD}[Note 4] ≤ 5.5 V			–0.9	mA

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P02 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P57, P70 to P77, P80 to P85, P125 to P127				20.0[Note 2]	mA
		Per pin for P60 to P62				15.0[Note 2]	mA
		Total of P02 to P07, P40 to P43 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV_{DD} ≤ 5.5 V			70.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			15.0	mA
			1.9 V ≤ EV_{DD} < 2.7 V			9.0	mA
			1.7 V ≤ EV_{DD} < 1.9 V			4.5	mA
		Total of P10 to P17, P30 to P37, P50 to P57, P60 to P62, P70 to P77, P80 to P85, P125 to P127 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV_{DD} ≤ 5.5 V			80.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			35.0	mA
			1.9 V ≤ EV_{DD} < 2.7 V			20.0	mA
			1.7 V ≤ EV_{DD} < 1.9 V			10.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])				150.0	mA
	I_{OL2}	Per pin for P20 to P25, P150 to P152	1.7 V ≤ V_{DD}[Note 4] ≤ 5.5 V			0.4[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	1.7 V ≤ V_{DD}[Note 4] ≤ 5.5 V			3.6	mA

Please refer details to RL78/I1C UM r01uh0587ej0210-rl78i1c.pdf Chapter 41.3.1

PRECAUTION ON GPIO
UNUSED PIN DESIGN

Connection of un-used pin basically follow the below guide line:

1. Input only pin
   - ❑ Connect 100K ohms resistor to EVDD/GND
2. Input and Output pin
   - ❑ Software configure to output ‘0’ for better ESD protection.

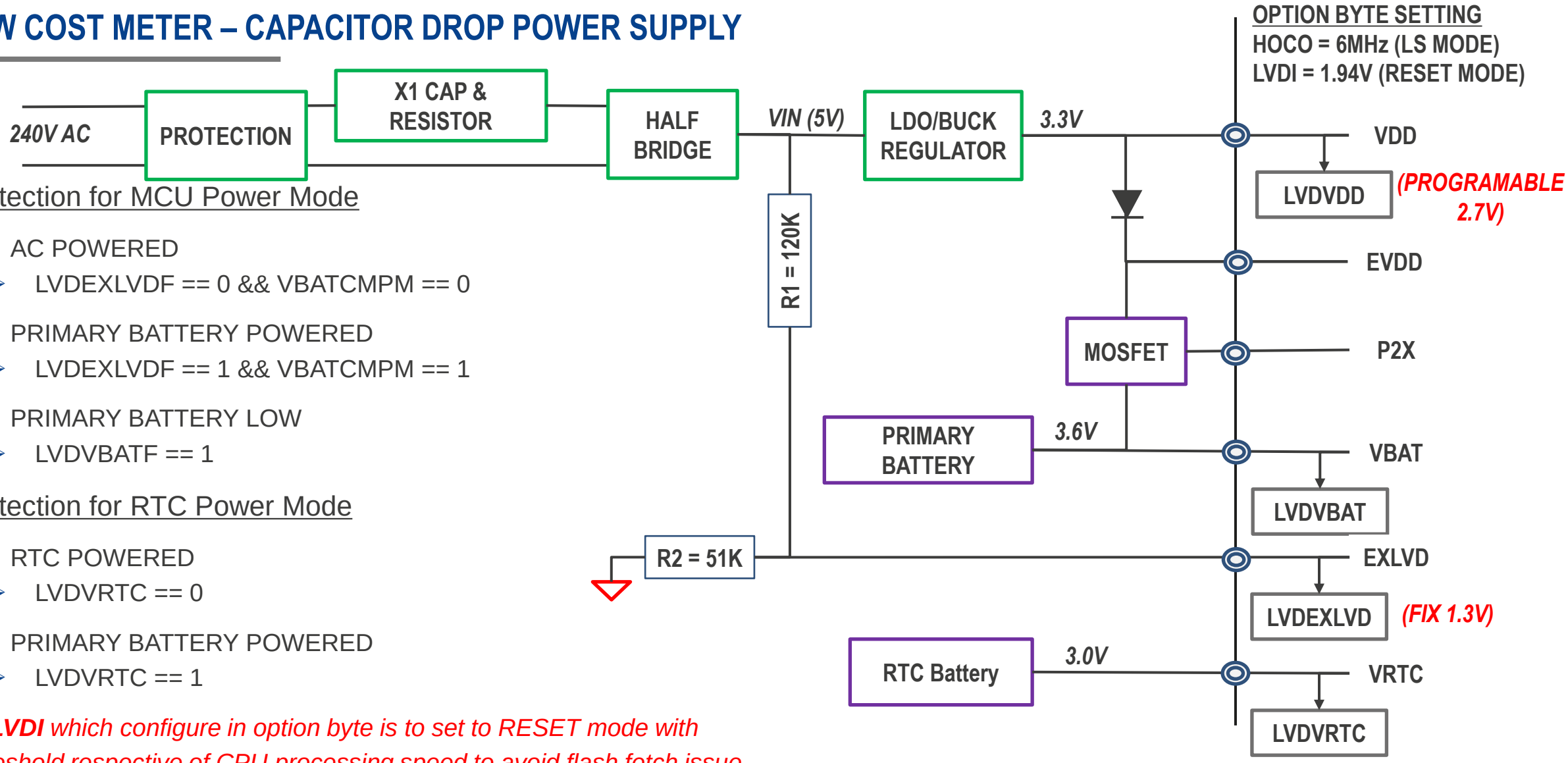
Please refer details to RL78/I1C UM r01uh0587ej0210-rl78i1c.pdf Chapter 2.3 Table 2-3

Pin Name	I/O	Recommended Connection of Unused Pins
P02 to P07	I/O	Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P10 to P17		<When setting to port I/O> Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When setting to segment output> Leave open.
P20 to P25		Input: Independently connect to V_{DD} or V_{SS} via a resistor. In addition, individually connect to V_{SS} via a resistor when using a battery backup function. Output: Leave open.
P30 to P37		<When setting to port I/O> Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When setting to segment output> Leave open.
P40/TOOL0		Input: Independently connect to EV_{DD0} via a resistor or leave open. Output: Leave open.
P41 to P43		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P50 to P57		<When setting to port I/O> Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When setting to segment output> Leave open.
P60 to P62		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Set the port’s output latch to 0 and leave the pin open, or set the port’s output latch to 1 and independently connect the pin to EV_{DD0} or EV_{SS0} via a resistor.
P70 to P77 P80 to P85	I/O	<When setting to port I/O> Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When setting to segment output> Leave open.
P121, P122	Input	Independently connect to V_{DD} or V_{SS} via a resistor. In addition, individually connect to V_{SS} via a resistor when using a battery backup function.
P123, P124	Input	Independently connect to V_{SS} via a resistor.
P125 to P127	I/O	Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open.
P137	Input	Independently connect to V_{DD} or V_{SS} via a resistor. In addition, individually connect to V_{SS} via a resistor when using a battery backup function.
P150 to P152	I/O	Leave open.
RESET	Input	Leave open.
REGC	–	Connect to V_{SS} via capacitor (0.47 to 1 μF).
COM0 to COM7	Output	Leave open.
ANIP0 to ANIP3	Input	Leave open.
ANIN0 to ANIN3		
V_{L1}, V_{L2}, V_{L4}	–	Leave open.
VBAT	–	Connect directly to V_{SS}. In addition, if the VBAT pin is not used, be sure to set the VBATEN bit to 0 with software.
VRTC	–	Directly connect to V_{SS}.
AVRT, AVCM	–	Connect to AV_{SS} via capacitor (0.47 μF).
AV_{SS}	–	Make AV_{SS} the same potential as V_{SS}.
AREGC	–	Connect to AV_{SS} via capacitor (0.47 μF).

RL78/I1C POWER MANAGEMENT DESIGN

POWER MANAGEMENT DESIGN

LOW COST METER – CAPACITOR DROP POWER SUPPLY



Detection for MCU Power Mode

1. AC POWERED
   - LVDEXLVDF == 0 && VBATCMPM == 0
2. PRIMARY BATTERY POWERED
   - LVDEXLVDF == 1 && VBATCMPM == 1
3. PRIMARY BATTERY LOW
   - LVDVBATF == 1

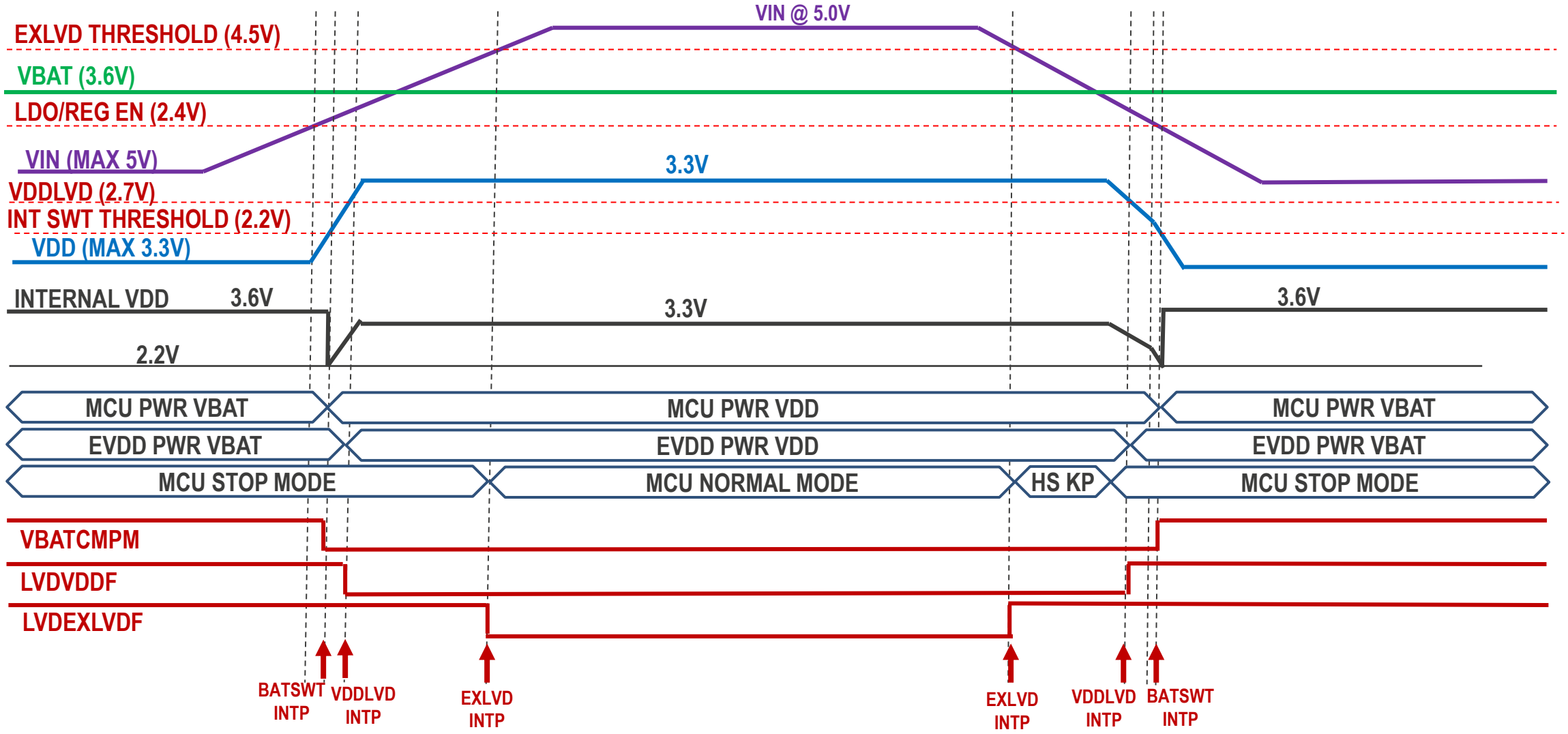
Detection for RTC Power Mode

1. RTC POWERED
   - LVDVRTC == 0
2. PRIMARY BATTERY POWERED
   - LVDVRTC == 1

*** LVDI** *which configure in option byte is to set to RESET mode with threshold respective of CPU processing speed to avoid flash fetch issue.*

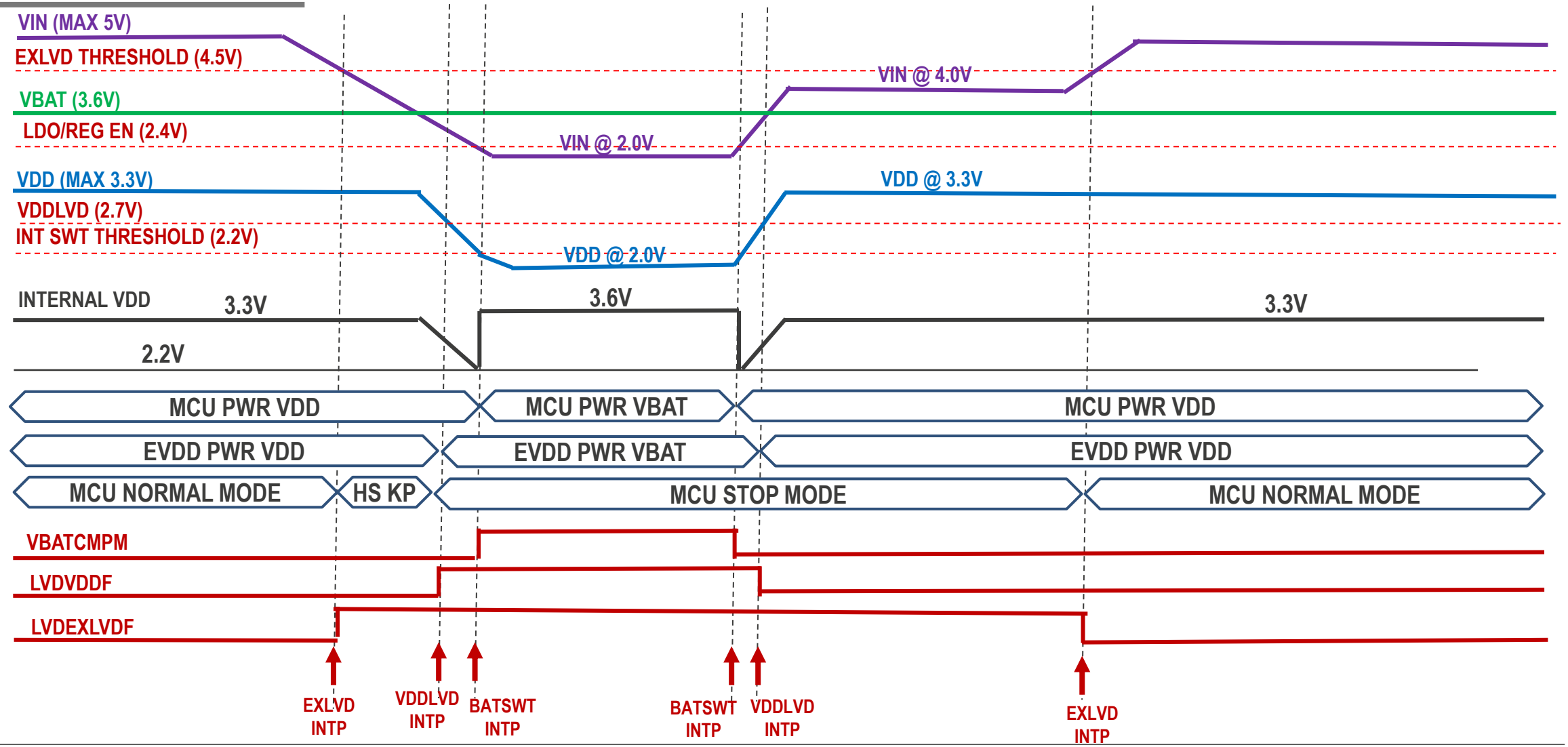
POWER MANAGEMENT DESIGN

LOW COST METER – CAPACITOR DROP POWER SEQUENCE



POWER MANAGEMENT DESIGN

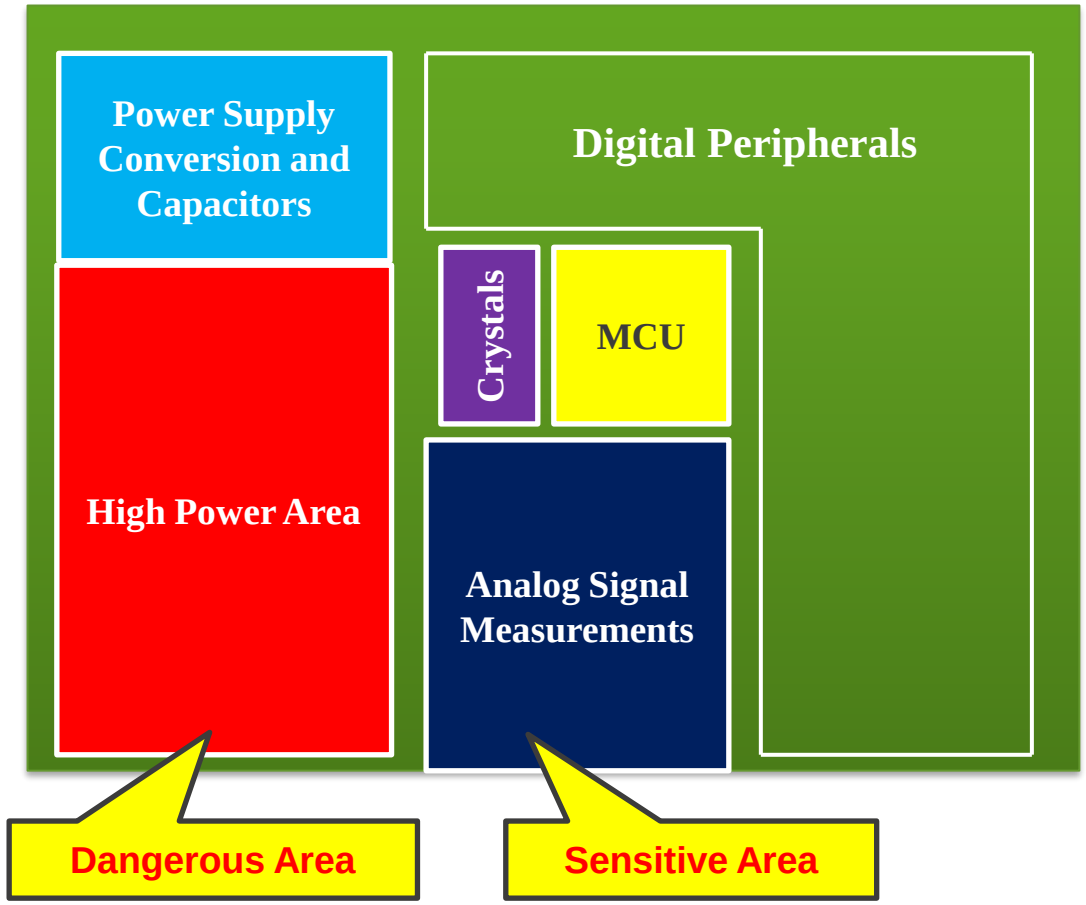
LOW COST METER – CAPACITOR DROP POWER SEQUENCE



RL78/I1C LAYOUT RECOMMENDATION

COMPONENT PLACEMENT

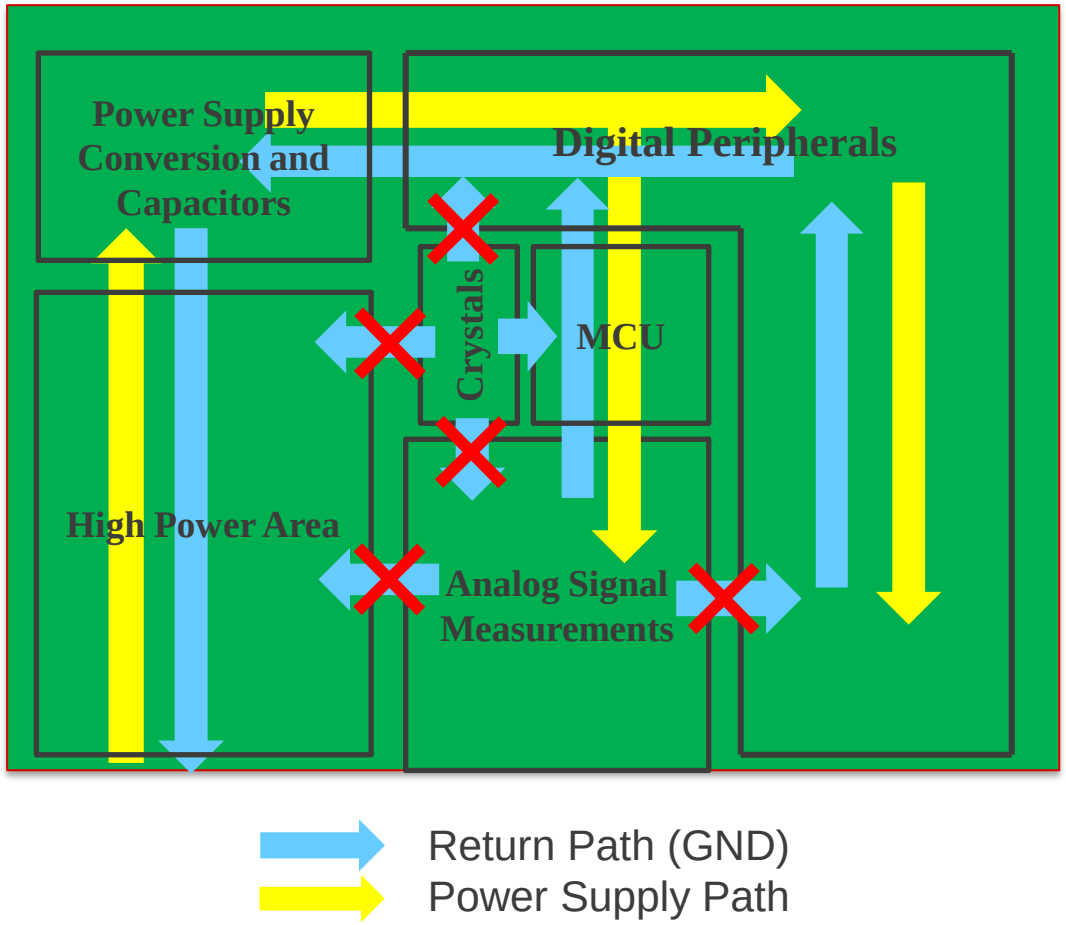
Component Placement plays a very important role on EMI and EMC reduction. In order to reduce noise effect on DSAD Signal measurements, below precaution was taken



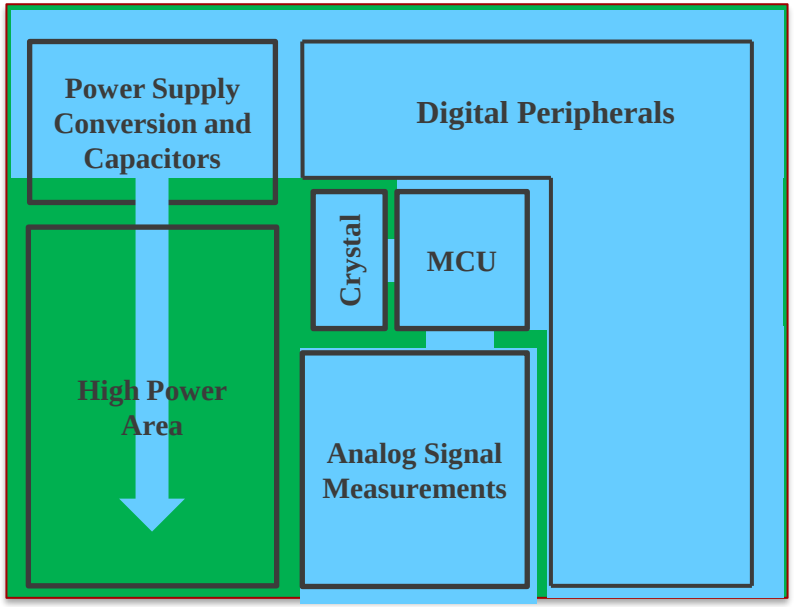
- Group the components into different category
  - ***High Voltage Part***
  - ***Power Supply***
  - ***Crystals***
  - ***Analogue Measurements parts***
  - ***Digitals Peripherals***
- Place each group in a different territory with a reasonable distance.
- Do not put High Voltage parts near to Analogue Measurements' parts
- Carefully plan the Power Source and Ground path. Power Source and Ground must come in pair as Ground acts as the return path for the current draw from the supply.

POWER & GROUND LAYOUT PRECAUTIONS

Power Supply and Ground Path Planning



- Power and its return paths should come in pair
- Return path of Digital Peripherals should not cross Analog Signal and Crystal Area



REASONABLE DISTANCE

Below tables show the minimum creepage and clearance specified in IEC 62052-11 for the terminals that have 40V and above. (applicable to High Power Area)

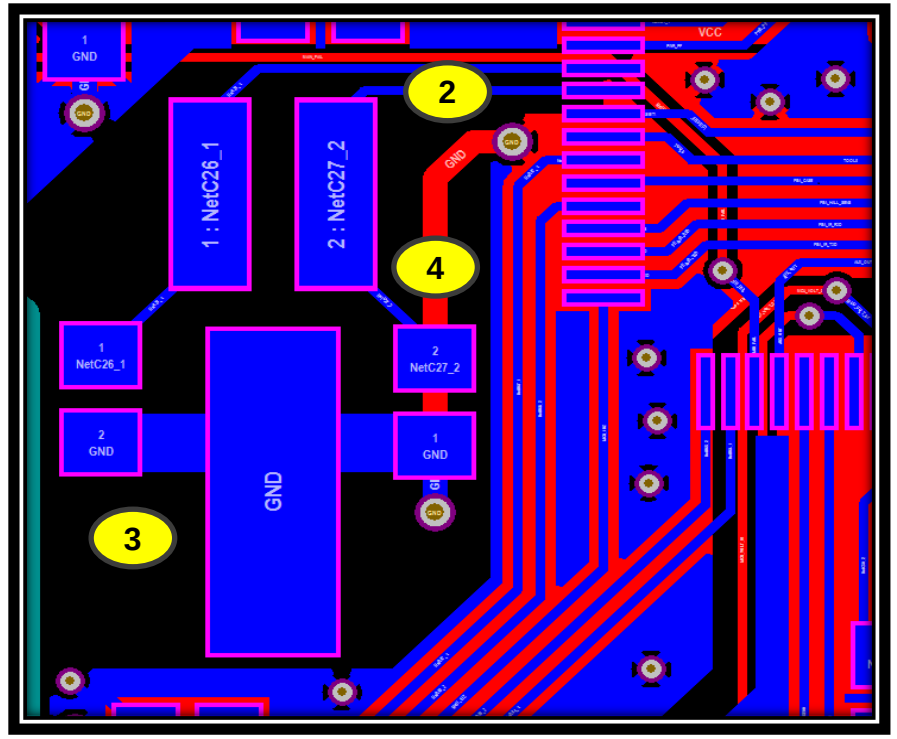
Protective Class I					
Voltage phase to earth derived from rated system voltage	Rated Impulse voltage	Minimum Clearance		Minimum Creepage Distance	
		Indoor Meter	Outdoor Meter	Indoor Meter	Outdoor Meter
V	V	mm	mm	mm	mm
≤ 100	1500	0.5	1.0	1.4	2.2
≤ 150	2500	1.5	1.5	1.6	2.5
≤ 300	4000	3.0	3.0	3.2	5.0
≤ 600	6000	5.5	5.5	6.3	10.0

Protective Class II					
Voltage phase to earth derived from rated system voltage	Rated Impulse voltage	Minimum Clearance		Minimum Creepage Distance	
		Indoor Meter	Outdoor Meter	Indoor Meter	Outdoor Meter
V	V	mm	mm	mm	mm
≤ 100	2500	1.5	1.5	2.0	3.2
≤ 150	4000	3.0	3.0	3.2	5.0
≤ 300	6000	5.5	5.5	6.3	10.0
≤ 600	8000	8.0	8.0	12.5	20.0

CRYSTAL LAYOUT PRECAUTIONS

Crystal Layout is to follow the below rules

1. Crystal is to be place as near as possible to RL78/I1C XT1 and XT2.
2. Please do not allow other signal to cross the XT1 and XT2 line even in other layer to avoid cross talk.
3. Not to put Ground Plane to avoid additional capacitance (created by the PCB layout)
4. Ground connection for the coupling Capacitors are to connect directly to the microcontroller.

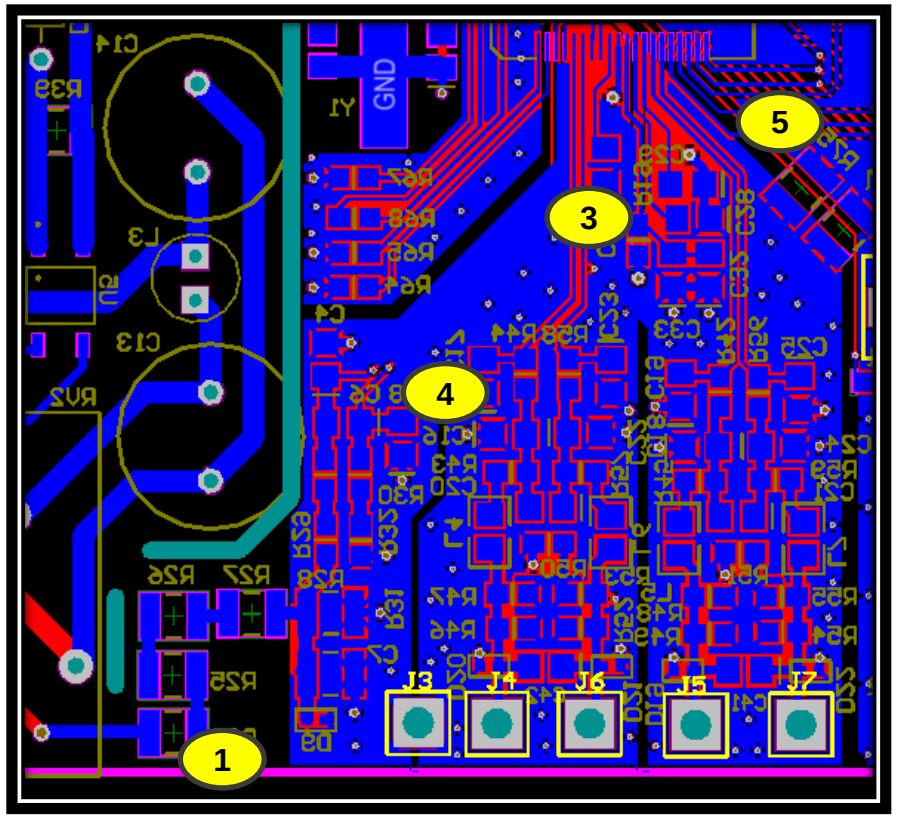


Please refer details to RL78/I1C UM r01uh0587ej0210-rl78i1c.pdf Chapter 6.4.2 Figure 6-22

ANALOG MEASUREMENT LAYOUT PRECAUTIONS

Analog Measurement Layout is to follow the below rules

1. Voltage divider resistor is to place outside the AGND plane.
2. Burden resistance of current transformer are recommended to place near the terminals
3. Anti-aliasing filter circuitry is to place near to the MCU
4. Please do not allow other signal to cross the DSAD input signal.
5. The differential signal is to place as near as to each other with no other signal in between. E.g. ANIP2 signal stay close to ANIN2.
6. Separate different set of DSAD signal with AGND. E.g, Separate ANIx1 signal and ANIx0 with AGND in between
7. AGND is to connect to GND near to MCU.



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