



### Försättsblad tentamen / Examination cover

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Skriv din anonymitetskod på varje inlämnat papper Write your anonymous code on each sheet submitted

Sätt ett kryss (x) för varje inlämnad uppgift Use an x to indicate which questions has been submitted

	edan med X / w with an X	Poäng / Credit	Lärarens anteckningar / Teacher's notes	Markera nedan Mark below wit	Poäng / Credit	Lärarens anteckningar / Teacher's notes
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3	<i>V</i>	4		18		
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7	X	3.5		22		
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## Fylls i av tentamensvakt / To be filled in by the invigilator





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2) Instruction 1:	Lärarens anteckning /
assembly syntax: mov R4, (110 1100 101 1010) vor mov R4, DCBA	
R4 is modified, and its new value is 6000 x 000 ODCBA.	
No status flags have been modified.	
2) Instruction 2:	
assenbly syntax: mov Ra orh R4, (1010 1011 100 1101) or orh R4, HBC	D
R4 is modified, and its new value is DX ABCDOCBA.	
Abstatus flogo Nand Zane modified. The new value of N is 1,	
The new value of Z is D. The value of Z is O. The value of Z is O.	
3 Instruction 3:	
assembly syntax: mar R3, (1010 aco   oud 1010)2 or mor R3, All A.	
R3 is modified, and its new value is 0x0000A11A.	
No status flags have been modified.	
@ Instruction 4:	
assembly syntax: orh R3, (0000 lol   lol   two) , or orh R3, OBBO.	
Ro is modified, and its new value is 0x0BBOAIIA.	
Status flago N is modified. The new value of N is O.	
The value of z is 0.	
5. Instruction 5:	
assembly syntax: add R5, R3, R4<<2 BAF8/402	
De is modified, and its new value is 0x DAS Line.	
B Status flag N is modified. The new value of N is 1.	
D Instruction 6:	
assembly syntax: @lov R3, R4, R5>>2.	
R3 is modified and its new value is 0x857709BA	
No status fag has been modified. The value of N is	
Still 1.	



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3) "Volcofi	6 Menny "max	ons the memory lose	s data after the p	ower is La	rarens anteckning /
anitched	AF )				
		Umanac the mamo	u con votain data	often the	
			y can retain data.		
	switched off				
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1) It	coun still ret	an water after	the power is suite	m of.	
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A) DILLE sollato - donos	Lärarens anteckning						
4) 32 kHz oscillator is slower.	Teachers note:						
RC oxillator is completely interned in the microproce	XXV.						
KC OX MODERY IS compact any incomed in the more representation							
hill 11 4 4 4 4 10 to be availed because 4 au	amplifu						
PLL module is needed to be enabled because it can amplify							
the fee me in a greated secillatory will the die stall cir	must						
the frequency of crystal oscillator with the digital cir	caru						
inside.							
[h5100]							



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(1) Roza	d-Robin Arbitration  ped Priority Arbitration  1 Defaut Master" is best to use to minimize the		Lärarens antecknii			
2						Teachers note:
6) En	Red Prior	nity Arbitra	tion			
" , "		J   "   "			CC.	
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() 1 (0-7406-	Lärarens anteckning /
6). Local Bus Interface	Teachers note:
C 1 / Wantook H. COI2 and	GAPTER
It is faster because it conhects the CPU and	0120
1 00 - 1 - 00 11 -) + 11 0 11 3	2
pins directly and serves as a "shortcut" fir their c	on munication
There is no PBA involved during the process.	



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	DOUSART can communicate with external devices without a teachers no	500
BEIC and PM are needed to wake up the microprossor from the closepest sleep mode.  D.TC can measure the duty cycle of a external naneform.  D.RTC can keep tracking of the largest time internal.  D.PWM can generate a digital waveform with configurable duty cycle.  D.PM can set the sperating frequency of cpv.	clock pin connection.	
BEIC and PM are needed to wake up the microprossor from the closepest sleep mode.  D.TC can measure the duty cycle of a external naneform.  D.RTC can keep tracking of the largest time internal.  D.PWM can generate a digital waveform with configurable duty cycle.  D.PM can set the sperating frequency of cpv.	@ TWI has the slowest maximum communication deate roote	
D.TC can measure the duty cycle of a external nanoform.  S.RTC can keep tracking of the largest time internal.  B.PWM can generate a digital waveform with configurable duty cycle.  B.PM can set the sperating frequency of CPV.	with external devices	
D.TC can measure the duty cycle of a external naneform.  S.RTC can keep tracking of the largest time internal.  B.PWM can generate a digital waveform with configurable duty cycle.  B.PM can set the spending frequency of CPV.	3) EIC and PM are readed to wake up the microprocessor from the cleepest sleep mode.	
S.RTC can keep tracking of the largest time internal.  B.PWM can generate a digital waveform with configurable duty cycle.  B.PM can set the spending frequency of CPV.	@ TC can measure the duty cycle of a external nanoform.	
DIMM can generate a digital waveform with configurable duty cycle.  O PM can set the spending frequency of CPV.		
OPM can set the spenating frequency of CPV.		
© PM can set the operating frequency of CPU.  8. PDCA. and SIZ an communicate with a SD and.	duty cycle.	
8.PDCA. and SPI an communicate with a SD cord.	8 PM can set the operating frequency of CPU.	
	8. PDCA. and SPI an communicate with a SD and.	
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8) PDCA is thed for "DMA controller", and it is a	Lärarens anteckning / Teachers note:
for transmitting double between menin memory and exte	
dericosc Disk, BD cord and so on)	
	he Limos
It is recommended because it can decreases to	
of I/O interruption Thereby, it frees	
finideal with other tasketo CPV such as calculat	tion. The
efficiency of CPU can improve a lot.	



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powder is an object referring to another we intill stored transmit reaches not when with its address.  If bytes are precious in memory for a point definition.	A p	outer	300	e object	t re-	femi	ng ti	ano	ther	Wer in	suble	stimed	Lärarens	
f bytes are readed in memory for a point definition.	euh	eno un	th it	5 and	wess.				1					
				- 000				0						
	4 hutes are needed in memory for a point definition.													
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(1)	

D) In AT724C3/A, the data are stored in "Big-endian" way.	Lärarens anteckning / Teachers note:
TTT X=0x1777BBBB	
77 Y[0]= 0x7777	
BB YIJ= 0xBBBB	-
BB Vooldress	
Oz.x = mask   means "Z.X=Z.X   mask   The bituise OR is	
operated between zix and mask-1, and the result is stored back	
$iXZ_1X_2$	
Result: $X = 0 \times 77776FFB6$ . $YED] = 0 \times 7777$ , $YED] = 0 \times 8FFB$ .	
2) "Z.Y II] = MASK 2" moons "Z.Y I [] = Z.Y [] MASK_2", The bituis	9
Exclisive -OR is operated between ziyII) and MASK2, and the result is	
Stored back in zy[i].	
Result: X=0x7717B99B, 8ID=0x777, 4IIJ=0xB99B	
3 ! z.y [0] <= 3" means " z.y [0] = z.y [6] << 3", The bixony bits of	
z, y[o] logically left-shift; and the result is stored back in y[o].	
Result: X=OXBBB8B99B, NIOJ=DXBBB8, NIJ=DXB99B.	
@ if(z,x&(10) < c301) judges whether the 30th bit of z, x is 1.	
If the 30th bit of zix is I, execute the following expression.	
Z.X=0xBBB8B99B, So the con 30th birt of is O. The	
conditionals is not satisfied.	
11 Z.X = NZ.X" means oppositing every bit of Z.X. Howevers	
"Z. X=~Z. X" won't be executed.	
Result: X=0xBBB8B99B, y [0]=0xBBB8, 4 []=0xB99B.	



Anonyn	nitetsk	od/ Ano	nymu	s code:	
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11) unsigned char: D ~ 127255	Lärarens anteckning /
11) unsigned char: 0 ~ 127255	Teachers note:
minimum maximus	
519 nool chow: 356 = 256 -128 ~ 127 V U Winimum Maximum	
J -  28 ~  2	
MINIMUM Maximum	
1/552/	
unsigned Short int: 0 0000	
minimy haxinum	
unsigned short int: 0 ~ 65536  unsigned short int: 0 ~ 65536  minimum maximum  short  signed int: -32768 ~ 32767	
510 neal 1 not: -32160 ~32/6/	
L. V. Castona	
minimum haximum	
The same of the sa	2
The maximus funsional chart 150.	
The maximum of signed char + 1 is 728.	
The maximum of ansigned short out +1 is 0	
The maximum of signed short but +1 15 -32768	
The minimum of unsigned char -1 is 255	
To my invine I strayed char -1 is 127.	
the minimum of state of the sta	
The minimum of unsigned short their = 1 is 65576.	
The minimum of signed charr-1 is 127.  The minimum of unsigned short that = 1 is 65536.  The minimum of the signed short int-1 is 3267.	



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12) "Big-Endian" maans "The most significant byte data are	Lärarens anteckning / Teachers note:
Stored in the locations whose addresses are lawest.	
"Little-Endian" means that the Coast significant byte data are	
Stored in the Cocations whose addresses are Cowest.	
AT321C3A uses "Big-budian"!  Intel X86 processor uses "Little-enclian".	
If these two processors communicate, the disorder of bytes	
might appella pen (if the size of clata is tong bigger than I byte for example,  10x12345678" in "little-endian" machine may be	
interrepted as "Ox 78563412", which could give rose to some	
problems.	



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14) "D" & is legicon FALSE.	Lärarens anteckning / Teachers note:
Numbers other them "O" are logical TRUE.	
"while(!(-1));" can be regarded as "while(FAISE);", so it actually maons "nothery to do" in C.	
A actuary mashs thought to do the C.	



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15) Quello 1810	Lärarens anteckning /
15). Only one.	Teachers note:
Beause in ATILUCIA microprocessor, there are stores 3	
Stages of pipe lines. They are "Fetch", "Instruction Decode" and	
orgon from the content of the conten	
"Instruction Execution" In this way, it can only execute one	
instruction at the the stope of execution at any given time.	

# Exam in "Programming of Embedded Systems"

Course: "Programming of Embedded Systems": ET014G

Date: 17th of March, 2017

Examiner: Peng Cheng Office Tel: 010-1428495

Requirement: write very clear letters on paper, write only one question per page!!! Allowed to use: Pen (not pencil!), eraser, ruler. Pocket calculator is not allowed!

Marks: Each question has a different mark.

Number of marks (p)	Grade
>=36	A
>=32	В
>=28	C
>=24	D
>=20	E (Approved) ©
<20	F



1) In AT32UC3A microprocessor, which execution is faster, the 32bit fixed-point multiplication or the 32bit floating-point multiplication? And why? (2p)

2) After reading the reference material on the different instruction formats, write in the assembly syntax what the following AVR32 binary program is doing, and what registers and status flags have been modified and what are their new values after each instruction. (6p)

E 1110 A lolo F 1111 C 1100 AVR32 binary program: Instruction 1: 0xE064DCBA Instruction 2: 0xEA14ABCD Instruction 3: 0xE063A11A Instruction 4: 0xEA130BB0 Instruction 5: 0xE6040025

Instruction 6: 0xE9E52223

What are the meanings of "volatile memory" and "non-volatile memory"? And for the different memories available in AT32UC3A microprocessor and EVK1100 board, give at least two different examples of "volatile memory". And which memory is typically used to store program and what are its properties that make it suitable for storing program but not for storing data? (4p)

4) In AT32UC3A microprocessor, there are RC oscillator and 32KHz oscillator, which one is slower? And which one is completely internal in the microprocessor? And in order to run the CPU at 66MHz, except for the main crystal oscillator, which module also need to be enabled? And why? (2p)

5) In HMATRIX of AT32UC3A microprocessor, what are the names of arbitration mechanisms used to solve the conflict of multiple masters trying to access single slave? And in order to minimize the access latency between the CPU instruction master and the slave module which store application program, which of the following settings is best to use? "No Default Master", "Last Accessed Default Master", "Fixed Default Master". (2p)

6) What is the fastest way (which hardware interface to use) for CPU to access the registers of the GPIO controller in the AT32UC3A microprocessor? Why is this way faster than the conventional way of accessing the registers of the GPIO controller?

7) In AT32UC3A microprocessor, there are PM, TC, USART, INTC, RTC, EIC, SPI, ADC, TWI, PDCA and PWM modules. Which module can communicate with external devices without a clock pin connection? Which module has the slowest

maximum communication data rate with external devices? Which **two** modules are needed to wake up the microprocessor from the deepest sleep mode? Which module can measure the duty cycle of an external digital waveform? Which module can keep tracking of the longest time interval? Which module can generate a digital waveform with configurable duty cycle? Which module can set the operating frequency of CPU? Which **two** modules can communicate with a SD card?(4p)

8) In AT32UC3A microprocessor, what is PDCA module used for? And why is using it recommended for large amount of I/O data? (2p)

9) What is a pointer variable in C? In AT32UC3A microprocessor, how many bytes are B (0/0 needed in memory for a pointer definition? (2p)

10) Describe what this C code is doing in detail in each line of code and calculate the result in each line of code for x and y: (6p)

extern volatile mask\_1 = 0x000000cc0;
#define MASK\_2 0x0660
Union
{
Union
{
U32 x = 0x7777BBBB;

D000 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 050 | 0

Union {
U32 x = 0x7777BBBB;
U16 y[2];
} z;
z.x |= mask\_1;
z.y[1] ^= MASK\_2;
z.y[0] <<= 3;
if (z.x & (1UL << 30))
{
z.x = ~z.x;
}
U11 ol! | ol! | ol! | ol! |
U000 | [os (lus out) |
Iol | (ol! | lo! |
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1011 1001 1001 1011 B 8 9 B

11) What are the maximum and minimum numbers represented in an "unsigned char", a "signed char", an "unsigned short int" and a "signed short int"? What are the results of the maximum numbers of these four variables + 1? What are the results of the minimum numbers of these four variables - 1? (2p)

12) What do "big-endian" and "little-endian" mean? And what are the endianness used in an AT32UC3A microprocessor and an Intel X86 processor? And what problem could this bring if these two processors communicate?(2p)

13) For the "global variable" and "local variable" in C, which variable could have its memory location shared for other use? Which variable will be automatically initialized to 0 by the compiler before its use? (2p)

14) What decimal numbers are logical FALSE and TRUE represented in C programming language? What do you think "while(!(-1));" will be treated in C? (2p)

15) In the AT32UC3A microprocessor, how many instructions can it execute at any given time? And why? (2p)

011 011 011 011 011 000. B B B 8



The following is the reference material for question 2.

### MOV - Move Data Into Register

#### Description

Moves a value into a register. The value may be an immediate or the contents of another register.

Note that Rd may specify

PC, resulting in a jump. All flags are unchanged.

#### Operation:

I. Rd ← SE(imm8);

II. Rd ← SE(imm21);

III. Rd ← Rs;

#### Syntax:

I. mov Rd, imm

II. mov Rd, imm

III. mov Rd, Rs

### Operands:

 $I. d \in \{0, 1, ..., 15\}$ 

imm ∈ {-128, -127, ..., 127}

II.  $d \in \{0, 1, ..., 15\}$ 

imm ∈ {-1048576, -104875, ..., 1048575}

III. d,  $s \in \{0, 1, ..., 15\}$ 

#### Status Flags:

Q: Not affected.

V: Not affected.

N: Not affected.

Z: Not affected.

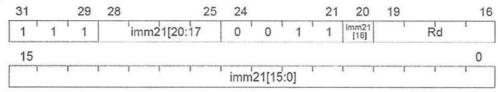
C: Not affected.

Opcode:

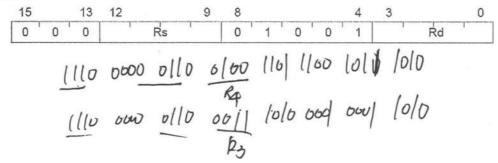
#### Format I:

15		13	12	11				4	3		0
0	0	1	1	1	1	imm8	L1		1	Rd	1

#### Format II:



#### Format III:



### ORH, ORL - Logical OR into high or low half of register

Description

Performs a bitwise logical OR between the high or low word in the specified register and a constant.

The result is stored in

the destination register.

Operation:

I. Rd[31:16] ← Rd[31:16] ∨ imm16;

II. Rd[15:0] ← Rd[15:0] ∨ imm16;

Syntax:

Vorh Rd, imm

II. orl Rd, imm

Operands:

I, II.  $d \in \{0, 1, ..., 15\}$ 

 $imm \in \{0, 1, ..., 65535\}$ 

Status Flags:

Q: Not affected

V: Not affected

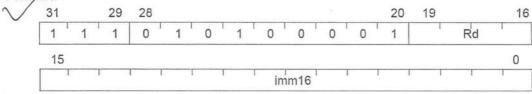
N: N ← RES[31]

**Z**: Z ← (RES[31:0] == 0)

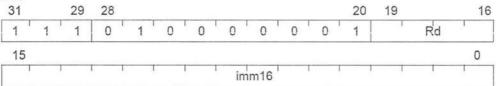
C: Not affected

Opcode:

Format I:



Format II:



1110 1010 000 | 6100 1010 (01) 1100 /10

R4

1110 1010 000 001) 6000 1011 /011 0000

R3

Adds the two registers specified and stores the result in destination register. Format II allows shifting
of the second operand.  Operation:
1. Rd ← Rd + Rs;
II. Rd - Rx + Ry << sa2;
Lodd Pd Pd
I. add Rd, Rs II. add Rd, Rx, Ry << sa
Operands:
I. {d, s} ∈ {0, 1,, 15}
II. {d, x, y}∈ {0, 1,, 15}
sa ∈ {0, 1, 2, 3}
Status Flags
Format I: OP1 = Rd, OP2 = Rs
Format II:OP1 = Rx, OP2 = Ry << sa2
Q: Not affected V: V + (OP1[31] \( \cdot \) OP2[31] \( \cdot \) . RES[31]) \( \cdot \) (. OP1[31] \( \cdot \) . OP2[31] \( \cdot \) RES[31])
N: N ← RES[31]
N. N. KEOPI
2: $Z \leftarrow (RES[31:0] == 0)$ C: $C \leftarrow OP1[31] \land OP2[31] \lor OP1[31] \land .RES[31] \lor OP2[31] \land .RES[31]$
Opcode:
Format I:
15 13 12 9 8 4 3 0
0 0 0 Rs 0 0 0 0 Rd
0 0 0 118 0 0 0 0 114
Format II:
31 29 28 25 24 20 19 16
1 1 1 Rx 0 0 0 0 Ry
15 12 11 8 7 6 5 4 3 0
0 0 0 0 0 0 0 0 0 Shift Amount Rd
0 0 0 0 0 0 0 0 0 Shift Amount Rd
0 0 0 0 0 0 0 0 0 Shift Amount Rd
(116 01)) 6000 blod 0000 0000 0000
1116 011) 0000 600 000 0000 0000 0000 00
(116 01)) 0000 600 000 0000 0000 0000 000
110 010 000 600 000 000 000 000 000 000
1116 011) 0000 600 000 0000 0000 0000 00
1110 0110 0000 600 0000 0000 0000 0000
1110 0110 0000 600 000 0000 0000 0000 0
1110 0110 0000 600 000 0000 0000 0000 0
1110 0110 0000 600 0000 0000 0000 0000
1110 0110 0000 600 0000 0000 0000 0000
1116 0110 0000 600 0000 0000 0000 0000

#### Performs a bitwise logical Exclusive-OR between the specified registers and stores the result in the destination register. Operation: I. Rd ← Rd ⊕ Rs; II. Rd ← Rx ⊕ Ry << sa5; III. Rd ← Rx ⊕ Ry >> sa5; Syntax: I. eor Rd, Rs II. eor Rd, Rx, Ry << sa III. eor Rd, Rx, Ry >> sa Operands: I. $\{d, s\} \in \{0, 1, ..., 15\}$ II, III. $\{d, x, y\} \in \{0, 1, ..., 15\}$ sa ∈ {0, 1, ..., 31} Status Flags Q: Not affected V: Not affected N: N ← RES[31] $Z: Z \leftarrow (RES[31:0] == 0)$ C: Not affected Opcode: Format I: Rd Rs Format II: Rx Ry sa5 Rd Format III: Rx Ry sa5 Rd 00 0 00(0 11/1

EOR - Logical Exclusive OR with optional logical shift