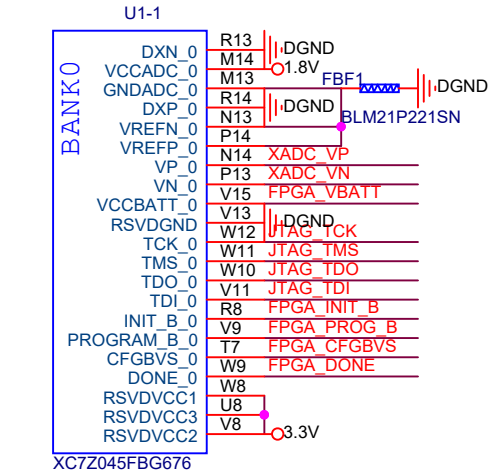
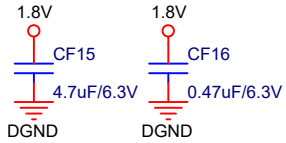
DeepRED REV1.1

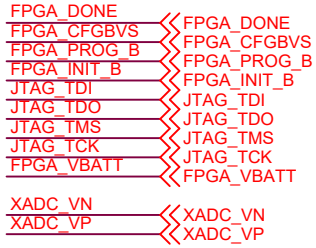
Change List
Date:
1.

Power on Sequence
1.0V->1.8V->1.35->3.3V

	V3BEST	
Title	DeepRED	
Size A4	Document Number 00 TOP	Rev V1.1
Date: Friday, October 13, 2017	Sheet 1 of 24	







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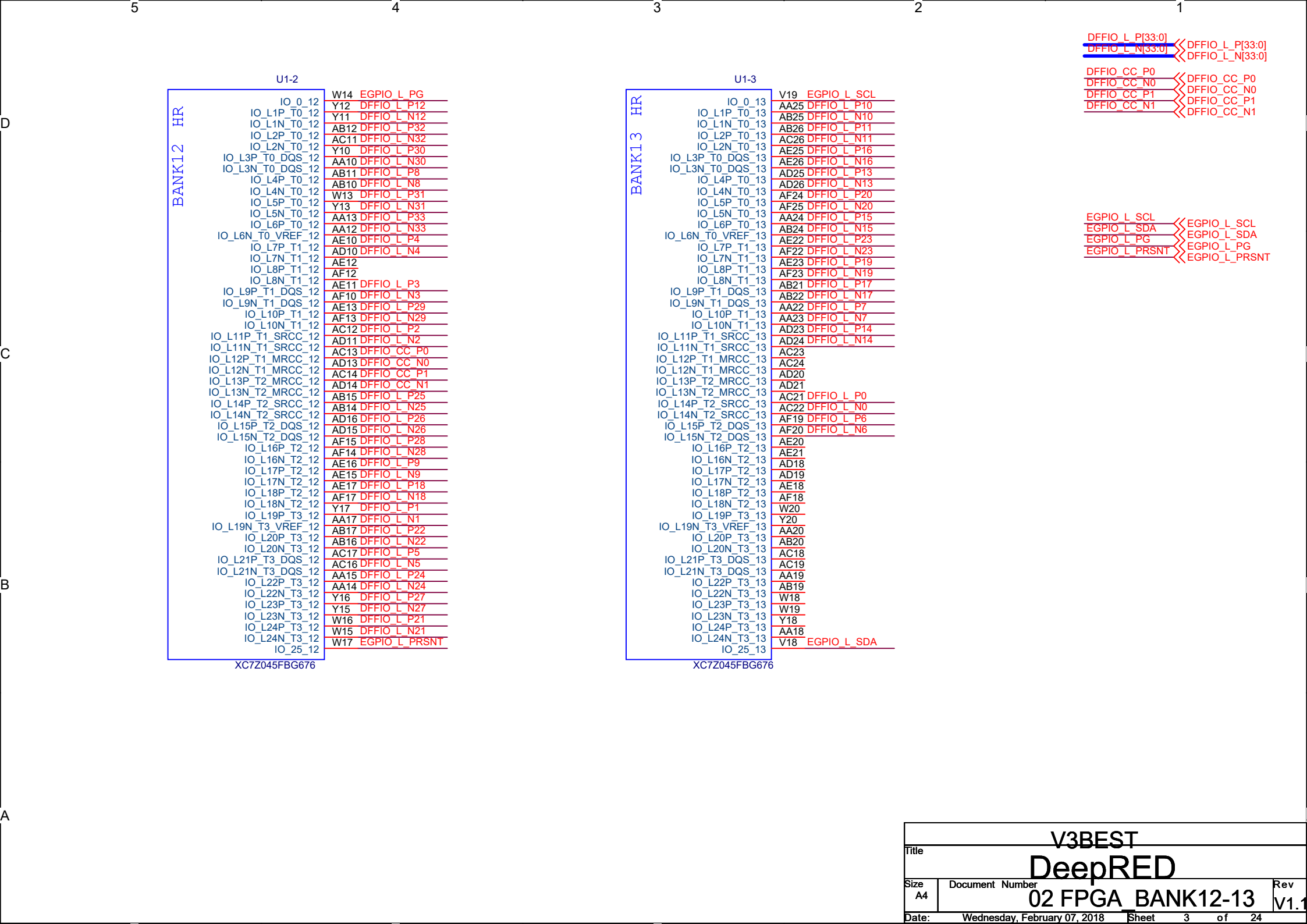
Size A4	Document Number 01 FPGA_BANK0	Rev V1.1
Date: Wednesday, February 07, 2018	Sheet 2 of 24	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3
2
1
D
C
B
A
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IO_L1N_T0_12 Y11 DFFIO_L_N12
IO_L2P_T0_12 AB12 DFFIO_L_P32
IO_L2N_T0_12 AC11 DFFIO_L_N32
IO_L3P_T0_DQS_12 Y10 DFFIO_L_P30
IO_L3N_T0_DQS_12 AA10 DFFIO_L_N30
IO_L4P_T0_12 AB11 DFFIO_L_P8
IO_L4N_T0_12 AB10 DFFIO_L_N8
IO_L5P_T0_12 W13 DFFIO_L_P31
IO_L5N_T0_12 Y13 DFFIO_L_N31
IO_L6P_T0_12 AA13 DFFIO_L_P33
IO_L6N_T0_VREF_12 AA12 DFFIO_L_N33
IO_L7P_T1_12 AE10 DFFIO_L_P4
IO_L7N_T1_12 AD10 DFFIO_L_N4
IO_L8P_T1_12 AE12
IO_L8N_T1_12 AF12
IO_L9P_T1_DQS_12 AE11 DFFIO_L_P3
IO_L9N_T1_DQS_12 AF10 DFFIO_L_N3
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IO_L10N_T1_12 AF13 DFFIO_L_N29
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IO_L11N_T1_SRCC_12 AD11 DFFIO_L_N2
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IO_L12N_T1_MRCC_12 AD13 DFFIO_CC_N0
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IO_L13N_T2_MRCC_12 AD14 DFFIO_CC_N1
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IO_L14N_T2_SRCC_12 AB14 DFFIO_L_N25
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IO_L15N_T2_DQS_12 AD15 DFFIO_L_N26
IO_L16P_T2_12 AF15 DFFIO_L_P28
IO_L16N_T2_12 AF14 DFFIO_L_N28
IO_L17P_T2_12 AE16 DFFIO_L_P9
IO_L17N_T2_12 AE15 DFFIO_L_N9
IO_L18P_T2_12 AE17 DFFIO_L_P18
IO_L18N_T2_12 AF17 DFFIO_L_N18
IO_L19P_T3_12 Y17 DFFIO_L_P1
IO_L19N_T3_VREF_12 AA17 DFFIO_L_N1
IO_L20P_T3_12 AB17 DFFIO_L_P22
IO_L20N_T3_12 AB16 DFFIO_L_N22
IO_L21P_T3_DQS_12 AC17 DFFIO_L_P5
IO_L21N_T3_DQS_12 AC16 DFFIO_L_N5
IO_L22P_T3_12 AA15 DFFIO_L_P24
IO_L22N_T3_12 AA14 DFFIO_L_N24
IO_L23P_T3_12 Y16 DFFIO_L_P27
IO_L23N_T3_12 Y15 DFFIO_L_N27
IO_L24P_T3_12 W16 DFFIO_L_P21
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XC7Z045FBG676
U1-3
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IO_L2P_T0_13 AB26 DFFIO_L_P11
IO_L2N_T0_13 AC26 DFFIO_L_N11
IO_L3P_T0_DQS_13 AE25 DFFIO_L_P16
IO_L3N_T0_DQS_13 AE26 DFFIO_L_N16
IO_L4P_T0_13 AD25 DFFIO_L_P13
IO_L4N_T0_13 AD26 DFFIO_L_N13
IO_L5P_T0_13 AF24 DFFIO_L_P20
IO_L5N_T0_13 AF25 DFFIO_L_N20
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IO_L6N_T0_VREF_13 AB24 DFFIO_L_N15
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IO_L7N_T1_13 AF22 DFFIO_L_N23
IO_L8P_T1_13 AE23 DFFIO_L_P19
IO_L8N_T1_13 AF23 DFFIO_L_N19
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IO_L9N_T1_DQS_13 AB22 DFFIO_L_N17
IO_L10P_T1_13 AA22 DFFIO_L_P7
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IO_L19N_T3_VREF_13 Y20
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IO_L23P_T3_13 W18
IO_L23N_T3_13 W19
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IO_25_13 V18 EGPIO_L_SDA
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DFFIO_L_P[33:0]
DFFIO_L_N[33:0]
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DFFIO_CC_N0
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DFFIO_CC_N1
DFFIO_CC_P0
DFFIO_CC_N0
DFFIO_CC_P1
DFFIO_CC_N1
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EGPIO_L_SDA
EGPIO_L_PG
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EGPIO_L_PRSNT
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Document Number
02 FPGA_BANK12-13
Rev
V1.1
Date:
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3
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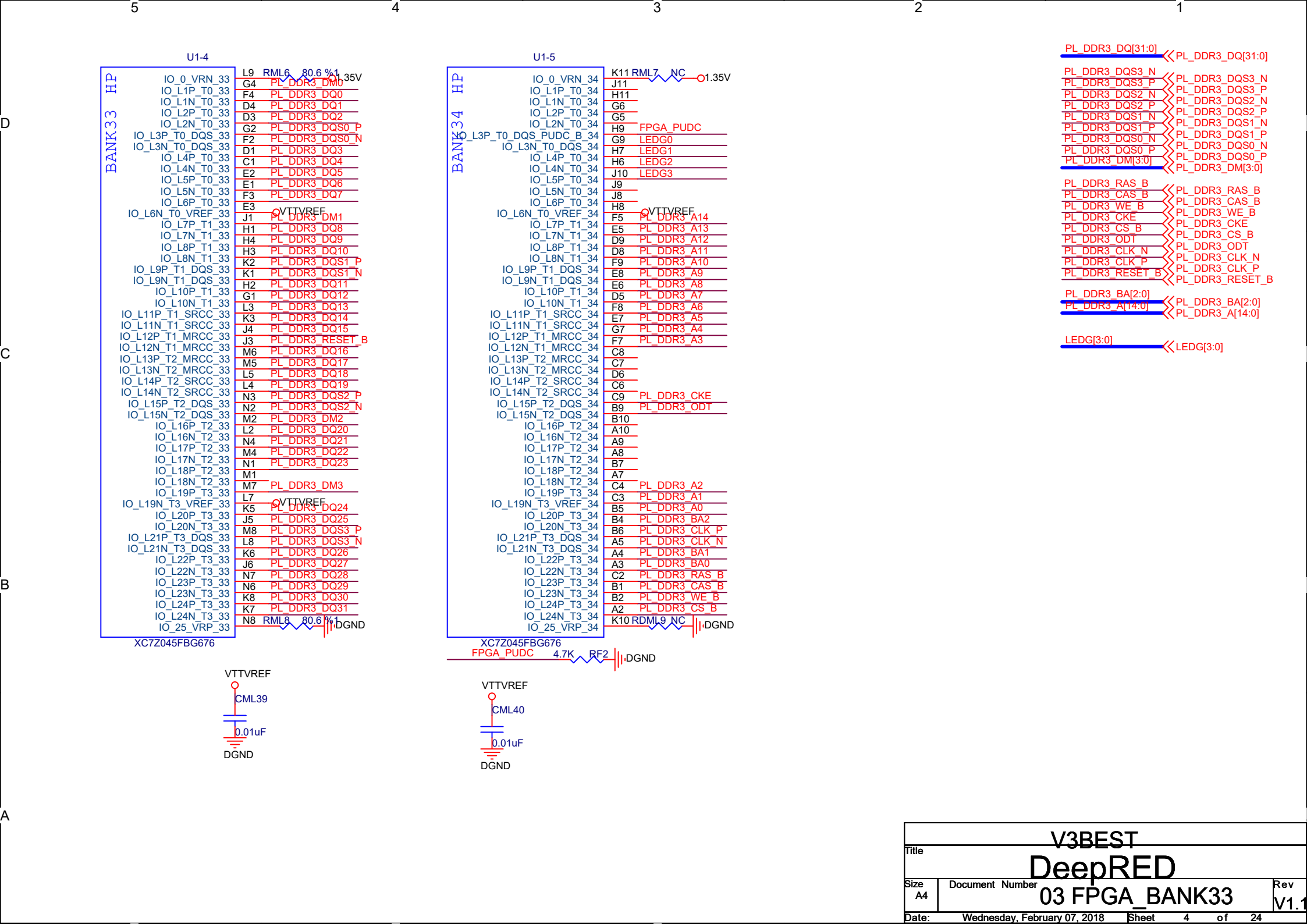
24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IO_L2P_T0_33
IO_L2N_T0_33
IO_L3P_T0_DQS_33
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IO_L22N_T3_33
IO_L23P_T3_33
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IO_L24N_T3_33
IO_25_VRP_33
L9 RML6 80.6 %1
1.35V
G4 PL_DDR3_DM0
F4 PL_DDR3_DQ0
D4 PL_DDR3_DQ1
D3 PL_DDR3_DQ2
G2 PL_DDR3_DQS0_P
F2 PL_DDR3_DQS0_N
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C1 PL_DDR3_DQ4
E2 PL_DDR3_DQ5
E1 PL_DDR3_DQ6
F3 PL_DDR3_DQ7
E3 VTTVREF
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H4 PL_DDR3_DQ9
H3 PL_DDR3_DQ10
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H2 PL_DDR3_DQ11
G1 PL_DDR3_DQ12
L3 PL_DDR3_DQ13
K3 PL_DDR3_DQ14
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J3 PL_DDR3_RESET_B
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M5 PL_DDR3_DQ17
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L4 PL_DDR3_DQ19
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L2 PL_DDR3_DQ20
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M7 PL_DDR3_DM3
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J5 PL_DDR3_DQ25
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L8 PL_DDR3_DQS3_N
K6 PL_DDR3_DQ26
J6 PL_DDR3_DQ27
N7 PL_DDR3_DQ28
N6 PL_DDR3_DQ29
K8 PL_DDR3_DQ30
K7 PL_DDR3_DQ31
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IO_L23N_T3_34
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IO_L24N_T3_34
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J11
H11
G6
G5
H9 FPGA_PUDC
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H7 LEDG1
H6 LEDG2
J10 LEDG3
J9
J8
H8
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D9 PL_DDR3_A12
D8 PL_DDR3_A11
F9 PL_DDR3_A10
E8 PL_DDR3_A9
E6 PL_DDR3_A8
D5 PL_DDR3_A7
F8 PL_DDR3_A6
E7 PL_DDR3_A5
G7 PL_DDR3_A4
F7 PL_DDR3_A3
C8
C7
D6
C6
C9 PL_DDR3_CKE
B9 PL_DDR3_ODT
B10
A10
A9
A8
B7
A7
C4 PL_DDR3_A2
C3 PL_DDR3_A1
B5 PL_DDR3_A0
B4 PL_DDR3_BA2
B6 PL_DDR3_CLK_P
A5 PL_DDR3_CLK_N
A4 PL_DDR3_BA1
A3 PL_DDR3_BA0
C2 PL_DDR3_RAS_B
B1 PL_DDR3_CAS_B
B2 PL_DDR3_WE_B
A2 PL_DDR3_CS_B
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PL_DDR3_DQS0_N
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PL_DDR3_CAS_B
PL_DDR3_WE_B
PL_DDR3_CKE
PL_DDR3_CS_B
PL_DDR3_ODT
PL_DDR3_CLK_N
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Size A4
Document Number
03 FPGA_BANK33
Rev V1.1
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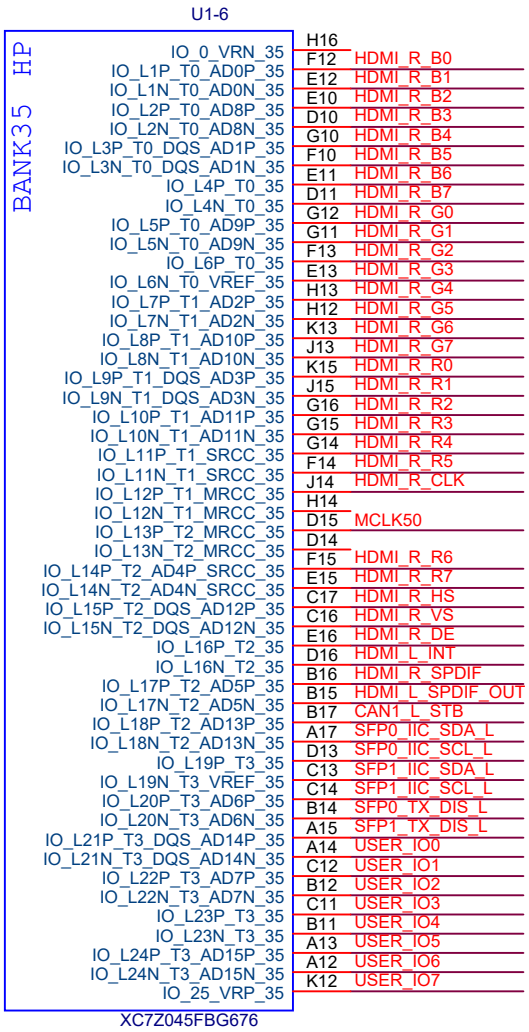

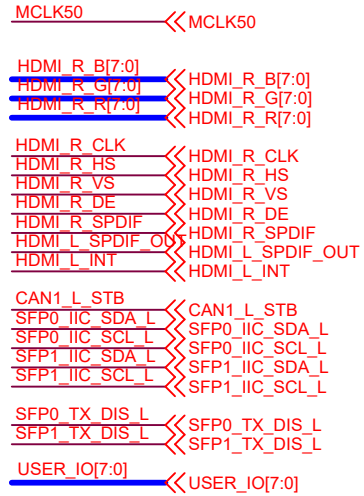

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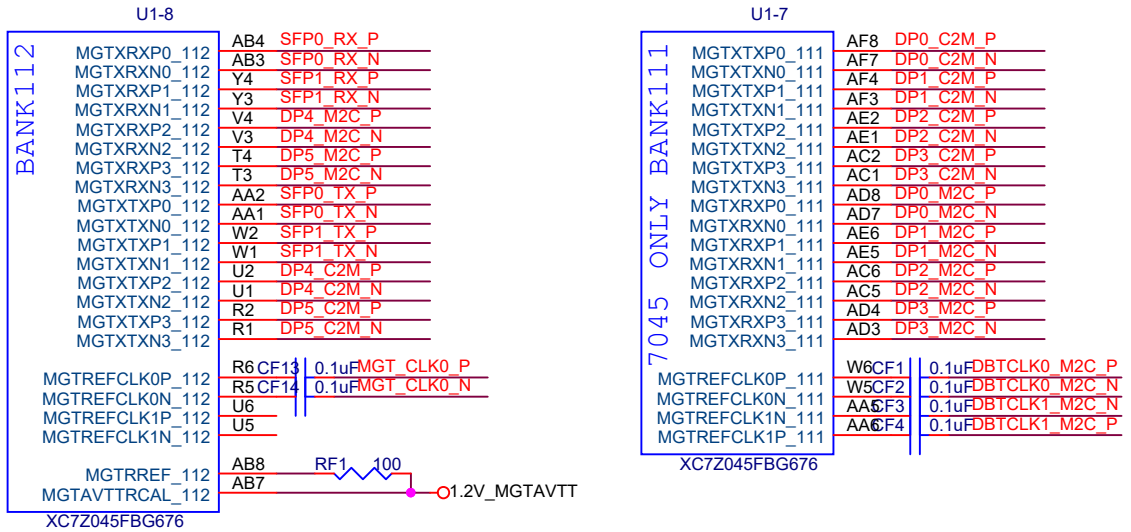
Size A4	Document Number 04 FPGA_BANK35	Rev V1.1
Date: Wednesday, February 07, 2018	Sheet 5 of 24	



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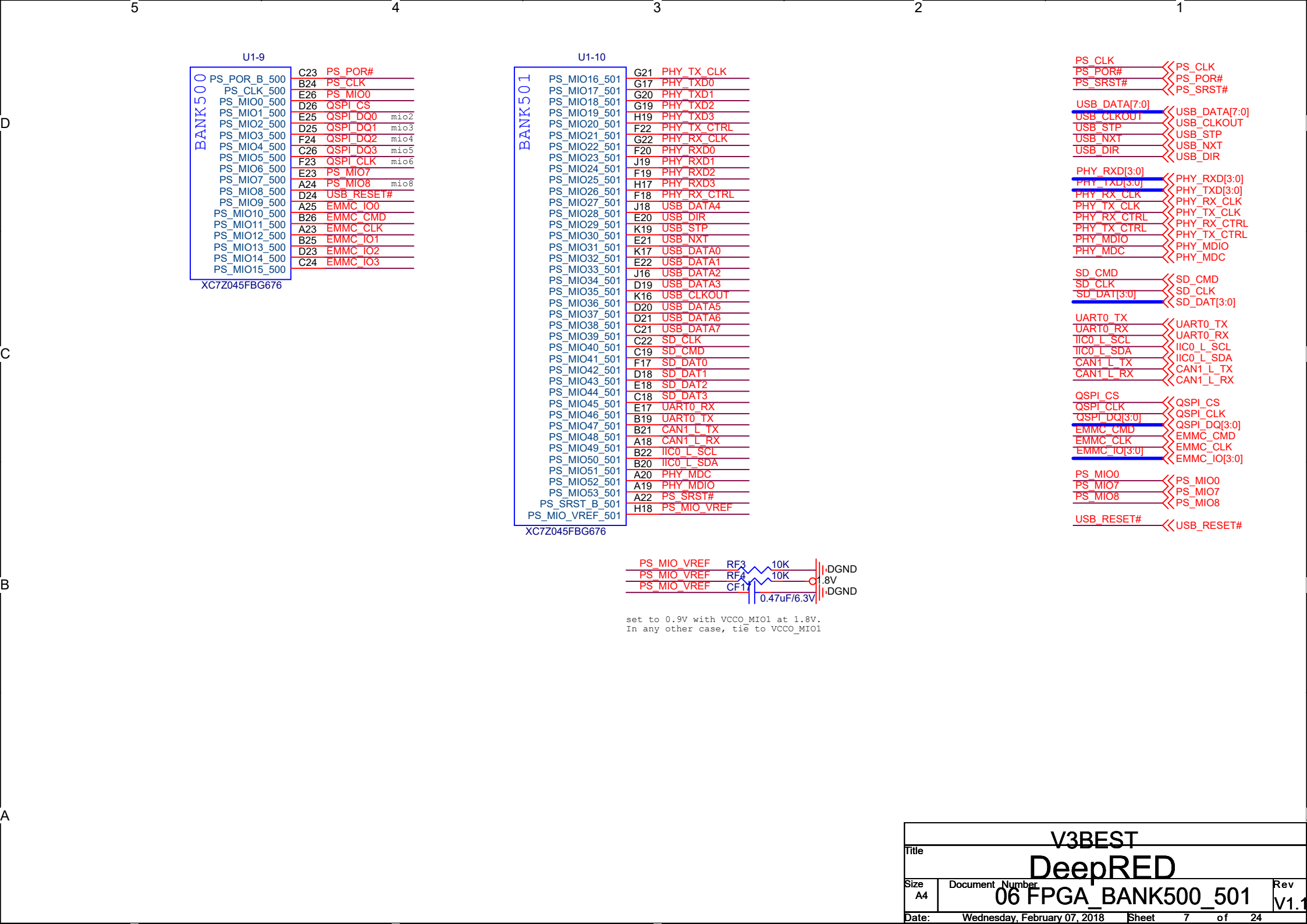
Size A4	Document Number 05 FPGA_BANK_GTX	Rev V1.1
Date: Wednesday, February 07, 2018	Sheet 6 of 24	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U1-9
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PS_MIO1_500
PS_MIO2_500
PS_MIO3_500
PS_MIO4_500
PS_MIO5_500
PS_MIO6_500
PS_MIO7_500
PS_MIO8_500
PS_MIO9_500
PS_MIO10_500
PS_MIO11_500
PS_MIO12_500
PS_MIO13_500
PS_MIO14_500
PS_MIO15_500
C23 PS_POR#
B24 PS_CLK
E26 PS_MIO0
D26 QSPI_CS
E25 QSPI_DQ0 mio2
D25 QSPI_DQ1 mio3
F24 QSPI_DQ2 mio4
C26 QSPI_DQ3 mio5
F23 QSPI_CLK mio6
E23 PS_MIO7
A24 PS_MIO8 mio8
D24 USB_RESET#
A25 EMMC_IO0
B26 EMMC_CMD
A23 EMMC_CLK
B25 EMMC_IO1
D23 EMMC_IO2
C24 EMMC_IO3
XC7Z045FBG676
U1-10
BANK501
PS_MIO16_501
PS_MIO17_501
PS_MIO18_501
PS_MIO19_501
PS_MIO20_501
PS_MIO21_501
PS_MIO22_501
PS_MIO23_501
PS_MIO24_501
PS_MIO25_501
PS_MIO26_501
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PS_MIO28_501
PS_MIO29_501
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PS_MIO51_501
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PS_MIO53_501
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G17 PHY_TXD0
G20 PHY_TXD1
G19 PHY_TXD2
H19 PHY_TXD3
F22 PHY_TX_CTRL
G22 PHY_RX_CLK
F20 PHY_RXD0
J19 PHY_RXD1
F19 PHY_RXD2
H17 PHY_RXD3
F18 PHY_RX_CTRL
J18 USB_DATA4
E20 USB_DIR
K19 USB_STP
E21 USB_NXT
K17 USB_DATA0
E22 USB_DATA1
J16 USB_DATA2
D19 USB_DATA3
K16 USB_CLKOUT
D20 USB_DATA5
D21 USB_DATA6
C21 USB_DATA7
C22 SD_CLK
C19 SD_CMD
F17 SD_DAT0
D18 SD_DAT1
E18 SD_DAT2
C18 SD_DAT3
E17 UART0_RX
B19 UART0_TX
B21 CAN1_L_TX
A18 CAN1_L_RX
B22 IIC0_L_SCL
B20 IIC0_L_SDA
A20 PHY_MDC
A19 PHY_MDIO
A22 PS_SRST#
H18 PS_MIO_VREF
XC7Z045FBG676
PS_MIO_VREF
PS_MIO_VREF
PS_MIO_VREF
RF3 10K
RF4 10K
CF11 0.47uF/6.3V
DGND
1.8V
DGND
set to 0.9V with VCCO_MIO1 at 1.8V.
In any other case, tie to VCCO_MIO1
PS_CLK
PS_POR#
PS_SRST#
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USB_CLKOUT
USB_STP
USB_NXT
USB_DIR
PHY_RXD[3:0]
PHY_TXD[3:0]
PHY_RX_CLK
PHY_TX_CLK
PHY_RX_CTRL
PHY_TX_CTRL
PHY_MDIO
PHY_MDC
SD_CMD
SD_CLK
SD_DAT[3:0]
UART0_TX
UART0_RX
IIC0_L_SCL
IIC0_L_SDA
CAN1_L_TX
CAN1_L_RX
QSPI_CS
QSPI_CLK
QSPI_DQ[3:0]
EMMC_CMD
EMMC_CLK
EMMC_IO[3:0]
PS_MIO0
PS_MIO7
PS_MIO8
USB_RESET#
V3BEST
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DeepRED
Size
A4
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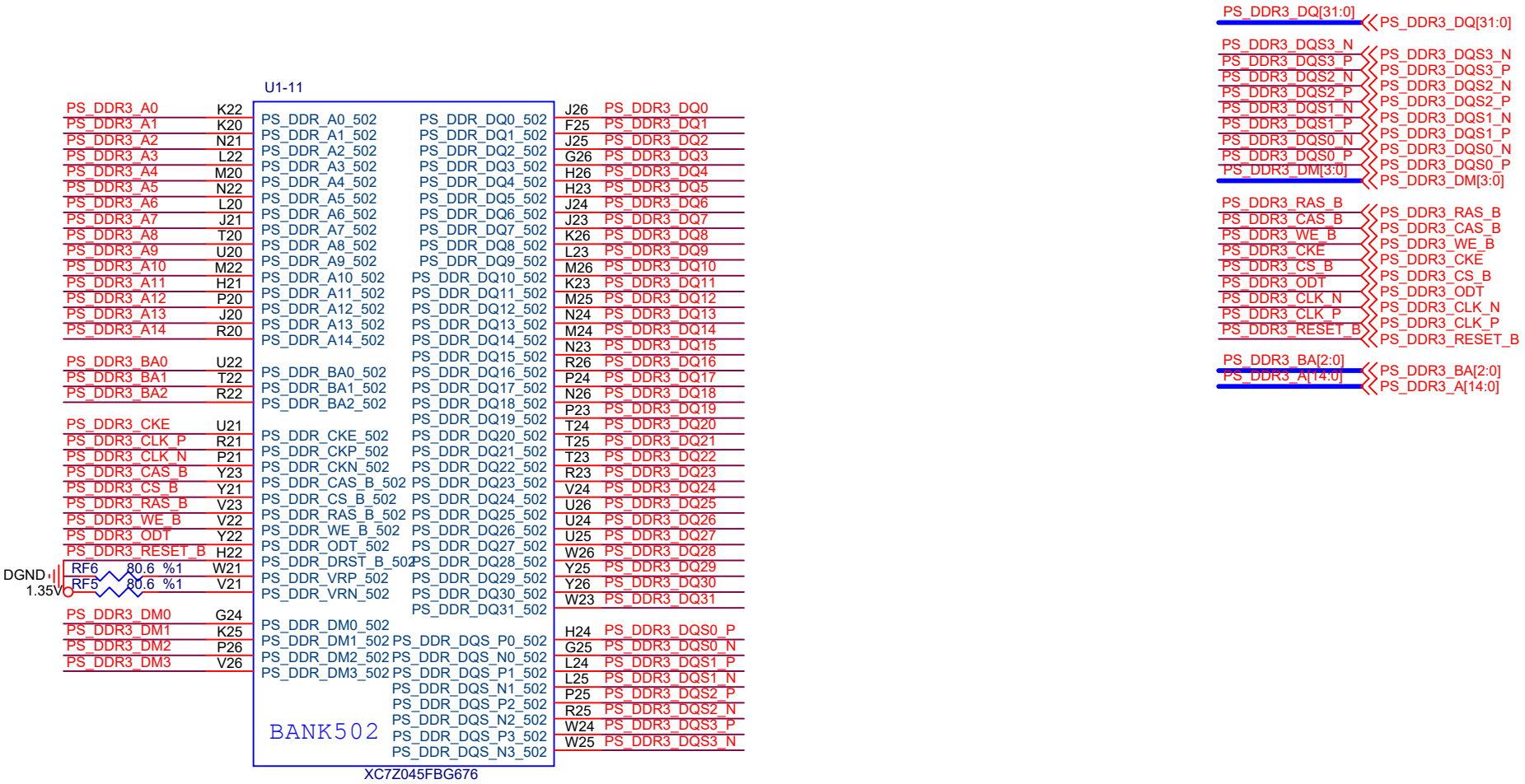

Title	V3BEST DeepRED	
Size A4	Document Number 07 FPGA_BANK502	Rev V1.1
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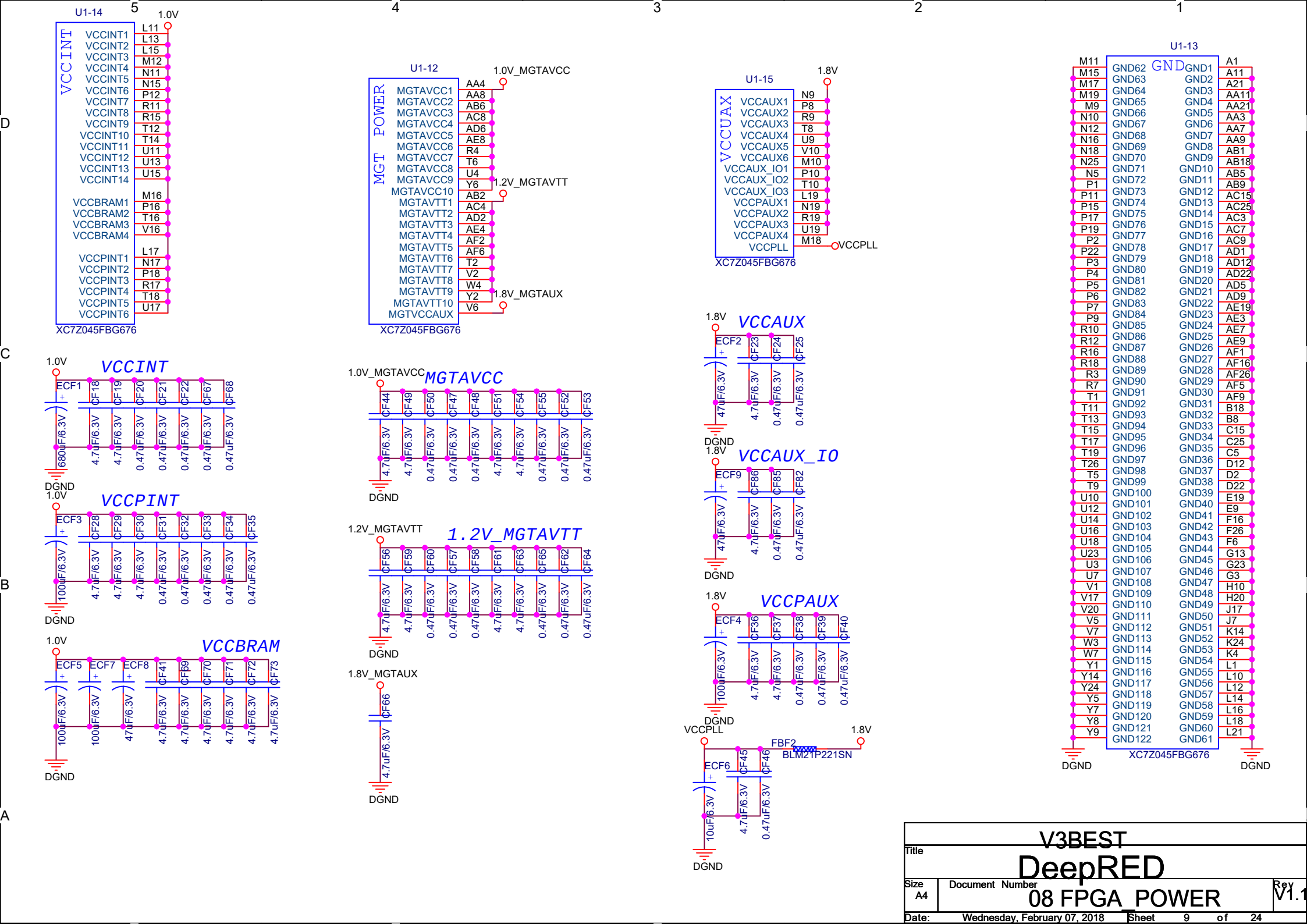

Title	V3BEST DeepRED			
Size A4	Document Number 08 FPGA_POWER			Rev V1.1
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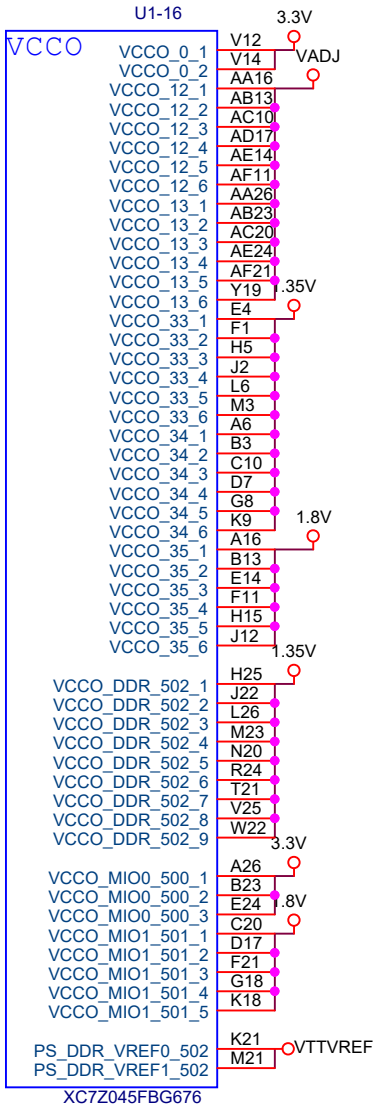
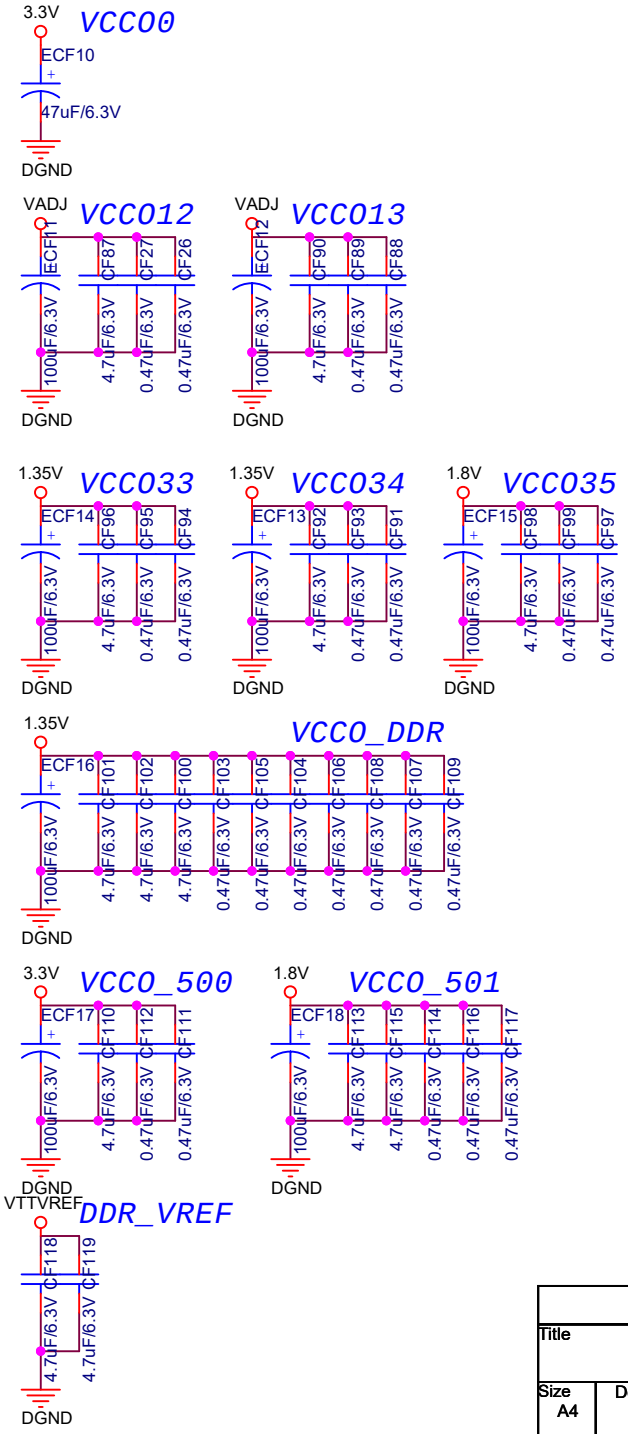
Bank Voltage should be checked for dedicated applications.





Title	V3BEST DeepRED		
Size A4	Document Number 09 FPGA_POWER_VCCO		Rev V1.1
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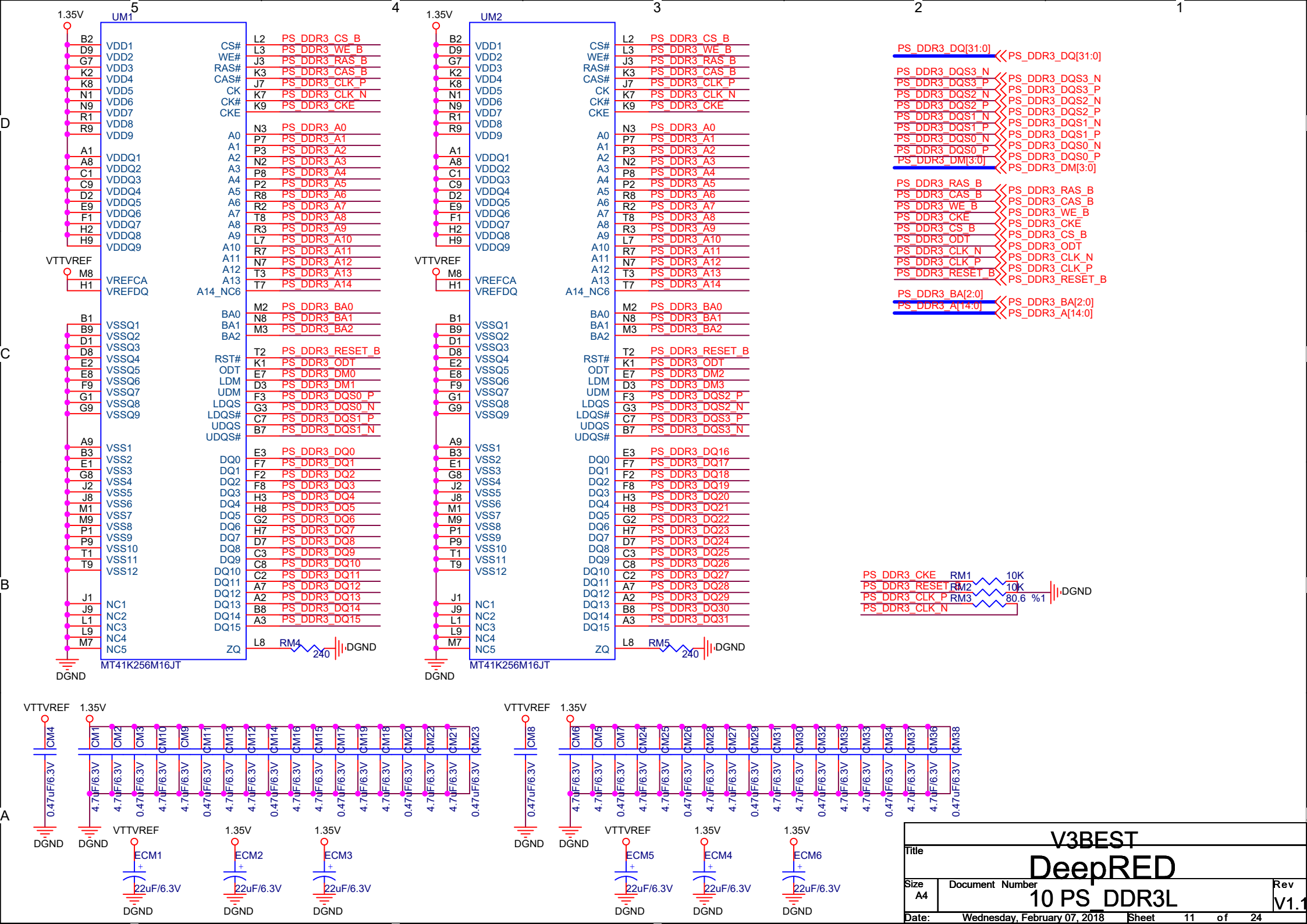
UM1
MT41K256M16JT
UM2
MT41K256M16JT
1.35V
VTTVREF
DGND
PS_DDR3_DQ[31:0]
PS_DDR3_DQS3_N
PS_DDR3_DQS3_P
PS_DDR3_DQS2_N
PS_DDR3_DQS2_P
PS_DDR3_DQS1_N
PS_DDR3_DQS1_P
PS_DDR3_DQS0_N
PS_DDR3_DQS0_P
PS_DDR3_DM[3:0]
PS_DDR3_RAS_B
PS_DDR3_CAS_B
PS_DDR3_WE_B
PS_DDR3_CKE
PS_DDR3_CS_B
PS_DDR3_ODT
PS_DDR3_CLK_N
PS_DDR3_CLK_P
PS_DDR3_RESET_B
PS_DDR3_BA[2:0]
PS_DDR3_A[14:0]
RM1 10K
RM2 10K
RM3 80.6 %1
RM4 240
RM5 240
ECM1 22uF/6.3V
ECM2 22uF/6.3V
ECM3 22uF/6.3V
ECM5 22uF/6.3V
ECM4 22uF/6.3V
ECM6 22uF/6.3V
0.47uF/6.3V
4.7uF/6.3V
V3BEST
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10 PS_DDR3L
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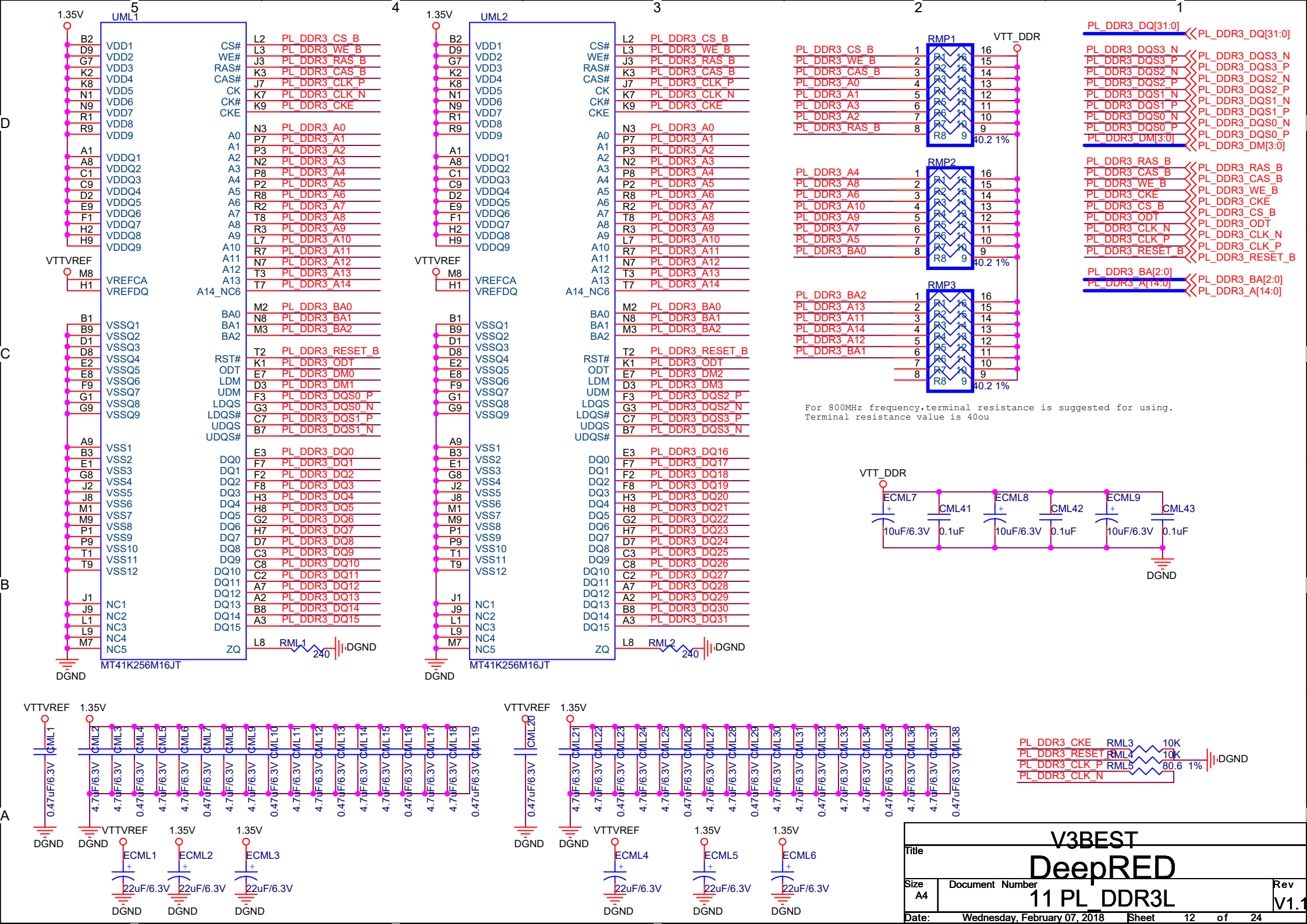
UML1
MT41K256M16JT
UML2
MT41K256M16JT
1.35V
VTTVREF
DGND
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDD9
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9
VREFCA
VREFDQ
VSSQ1
VSSQ2
VSSQ3
VSSQ4
VSSQ5
VSSQ6
VSSQ7
VSSQ8
VSSQ9
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
NC1
NC2
NC3
NC4
NC5
CS#
WE#
RAS#
CAS#
CK
CK#
CKE
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14_NC6
BA0
BA1
BA2
RST#
ODT
LDM
UDM
LDQS
LDQS#
UDQS
UDQS#
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
ZQ
PL_DDR3_CS_B
PL_DDR3_WE_B
PL_DDR3_RAS_B
PL_DDR3_CAS_B
PL_DDR3_CLK_P
PL_DDR3_CLK_N
PL_DDR3_CKE
PL_DDR3_A0
PL_DDR3_A1
PL_DDR3_A2
PL_DDR3_A3
PL_DDR3_A4
PL_DDR3_A5
PL_DDR3_A6
PL_DDR3_A7
PL_DDR3_A8
PL_DDR3_A9
PL_DDR3_A10
PL_DDR3_A11
PL_DDR3_A12
PL_DDR3_A13
PL_DDR3_A14
PL_DDR3_BA0
PL_DDR3_BA1
PL_DDR3_BA2
PL_DDR3_RESET_B
PL_DDR3_ODT
PL_DDR3_DM0
PL_DDR3_DM1
PL_DDR3_DQS0_P
PL_DDR3_DQS0_N
PL_DDR3_DQS1_P
PL_DDR3_DQS1_N
PL_DDR3_DQ0
PL_DDR3_DQ1
PL_DDR3_DQ2
PL_DDR3_DQ3
PL_DDR3_DQ4
PL_DDR3_DQ5
PL_DDR3_DQ6
PL_DDR3_DQ7
PL_DDR3_DQ8
PL_DDR3_DQ9
PL_DDR3_DQ10
PL_DDR3_DQ11
PL_DDR3_DQ12
PL_DDR3_DQ13
PL_DDR3_DQ14
PL_DDR3_DQ15
RML1
RML2
240
PL_DDR3_DM2
PL_DDR3_DM3
PL_DDR3_DQS2_P
PL_DDR3_DQS2_N
PL_DDR3_DQS3_P
PL_DDR3_DQS3_N
PL_DDR3_DQ16
PL_DDR3_DQ17
PL_DDR3_DQ18
PL_DDR3_DQ19
PL_DDR3_DQ20
PL_DDR3_DQ21
PL_DDR3_DQ22
PL_DDR3_DQ23
PL_DDR3_DQ24
PL_DDR3_DQ25
PL_DDR3_DQ26
PL_DDR3_DQ27
PL_DDR3_DQ28
PL_DDR3_DQ29
PL_DDR3_DQ30
PL_DDR3_DQ31
RMP1
RMP2
RMP3
VTT_DDR
40.2 1%
For 800MHz frequency,terminal resistance is suggested for using.
Terminal resistance value is 40ou
ECML7
CML41
ECML8
CML42
ECML9
CML43
10uF/6.3V
0.1uF
CML1
CML2
CML3
CML4
CML5
CML6
CML7
CML8
CML9
CML10
CML11
CML12
CML13
CML14
CML15
CML16
CML17
CML18
CML19
CML20
CML21
CML22
CML23
CML24
CML25
CML26
CML27
CML28
CML29
CML30
CML31
CML32
CML33
CML34
CML35
CML36
CML37
CML38
0.47uF/6.3V
4.7uF/6.3V
ECML1
ECML2
ECML3
ECML4
ECML5
ECML6
22uF/6.3V
PL_DDR3_CKE
PL_DDR3_RESET_B
PL_DDR3_CLK_P
PL_DDR3_CLK_N
RML3
RML4
RML5
10K
80.6 1%
V3BEST
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11 PL_DDR3L
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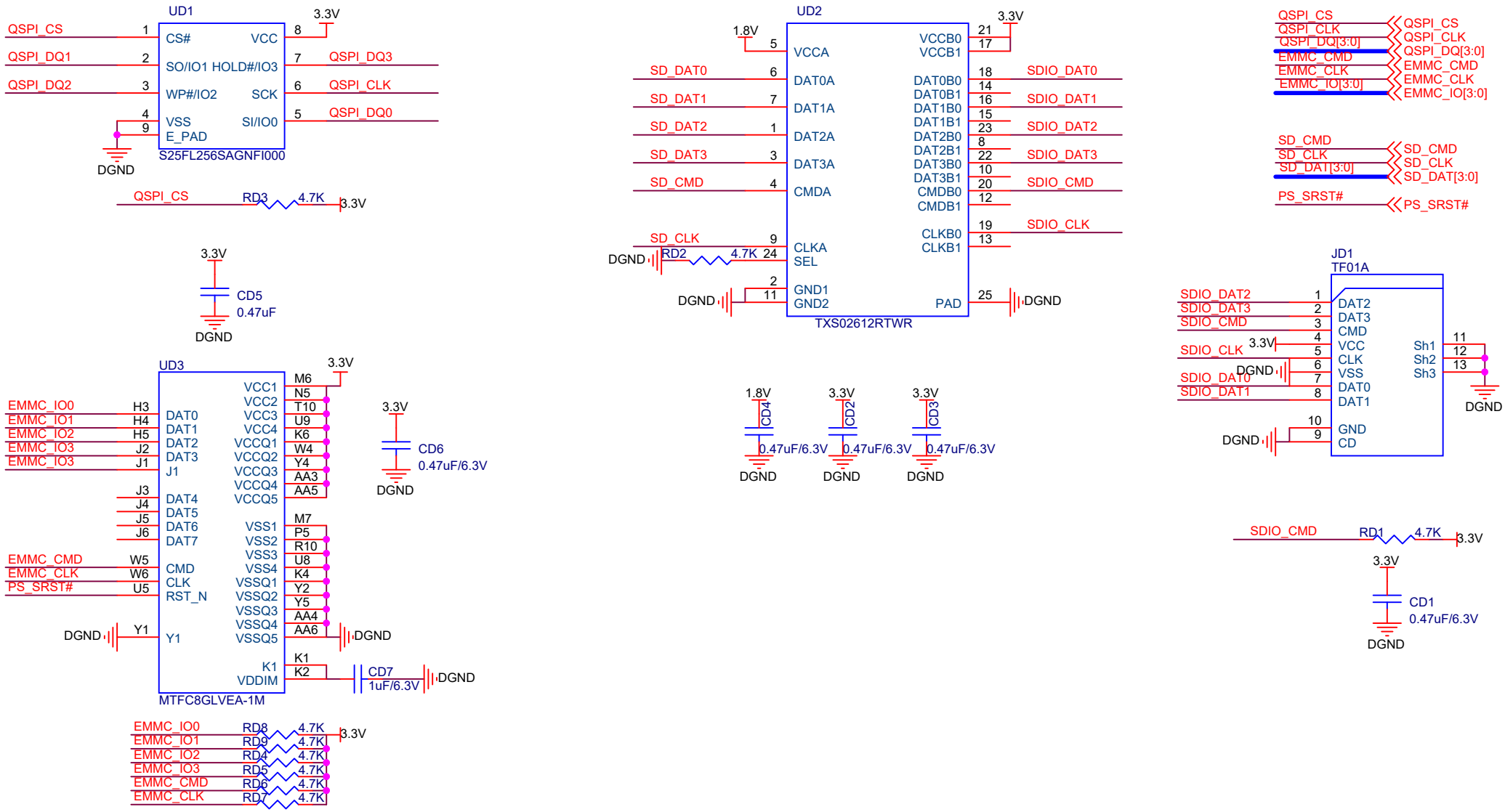

Title	V3BEST DeepRED			
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MARVELL 88E116R gets short of supply, should change SCH to 88E116

UL1-1

UL1-2 88E1116

88E1116

JL1 HR911130C

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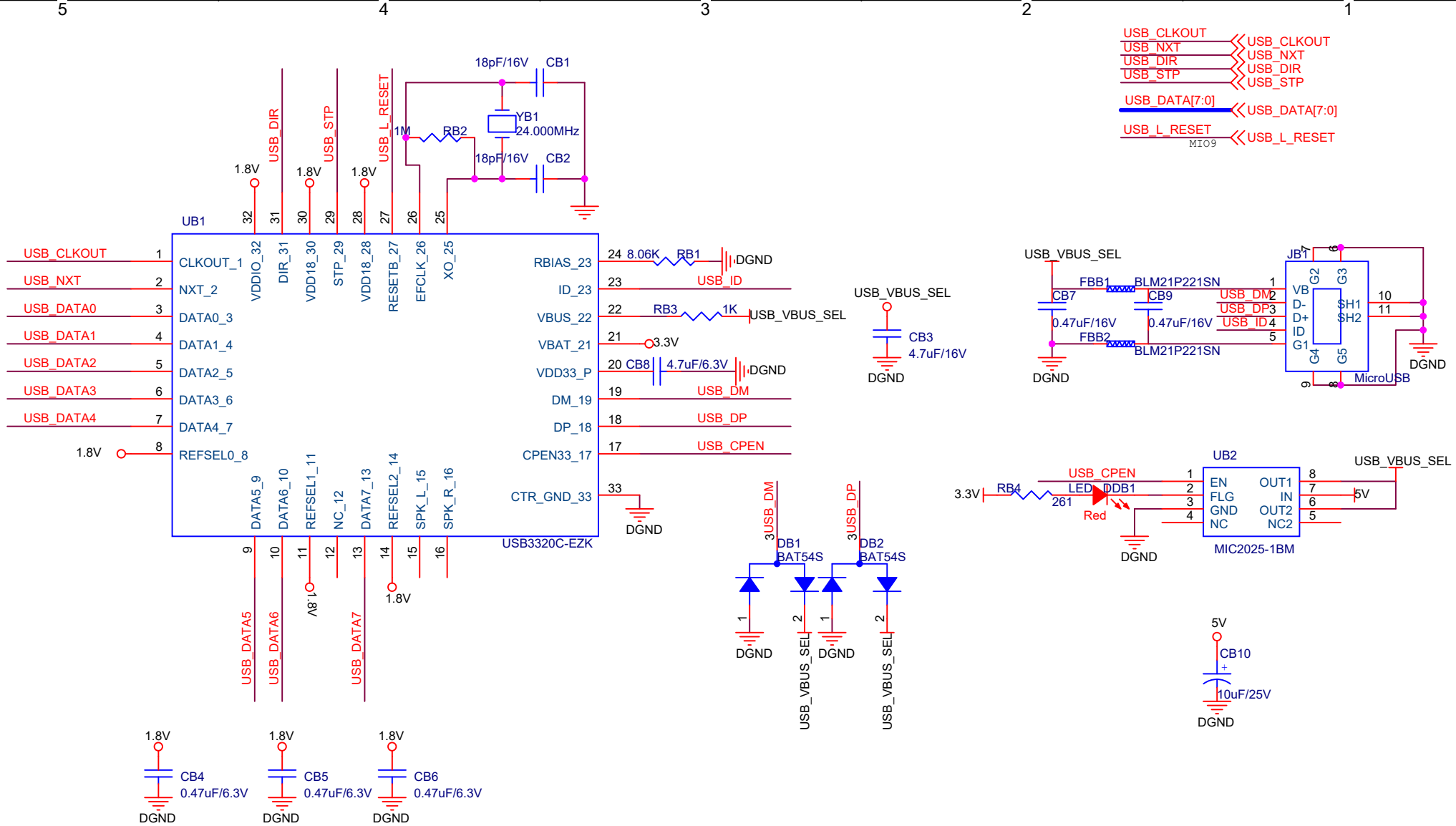

Title	V3BEST DeepRED		
Size A4	Document Number 14 USB_OTG		Rev V1.1
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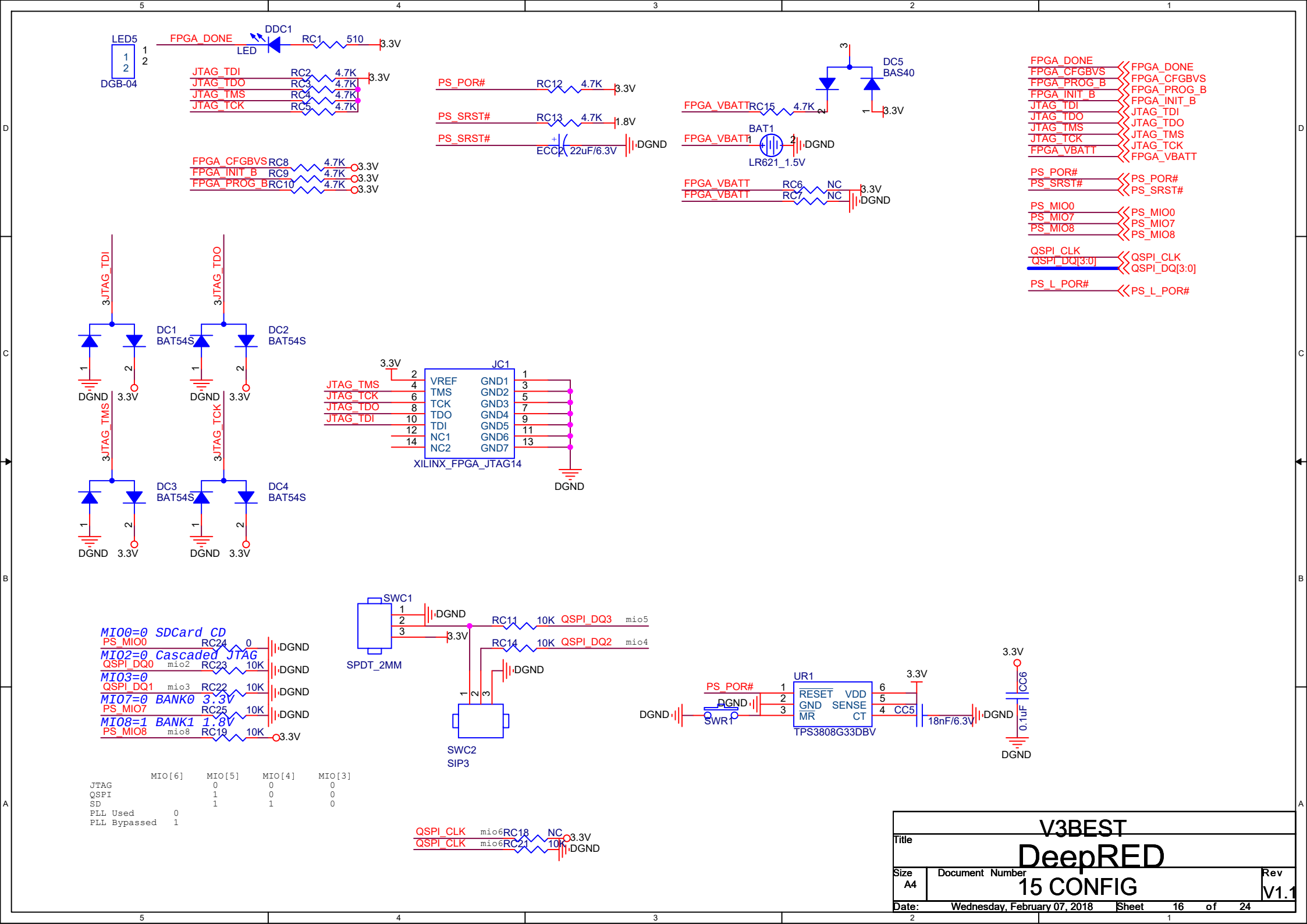

Title	V3BEST DeepRED
Size	A4
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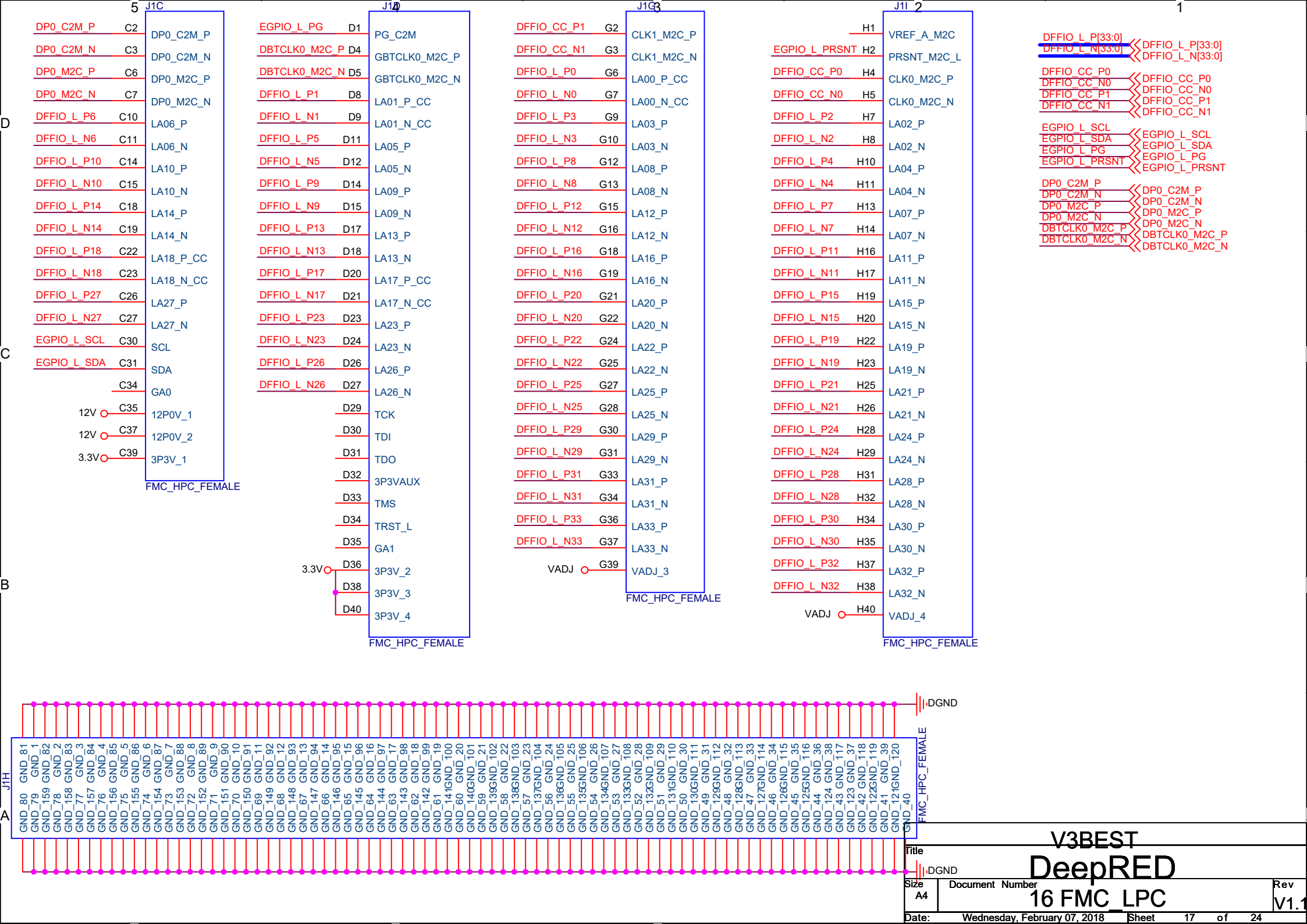
J1C
DP0_C2M_P C2
DP0_C2M_N C3
DP0_M2C_P C6
DP0_M2C_N C7
DFFIO_L_P6 C10
DFFIO_L_N6 C11
DFFIO_L_P10 C14
DFFIO_L_N10 C15
DFFIO_L_P14 C18
DFFIO_L_N14 C19
DFFIO_L_P18 C22
DFFIO_L_N18 C23
DFFIO_L_P27 C26
DFFIO_L_N27 C27
EGPIO_L_SCL C30
EGPIO_L_SDA C31
C34
12V C35
12V C37
3.3V C39
DP0_C2M_P
DP0_C2M_N
DP0_M2C_P
DP0_M2C_N
LA06_P
LA06_N
LA10_P
LA10_N
LA14_P
LA14_N
LA18_P_CC
LA18_N_CC
LA27_P
LA27_N
SCL
SDA
GA0
12P0V_1
12P0V_2
3P3V_1
FMC_HPC_FEMALE
J1D
EGPIO_L_PG D1
DBTCLK0_M2C_P D4
DBTCLK0_M2C_N D5
DFFIO_L_P1 D8
DFFIO_L_N1 D9
DFFIO_L_P5 D11
DFFIO_L_N5 D12
DFFIO_L_P9 D14
DFFIO_L_N9 D15
DFFIO_L_P13 D17
DFFIO_L_N13 D18
DFFIO_L_P17 D20
DFFIO_L_N17 D21
DFFIO_L_P23 D23
DFFIO_L_N23 D24
DFFIO_L_P26 D26
DFFIO_L_N26 D27
D29
D30
D31
D32
D33
D34
D35
3.3V D36
D38
D40
PG_C2M
GBTCLK0_M2C_P
GBTCLK0_M2C_N
LA01_P_CC
LA01_N_CC
LA05_P
LA05_N
LA09_P
LA09_N
LA13_P
LA13_N
LA17_P_CC
LA17_N_CC
LA23_P
LA23_N
LA26_P
LA26_N
TCK
TDI
TDO
3P3VAUX
TMS
TRST_L
GA1
3P3V_2
3P3V_3
3P3V_4
FMC_HPC_FEMALE
J1G
DFFIO_CC_P1 G2
DFFIO_CC_N1 G3
DFFIO_L_P0 G6
DFFIO_L_N0 G7
DFFIO_L_P3 G9
DFFIO_L_N3 G10
DFFIO_L_P8 G12
DFFIO_L_N8 G13
DFFIO_L_P12 G15
DFFIO_L_N12 G16
DFFIO_L_P16 G18
DFFIO_L_N16 G19
DFFIO_L_P20 G21
DFFIO_L_N20 G22
DFFIO_L_P22 G24
DFFIO_L_N22 G25
DFFIO_L_P25 G27
DFFIO_L_N25 G28
DFFIO_L_P29 G30
DFFIO_L_N29 G31
DFFIO_L_P31 G33
DFFIO_L_N31 G34
DFFIO_L_P33 G36
DFFIO_L_N33 G37
VADJ G39
CLK1_M2C_P
CLK1_M2C_N
LA00_P_CC
LA00_N_CC
LA03_P
LA03_N
LA08_P
LA08_N
LA12_P
LA12_N
LA16_P
LA16_N
LA20_P
LA20_N
LA22_P
LA22_N
LA25_P
LA25_N
LA29_P
LA29_N
LA31_P
LA31_N
LA33_P
LA33_N
VADJ_3
FMC_HPC_FEMALE
J1I
H1
EGPIO_L_PRSNT H2
DFFIO_CC_P0 H4
DFFIO_CC_N0 H5
DFFIO_L_P2 H7
DFFIO_L_N2 H8
DFFIO_L_P4 H10
DFFIO_L_N4 H11
DFFIO_L_P7 H13
DFFIO_L_N7 H14
DFFIO_L_P11 H16
DFFIO_L_N11 H17
DFFIO_L_P15 H19
DFFIO_L_N15 H20
DFFIO_L_P19 H22
DFFIO_L_N19 H23
DFFIO_L_P21 H25
DFFIO_L_N21 H26
DFFIO_L_P24 H28
DFFIO_L_N24 H29
DFFIO_L_P28 H31
DFFIO_L_N28 H32
DFFIO_L_P30 H34
DFFIO_L_N30 H35
DFFIO_L_P32 H37
DFFIO_L_N32 H38
VADJ H40
VREF_A_M2C
PRSNT_M2C_L
CLK0_M2C_P
CLK0_M2C_N
LA02_P
LA02_N
LA04_P
LA04_N
LA07_P
LA07_N
LA11_P
LA11_N
LA15_P
LA15_N
LA19_P
LA19_N
LA21_P
LA21_N
LA24_P
LA24_N
LA28_P
LA28_N
LA30_P
LA30_N
LA32_P
LA32_N
VADJ_4
FMC_HPC_FEMALE
DFFIO_L_P[33:0]
DFFIO_L_N[33:0]
DFFIO_L_P[33:0]
DFFIO_L_N[33:0]
DFFIO_CC_P0
DFFIO_CC_N0
DFFIO_CC_P1
DFFIO_CC_N1
DFFIO_CC_P0
DFFIO_CC_N0
DFFIO_CC_P1
DFFIO_CC_N1
EGPIO_L_SCL
EGPIO_L_SDA
EGPIO_L_PG
EGPIO_L_PRSNT
EGPIO_L_SCL
EGPIO_L_SDA
EGPIO_L_PG
EGPIO_L_PRSNT
DP0_C2M_P
DP0_C2M_N
DP0_M2C_P
DP0_M2C_N
DBTCLK0_M2C_P
DBTCLK0_M2C_N
DP0_C2M_P
DP0_C2M_N
DP0_M2C_P
DP0_M2C_N
DBTCLK0_M2C_P
DBTCLK0_M2C_N
J1H
GND_81 GND_80 GND_1 GND_79 GND_82 GND_159 GND_2 GND_78 GND_83 GND_158 GND_3 GND_77 GND_84 GND_157 GND_4 GND_76 GND_85 GND_156 GND_5 GND_75 GND_86 GND_155 GND_6 GND_74 GND_87 GND_154 GND_7 GND_73 GND_88 GND_153 GND_8 GND_72 GND_89 GND_152 GND_9 GND_71 GND_90 GND_151 GND_10 GND_70 GND_91 GND_150 GND_11 GND_69 GND_92 GND_149 GND_12 GND_68 GND_93 GND_148 GND_13 GND_67 GND_94 GND_147 GND_14 GND_66 GND_95 GND_146 GND_15 GND_65 GND_96 GND_145 GND_16 GND_64 GND_97 GND_144 GND_17 GND_63 GND_98 GND_143 GND_18 GND_62 GND_99 GND_142 GND_19 GND_61 GND_100 GND_141 GND_20 GND_60 GND_101 GND_140 GND_21 GND_59 GND_102 GND_139 GND_22 GND_58 GND_103 GND_138 GND_23 GND_57 GND_104 GND_137 GND_24 GND_56 GND_105 GND_136 GND_25 GND_55 GND_106 GND_135 GND_26 GND_54 GND_107 GND_134 GND_27 GND_53 GND_108 GND_133 GND_28 GND_52 GND_109 GND_132 GND_29 GND_51 GND_110 GND_131 GND_30 GND_50 GND_111 GND_130 GND_31 GND_49 GND_112 GND_129 GND_32 GND_48 GND_113 GND_128 GND_33 GND_47 GND_114 GND_127 GND_34 GND_46 GND_115 GND_126 GND_35 GND_45 GND_116 GND_125 GND_36 GND_44 GND_117 GND_124 GND_38 GND_43 GND_118 GND_123 GND_37 GND_42 GND_119 GND_122 GND_39 GND_41 GND_120 GND_121 GND_40
FMC_HPC_FEMALE
DGND
DGND
V3BEST
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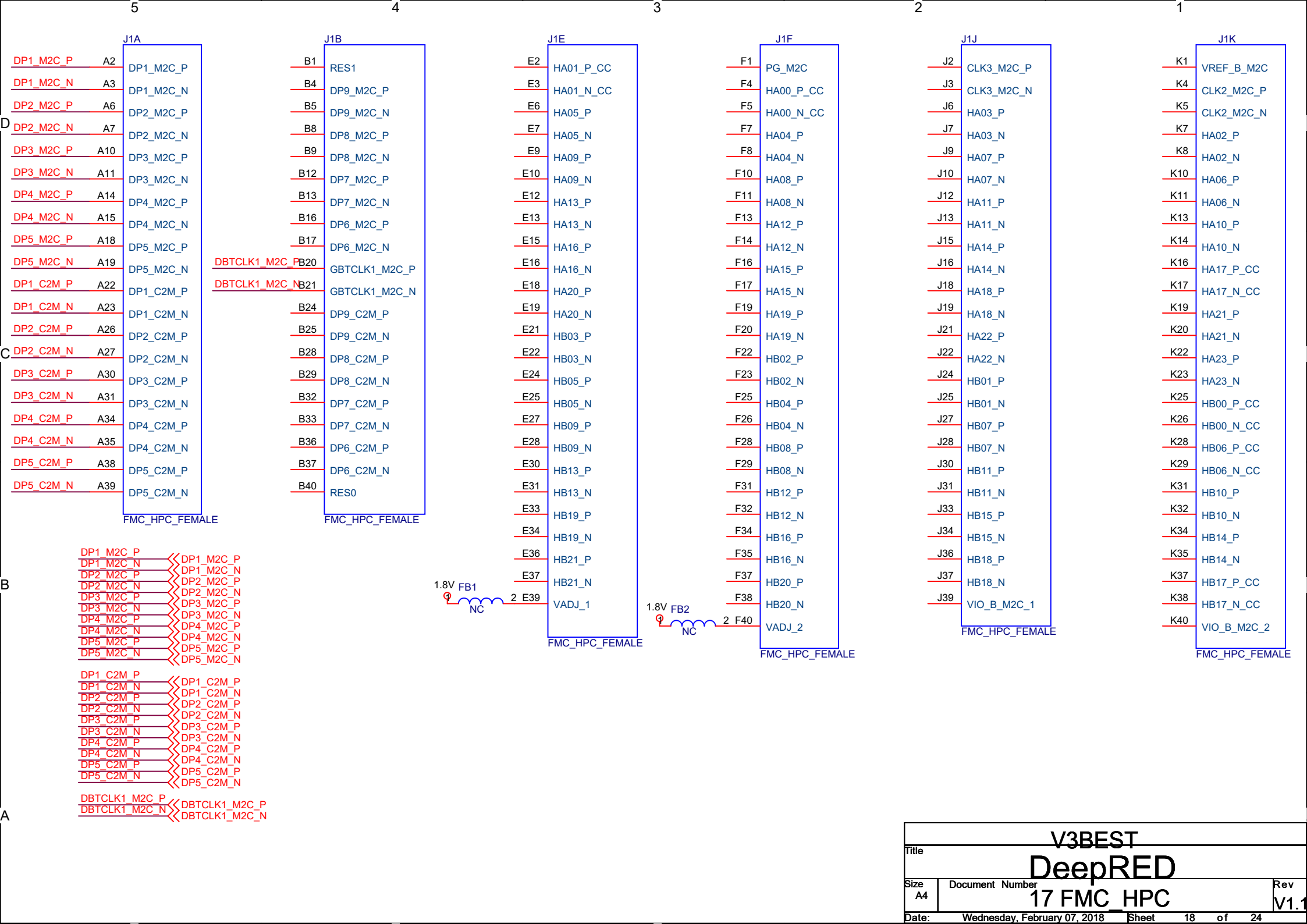
5
4
3
2
1
D
C
B
A
J1A
DP1_M2C_P A2
DP1_M2C_N A3
DP2_M2C_P A6
DP2_M2C_N A7
DP3_M2C_P A10
DP3_M2C_N A11
DP4_M2C_P A14
DP4_M2C_N A15
DP5_M2C_P A18
DP5_M2C_N A19
DP1_C2M_P A22
DP1_C2M_N A23
DP2_C2M_P A26
DP2_C2M_N A27
DP3_C2M_P A30
DP3_C2M_N A31
DP4_C2M_P A34
DP4_C2M_N A35
DP5_C2M_P A38
DP5_C2M_N A39
DP1_M2C_P
DP1_M2C_N
DP2_M2C_P
DP2_M2C_N
DP3_M2C_P
DP3_M2C_N
DP4_M2C_P
DP4_M2C_N
DP5_M2C_P
DP5_M2C_N
DP1_C2M_P
DP1_C2M_N
DP2_C2M_P
DP2_C2M_N
DP3_C2M_P
DP3_C2M_N
DP4_C2M_P
DP4_C2M_N
DP5_C2M_P
DP5_C2M_N
FMC_HPC_FEMALE
J1B
B1 RES1
B4 DP9_M2C_P
B5 DP9_M2C_N
B8 DP8_M2C_P
B9 DP8_M2C_N
B12 DP7_M2C_P
B13 DP7_M2C_N
B16 DP6_M2C_P
B17 DP6_M2C_N
DBTCLK1_M2C_P B20 GBTCLK1_M2C_P
DBTCLK1_M2C_N B21 GBTCLK1_M2C_N
B24 DP9_C2M_P
B25 DP9_C2M_N
B28 DP8_C2M_P
B29 DP8_C2M_N
B32 DP7_C2M_P
B33 DP7_C2M_N
B36 DP6_C2M_P
B37 DP6_C2M_N
B40 RES0
DBTCLK1_M2C_P
DBTCLK1_M2C_N
FMC_HPC_FEMALE
J1E
E2 HA01_P_CC
E3 HA01_N_CC
E6 HA05_P
E7 HA05_N
E9 HA09_P
E10 HA09_N
E12 HA13_P
E13 HA13_N
E15 HA16_P
E16 HA16_N
E18 HA20_P
E19 HA20_N
E21 HB03_P
E22 HB03_N
E24 HB05_P
E25 HB05_N
E27 HB09_P
E28 HB09_N
E30 HB13_P
E31 HB13_N
E33 HB19_P
E34 HB19_N
E36 HB21_P
E37 HB21_N
2 E39 VADJ_1
1.8V FB1 NC
FMC_HPC_FEMALE
J1F
F1 PG_M2C
F4 HA00_P_CC
F5 HA00_N_CC
F7 HA04_P
F8 HA04_N
F10 HA08_P
F11 HA08_N
F13 HA12_P
F14 HA12_N
F16 HA15_P
F17 HA15_N
F19 HA19_P
F20 HA19_N
F22 HB02_P
F23 HB02_N
F25 HB04_P
F26 HB04_N
F28 HB08_P
F29 HB08_N
F31 HB12_P
F32 HB12_N
F34 HB16_P
F35 HB16_N
F37 HB20_P
F38 HB20_N
2 F40 VADJ_2
1.8V FB2 NC
FMC_HPC_FEMALE
J1J
J2 CLK3_M2C_P
J3 CLK3_M2C_N
J6 HA03_P
J7 HA03_N
J9 HA07_P
J10 HA07_N
J12 HA11_P
J13 HA11_N
J15 HA14_P
J16 HA14_N
J18 HA18_P
J19 HA18_N
J21 HA22_P
J22 HA22_N
J24 HB01_P
J25 HB01_N
J27 HB07_P
J28 HB07_N
J30 HB11_P
J31 HB11_N
J33 HB15_P
J34 HB15_N
J36 HB18_P
J37 HB18_N
J39 VIO_B_M2C_1
FMC_HPC_FEMALE
J1K
K1 VREF_B_M2C
K4 CLK2_M2C_P
K5 CLK2_M2C_N
K7 HA02_P
K8 HA02_N
K10 HA06_P
K11 HA06_N
K13 HA10_P
K14 HA10_N
K16 HA17_P_CC
K17 HA17_N_CC
K19 HA21_P
K20 HA21_N
K22 HA23_P
K23 HA23_N
K25 HB00_P_CC
K26 HB00_N_CC
K28 HB06_P_CC
K29 HB06_N_CC
K31 HB10_P
K32 HB10_N
K34 HB14_P
K35 HB14_N
K37 HB17_P_CC
K38 HB17_N_CC
K40 VIO_B_M2C_2
FMC_HPC_FEMALE
V3BEST
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DeepRED
Size A4
Document Number
17 FMC_HPC
Rev V1.1
Date: Wednesday, February 07, 2018
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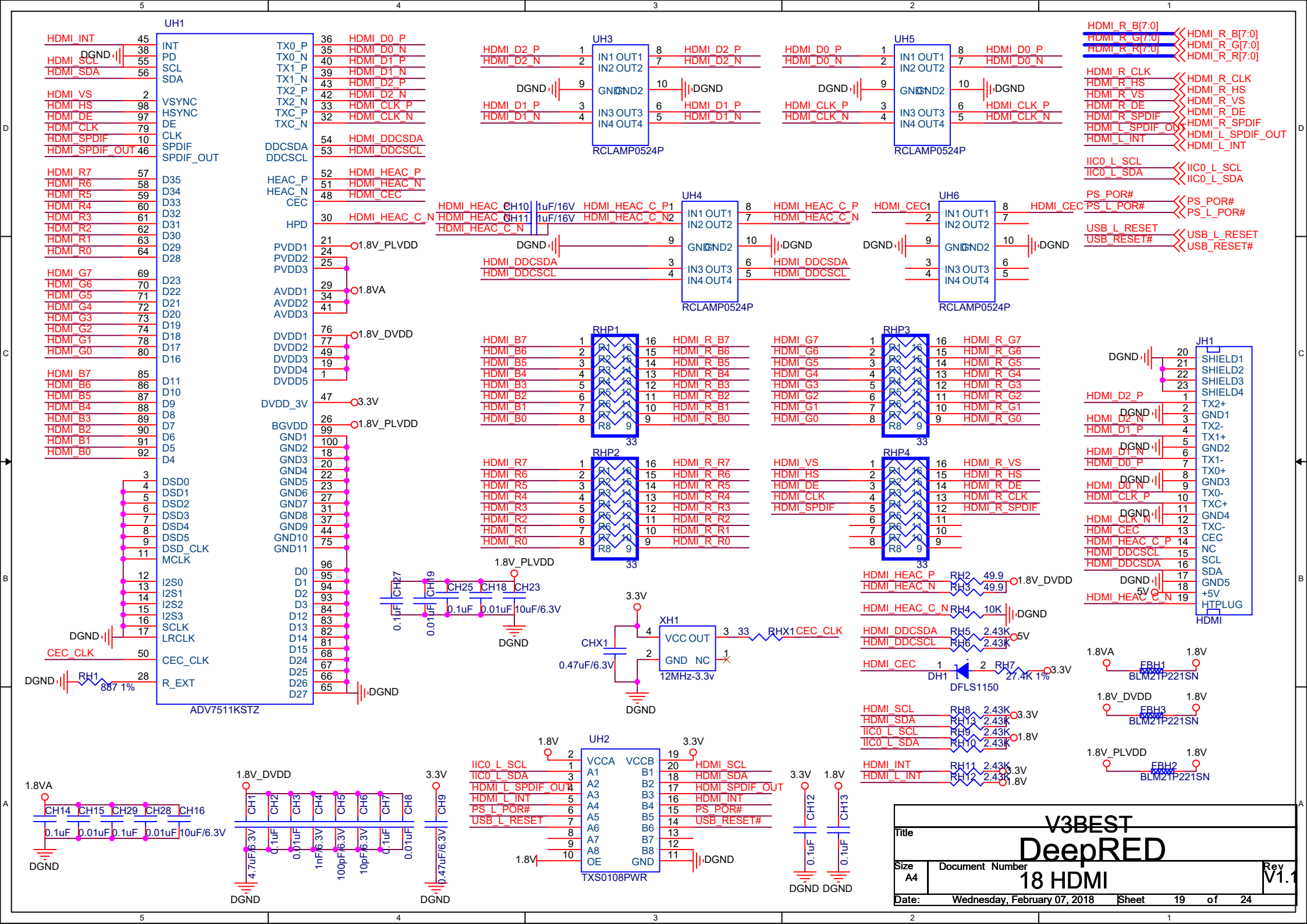

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Size A4	Document Number 18 HDMI		Rev V1.1
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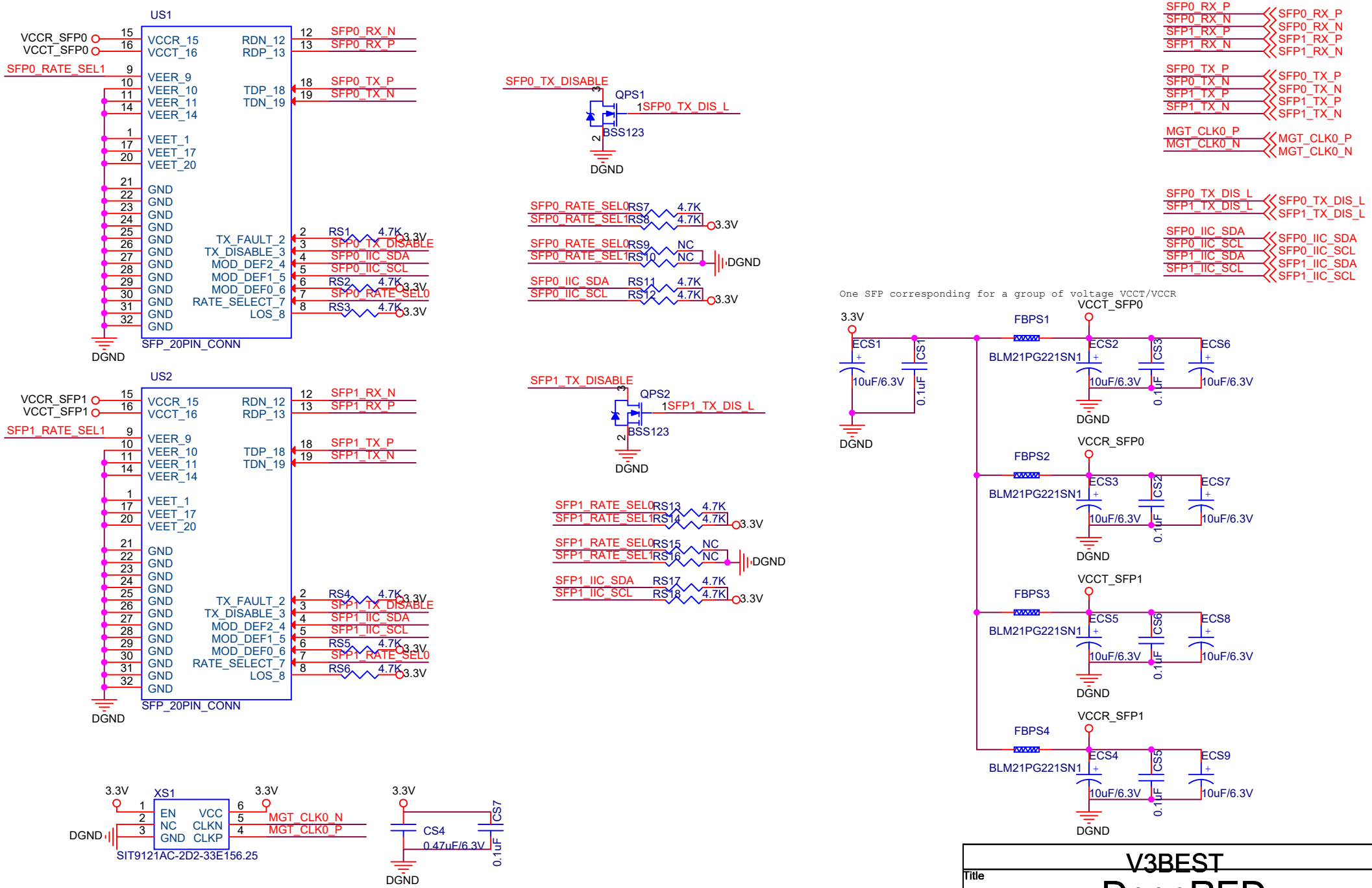

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Size A4	Document Number 19 SFP+	Rev V1.1
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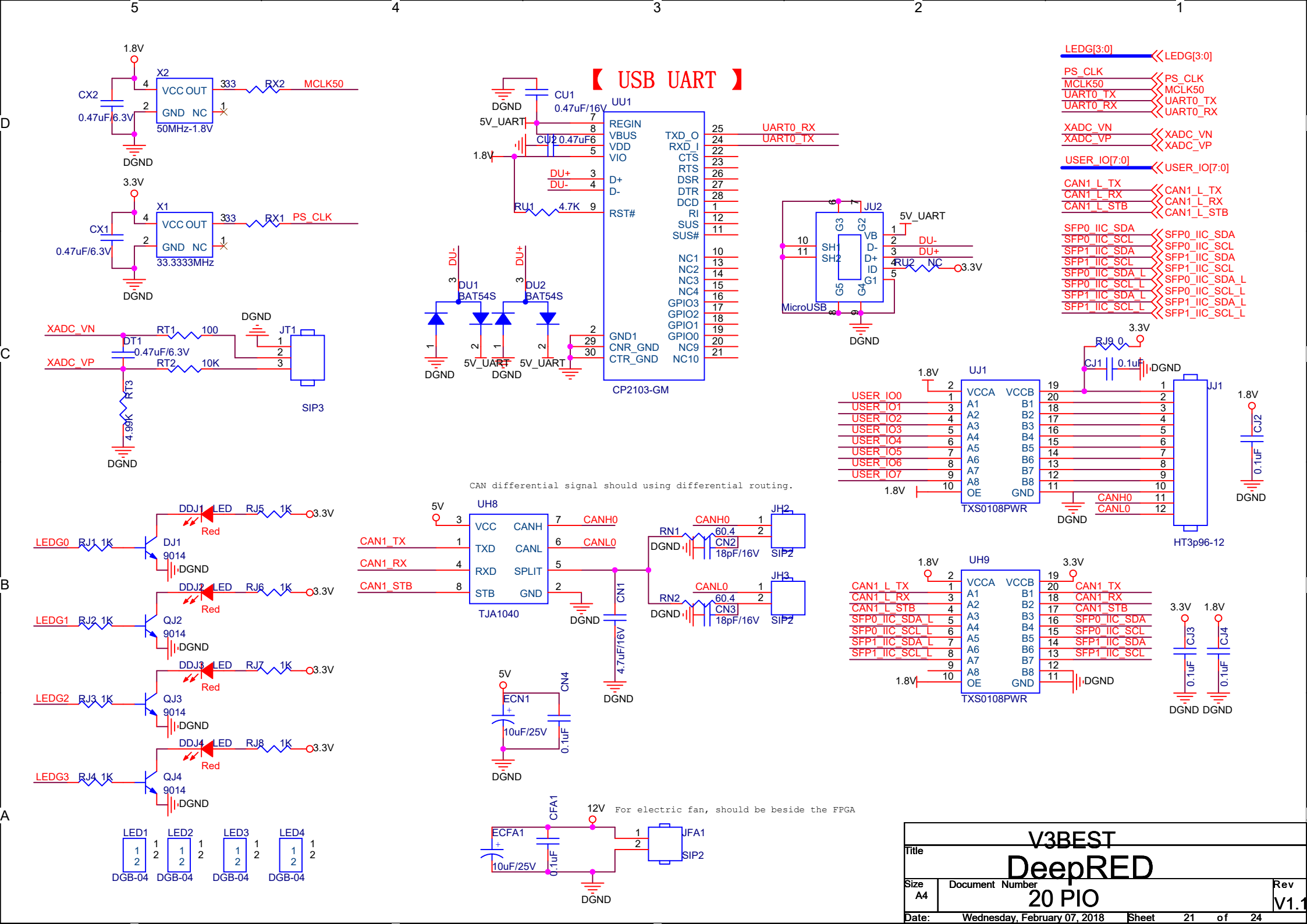
【 USB UART 】
CP2103-GM
TJA1040
TXS0108PWR
TXS0108PWR
HT3p96-12
CAN differential signal should using differential routing.
For electric fan, should be beside the FPGA
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DeepRED
20 PIO
Size A4
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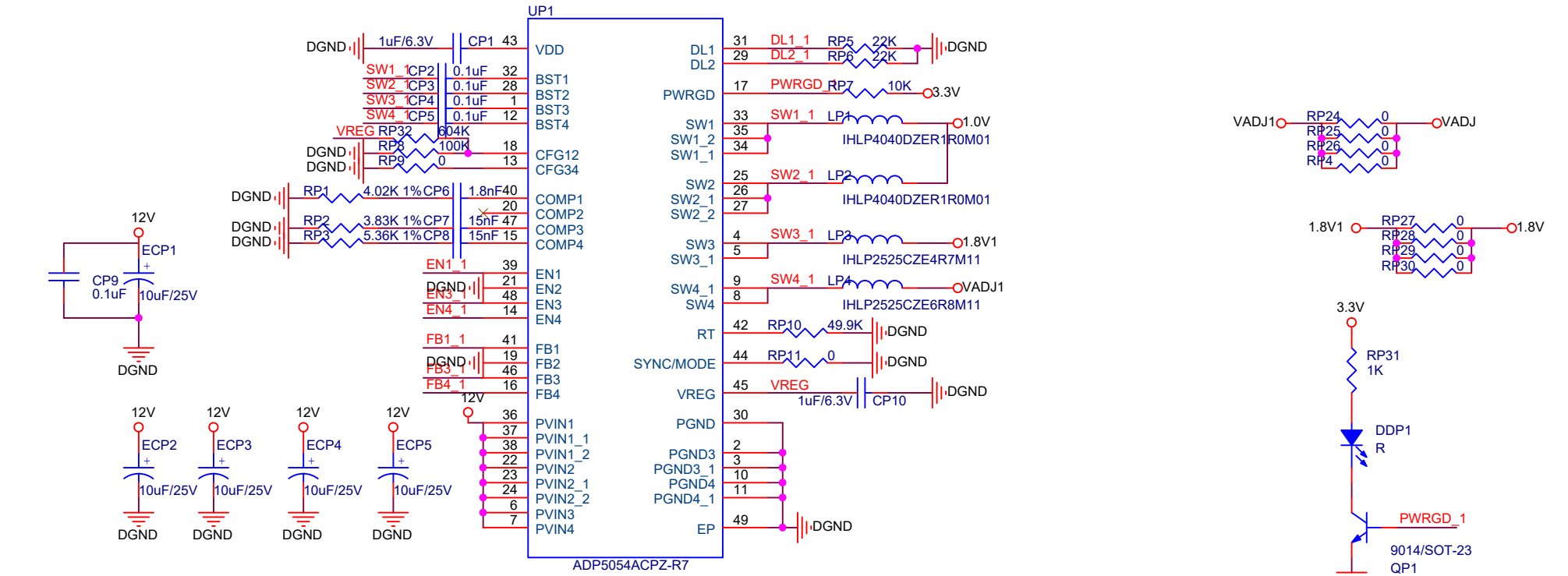

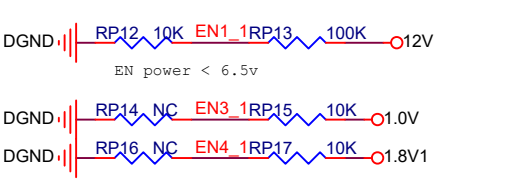

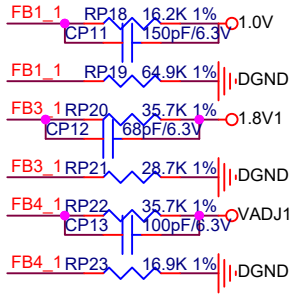

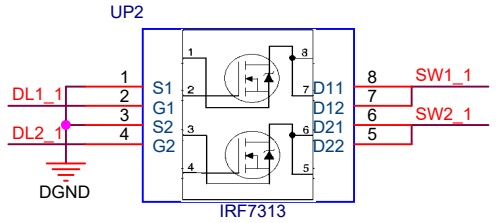

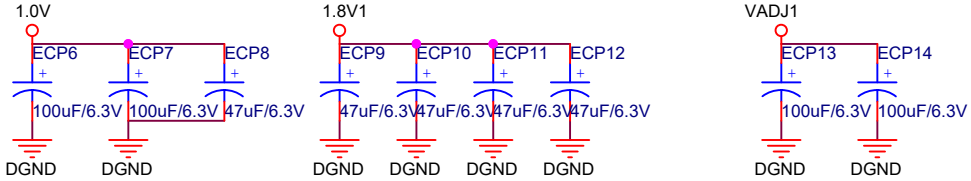

Title	V3BEST DeepRED		
Size A4	Document Number 21 SYS POWER1		Rev V1.1
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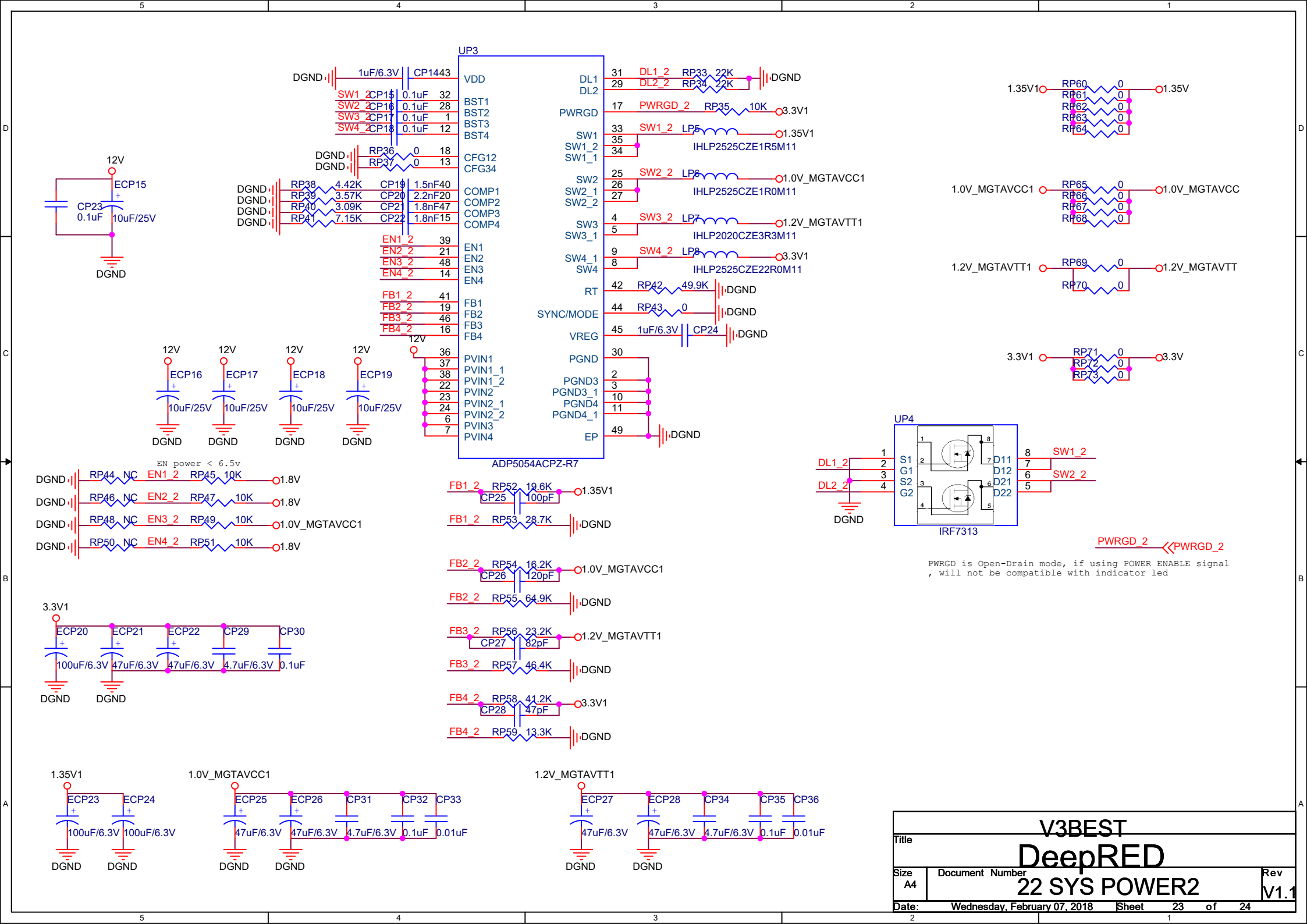

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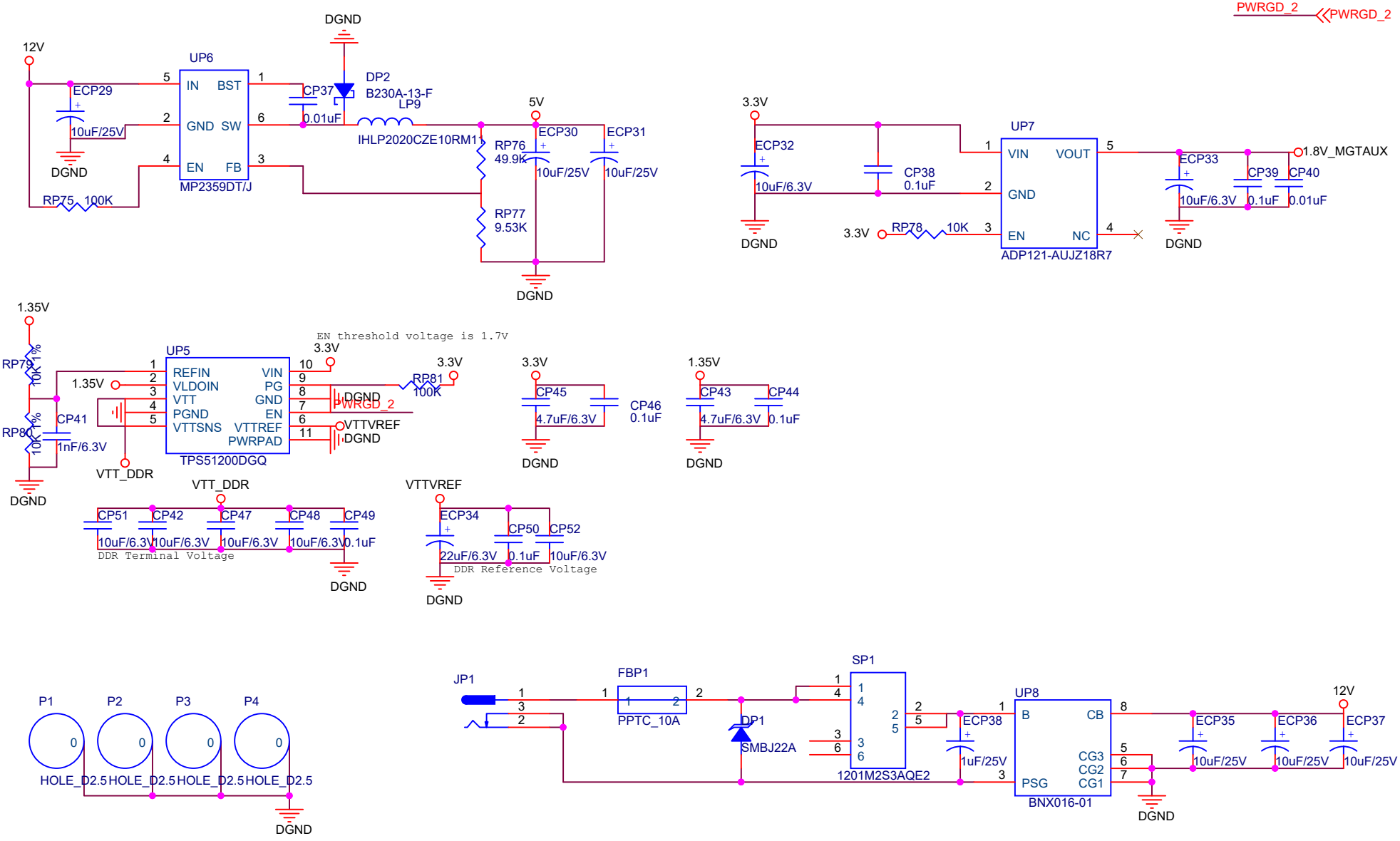
Size A4	Document Number 22 SYS POWER2		Rev V1.1
Date: Wednesday, February 07, 2018	Sheet 23 of 24		



Title	V3BEST DeepRED		
Size A4	Document Number 23 SYS POWER3		Rev V1.1
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