# Digital System Design

Experiment

Hancong Wu

hancongwu@scut.edu.cn

# Seats

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 讲台 | | | | | | | 门口 |
| | | | | | | | | |
| 汪思佟 | | 周钰欣 | | 蔡若潇 | | 周奕 | | 王子寒 |
| 陈子豪 | | 李雨桐 | | 陈诺 | | 秦可 | | 谢金璇 |
| 杨启帆 | | 曾子乘 | | 贾昊明 | | 刘昶玮 | | 陈健宇 |
| | | | | | | | | |
| 刘彦志 | | 程子航 | | 陈子轩 | | 赵容辰 | | 王实依 |
| 张济凡 | | 魏海川 | | 陈博灵 | | 韩诚 | | 全飞扬 |
| 殷嘉成 | | | | | | | | 梁沃林 |
| | | | | | | | | |
| 余幸桐 | | 刘子泓 | | 胡天屹 | | 邹易航 | | 刘兴琰 |
| 龙泓宇 | | 孙奥博 | | 郑旻翚 | | 孙振宇 | | 韦华泰 |
| 贺奕扬 | | | | | | | | 朱逸楠 |
| 吴潼 | | 王云帆 | | 渠开源 | | 朱轩霆 | | 余浩然 |
| 叶子绿 | | 朱斯玙 | | 王一凡 | | 赵崇杰 | | 张泰豪 |
| 康智乔 | | 乔羽桐 | | | | 王思颖 | | 李思瑶 |
| | | | | | | | | |
| 陈奕扬 | | 孙伟太 | | 黄浩铭 | | 王彧竹 | | 洪昌佑 |
| 李浩东 | | 张辰旭 | | 文闻 | | 殷聚贤 | | 林涛 |
| 吕昶玮 | | | | | | | | 卢泽宁 |
| | | | | | | | | |
| 黄炜琪 | | 董兴舒 | | 庞烨 | | 王城楷 | | 张翔 |
| 杨信庭 | | 方润泽 | | 姚舒颖 | | 张恩华 | | 马天越 |
| | | | | 赵伊伦 | | | | |

# Rules

- 40% Attendance + 60% Report
  - Attendance is related to: Check-in & check-out, experiment completion, device maintenance, etc.
  - Report is related to: Correct experimental results, quality of the report, comments and feedback, etc.
- Finish the experiment in a group but write the report on your own.
- Submit the report to the class rep before the next experiment (Late submission will lower your grade)
- Turn of the device and tidy up the bench before you leave.

# Digital System Design

## Experiment 1
## Familiar with Quartus II and VHDL

Hancong Wu

hancongwu@scut.edu.cn

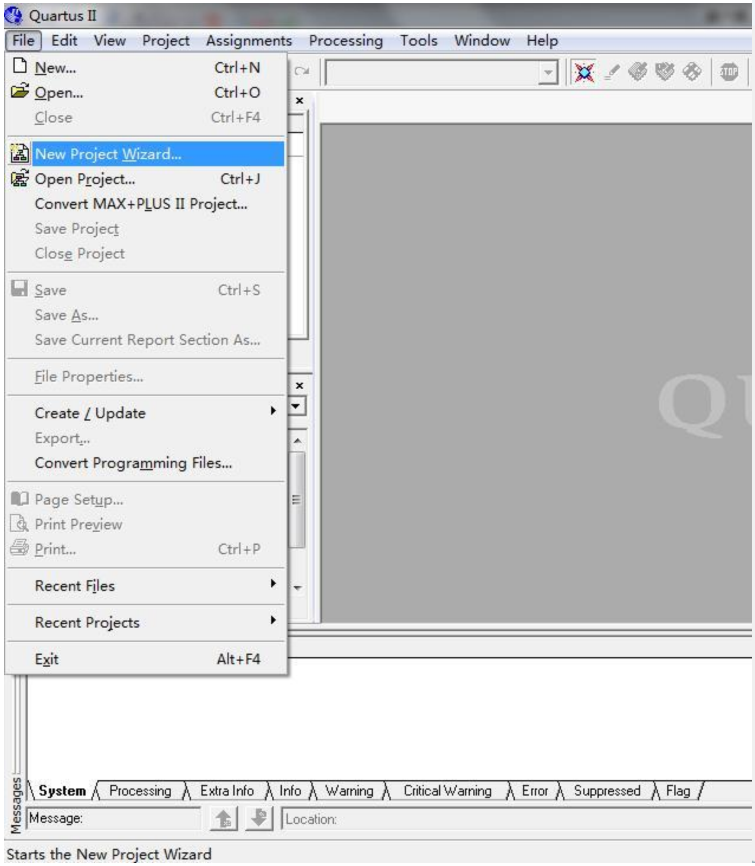
- Purpose
    - Familiarize with the basic structure of VHDL programming.
    - Learn how to compile VHDL code in quartus II and define components.
    - Learn how to test and verify the function of your design in quartus II.
- Tools
    - Quartus II 13.0
    - Modelsim

# Tasks

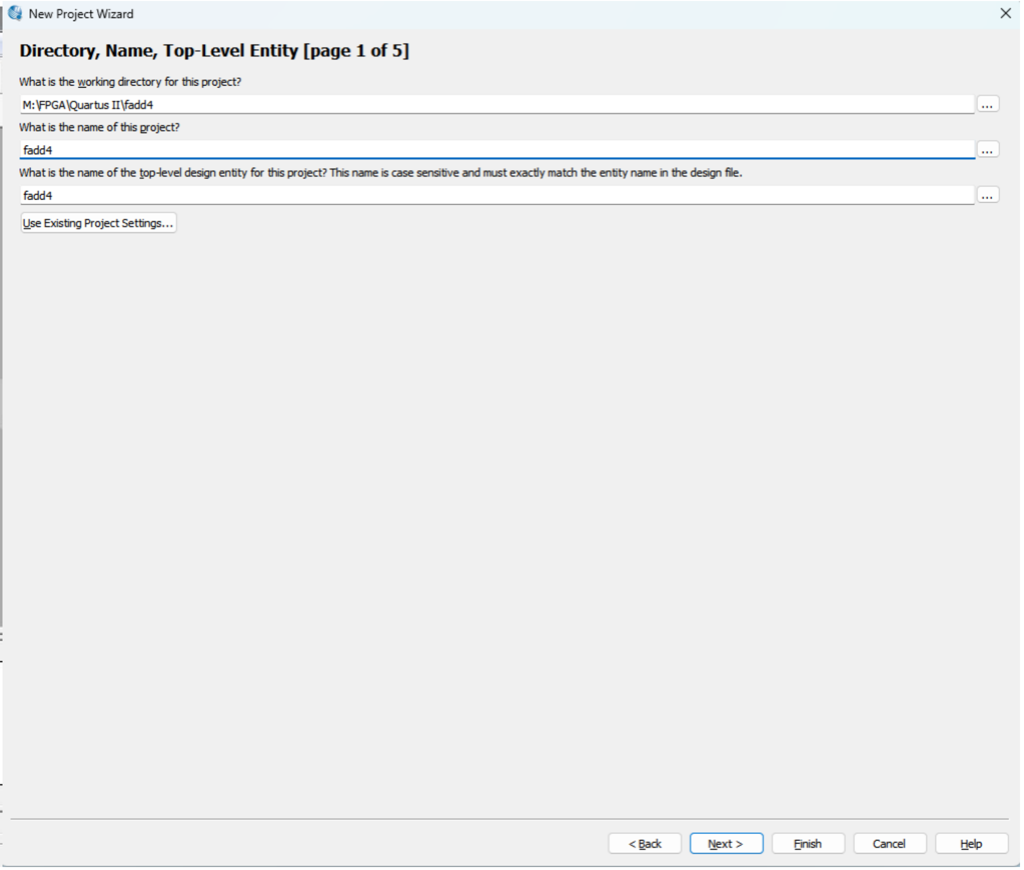
- Design a 1 bit adder following the instructions.
- Design the componennt on VHDL file following the description on the manual and comply it.
- Design an example of a four-bit adder using component.
- Perform the waveform simulation Using Quartus II and Modelsim.
- Run the simulation and record the results of Modelsim.

# Brief introduction to the experiment

- Create a project



Starts the New Project Wizard



**Directory, Name, Top-Level Entity [page 1 of 5]**

What is the working directory for this project?

M:\FPGA\Quartus II\fadd4

What is the name of this project?

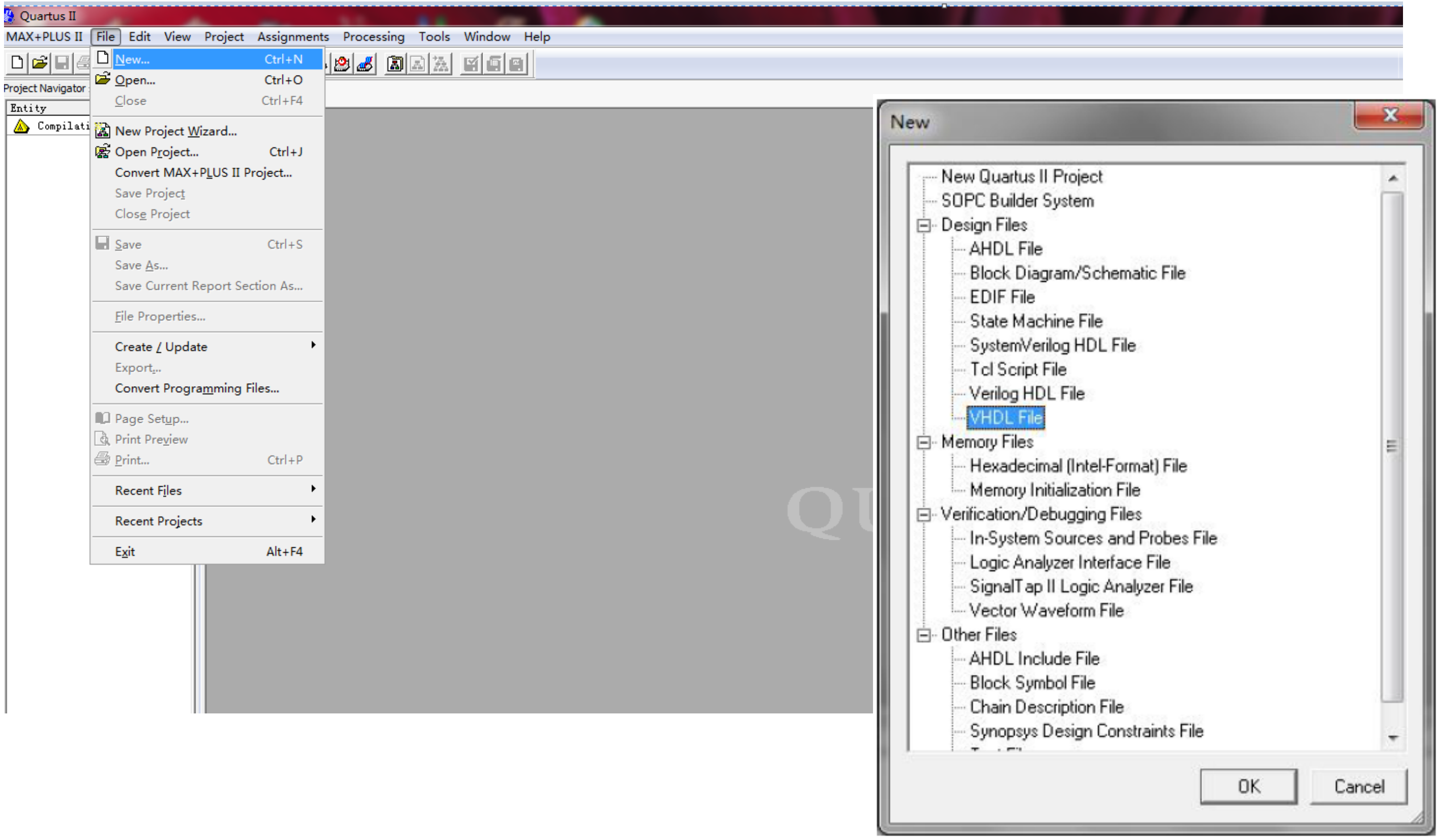
fadd4

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

fadd4

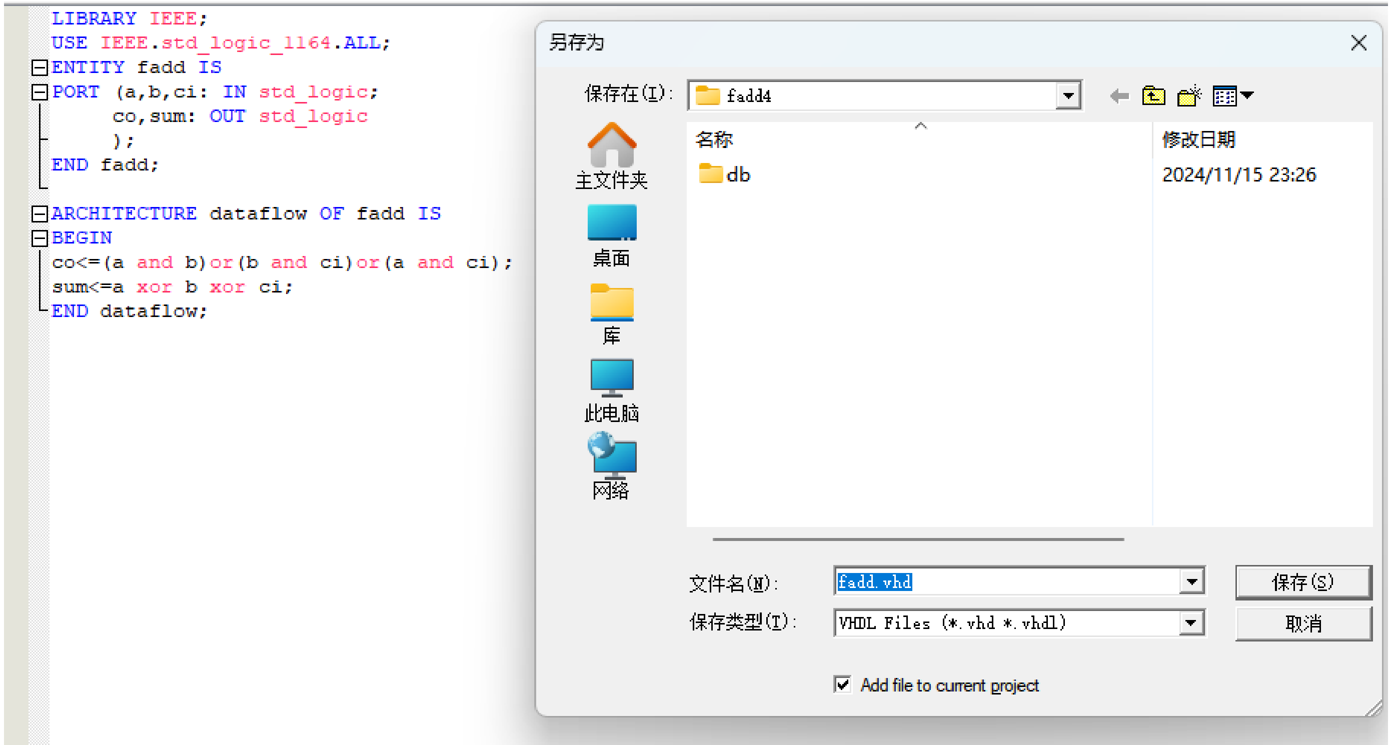
# Brief introduction to the experiment

- Create a VHDL file



# Brief introduction to the experiment

- Develop and save your program
  - Normally, save the .vhd file in the name of the ENTITY to increase the readability of the project.



```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
ENTITY fadd IS
PORT (a,b,ci: IN std_logic;
      co,sum: OUT std_logic
      );
END fadd;

ARCHITECTURE dataflow OF fadd IS
BEGIN
co<=(a and b)or(b and ci)or(a and ci);
sum<=a xor b xor ci;
END dataflow;
```

另存为

保存在(I): fadd4

| 名称 | 修改日期 |
|---|---|
| db | 2024/11/15 23:26 |

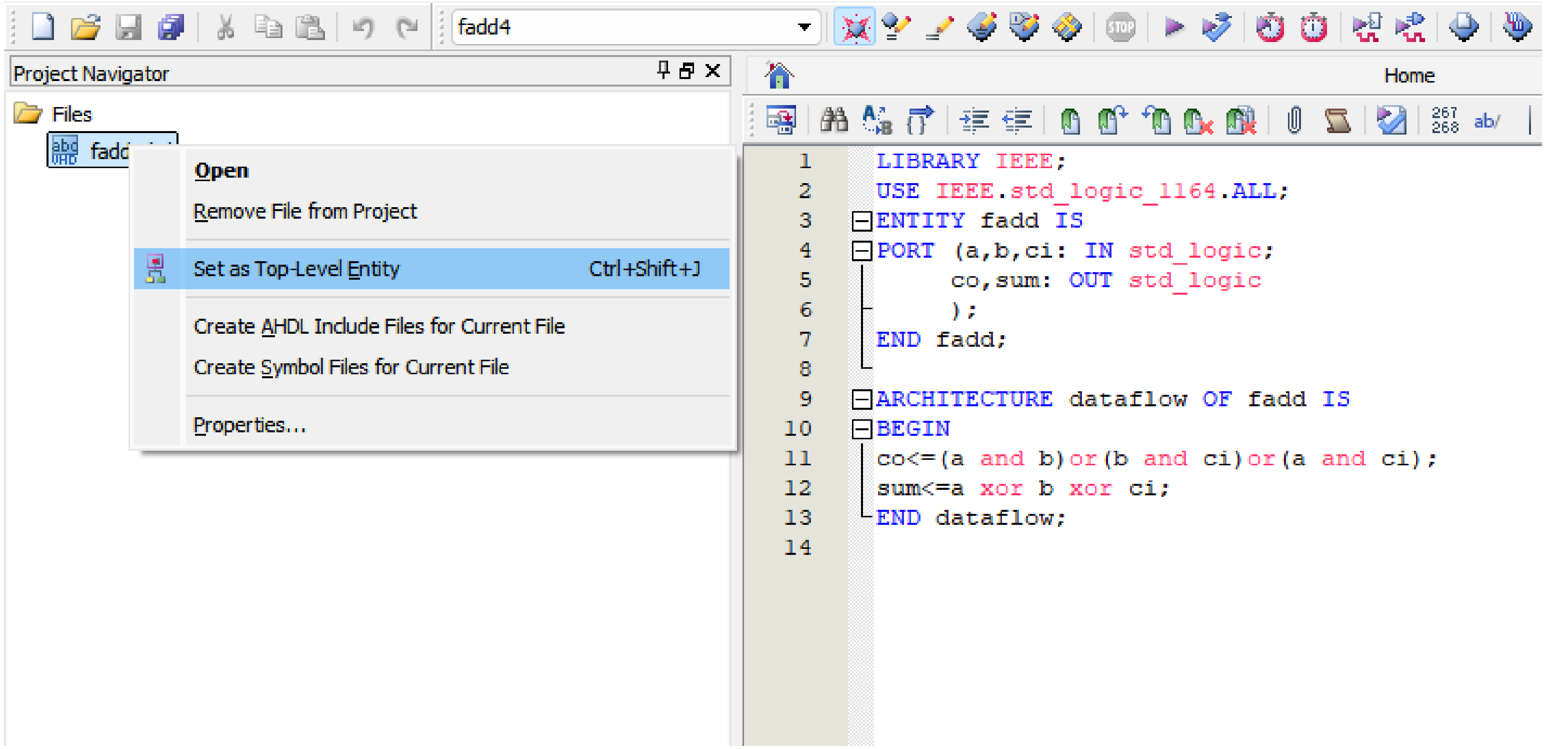
文件名(N): fadd.vhd

保存类型(T): VHDL Files (*.vhd *.vhdl)

☑ Add file to current project

# Brief introduction to the experiment

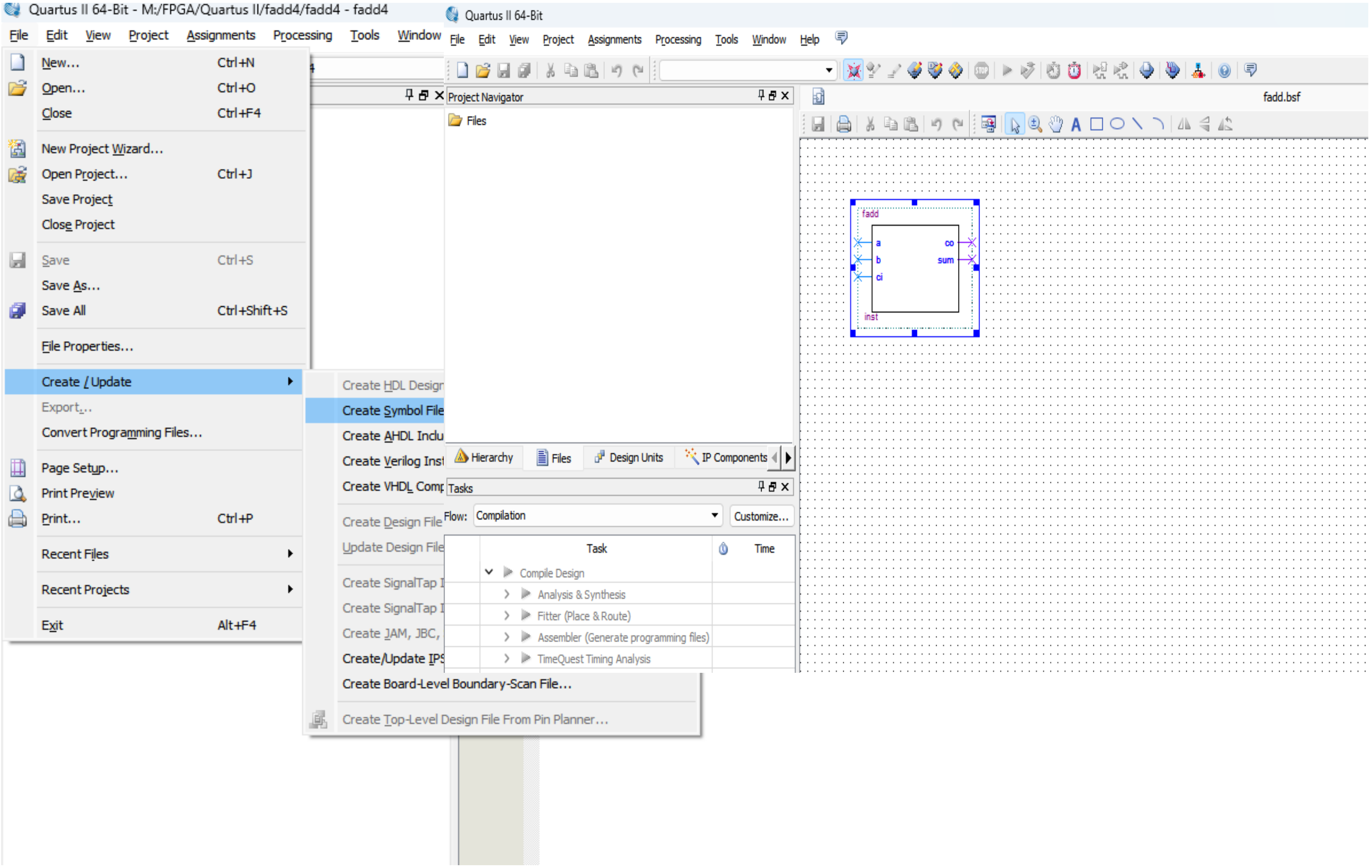
- Compliation
  - Set as Top-Level Entity and comply the file


fadd4
Project Navigator
Files
fadd
Home
Open
Remove File from Project
Set as Top-Level Entity Ctrl+Shift+J
Create AHDL Include Files for Current File
Create Symbol Files for Current File
Properties...

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
ENTITY fadd IS
PORT (a,b,ci: IN std_logic;
      co,sum: OUT std_logic
      );
END fadd;

ARCHITECTURE dataflow OF fadd IS
BEGIN
co<=(a and b)or(b and ci)or(a and ci);
sum<=a xor b xor ci;
END dataflow;
```

# Brief introduction to the experiment

- Create symbolic file



# Brief introduction to the experiment

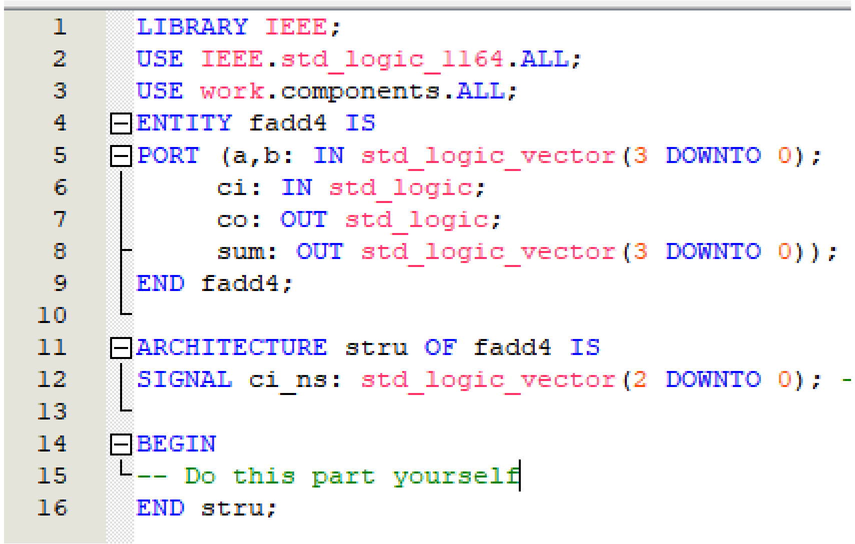
- Design component module for the 4 bit full adder:
  - Create a new .vhd file named component.vhd . The description of its function is on Page 14 of the tutorial.
  - Don’t set as top level and comply it.

**VHDL Code:**

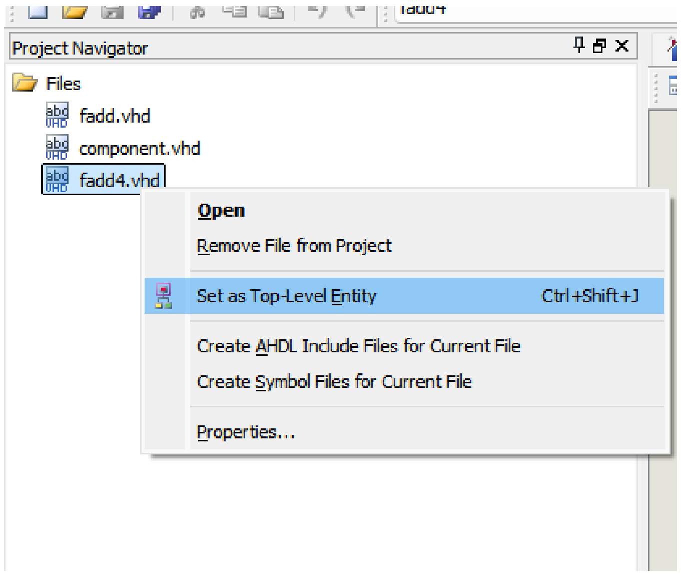
```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;PACKAGE components IS
 COMPONENT fadd IS
 PORT(a,b,ci: IN std_logic;
  co,sum: OUT std_logic);
 END COMPONENT;
END components;
```

# Brief introduction to the experiment

- Design an example of a four-bit adder
  - Create a VHDL File , use component to design a 4 bit adder and save as fadd4.vhd.
  - Set as Top-Level Entity and comply it.



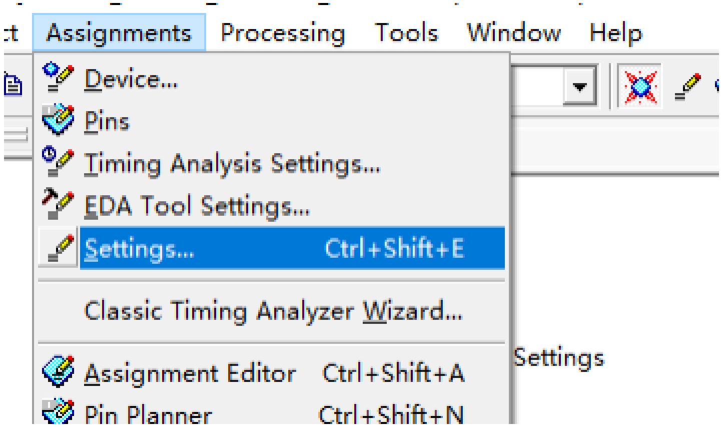
```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE work.components.ALL;
ENTITY fadd4 IS
PORT (a,b: IN std_logic_vector(3 DOWNTO 0);
      ci: IN std_logic;
      co: OUT std_logic;
      sum: OUT std_logic_vector(3 DOWNTO 0));
END fadd4;

ARCHITECTURE stru OF fadd4 IS
SIGNAL ci_ns: std_logic_vector(2 DOWNTO 0); -

BEGIN
-- Do this part yourself
END stru;
```

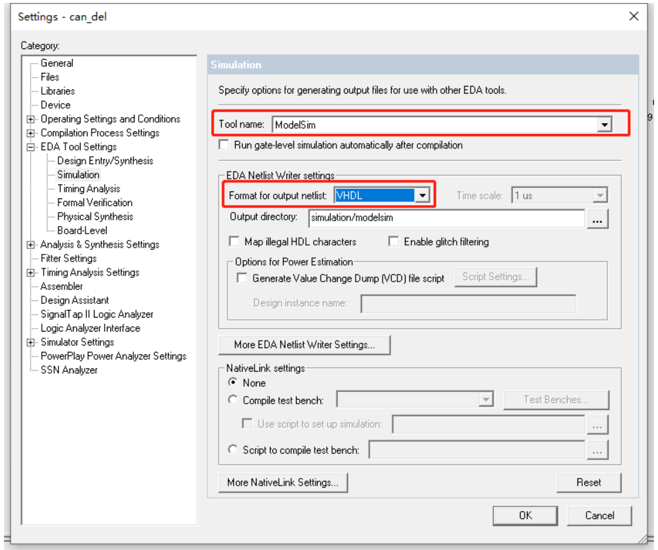


Project Navigator
Files
fadd.vhd
component.vhd
fadd4.vhd
Open
Remove File from Project
Set as Top-Level Entity Ctrl+Shift+J
Create AHDL Include Files for Current File
Create Symbol Files for Current File
Properties...

# Brief introduction to the experiment

- The first part of Simulation ( Quartus II )





Tool name: ModelSim

□ Run gate-level simulation automatically after compilation

EDA Netlist Writer settings

Format for output netlist: VHDL

Time scale: 1 us

Output directory: simulation/modelsim

□ Map illegal HDL characters □ Enable glitch filtering

Options for Power Estimation

□ Generate Value Change Dump (VCD) file script

Design instance name:

NativeLink settings

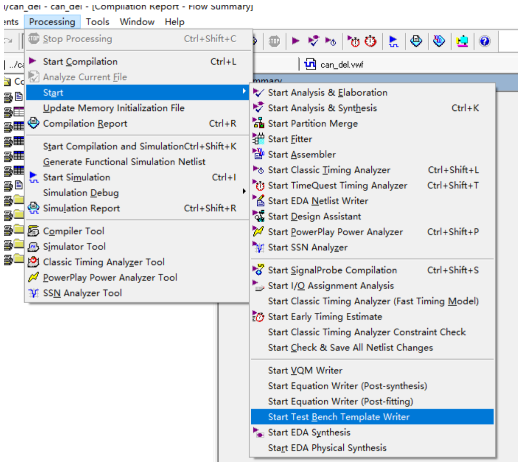
● None

○ Compile test bench:

□ Use script to set up simulation:

○ Script to compile test bench:

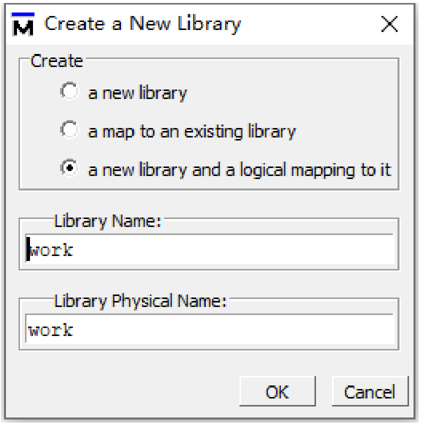
Script Settings...
More EDA Netlist Writer Settings...
Test Benches...
More NativeLink Settings...
Reset
OK
Cancel


/can_del - can_del - [Compilation Report - Flow Summary]
Processing
Tools
Window
Help
Stop Processing Ctrl+Shift+C
Start Compilation Ctrl+L
Analyze Current File
Start
Update Memory Initialization File
Compilation Report Ctrl+R
Start Compilation and Simulation Ctrl+Shift+K
Generate Functional Simulation Netlist
Start Simulation Ctrl+I
Simulation Debug
Simulation Report Ctrl+Shift+R
Compiler Tool
Simulator Tool
Classic Timing Analyzer Tool
PowerPlay Power Analyzer Tool
SSN Analyzer Tool
can_del.vwf
Start Analysis & Elaboration
Start Analysis & Synthesis Ctrl+K
Start Partition Merge
Start Fitter
Start Assembler
Start Classic Timing Analyzer Ctrl+Shift+L
Start TimeQuest Timing Analyzer Ctrl+Shift+T
Start EDA Netlist Writer
Start Design Assistant
Start PowerPlay Power Analyzer Ctrl+Shift+P
Start SSN Analyzer
Start SignalProbe Compilation Ctrl+Shift+S
Start I/O Assignment Analysis
Start Classic Timing Analyzer (Fast Timing Model)
Start Early Timing Estimate
Start Classic Timing Analyzer Constraint Check
Start Check & Save All Netlist Changes
Start VQM Writer
Start Equation Writer (Post-synthesis)
Start Equation Writer (Post-fitting)
Start Test Bench Template Writer
Start EDA Synthesis
Start EDA Physical Synthesis

Open the Modelsim

# Brief introduction to the experiment

- The second part of Simulation ( Modelsim)



Create a New Library

Create

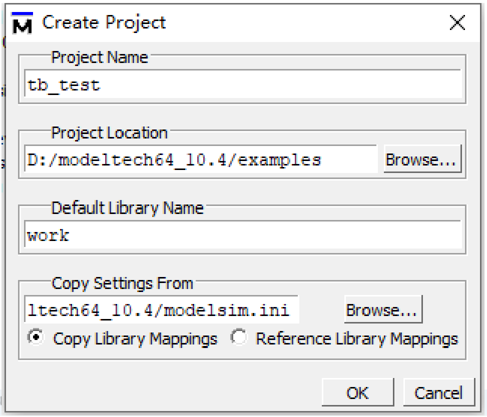
○ a new library

○ a map to an existing library

● a new library and a logical mapping to it

Library Name: work

Library Physical Name: work



Create Project

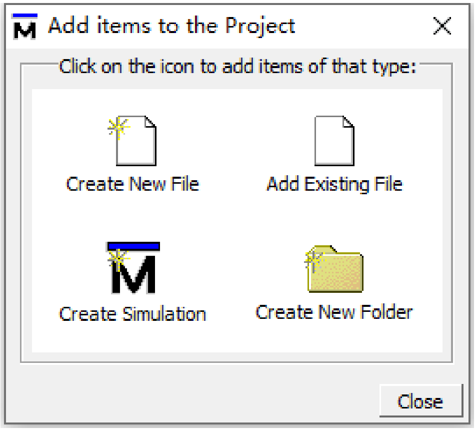
Project Name: tb_test

Project Location: D:/modeltech64_10.4/examples

Default Library Name: work

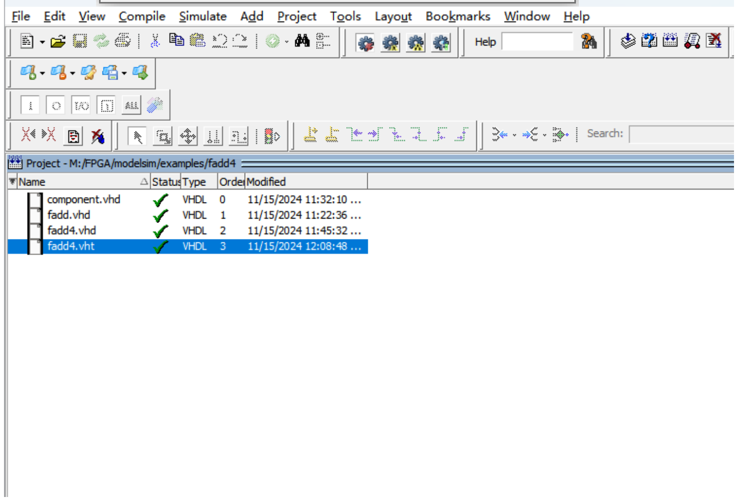
Copy Settings From: ltech64_10.4/modelsim.ini

● Copy Library Mappings ○ Reference Library Mappings



Add items to the Project

Click on the icon to add items of that type:

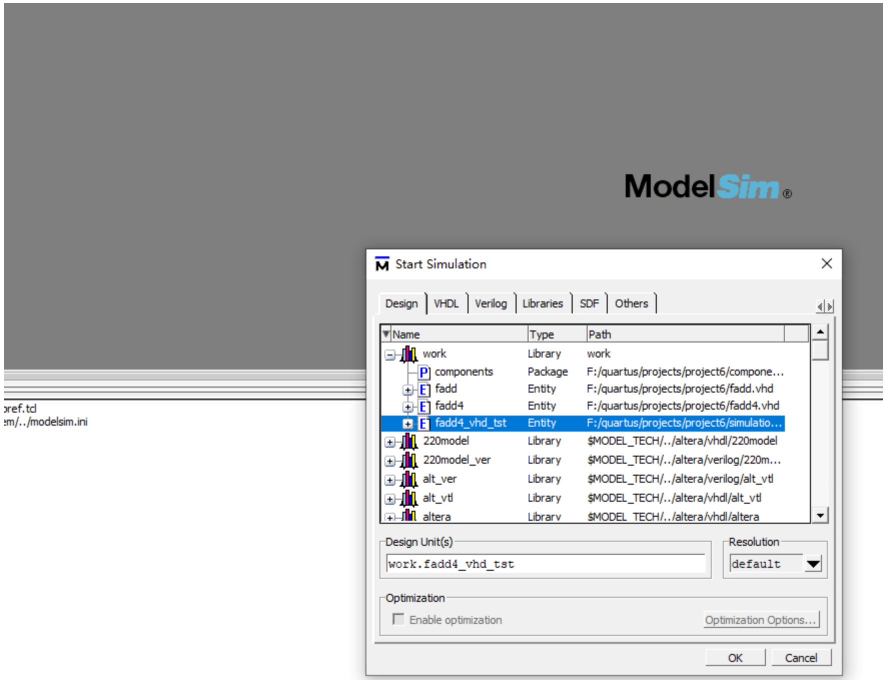


Project - M:/FPGA/modelsim/examples/fadd4

| Name | Status | Type | Order | Modified |
|---|---|---|---|---|
| component.vhd | ✓ | VHDL | 0 | 11/15/2024 11:32:10 ... |
| fadd.vhd | ✓ | VHDL | 1 | 11/15/2024 11:22:36 ... |
| fadd4.vhd | ✓ | VHDL | 2 | 11/15/2024 11:45:32 ... |
| fadd4.vht | ✓ | VHDL | 3 | 11/15/2024 12:08:48 ... |

# Brief introduction to the experiment

- The second part of Simulation ( Modelsim)
  - Run the testbench following the experiment tutorial in Modelsim



| Name | Type | Path |
|---|---|---|
| work | Library | work |
| components | Package | F:/quartus/projects/project6/compone… |
| fadd | Entity | F:/quartus/projects/project6/fadd.vhd |
| fadd4 | Entity | F:/quartus/projects/project6/fadd4.vhd |
| fadd4_vhd_tst | Entity | F:/quartus/projects/project6/simulatio… |
| 220model | Library | $MODEL_TECH/../altera/vhdl/220model |
| 220model_ver | Library | $MODEL_TECH/../altera/verilog/220m… |
| alt_ver | Library | $MODEL_TECH/../altera/verilog/alt_vtl |
| alt_vtl | Library | $MODEL_TECH/../altera/vhdl/alt_vtl |
| altera | Library | $MODEL_TECH/../altera/vhdl/altera |

Design Unit(s): work.fadd4_vhd_tst

Resolution: default

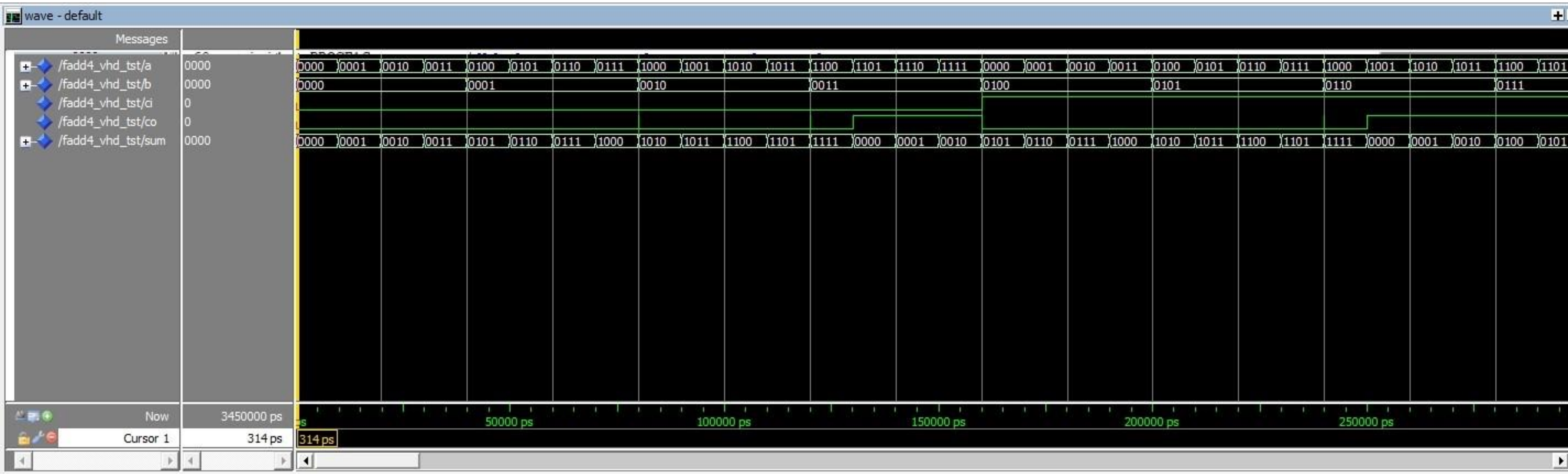
Optimization

□ Enable optimization

Optimization Options...

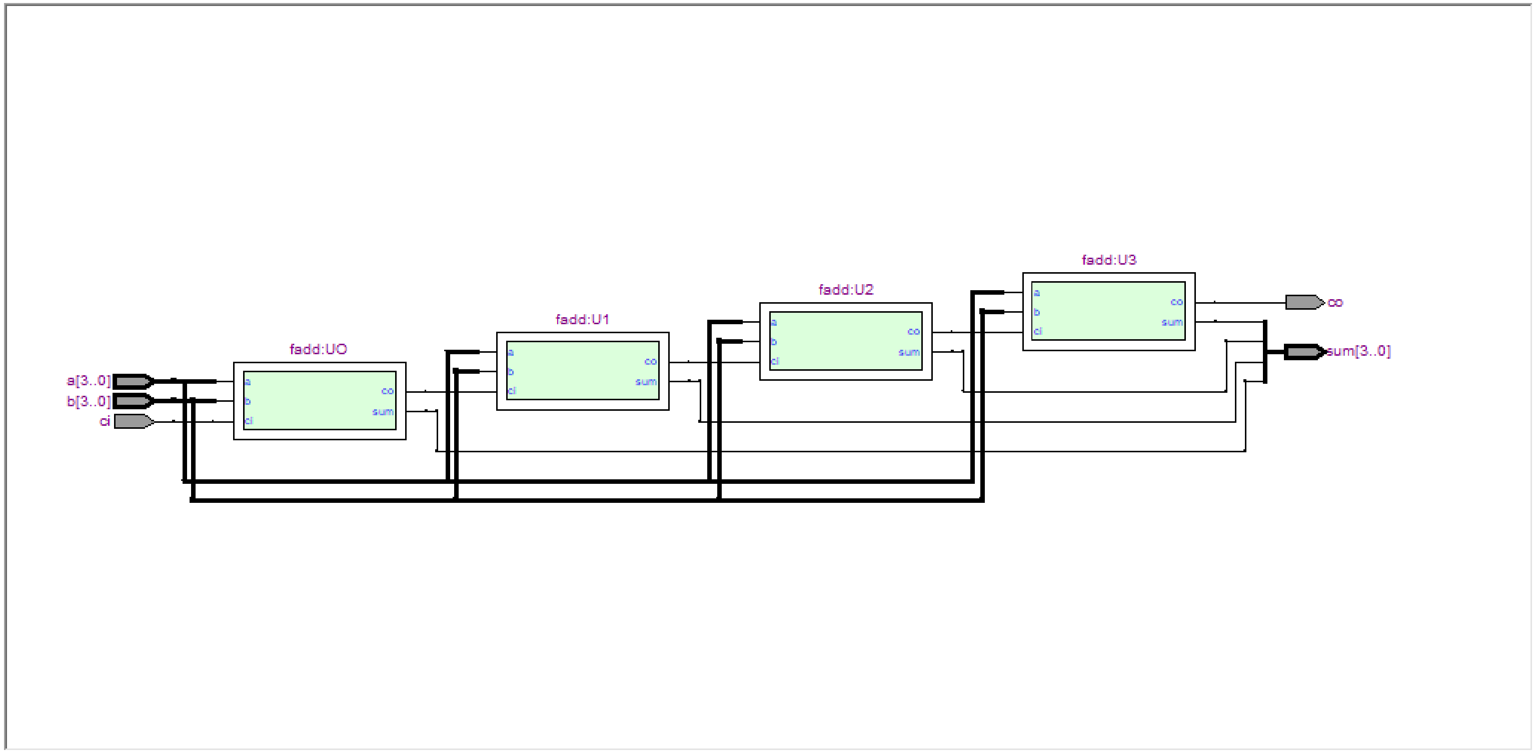
# Brief introduction to the experiment

- Testbench waveform



# Brief introduction to the experiment

- Example



# Example

- Full adder

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
ENTITY fadd IS
PORT (a,b,ci: IN std_logic;
        co,sum: OUT std_logic
        );
END fadd;

ARCHITECTURE dataflow OF fadd IS
BEGIN
co<=(a and b)or(b and ci)or(a and ci);
sum<=a xor b xor ci;
END dataflow;
```

# Example

- Instantiated as a component

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;

PACKAGE components IS
 COMPONENT fadd IS
        PORT(a,b,ci: IN std_logic;
                 co,sum: OUT std_logic);
 END COMPONENT;
END components;
```

# Example

- 4-bit full adder

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE work.components.ALL;
ENTITY fadd4 IS
PORT (a,b: IN std_logic_vector(3 DOWNTO 0);
        ci: IN std_logic;
        co: OUT std_logic;
        sum: OUT std_logic_vector(3 DOWNTO 0));
END fadd4;

ARCHITECTURE stru OF fadd4 IS
SIGNAL ci_ns: std_logic_vector(2 DOWNTO 0);
--connections between full adder

BEGIN
--Do this part yourself
END stru;
```