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# **Stylus Common UI Database Object Information**

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# Types and Definitions

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The following is the list of allowed data types and their descriptions:

Type	Description	Accepted Input (from TCL)	Output Format (to TCL)
bool	A boolean value.	true: true/1/on/yes false: false/0/off/no	true or false
int	Signed 32-bit integer corresponding to Tcl integer.	Any integer value.	26
double	Double-precision (64-bit) signed float.	Any numeric value.	26.4 A .0 is added to the output of integer values to force it to be a double (e.g. 1.0 rather than 1).
string	A string. Unlike other types, the empty string is a valid value.	Any Tcl string value, like "abc" or {abc}.	abc
enum	One of a fixed set of string values (provided in the type qualification).	If "true" or "false" are enum values, these are interpreted as booleans.  For example: enum (true false auto) accepts <ul style="list-style-type: none"><li>- "0", "no" and "off" as synonyms for "false"</li><li>- "1", "yes" and "on" as synonyms for "true"</li><li>- "auto" for "auto"</li></ul>	auto

**Stylus Common UI Database Object Information**  
**Types and Definitions**

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obj	<p>A database object pointer. It is followed by the list of object types allowed for this attribute. It is optionally followed by</p> <ul style="list-style-type: none"> <li>* object list of 0 or more</li> <li>+ object list of 1 or more</li> <li>? object link may be empty</li> </ul> <p>For example, obj(inst hinst)+ is a list of 1 or more inst or hinst objects. A mixture of both inst and hinst objects is possible.</p>	<p>A dual-ported Tcl object or object list. The string form for netlist objects is &lt;obj_type&gt;:&lt;design_name&gt;/&lt;object_name&gt;, for example:</p> <p>inst:my_design/i1/i2</p> <p>For technology or library objects it is just &lt;obj_type&gt;:&lt;name&gt;, for example:</p> <p>layer:metal1</p> <p>For objects with no useful name (like a wire), it is just the hex memory pointer, for example:</p> <p>wire:0x123300012</p> <p>Type "man get_db" for more details on dual-ported Tcl objects.</p>	layer:metal1 inst:my_design/i1/i2 wire:0x123300012
in_file	A file name that will be read in.	A Unix path name (relative or absolute). The file must exist and be readable.	my_dir/myfile.tcl
out_file	A file that will be written to.	A Unix path name (relative or absolute). The file must be writable.	my_dir/my_file.tcl
in_dir	A directory to read from.	A Unix path name (relative or absolute). The directory must exist and be readable.	my_dir
out_dir	A directory to write into.	A Unix path name (relative or absolute). The directory must be writable.	my_dir

**Stylus Common UI Database Object Information**  
**Types and Definitions**

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coord	A single, linear distance in microns that type double..	Any numerical value in units of microns.	26.4 A .0 is added to the output of integer values to force it to be a double (e.g. 1.0 rather than 1).
point	A point in 2D space, expressed as a two-element Tcl list of coord types: {<x> <y>}. Has sub types: .x - the first coordinate .y - the second coordinate	Any list format that can be translated into two coordinates. For example, the following are allowed: {1.0 2.2} {{1} {2.2}}	{1.0 2.2}
line	A line in 2D space, expressed as a two-element Tcl list of points: {{<x1> <y1>} <x2> <y2>}}. Has sub types: .begin - first point .end - second point .length - length of the line .dx - difference in x coordinates .dy - difference in y coordinates	Any list format that can be translated into two points. For example, the following are allowed as input. {{1.0 2} {3 4.0}} {1 2 3 4} {{1} {2} {3} {4.0}}	{1.0 2.2} {3.0 4.0}}

**Stylus Common UI Database Object Information**  
**Types and Definitions**

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rect	<p>A rectangle in 2D space, expressed as an ordered list of coordinates {&lt;left_x&gt; &lt;lower_y&gt; &lt;right_x&gt; &lt;upper_y&gt;}.  Has sub types:  .ll - lower left point  .ur - upper right point  .dx - difference in x coordinates  .dy - difference in y coordinates  .area - area of the rectangle  .width - shorter of dx &amp; dy  .length - longer of dx and dy  .perimeter - perimeter of the rect</p>	<p>Any list format that can be translated into two points. For example, the following are equivalent:  {{1 2} {3 4}}  {1 2 3 4}  The two X coordinates and two Y coordinates can be input in either order. They will be ordered as lower-left for the first point, and upper-right as the second point for output.</p>	A list of four coords: {1.0 2.0 3.0 4.0}
polygon	<p>A polygon in 2D space, expressed as a list of points {{&lt;x1&gt; &lt;y1&gt;} {&lt;x2&gt; &lt;y2&gt;} {&lt;x3&gt; &lt;y3&gt;}...}.  Has sub types:  .bbox - bounding box (rect type)  .area - area of the rectangle  .perimeter - perimeter of the rectangle</p>	<p>Any list format that can be translated into multiple points. For example, the following are equivalent:  {{1 2} {3 4} {5 6}}  {1 2 3 4 5 6}</p>	A list of points: {{1.0 2.0} {3.0 4.0} {5.0 6.0}}.

**Stylus Common UI Database Object Information**  
**Types and Definitions**

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area	An area in units of micron squared that is type double.	Any numerical value in units of microns squared. 26.4	Value in micron squared without units. Example: 26.4 A .0 is added to the output of integer values to force it to be a double (e.g. 1.0 rather than 1).
delay	A time duration that is type double.	Any numerical value in user units. The units can be queried with "get_db_timing_time_unit".	26.4 A .0 is added to the output of integer values to force it to be a double (e.g. 1.0 rather than 1).
resistance	A resistance that is type double.	Any numerical value in user units. The units can be queried with "get_resistance_unit".	26.4 A .0 is added to the output of integer values to force it to be a double (e.g. 1.0 rather than 1).
capacitance	A capacitance that is type double.	Any numerical value in user units. The units can be queried with "get_db_timing_cap_unit".	26.4 A .0 is added to the output of integer values to force it to be a double (e.g. 1.0 rather than 1).
voltage	A voltage that is type double.	Any numerical value in units of volts.	1.4 A .0 is added to the output of integer values to force it to be a double (e.g. 1.0 rather than 1).

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# Database Objects

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## analysis\_view

### Parent Objects

[design](#), [root](#)

### Definition

An analysis view binds together a constraint mode with a delay corner, providing all the information needed to control a single MMMC analysis. Use the `create_analysis_view` and `update_analysis_view` commands to create and modify `analysis_views`.

Attribute	Description
constraint_mode	<p>The constraint_mode object associated with the analysis_view.</p> <p><b>Type:</b> <a href="#">obj(constraint_mode)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
delay_corner	<p>The delay_corner object associated with the analysis_view.</p> <p><b>Type:</b> <a href="#">obj(delay_corner)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_active	<p>Indicates that the analysis_view is part of any leakage/dynamic/setup/hold designation</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_dormant	

**Stylus Common UI Database Object Information**  
Database Objects--analysis\_view

	Indicates that the analysis_view is not being timing analyzed, but a minimum set of data is loaded to keep the view in sync with potential design changes. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_dynamic	Indicates that the analysis_view is dynamic power view. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_em	Indicates that the analysis_view is used for electromigration analysis. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_hold	Indicates that the analysis_view is active for hold analysis <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_hold_default	Indicates that the analysis_view is the default view for hold analysis <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_leakage	Indicates that the analysis_view is leakage power view. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_setup	Indicates that the analysis_view is active for setup analysis <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No

is_setup_default	Indicates that the analysis_view is the default view for setup analysis <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
latency_file	Specifies an optional file containing view-specific set_clock_latency constraints used for balancing post_CTS IO timing. This file is normally generated automatically as part of the clock tree implementation flow. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
name	Provides the name of this analysis_view object as specified by the create_analysis_view command. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (analysis_view) <b>Default:</b> "" <b>Edit:</b> No
power_modes	Specifies an optional list of power_mode objects defined by the power intent specification. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No

## antenna\_data

### Parent Objects

[base\\_pin](#), [port](#)

## Definition

Antenna information for terminals

Attribute	Description
area	<p>Area value for non *Car type cases, 0 value used for *Car type cases as area is not applicable in those cases.</p> <p><b>Type:</b> <a href="#">area</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
layer	<p>The layer of antenna data. If layer is null(0x0), data applies to all layers.</p> <p><b>Type:</b> <a href="#">obj(layer)</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
model	<p>Oxide model, none is used for cases where oxide model does not apply.</p> <p><b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> none oxide1 oxide2 oxide3 oxide4  <b>Default:</b> ""  <b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (antenna_data)</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
ratio	<p>Ratio value for *Car type cases. 0 value used for non *Car enums as ratio is not applicable in those cases.</p> <p><b>Type:</b> <a href="#">double</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
type	

	Type of antenna data. Equivalent to LEF MACRO PIN ANTENNA* constructs.  <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> lib_gate_area lib_diff_area lib_partial_metal_area lib_partial_metal_side_area lib_max_area_car lib_max_side_area_car lib_partial_cut_area lib_max_cut_car top_partial_metal_area top_partial_metal_side_area top_gate_area top_diff_area top_max_area_car top_max_side_area_car top_partial_cut_area top_max_cut_car <b>Default:</b> "" <b>Edit:</b> No
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## antenna\_model

### Parent Objects

[layer](#)

### Definition

Antenna model information for one layer & oxide

Attribute	Description
area_factor	Specifies the multiply factor for the antenna metal area calculation (default value 1.0), LEF(ANTENNAAREAFCTOR)  <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No
area_factor_diff_use_only	Specifies that the current antenna area factor should only be used when the corresponding layer is connected to the diffusion, LEF(DIFFUSEONLY)  <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
area_ratio	

**Stylus Common UI Database Object Information**  
Database Objects--antenna\_model

	<p>Specifies the maximum legal antenna ratio, using the area of the metal wire that is not connected to the diffusion diode (0 indicates that the attribute does not apply), LEF(ANTENNAAREARATIO)</p> <p><b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No</p>
cum_area_ratio	<p>Specifies the cumulative antenna ratio, using the area of the wire that is not connected to the diffusion diode (0 indicates that the attribute does not apply), LEF(ANTENNACUMAREARATIO)</p> <p><b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No</p>
cum_routing_plus_cut	<p>Indicates that the cumulative ratio rules (ANTENNACUMAREARATIO and ANTENNACUMDIFFAREARATIO) accumulate with the previous cut layer instead of the previous metal layer, LEF(ANTENNACUMROUTINGPLUSCUT)</p> <p><b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No</p>
cum_side_area_ratio	<p>Specifies the cumulative antenna ratio, using the side wall area of the metal wire that is not connected to the diffusion diode (0 indicates that the attribute does not apply), LEF(ANTENNACUMSIDEAREARATIO)</p> <p><b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No</p>
gate_minus_diff	<p>Indicates that the antenna ratio metal area should subtract the diffusion area connected to it (0 indicates that the attribute does not apply), LEF(ANTENNAAREAMINUSDIFF)</p> <p><b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No</p>
obj_type	

	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (antenna_model) <b>Default:</b> "" <b>Edit:</b> No
side_area_factor	Specifies the multiply factor for the antenna metal side wall area calculation (default value 1.0), LEF(ANTENNASIDEAREAFATOR) <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
side_area_factor_diff_use_only	Specifies that the current antenna side area factor should only be used when the corresponding layer is connected to the diffusion, LEF(DIFFUSEONLY) <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
side_area_ratio	Specifies the antenna ratio, using the side wall area of the metal wire that is not connected to the diffusion diode (0 indicates that the attribute does not apply), LEF(ANTENNASIDEAREARATIO) <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No

## arc

### Parent Objects

[inst](#), [pin](#), [net](#)

### Definition

cte timing arc

Attribute	Description
aocv_derate_capture_clock_early_fall	

	Returns graph based AOCV derate factors in AOCV mode for a given timing arc that is a part of early capture clock paths with fall sink pin transitions. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
aocv_derate_capture_clock_early_rise	
	Returns graph based AOCV derate factors in AOCV mode for a given timing arc that is a part of early capture clock paths with rise sink pin transitions. You can use -index to return the value for a specific view <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
aocv_derate_capture_clock_late_fall	
	Returns graph based AOCV derate factors in AOCV mode for a given timing arc that is a part of late capture clock paths with fall sink pin transitions. You can use -index to return the value for a specific view <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
aocv_derate_capture_clock_late_rise	
	Returns graph based AOCV derate factors in AOCV mode for a given timing arc that is a part of late capture clock paths with rise sink pin transitions. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
aocv_derate_data_early_fall	
	Returns AOCV derate values for a timing arc on an early data path with fall sink pin transitions. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No

aocv_derate_data_early_rise	Returns AOCV derate values for a timing arc on an early data path with rise sink pin transitions. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
aocv_derate_data_late_fall	Returns AOCV derate values for a timing arc on a late data path with fall sink pin transitions. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
aocv_derate_data_late_rise	Returns AOCV derate values for a timing arc on a late data path with rise sink pin transitions. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
aocv_derate_launch_clock_early_fall	Returns graph based AOCV derate factors in AOCV mode for a given timing arc that is a part of early launch clock paths with fall sink pin transitions. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
aocv_derate_launch_clock_early_rise	Returns graph based AOCV derate factors in AOCV mode for a given timing arc that is a part of early launch clock paths with rise sink pin transitions. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No

aocv_derate_launch_clock_late_fall	Returns graph based AOCV derate factors in AOCV mode for a given timing arc that is a part of late launch clock paths with fall sink pin transitions. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
aocv_derate_launch_clock_late_rise	Returns graph based AOCV derate factors in AOCV mode for a given timing arc that is a part of late launch clock paths with rise sink pin transitions. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
aocv_stage_count_capture_clock_early	Returns graph based AOCV stage count values in AOCV mode for a given timing arc that is a part of early capture clock paths. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
aocv_stage_count_capture_clock_late	Returns graph based AOCV stage count values in AOCV mode for a given timing arc that is a part of late capture clock paths. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
aocv_stage_count_data_early	Returns AOCV stage count values for a timing arc on an early data path. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No

aocv_stage_count_data_late	<p>Returns AOCV stage count values for a timing arc on a late data path. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
aocv_stage_count_launch_clock_early	<p>Returns AOCV stage count values in AOCV mode for a given timing arc that is a part of early launch clock paths. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
aocv_stage_count_launch_clock_late	<p>Returns AOCV stage count values in AOCV mode for a given timing arc that is a part of late launch clock paths. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
aocv_weight	<p>Returns the AOCV stage weight for this arc. By default, all cells and arcs have default stage weight of 1.0. The aocv_weight property is specified as a user-defined library attribute in the Liberty timing library explicitly - or, by asserting it via command. This attribute is inherited from the associated library arc. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
delay_max_fall	<p>Returns the largest falling delay through the arc across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>

delay\_max\_rise

Returns the largest rising delay through the arc across all concurrent MMMC views. You can use -index to return the value for a specific view.  
**Type:** double  
**Allowed -index values:** analysis\_view  
**Default:** ""  
**Edit:** No

delay\_mean\_max\_fall

In SOCV analysis mode, this returns the mean component of the largest falling delay through the arc across all concurrent MMMC views. You can use -index to return the value for a specific view.  
**Type:** double  
**Allowed -index values:** analysis\_view  
**Default:** ""  
**Edit:** No

delay\_mean\_max\_rise

In SOCV analysis mode, this returns the mean component of the largest rising delay through the arc across all concurrent MMMC views. You can use -index to return the value for a specific view.  
**Type:** double  
**Allowed -index values:** analysis\_view  
**Default:** ""  
**Edit:** No

delay\_mean\_min\_fall

In SOCV analysis mode, this returns the mean component of the smallest falling delay through the arc across all concurrent MMMC views. You can use -index to return the value for a specific view.  
**Type:** double  
**Allowed -index values:** analysis\_view  
**Default:** ""  
**Edit:** No

delay\_mean\_min\_rise

	<p>In SOCV analysis mode, this returns the mean component of the smallest rising delay through the arc across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p>delay_min_fall</p> <p>Returns the smallest falling delay through the arc across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p>delay_min_rise</p> <p>Returns the smallest rising delay through the arc across all concurrent MMMC views can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p>delay_sigma_max_fall</p> <p>In SOCV analysis mode, this returns the variation component of the largest falling delay through the arc across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p>delay_sigma_max_rise</p> <p>In SOCV analysis mode, this returns the variation component of the largest rising delay through the arc across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p>delay_sigma_min_fall</p>

	<p>In SOCV analysis mode, this returns the variation component of the smallest falling delay through the arc across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>delay_sigma_min_rise</b>	
	<p>In SOCV analysis mode, this returns the variation component of the smallest rising delay through the arc across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>delta_delay_max_fall</b>	
	<p>Returns the delta/SI delay component of the largest falling delay through this arc across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>delta_delay_max_rise</b>	
	<p>Returns the delta/SI delay component of the largest rising delay through this arc across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>delta_delay_min_fall</b>	
	<p>Returns the delta/SI delay component of the smallest falling delay through this arc across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>delta_delay_min_rise</b>	

	<p>Returns the delta/SI delay component of the smallest rising delay through this arc across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
dynamic_delta_delay_max_fall	<p>Returns the dynamic delay component of the largest falling delay through this arc across all concurrent MMMC views. This is computed if dynamic voltages have been specified. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
dynamic_delta_delay_max_rise	<p>Returns the dynamic delay component of the largest rising delay through this arc across all concurrent MMMC views. This is computed if dynamic voltages have been specified. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
dynamic_delta_delay_min_fall	<p>Returns the dynamic delay component of the smallest falling delay through this arc across all concurrent MMMC views. This is computed if dynamic voltages have been specified. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
dynamic_delta_delay_min_rise	<p>Returns the dynamic delay component of the smallest rising delay through this arc across all concurrent MMMC views. This is computed if dynamic voltages have been specified. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

from_pin	Returns a pin object for the beginning pin of this timing arc <b>Type:</b> <a href="#">obj(pin)*</a> <a href="#">obj(hpin)*</a> <a href="#">obj(hport)*</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_cell_arc	Returns true if the arc is a cell arc. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_disabled	Returns a value of true if this library timing arc has been explicitly disabled by the user via a set_disable_timing constraint <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
lib_arcs	Returns a list of the associated lib_arc objects. You can use -index to return the value for a specific view. <b>Type:</b> <a href="#">obj(lib_arc)*</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
mode	If the associated lib_arc is defined as part of a Liberty mode group, this attribute will return the name of the library group <b>Type:</b> <a href="#">string</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
obj_type	

	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (arc)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
sdf_cond	<p>Returns the value of the Liberty sdf_cond attribute if specified for the associated lib_arc</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
sdf_cond_end	<p>Returns the value of the Liberty sdf_cond_end attribute if specified for the associated lib_arc</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
sdf_cond_start	<p>Returns the value of the Liberty sdf_cond_start attribute if specified for the associated lib_arc</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
sense	<p>Returns the Liberty timing_sense value associated with this arc. This value is one of:positive_unate, negative_unate, or non_unate. This is inherited from the lib_arc.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
ssi_derate_fall	<p>Returns the fall ssi_derate for the arc.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
ssi_derate_rise	

	<p>Returns the rise ssi_derate for the arc.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
timing_type	<p>Returns the Liberty timing_type associated with this arc. You can consult the Liberty documentation for the list of possible values for this attribute. This is inherited from the lib_arc.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
to_pin	<p>Returns a pin object for the terminating pin of this timing arc</p> <p><b>Type:</b> <a href="#">obj(pin)* obj(hpin)* obj(hport)*</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
when	<p>Returns the value of the Liberty 'when' attribute if specified for the related lib_arc</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
when_end	<p>Returns the value of the Liberty 'when_end' attribute if specified for the related lib_arc</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
when_start	<p>Returns the value of the Liberty 'when_start' attribute if specified for the related lib_arc</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

# attribute

## Parent Objects

[root](#), [obj\\_type](#)

## Definition

Attribute	Description
additional_help	<p>Range info or other additional help.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
base_name	<p>The name without the obj_type (e.g. place_status rather than inst/place_status).</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
category	<p>Defines the category of the attribute. Categories group attributes that perform similar functions whereas object types describe where in the design an attribute is valid. You can specify any category name: both new and existing category names are valid. (examples: physical, timing, etc). Note: the value also be an empty string "".</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
check_function	<p>Specifies a previously defined Tcl procedure's name in order to ensure that the newly defined attribute is valid. Procedure argument list: object value</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
compute_function	

**Stylus Common UI Database Object Information**  
Database Objects--attribute

	Specifies a previously defined Tcl procedure's name in order to get the newly defined attribute's value later command. Procedure argument list: object <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
data_type	
	data type attribute <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
default_value	
	Specifies a default value for the attribute, most attributes do not have default values and will use "". <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
help	
	Specifies the help text for the attribute <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
indices	
	List of object type names that represent indices for an attribute value. <b>Type:</b> enum <b>Enum Values:</b> analysis_view clock delay_corner clock_tree skew_group power_domain layer <b>Default:</b> "" <b>Edit:</b> No
is_computed	
	Specifies whether the defined attribute will be computed. For .? use, the value will not be displayed if it needs to be recomputed. For direct access of the attribute the value will be returned or computed as needed (0 = static, 1 = computed) <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_settable	

	whether the defined attribute is a read-only or settable attribute (0 = read-only, 1 = settable) <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_user_defined	Specifies whether the defined attribute was defined by the user via Tcl (define_attribute) or is a system defined attribute (0 = system defined, 1 = user defined) <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
name	name of attribute <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (attribute)</a> <b>Default:</b> "" <b>Edit:</b> No
parent	The attribute's parent object <b>Type:</b> <a href="#">obj(obj_type)</a> <b>Default:</b> "" <b>Edit:</b> No
possible_values	enum possible values attribute <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
set_function	

	<p>Specifies a previously defined Tcl procedure's name. This option allows you to override user-defined values provided it conforms to the parameters in the Tcl procedure you created.</p> <p>Procedure argument list: object new_value current_value</p> <p><b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
skip_in_db	<p>Prevents write_db command to write out the defined</p> <p><b>Type:</b> <a href="#">bool</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>

## base\_cell

### Parent Objects

[lib\\_cell](#), [inst](#), [pin\\_group](#), [pg\\_base\\_pin](#), [bump](#), [pin\\_guide](#), [root](#), [base\\_pin](#)

### Definition

base cell

Attribute	Description
aocv_weight	<p>Returns the AOCV stage weight specified for the cell either explicitly in the library or as a user-defined library attribute</p> <p><b>Type:</b> <a href="#">double</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
area	<p>The area of the cell</p> <p><b>Type:</b> <a href="#">area</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
base_class	

**Stylus Common UI Database Object Information**  
Database Objects--base\_cell

	<p>The base class is the prefix of the .class enum value. It is useful to separate the major cell categories. See the .class description for the definition of each enum value</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none cover block pad core corner</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
base_name	<p>Base name of the cell.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
base_pins	<p>The base_pins for this cell</p> <p><b>Type:</b> <a href="#">obj(base_pin)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
bbox	<p>The bounding box of the overlap rects that define the placement area used by this cell.</p> <p><b>Type:</b> <a href="#">rect*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
bottom_edge_type	<p>Name of cell edge type for the bottom edge of the cell (R0/N orientation), used to indicate which cells need extra spacing to other cells.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
bottom_padding	<p>The placer will leave this much extra space to the bottom side of the cell (in r0 orientation). It is only valid for standard cells. It is in units of site width.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
class	

All the LEF CLASS and PROPERTY LEF58\_CLASS values (and equivalent OpenAccess values). Refer to the LEF documentation for the complete list and descriptions. They are separated into 5 classes with a unique prefix based on their usage as described here:

- CLASS COVER types all start with cover.
- CLASS RING or BLOCK start with block.
- CLASS PAD start with pad.
- CLASS CORE start with core.
- CLASS ENDCAP that are corner cells (TOPLEFT, TOPRIGHT, BOTTOMLEFT, BOTTOMRIGHT) start with corner.
- CLASS ENDCAP that are not corner cells all start with core because they are all placed in the core rows like CLASS CORE cells.
- No CLASS means the value is none.
- Modifications are valid only for the current session.

**Type:** enum

**Enum Values:** none cover cover\_bump cover\_fill block block\_ring block block\_blackbox  
block\_soft pad pad\_input pad\_output pad\_inout pad\_power pad\_spacer pad\_area\_io core  
core\_feedthru core\_tie\_high core\_tie\_low core\_spacer core\_antenna core\_welltap  
core\_endcap\_pre core\_endcap\_post corner\_top\_left corner\_top\_right corner\_bottom\_left  
corner\_bottom\_right core\_endcap\_top\_edge core\_endcap\_bottom\_edge  
core\_endcap\_left\_edge core\_endcap\_right\_edge core\_endcap\_left\_top\_edge  
core\_endcap\_right\_top\_edge core\_endcap\_left\_bottom\_edge  
core\_endcap\_right\_bottom\_edge core\_endcap\_left\_top\_corner  
core\_endcap\_right\_top\_corner core\_endcap\_left\_bottom\_corner  
core\_endcap\_right\_bottom\_corner core\_endcap\_left\_even\_site\_edge  
core\_endcap\_left\_odd\_site\_edge core\_endcap\_right\_even\_site\_edge  
core\_endcap\_right\_odd\_site\_edge core\_endcap\_left\_top\_even\_site\_edge  
core\_endcap\_left\_top\_odd\_site\_edge core\_endcap\_right\_top\_even\_site\_edge  
core\_endcap\_right\_top\_odd\_site\_edge core\_endcap\_left\_bottom\_even\_site\_edge  
core\_endcap\_left\_bottom\_odd\_site\_edge core\_endcap\_right\_bottom\_even\_site\_edge  
core\_endcap\_right\_bottom\_odd\_site\_edge core\_endcap\_left\_top\_even\_site\_corner  
core\_endcap\_left\_top\_odd\_site\_corner core\_endcap\_right\_top\_even\_site\_corner  
core\_endcap\_right\_top\_odd\_site\_corner core\_endcap\_left\_bottom\_even\_site\_corner  
core\_endcap\_left\_bottom\_odd\_site\_corner core\_endcap\_right\_bottom\_even\_site\_corner  
core\_endcap\_right\_bottom\_odd\_site\_corner core\_endcap\_left\_edge\_bottom\_border  
core\_endcap\_left\_edge\_top\_border core\_endcap\_right\_edge\_bottom\_border  
core\_endcap\_right\_edge\_top\_border core\_endcap\_left\_bottom\_edge\_neighbor  
core\_endcap\_left\_top\_edge\_neighbor core\_endcap\_right\_bottom\_edge\_neighbor  
core\_endcap\_right\_top\_edge\_neighbor core\_endcap\_left\_bottom\_corner\_neighbor  
core\_endcap\_left\_top\_corner\_neighbor core\_endcap\_right\_bottom\_corner\_neighbor  
core\_endcap\_right\_top\_corner\_neighbor

**Default:** ""

**Edit:** Yes

cts\_cell\_halo\_x

	<p>Specifies the cell halo distance in the x direction. The default value of this attribute is auto. By default, CCOpt can automatically compute a cts_cell_halo_x in terms of cts_cell_density attribute.</p> <p>See also:  <a href="#">.cts_cell_density</a></p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> <a href="#">clock_tree power_domain</a></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p>
	<p><b>cts_cell_halo_y</b></p>
	<p>Specifies the cell halo distance in the y direction. The default value of this attribute is auto. By default, CCOpt can automatically compute a cts_cell_halo_y in terms of cts_cell_density attribute.</p> <p>See also:  <a href="#">.cts_adjacent_rows_legal</a></p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> <a href="#">clock_tree power_domain</a></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p>
	<p><b>dont_touch</b></p>
	<p>This attribute says any inst of this base_cell cannot be modified during optimization. This is the effective dont_touch value for all lib_cells. It is set to the worst case of the lib_cells during init_design and can only be updated by set_db / set_dont_touch after that (subsequent library reads will not affect). This attribute will get restored back to the state during write_db regardless if the library files have been altered.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
	<p><b>dont_use</b></p>
	<p>This attribute says do not use this base_cell during optimization. This is the effective dont_use value for all lib_cells. It is set to the worst case of the lib_cells during init_design and can only be updated by set_db / set_dont_use after that (subsequent library reads will not affect). This attribute is saved by write_db, and restored by read_db regardless if the library files have been altered.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
	<p><b>eeq_cells</b></p>

**Stylus Common UI Database Object Information**  
**Database Objects--base\_cell**

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	<p>Electrically equivalent base_cells. Same as LEF MACRO EEQ statement.</p> <p><b>Type:</b> <a href="#">obj(base_cell)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
eeq_variant	<p>The LEF EEQ cell variant number from the LEF58_EEQ property 'EEQ macroName VARIANT num'</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p>
escaped_name	<p>Escaped name of the cell.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
foreign_cells	<p>List of foreign references. Equivalent to LEF MACRO FOREIGN.</p> <p><b>Type:</b> <a href="#">obj(foreign_cell)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_always_on	<p>Specifies the cell is an always-on cell. An always-on cell normally has two power pins. One is primary which aligns with the normal cell power-rail, and the other is the secondary which actually powers the cell, even when the primary power is off. This attribute can be set by liberty files, or by CPF commands.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> No</p>
is_black_box	<p>Returns a value of true if the cell is a black box cell.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_buffer	

**Stylus Common UI Database Object Information**  
Database Objects--base\_cell

	This cell is a buffer. <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_combinational	
	Returns a value of true if the cell is a combinational cell (not a sequential cell). <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_fall_edge_triggered	
	Returns a value of true if the cell is triggered by the falling edge of the clock. <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_fixed_mask	
	Indicates the cell has FIXEDMASK keyword in LEF. <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_flop	
	Returns true if the cell is recognized as flip-flop/register type cell <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_integrated_clock_gating	
	Returns true if the cell has the Liberty clock_gating_integrated_cell set to true <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_interface_timing	
	Returns a value of true if a cell has the Liberty interface_timing attribute set to true <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_inverter	

**Stylus Common UI Database Object Information**  
Database Objects--base\_cell

	This cell is an inverter. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_iso_nor	
	Specifies the cell is an ISONOR cell. An ISONOR cell is a kind of isolation cell, which has only one primary power pin and one primary ground pin. An ISONOR cell is defined by library files. In cell library, it has permit_power_down true for primary power pin, alive_during_power_up true for input signal pin, and alive_during_partial_power_down true for enable pin and output signal pin. The attribute should be queried after read and commit power intent. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_isolation_cell	
	Specifies the cell is an isolation cell. An isolation cell is used to clamp the signal to high or low when its input is shutoff(unknown). This attribute can be set by liberty files, or by CPF commands. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> No
is_latch	
	Returns true if the cell is recognized as latch type cell <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_level_shifter	
	Specifies the cell is a level shifter cell. A level-shifter cell is used to shift the signal voltage from low(high) to high(low). This attribute can be set by liberty files, or by CPF commands. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> No
is_macro	
	Returns a value of true if the Liberty attribute is_macro_cell is set true <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No

**Stylus Common UI Database Object Information**  
Database Objects--base\_cell

is_master_slave_flop	Returns true if the cell is recognized as a master/slave flip-flop type cell <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_master_slave_lssd_flop	Returns true if this cell has been recognized as a master/slave LSSD type cell <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_memory	Returns true or false depending on whether the associated library cell is recognized as a Liberty memory cell. Cells which include a Liberty memory group definition are recognized as memory cells. <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_negative_level_sensitive	Returns a value of true if the cell is identified as a negative level-sensitive latch <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_pad	Returns a value of true if Liberty attribute is_pad is set to true <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_physical_defined	This cell has a physical abstract loaded from LEF or OA so the various physical attributes have been set <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_pll	

**Stylus Common UI Database Object Information**  
**Database Objects--base\_cell**

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	Returns a value of true if the Liberty library is_pli_cell attribute is set to true for this cell <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
<b>is_positive_level_sensitive</b>	
	Returns a value of true if the cell is identified as a positive level-sensitive latch <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
<b>is_power_on_bottom</b>	
	Indicates this standard cell has a power pin along the bottom of the cell. This is derived from the power and ground pin information in the cell. It is used by the placer to align multi-height cells properly to the rows. It is not meaningful for non standard cells. Modifications are not saved and are only valid for the current session. <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes
<b>is_power_switch</b>	
	Specifies the cell is a power switch cell. The power switch cell is used to switch off the power/ground during shutoff. This attribute can be set by liberty files, or by CPF commands. <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> No
<b>is_retention_cell</b>	
	Specifies the cell is a state-retention cell. A state-retention cell is used to retain its state during shutoff. It has a secondary power pin which powers the cell and retains its state, even when the primary power is off. This attribute can be set by liberty files, or by CPF commands. <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> No
<b>is_rise_edge_triggered</b>	
	Returns a value of true if the cell is triggered by the rising edge of the clock <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
<b>is_sequential</b>	

**Stylus Common UI Database Object Information**  
Database Objects--base\_cell

	This cell is sequential. Derived from .lib information <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_timing_defined	
	This cell has a .lib file definition loaded, so the various timing attributes have been set <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_tristate	
	Returns a value of true if the cell definition includes the Liberty attribute three_state set to true . <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
lef_file_name	
	Specifies the LEF file name of the base_cell <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
left_edge_type	
	Name of cell edge type for the left edge of the cell (R0/N orientation), used to indicate which cells need extra spacing to other cells. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
left_padding	
	The placer will leave this much extra space to the left side of the cell (in r0 orientation). It is only valid for standard cells. It is in units of site width. <b>Type:</b> <a href="#">int</a> <b>Default:</b> 0 <b>Edit:</b> Yes
lib_cells	

**Stylus Common UI Database Object Information**  
Database Objects--base\_cell

	Returns a list of lib_cell objects which are associated with this base_cell <b>Type:</b> obj(lib_cell)* <b>Default:</b> "" <b>Edit:</b> No
must_join_base_pins	Must join pins are physical-only pins that do not exist in the logical netlist. They do not appear in Verilog or DEF files. The router will connect the must-join base_pin to its corresponding logical pin. See the base_pin .must_join_pins attribute, and the LEF MACRO PIN MUSTJOIN statement for more details <b>Type:</b> obj(base_pin)* <b>Default:</b> "" <b>Edit:</b> No
name	Name of the cell. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
num_base_pins	Number of signal base_pins for this cell. It does not include pg_base_pins or must_join_base_pins. <b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No
num_drivers	The number of driver base_pins for this base_cell. Signal base_pins that have direction = out or inout are considered drivers. <b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No
num_loads	The number of load base_pins for this base_cell. Signal base_pins that have direction = in or inout are considered loads. <b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No
oa_abstract_lib	

	<p>OpenAccess library name of the physical abstract for the cell if read from OA.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
oa_abstract_view	<p>OpenAccess view name for the physical abstract for this cell if read from OA (equivalent of LEF MACRO data). The OA cell name is the same as this cell's 'name' attribute</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
oa_layout_lib	<p>OpenAccess library name of physical layout for the cell if read from OA.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
oa_layout_view	<p>OpenAccess view name for the physical layout for this cell if read from OA (equivalent of GDSII data). The layout view data can optionally be displayed instead of the abstract view data, but otherwise this layout data is not used in Innovus. The OA cell name is the same as this cell's 'name' attribute</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (base_cell)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obs_layer_shapes	<p>A list of cell obstruction layer_shapes (LEF OBS or OA abstract blockages that are not vias). Note, use obs_via_shapes for obstructions that are from vias (LEF OBS VIA).</p> <p><b>Type:</b> <a href="#">obj(layer_shape)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obs_shape_vias	

**Stylus Common UI Database Object Information**  
Database Objects--base\_cell

	A list of cell obstruction shape_vias (LEF OBS VIA or OA abstract via blockages). Use obs_layer_shapes for obstructions on a single layer. <b>Type:</b> <a href="#">obj(shape_via)</a> * <b>Default:</b> "" <b>Edit:</b> No
<b>pg_base_pins</b>	
	The power/ground base_pins for this cell. <b>Type:</b> <a href="#">obj(pg_base_pin)</a> * <b>Default:</b> "" <b>Edit:</b> No
<b>right_edge_type</b>	
	Name of cell edge type for the right edge of the cell (R0/N orientation), used to indicate which cells need extra spacing to other cells. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
<b>right_padding</b>	
	The placer will leave this much extra space to the right side of the cell (in r0 orientation). It is only valid for standard cells. It is in units of site width. <b>Type:</b> <a href="#">int</a> <b>Default:</b> 0 <b>Edit:</b> Yes
<b>site</b>	
	The site for this cell. Modifications are valid only for the current session. <b>Type:</b> <a href="#">obj(site)</a> * <b>Default:</b> "" <b>Edit:</b> Yes
<b>symmetry</b>	

**Stylus Common UI Database Object Information**  
**Database Objects--base\_cell**

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	<p>The allowed orientations for the placer to try. none means r0 only, x means ok to flip about X axis (r0, mx), y means ok to flip about Y axis (r0, my), xy means ok to flip about X or Y axis (r0, mx, my, r180), any means all orientations are allowed. Equivalent to LEF MACRO SYMMETRY or OA oaSymmetry. LEF values of R90, X R90, Y R90, and X Y R90 are all equivalent to the value = any. Modifications are not saved and are only valid for the current session.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none x y xy any</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
tap_type	<p>Specifies the name of a well tap type for this cell. Various rules for well taps are grouped together for each tap_type. See the LEF documentation on the TAPTYPE keyword for more details.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
tap_wall	<p>Specifies a special well tap cell (LEF CLASS CORE WELLTAP) or a special end_cap (LEF CLASS ENDCAP ...) cell that can be used for a tap wall purpose, which is used to break OD diffusion and aligned vertically to form a tap wall. See the LEF docs about the keyword TAPWALL for more details.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
timing_model_type	<p>Returns the Liberty model type for a given cell or instance. The supported values are abstracted , extracted , and qtm .</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
top_edge_type	<p>Name of cell edge type for the top edge of the cell (R0/N orientation), used to indicate which cells need extra spacing to other cells.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
top_padding	

	The placer will leave this much extra space to the top side of the cell (in r0 orientation). It is only valid for standard cells. It is in units of site width. <b>Type:</b> int <b>Default:</b> 0 <b>Edit:</b> Yes
<b>voltage_threshold_group</b>	
	This attribute allows the user to assign a base_cell to a voltage threshold group for metric capture. The threshold group name can be any valid string. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes

## base\_pin

### Parent Objects

[partition](#), [bump\\_pin](#), [base\\_cell](#), [pin\\_group](#), [pin](#), [root](#), [lib\\_pin](#),

### Definition

base pin

Attribute	Description
antenna_data	The various process antenna_data values for this pin, including area of gate, diffusion, metal, cut, and cumulative area ratios for metal, cut attached to this pin. <b>Type:</b> obj(antenna_data)* <b>Default:</b> "" <b>Edit:</b> No
base_cell	The base_cell of base pin. <b>Type:</b> obj(base_cell) <b>Default:</b> "" <b>Edit:</b> No
base_name	

	<p>The name without the base_cell name (e.g. out rather than and2/out).</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>cts_max_fanout</b>	
	<p>The maximum fanout at any point in the clock tree.</p> <p>Valid values: integer ranged between 2 and 1000 inclusive</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 100</p> <p><b>Edit:</b> Yes</p>
<b>cts_max_source_to_sink_net_length</b>	
	<p>The maximum routing length in microns between driving source pin and driven sink pin on each net that clock tree synthesis should observe.</p> <p>This constraint can be applied to either a pin, a clock tree, or a net type.</p> <p>By default (if this attribute is not set) no explicit clock tree net length constraint is enforced. However, other clock tree constraints such as maximum slew (transition) and maximum capacitance will indirectly limit the maximum net length.</p> <p>Valid values: double</p> <p><b>Type:</b> string</p> <p><b>Allowed -index values:</b> clock_tree</p> <p><b>Default:</b> top auto trunk auto leaf auto</p> <p><b>Edit:</b> Yes</p>
<b>cts_max_source_to_sink_net_length_leaf</b>	
	<p>The maximum routing length in microns between driving source pin and driven sink pin on each net that clock tree synthesis should observe.</p> <p>This constraint can be applied to either a pin, a clock tree, or a net type.</p> <p>By default (if this attribute is not set) no explicit clock tree net length constraint is enforced. However, other clock tree constraints such as maximum slew (transition) and maximum capacitance will indirectly limit the maximum net length.</p> <p>Valid values: double</p> <p><b>Type:</b> string</p> <p><b>Allowed -index values:</b> clock_tree</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p>
<b>cts_max_source_to_sink_net_length_top</b>	

	<p>The maximum routing length in microns between driving source pin and driven sink pin on each net that clock tree synthesis should observe. This constraint can be applied to either a pin, a clock tree, or a net type. By default (if this attribute is not set) no explicit clock tree net length constraint is enforced. However, other clock tree constraints such as maximum slew (transition) and maximum capacitance will indirectly limit the maximum net length. Valid values: double</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> <code>clock_tree</code></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p>
	<p><code>cts_max_source_to_sink_net_length_trunk</code></p> <p>The maximum routing length in microns between driving source pin and driven sink pin on each net that clock tree synthesis should observe. This constraint can be applied to either a pin, a clock tree, or a net type. By default (if this attribute is not set) no explicit clock tree net length constraint is enforced. However, other clock tree constraints such as maximum slew (transition) and maximum capacitance will indirectly limit the maximum net length. Valid values: double</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> <code>clock_tree</code></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p>
	<p><code>cts_spec_config_base_pin_trace_through_to</code></p>

	<p>Clock tree definition will, by default, not continue through certain types of cell arc (for instance, the clock to Q arc in a DFF). This attribute allows you to override this default behavior, permitting the clock tree to trace through all instances of such a cell.</p> <p>This attribute serves the same function as trace_through_to, except that here the clock path is specified at the level of the library cell.</p> <p>The attribute should be configured on the input library pin at which the clock will arrive. The value of the attribute specifies the output library pin to which the clock should propagate. The specified output pin must be another pin on the same library cell. The output pin may be specified either by its fully qualified name (i.e. inclusive of the cell name), or else simply by its local (cell-relative) name.</p> <p>There must be a pre-existing (library-defined) chain of one or more delay arcs that connect the input and output pins together. It is not possible to use library_trace_through_to to synthesize delay arcs.</p> <p>If multiple input pins are annotated on a given library cell, the value of library_trace_through_to at each of those pins must select the same output pin: i.e. the configuration must identify a single clock output for the cell. If multiple clock outputs are necessary then library_trace_through_to should not be used: instead for each instance of the library cell, define a generated clock tree at each of the clock-carrying outputs.</p> <p>If the configuration of library_trace_through_to settings for a given library cell does not meet these requirements, a warning will be issued and the settings for that cell will be ignored.</p> <p>All instances of the library cell will be affected by this setting. If both trace_through_to and library_trace_through_to are applicable at a given instance pin, the trace_through_to value will take precedence.</p> <p>Valid values: base_pin</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
cts_stack_via_rule	<p>The preferred stack via rule for terminal connections.</p> <p>This attribute helps guide the choice of stack via rule (via pillar) used for connecting routes to netlist terminals. If the specified value names a valid candidate for terminal in question (it is a member of list the candidate rules associated with the terminal's cell pin), then it will used as the preferred stack via rule for connecting to that terminal.</p> <p>Valid values: 'auto' or stack via rule name</p> <p><b>Type:</b> string</p> <p><b>Allowed -index values:</b> clock_tree</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>

#### cts\_stack\_via\_rule\_leaf

The preferred stack via rule for terminal connections.  
This attribute helps guide the choice of stack via rule (via pillar) used for connecting routes to netlist terminals. If the specified value names a valid candidate for terminal in question (it is a member of list the candidate rules associated with the terminal's cell pin), then it will be used as the preferred stack via rule for connecting to that terminal.  
Valid values: 'auto' or stack via rule name

**Type:** [string](#)

**Allowed -index values:** clock\_tree

**Default:** ""

**Edit:** Yes

#### cts\_stack\_via\_rule\_required

The pin-specific required field for stack via rule connections.

**Type:** [bool](#)

**Allowed -index values:** clock\_tree

**Default:** false

**Edit:** Yes

#### cts\_stack\_via\_rule\_required\_leaf

The pin-specific required field for stack via rule connections.

**Type:** [bool](#)

**Allowed -index values:** clock\_tree

**Default:** false

**Edit:** Yes

#### cts\_stack\_via\_rule\_required\_top

The pin-specific required field for stack via rule connections.

**Type:** [bool](#)

**Allowed -index values:** clock\_tree

**Default:** false

**Edit:** Yes

#### cts\_stack\_via\_rule\_required\_trunk

The pin-specific required field for stack via rule connections.

**Type:** [bool](#)

**Allowed -index values:** clock\_tree

**Default:** false

**Edit:** Yes

#### cts\_stack\_via\_rule\_top

	<p>The preferred stack via rule for terminal connections.</p> <p>This attribute helps guide the choice of stack via rule (via pillar) used for connecting routes to netlist terminals. If the specified value names a valid candidate for terminal in question (it is a member of list the candidate rules associated with the terminal's cell pin), then it will used as the preferred stack via rule for connecting to that terminal.</p> <p>Valid values: 'auto' or stack via rule name</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> clock_tree</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>cts_stack_via_rule_trunk</b>	
	<p>The preferred stack via rule for terminal connections.</p> <p>This attribute helps guide the choice of stack via rule (via pillar) used for connecting routes to netlist terminals. If the specified value names a valid candidate for terminal in question (it is a member of list the candidate rules associated with the terminal's cell pin), then it will used as the preferred stack via rule for connecting to that terminal.</p> <p>Valid values: 'auto' or stack via rule name</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> clock_tree</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>cts_target_max_capacitance</b>	
	<p>The target maximum capacitive load to allow during clock tree synthesis. This attribute specifies a maximum (combined pin and wire) capacitance that the clock tree synthesis algorithm will allow any given base_pin to drive in a given clock tree when driving a given net_type. It is specified in library units. It currently only constrains the primary delay corner capacitance values - other delay corners can be specified but will not be constrained. This attribute is applied in addition to the max_capacitance constraints read from the liberty library data - the tightest (lowest) of the constraint specified by this attribute and the constraint present in the liberty data will be used. It also does not apply at the root pins of clock trees - to constrain those nets the cts_clock_tree_source_max_capacitance CCOpt attribute should be used instead.</p> <p>Valid values: auto   double</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> delay_corner clock_tree</p> <p><b>Default:</b> top auto trunk auto leaf auto</p> <p><b>Edit:</b> Yes</p>
<b>cts_target_max_capacitance_leaf</b>	

The target maximum capacitive load to allow during clock tree synthesis. This attribute specifies a maximum (combined pin and wire) capacitance that the clock tree synthesis algorithm will allow any given base\_pin to drive in a given clock tree when driving a given net\_type. It is specified in library units. It currently only constrains the primary delay corner capacitance values - other delay corners can be specified but will not be constrained. This attribute is applied in addition to the max\_capacitance constraints read from the liberty library data - the tightest (lowest) of the constraint specified by this attribute and the constraint present in the liberty data will be used. It also does not apply at the root pins of clock trees - to constrain those nets the cts\_clock\_tree\_source\_max\_capacitance CCOpt attribute should be used instead. Valid values: auto | double

**Type:** string

**Allowed -index values:** delay\_corner clock\_tree

**Default:** auto

**Edit:** Yes

#### cts\_target\_max\_capacitance\_top

The target maximum capacitive load to allow during clock tree synthesis. This attribute specifies a maximum (combined pin and wire) capacitance that the clock tree synthesis algorithm will allow any given base\_pin to drive in a given clock tree when driving a given net\_type. It is specified in library units. It currently only constrains the primary delay corner capacitance values - other delay corners can be specified but will not be constrained. This attribute is applied in addition to the max\_capacitance constraints read from the liberty library data - the tightest (lowest) of the constraint specified by this attribute and the constraint present in the liberty data will be used. It also does not apply at the root pins of clock trees - to constrain those nets the cts\_clock\_tree\_source\_max\_capacitance CCOpt attribute should be used instead. Valid values: auto | double

**Type:** string

**Allowed -index values:** delay\_corner clock\_tree

**Default:** auto

**Edit:** Yes

#### cts\_target\_max\_capacitance\_trunk

	<p>The target maximum capacitive load to allow during clock tree synthesis. This attribute specifies a maximum (combined pin and wire) capacitance that the clock tree synthesis algorithm will allow any given base_pin to drive in a given clock tree when driving a given net_type. It is specified in library units. It currently only constrains the primary delay corner capacitance values - other delay corners can be specified but will not be constrained. This attribute is applied in addition to the max_capacitance constraints read from the liberty library data - the tightest (lowest) of the constraint specified by this attribute and the constraint present in the liberty data will be used. It also does not apply at the root pins of clock trees - to constrain those nets the cts_clock_tree_source_max_capacitance CCOpt attribute should be used instead.</p> <p>Valid values: auto   double</p> <p><b>Type:</b> string</p> <p><b>Allowed -index values:</b> delay_corner clock_tree</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p>
direction	<p>Base_pins's direction from .lib if available, otherwise from LEF/OA. It can be in, out, inout or internal. Internal means it is an internal pin from a .lib file for the timing model, and is not part of the netlist. If there is no .lib for this cell, then the direction comes from the LEF PIN DIRECTION or equivalent OA oaTermType. The LEF DIRECTION values (and equivalent oaTermType values) are mapped this way: INPUT = in, OUTPUT = out, OUTPUT TRISTATE = out, INOUT = inout, FEEDTHRU = inout, and the oaTermType unknown = inout.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> in out inout internal</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
effective_stack_via_rule	<p>The stack_via_rule that is expected, but not required, to be used by the router for connecting to the instance pins instantiated from this base_pin. The actual stack via rule used (if any) may be effected by other pin and base_pin attributes, or by choices made by the software (optimization, clock tree synthesis, the router etc.)</p> <p><b>Type:</b> obj(stack_via_rule)</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_always_on	

	<p>The always on pin of an always on cell.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> No</p>
is_analog	<p>Specifies the pin is an analog signal. This attribute can be set by liberty files.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> No</p>
is_isolated	<p>Specifies the pin is isolated internally in the cell. It is used for cells where some pins are internally isolated and some are not. This attribute can be set by liberty files.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> No</p>
is_isolation_cell_enable	<p>Identifies the pin is an isolation enable pin. This pin is used to control when to clamp the output and isolate it from the input. This attribute can be set by liberty files, or by CPF commands.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> No</p>
is_level_shifter_enable	<p>Identifies the pin is a level shifter enable pin. This pin is used to control when to clamp the output and isolate it from the input. This attribute can be set by liberty files, or by CPF commands.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> No</p>
is_power_switch_enable	<p>Identifies the pin is a power switch enable pin. This pin is used to control when to turn on/off the power switch. This attribute can be set by liberty files, or by CPF commands.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> No</p>
is_retention_cell_enable	

	<p>Identifies the pin as a retention cell enable pin. This pin is used to control when to retain the state and ignore other inputs. This attribute can be set by liberty files, or by CPF commands.</p> <p><b>Type:</b> bool  <b>Default:</b> false  <b>Edit:</b> No</p>
is_unconnected	<p>Specifies the pin is floating internally. This is used for cells where some of the inputs or outputs are unused by the cell. This attribute can be set by liberty files.</p> <p><b>Type:</b> bool  <b>Default:</b> false  <b>Edit:</b> No</p>
is_via_in_pin_only	<p>Indicates that the pin has a LEF VIAINPINONLY property. It means that vias must be dropped inside the original pin shapes to connect to the pin. In some advanced nodes, the pin shapes can be extended for metal alignment purposes. However, via insertion is not allowed in that extended portion if this attribute is true.</p> <p><b>Type:</b> bool  <b>Default:</b> ""  <b>Edit:</b> No</p>
layer	<p>Layer of the base_pin. For base_pins with more than one shape, it is the layer of the first shape (which is the same shape used for the .location value).</p> <p><b>Type:</b> obj(layer)  <b>Default:</b> ""  <b>Edit:</b> No</p>
must_join_pins	<p>The must join base_pin</p> <p><b>Type:</b> obj(base_pin)  <b>Default:</b> ""  <b>Edit:</b> No</p>
name	<p>Terminal name</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>
obj_type	

	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (base_pin)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
pg_type	<p>Specifies the type of the power or ground pin from liberty data. Signal pins and PG pins with no liberty entry will have "invalid".</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> primary_power primary_ground backup_power backup_ground internal_power internal_ground pwell nwell deeppwell deepnwell invalid</p> <p><b>Default:</b> invalid</p> <p><b>Edit:</b> No</p>
physical_direction	<p>Direction of this pin.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> input output inout unknown feedthrough tristate</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
physical_pins	<p>Physical pins for the base_pin. One logical base_pin can have multiple physical_pins. Each physical_pin had a list of strongly connected shapes (equivalent to LEF or DEF PORT or OA pin). The internal connection between physical_pins is weak (e.g. through poly or other high resistance paths)</p> <p><b>Type:</b> <a href="#">obj(physical_pin)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
pin_edge	<p>If this base_pin is for a partition, or inst that is a black-box, and the base_pin is assigned, the edge value indicates along which edge of the boundary polygon the base_pin is assigned. The edge number starts from the lowest Y, then left-most X vertex, staring with 0, and then counting clock-wise. See the set_pin_constraint command document for a figure showing the edge numbering. If the base_pin is not assigned, or not for a partition, or black-box inst, the value of -1 is returned.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
related_ground_pin	

	<p>Specifies which ground pin drives this signal pin. It must be one of the ground pins defined for this cell. It can be set by CPF, Liberty, or LEF/OA, with CPF having highest precedence, then Liberty, then LEF/OA. It is often only set when there is more than one ground pin for the cell.</p> <p><b>Type:</b> <a href="#">obj(base_pin)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>related_power_pin</b>	
	<p>Specifies which power pin drives this signal pin. It must be one of the power pins defined for this cell. It can be set by CPF, Liberty, or LEF/OA, with CPF having highest precedence, then Liberty, then LEF/OA. It is often only set when there is more than one power pin for the cell.</p> <p><b>Type:</b> <a href="#">obj(base_pin)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>stack_via_required</b>	
	<p>Specifies whether a stack via is required when connecting to the instance pins instantiated from this base_pin. If true, one of the stack_via_rule from stack_via_rule_list must be used to generate a stack via even if a design rule violation occurs. If false, a stack via is optional. Note that the pin stack_via_rule_required value may override this base_pin setting.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>stack_via_rule_list</b>	
	<p>List of stack_via_rule that are valid choices for connecting to the instance pins instantiated from this base_pin. If the list is empty, no stack via is allowed.</p> <p><b>Type:</b> <a href="#">obj(stack_via_rule)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>taper_rule</b>	
	<p>The taper route_rule for the pin. By default, if tapered routing is needed to access the pin, the default route_rule will be used unless this attribute is set (see LEF MACRO PIN TAPERRULE).</p> <p><b>Type:</b> <a href="#">obj(route_rule)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>tied_to</b>	

	<p>Specifies the PG pin name or 'empty' which the PG pin tied to.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
use	<p>Indicates how this pin is used from the LEF USE value or OA equivalent. The legal values are: signal analog power ground clock. Note that timing analysis does not use these values, it uses the .lib data instead (e.g. is_clock, is_analog, etc.). So the signal, clock or analog values are not normally used by applications. The power/ground values are used by many applications.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> signal analog power ground clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## boundary

### Parent Objects

[hinst](#), [design](#), [root](#)

### Definition

A boundary object can only be attached to an hinst, normally when the hinst is a partition. It is used to constrain the placement of all the insts of the hinst. See the group object for placement constraint information attached to the group object (e.g. a list of insts, hinsts, or groups).

Attribute	Description
area	<p>Sum of the area of the .rects that define the boundary</p> <p><b>Type:</b> <a href="#">area</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
bbox	

	Bounding box of the boundary rects. <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No
hinst	The parent hinst. This boundary affects all the insts inside the parent hinst. <b>Type:</b> <a href="#">obj(hinst)</a> <b>Default:</b> "" <b>Edit:</b> Yes
is_floating	Only affects boundary with .type = fence or region. If true, the global placer can move the fence or region. The .bbox and .rects value must also be set. The global placer will not change the size of the rect, but may move it. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (boundary)</a> <b>Default:</b> "" <b>Edit:</b> No
rects	List of non-overlapping rectangles that defines the shape of the boundary <b>Type:</b> <a href="#">rect*</a> <b>Default:</b> "" <b>Edit:</b> No
type	fence: all the insts are inside the boundary, and only these insts can be inside. region: all the insts are inside, but other insts can also be inside. guide: lower cost for insts to be inside boundary, but not required. cluster: keep insts near each other (the .rects field is empty). none: no affect on placement. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> guide region fence cluster none <b>Default:</b> "" <b>Edit:</b> Yes

# bump

## Parent Objects

[bump\\_pin](#), [design](#), [io\\_constraint](#), [root](#)

## Definition

Bump instance

Attribute	Description
base_cell	<p>The base_cell master of the bump.</p> <p><b>Type:</b> <a href="#">obj(base_cell)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
base_name	<p>The base_name of the bump</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
bbox	<p>Bounding box of the bump shape for a package connection, which is the widest shape found on the top routing layer in the base_cell. If there is more than one wide shape of the same size, the bbox of all the wide shapes is returned.</p> <p><b>Type:</b> <a href="#">rect</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
bump_pins	<p>The pins of the bump. A bump with ALLPINSCONNECTED LEF syntax can have multiple bump_pins which are internally connected.</p> <p><b>Type:</b> <a href="#">obj(bump_pin)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
center	

	<p>The center of the bump shape for a package connection, which is the center of the .bbox attribute. This is not the same as the .location of the bump which is normally at the lower-left corner of the cell.</p> <p><b>Type:</b> <a href="#">point</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
escaped_name	
	<p>The escaped name of the bump</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_fixed_assignment	
	<p>Indicates that the bump is connected to one port</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
location	
	<p>Location of the bump.</p> <p><b>Type:</b> <a href="#">point</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
name	
	<p>Name of the bump</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
net	
	<p>The net connected to the bump.</p> <p><b>Type:</b> <a href="#">obj(net)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obj_type	
	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (bump)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

orient	
	<p>Bump orientation.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> r0 r90 r180 r270 mx mx90 my my90</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
place_status	<p>Placement status of bump.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> unplaced placed fixed cover soft_fixed</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
ports	<p>The ports the bump is assigned to.</p> <p><b>Type:</b> <a href="#">obj(port)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## bus

### Parent Objects

[design](#), [net](#), [root](#), [port](#)

### Definition

The Verilog bus definitions in the top Verilog module.

Attribute	Description
bits	<p>The nets or ports of the bus. All the bits of one bus will have the same obj_type.</p> <p><b>Type:</b> <a href="#">obj(port)*</a> <a href="#">obj(net)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
lsb	

	Bottom bit index of bus. <b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No
msb	
	Top bit index of bus. <b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No
name	
	Non-vector portion of the bus name (eg. A for bus A[7:0]) <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
obj_type	
	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (bus) <b>Default:</b> "" <b>Edit:</b> No

## bus\_guide

### Parent Objects

[design](#)

### Definition

Bus guide

Attribute	Description
area	
	Area of the bus_guide as defined by the LEF MACRO SIZE or OVERLAP information <b>Type:</b> area <b>Default:</b> "" <b>Edit:</b> No

bottom_layer	The bottom layer of allowed layer range <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> Yes
net_group	The net group with list of nets to be routed within the bus_guide <b>Type:</b> <a href="#">obj(net_group)*</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (bus_guide)</a> <b>Default:</b> "" <b>Edit:</b> No
rect	Rectangel that defines the bus_guide shape. <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No
top_layer	The top layer of allowed layer range <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> Yes
type	The type of bus_guide. hard: Specifies the bus_guide as a hard constraint for routing. eGR, NR and NRHF should obey the path of bus guide. soft: Specifies the bus_guide as a soft constraint for routing. eGR, NR and NRHF should be guided by the route path. But tool can route the net out of the bus guide. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> soft hard <b>Default:</b> "" <b>Edit:</b> Yes

# clock

## Parent Objects

[pin](#), [timing\\_path](#), [root](#), [port](#)

## Definition

cte clock

Attribute	Description
base_name	<p>The base_name of the clock.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
clock_hold_uncertainty	<p>clock_hold_uncertainty</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
clock_network_pins	<p>Returns a list of pin and hpin objects in the extended fanout of the clock source. The extended fanout includes the fanout of generated clocks which the current clock is the master for.</p> <p><b>Type:</b> <a href="#">obj(port)* obj(pin)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
clock_setup_uncertainty	<p>clock_setup_uncertainty</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
delay_max_fall	

	Returns the maximum falling delay value for the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
delay_max_rise	Returns the maximum rising delay value for the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
delay_min_fall	Returns the minimum falling delay value for the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
delay_min_rise	Returns the minimum rising delay value for the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
divide_by	Returns the create_generated_clock -divide_by option of a generated clock. <b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No
duty_cycle	Returns the create_generated_clock -duty_cycle option of a generated clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
edge_shift	Returns the create_generated_clock -edge_shift option of a generated clock. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
edges	

	Returns the create_generated_clock -edges option of a generated clock. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
generated_clocks	
	Returns a list of clock object which are the generated clocks derived from this master clock. <b>Type:</b> <a href="#">obj(clock)</a> * <b>Default:</b> "" <b>Edit:</b> No
hierarchical_name	
	hierarchical_name <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
ideal_transition_max_fall	
	Returns the set_clock_transition -max -fall asserted on the clock and used during ideal mode analysis. <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No
ideal_transition_max_rise	
	Returns the set_clock_transition -max -rise asserted on the clock and used during ideal mode analysis. <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No
ideal_transition_min_fall	
	Returns the set_clock_transition -min -fall asserted on the clock and used during ideal mode analysis. <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No
ideal_transition_min_rise	

	Returns the set_clock_transition -min -rise asserted on the clock and used during ideal mode analysis. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
is_active	
	Returns true if the clock has been set active by the set_active_clocks constraint. <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_combinational_source_path	
	Returns true if the create_generated_clock -combinational option was specified for the creation of this generated clock. <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_generated	
	Returns true if this clock object represents a generated clock <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_inverted	
	Returns true if the create_generated_clock -invert option was specified for the creation of this generated clock. <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_library_created	
	Returns true if this generated_clock was specified in a Liberty generated_clock group and not created by a create_generated_clock constraint <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_propagated	

	Returns true if set_propagated_clock was asserted explicitly on this clock object. <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
<b>is_virtual</b>	
	Returns true if this clock is virtual <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
<b>master_clock</b>	
	Returns the master clock of this generated clock as specified by the create_generated_clock -master_clock option when this generated clock was created. <b>Type:</b> obj(clock)* <b>Default:</b> "" <b>Edit:</b> No
<b>master_source</b>	
	Returns the master clock source pin of this generated clock as specified by the create_generated_clock -source option when this generated clock was created. <b>Type:</b> obj(pin)* obj(hpin)* obj(hport)* <b>Default:</b> "" <b>Edit:</b> No
<b>max_capacitance_clock_path_fall</b>	
	Returns the value asserted by set_max_capacitance -clock_path -fall on this clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>max_capacitance_clock_path_rise</b>	
	Returns the value asserted by set_max_capacitance -clock_path -rise on this clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>max_capacitance_data_path_fall</b>	
	Returns the value asserted by set_max_capacitance -data_path -fall on this clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No

max_capacitance_data_path_rise	Returns the value asserted by set_max_capacitance -data_path -rise on this clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
max_transition_clock_path_fall	Returns the value asserted by set_max_transition -clock_path -fall on this clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
max_transition_clock_path_rise	Returns the value asserted by set_max_transition -clock_path -rise on this clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
max_transition_data_path_fall	Returns the value asserted by set_max_transition -data_path -fall on this clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
max_transition_data_path_rise	Returns the value asserted by set_max_transition -data_path -rise on this clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
min_pulse_width_high	Returns the minimum pulse width high requirement set by set_min_pulse_width . <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
min_pulse_width_low	Returns the minimum pulse width low requirement set by set_min_pulse_width. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No

<b>multiply_by</b>	Returns the create_generated_clock -multiply_by option of a generated clock. <b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No
<b>name</b>	The name of the clock. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
<b>network_latency_fall_max</b>	Returns the maximum fall insertion delay specified by an explicit set_clock_latency on the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>network_latency_fall_min</b>	Returns the minimum fall insertion delay specified by an explicit set_clock_latency on the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>network_latency_rise_max</b>	Returns the maximum rise insertion delay specified by an explicit set_clock_latency on the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>network_latency_rise_min</b>	Returns the minimum rise insertion delay specified by an explicit set_clock_latency on the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>obj_type</b>	

	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> enum (clock) <b>Default:</b> "" <b>Edit:</b> No</p>
period	<p>Returns the period of the clock. The period is either specified directly with create_clock or derived from a generated clock.</p> <p><b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No</p>
source_jitter_early_fall_max	<p>Returns the amount of the maximum early fall source insertion delay that is due to cycle-to-cycle variation. This is specified by using the set_clock_latency -jitter option.</p> <p><b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No</p>
source_jitter_early_fall_min	<p>Returns the amount of the minimum early fall source insertion delay that is due to cycle-to-cycle variation. This is specified by using the set_clock_latency -jitter option.</p> <p><b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No</p>
source_jitter_early_rise_max	<p>Returns the amount of the maximum early rise source insertion delay that is due to cycle-to-cycle variation. This is specified by using the set_clock_latency -jitter option.</p> <p><b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No</p>
source_jitter_early_rise_min	<p>Returns the amount of the minimum early rise source insertion delay that is due to cycle-to-cycle variation. This is specified by using the set_clock_latency -jitter option.</p> <p><b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No</p>
source_jitter_late_fall_max	

	Returns the amount of the maximum late fall source insertion delay that is due to cycle-to-cycle variation. This is specified by using the set_clock_latency -jitter option. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
source_jitter_late_fall_min	
	Returns the amount of the minimum late fall source insertion delay that is due to cycle-to-cycle variation. This is specified by using the set_clock_latency -jitter option. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
source_jitter_late_rise_max	
	Returns the amount of the maximum late rise source insertion delay that is due to cycle-to-cycle variation. This is specified by using the set_clock_latency -jitter option. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
source_jitter_late_rise_min	
	Returns the amount of the minimum late rise source insertion delay that is due to cycle-to-cycle variation. This is specified by using the set_clock_latency -jitter option. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
source_latency_early_fall_max	
	Returns the maximum early fall source insertion delay specified by an explicit set_clock_latency on the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
source_latency_early_fall_min	
	Returns the minimum early fall source insertion delay specified by an explicit set_clock_latency on the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
source_latency_early_rise_max	

	Returns the maximum early rise source insertion delay specified by an explicit set_clock_latency on the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>source_latency_early_rise_min</b>	
	Returns the minimum early rise source insertion delay specified by an explicit set_clock_latency on the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>source_latency_late_fall_max</b>	
	Returns the maximum late fall source insertion delay specified by an explicit set_clock_latency on the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>source_latency_late_fall_min</b>	
	Returns the minimum late fall source insertion delay specified by an explicit set_clock_latency on the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>source_latency_late_rise_max</b>	
	Returns the maximum late rise source insertion delay specified by an explicit set_clock_latency on the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>source_latency_late_rise_min</b>	
	Returns the minimum late rise source insertion delay specified by an explicit set_clock_latency on the clock. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>sources</b>	

	Returns the pin or port objects where the clock is attached to the design - as specified by create_clock or create_generated_clock <b>Type:</b> obj(port)* obj(pin)* <b>Default:</b> "" <b>Edit:</b> No
<b>view_name</b>	
	The name of the analysis view for the clock. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
<b>waveform</b>	
	Returns a list of the sequence of rising and falling edge times of a single period of the clock. The first list entry is always the first rising edge time, and the second entry is always the subsequent falling edge time. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No

## clock\_spine

### Parent Objects

### Definition

clock tree spine

Attribute	Description
name	
	name of clock_spine <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
obj_type	

	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (clock_spine)</a> <b>Default:</b> "" <b>Edit:</b> No
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## clock\_tree

### Parent Objects

[clock\\_tree\\_source\\_group](#), [pin](#), [root](#), [port](#)

### Definition

clock tree in ccopt

Attribute	Description
<a href="#">clock_tree_source_group</a>	the clock_tree_source_group this clock_trees is a member of <b>Type:</b> <a href="#">obj(clock_tree_source_group)*</a> <b>Default:</b> "" <b>Edit:</b> No
<a href="#">cts_buffer_cells</a>	

	<p>Specifies the buffer cells for CTS. If none are specified CCOpt will choose buffers from the libraries.</p> <p>Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names.</p> <p>If set explicitly, CCOpt will ignore any dont_use settings for the cells specified.</p> <p>Different buffer cells may be specified for any combination of clock tree and power domain.</p> <p>To use different buffers for each net type set the cts_buffer_cells_top and cts_buffer_cells_leaf attributes .</p> <p>Some examples follow:</p> <p>To specify buffer cells for all clock trees and all power domains:</p> <pre>set_db cts_buffer_cells {bufAX* bufBX*}</pre> <p>To specify buffer cells for a particular clock tree and all power domains:</p> <pre>set_db clock_tree:&lt;clk&gt;.cts_buffer_cells {bufX20 bufX18}</pre> <p>To specify buffer cells for a particular clock tree and power domain:</p> <pre>set_db clock_tree:&lt;clk&gt;.cts_buffer_cells -index {power_domain &lt;pd&gt;} {bufX12 bufX8}</pre> <p>Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> string</p> <p><b>Allowed -index values:</b> power_domain</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>cts_buffer_cells_leaf</b>	
	<p>Specifies the buffer cells available for CTS to use on leaf nets. If none are specified CCOpt will use the same buffers as on trunk nets (as specified in the cts_buffer_cells attribute).</p> <p>Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names.</p> <p>If set explicitly, CCOpt will ignore any dont_use settings for the cells specified.</p> <p>Different leaf buffer cells may be specified for any combination of clock tree and power domain.</p> <p>Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> string</p> <p><b>Allowed -index values:</b> power_domain</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>cts_buffer_cells_top</b>	

	<p>Specifies the buffers cells available for CTS to use on top nets. If none are specified CCOpt will use the same buffers as on trunk nets (as specified in the cts_buffer_cells attribute). Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names. If set explicitly, CCOpt will ignore any dont_use settings for the cells specified. Different top buffer cells may be specified for any combination of clock tree and power domain. Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> string  <b>Allowed -index values:</b> power_domain  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
cts_clock_gating_cells	<p>Specifies the clock gates for CTS. If none are specified CCOpt will choose clock gates from the libraries. Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names. If set explicitly, CCOpt will ignore any dont_use settings for the cells specified. Different clock gates may be specified for any combination of clock tree and power domain. Some examples follow:</p> <p>To specify clock gates for all clock trees and all power domains:  <code>set_db cts_clock_gating_cells {cgAX* cgBX*}</code></p> <p>To specify clock gates for a particular clock tree and all power domains:  <code>set_db clock_tree:&lt;clk&gt;.cts_clock_gating_cells {cgX20 cgX18}</code></p> <p>To specify clock gates for a particular clock tree and power domain:  <code>set_db clock_tree:&lt;clk&gt;.cts_clock_gating_cells -index {power_domain &lt;pd&gt;} {cgX12 cgX8}</code></p> <p>Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> string  <b>Allowed -index values:</b> power_domain  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
cts_clock_source_cells	

	<p>Specifies the cells available for CTS to size clock sources if the cts_size_clock_sources attribute is set to true. If none are specified the tool will choose cells from the libraries. Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names.</p> <p>If set explicitly, the tool will ignore any dont_use settings for the cells specified.</p> <p>Different cells may be specified for clock trees or power domains. Only clock sources that are buffers, inverters, logic and clock gating cells with a single output can be resized.</p> <p>Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> string  <b>Allowed -index values:</b> power_domain  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
<b>cts_clock_tree_parents</b>	
	<p>The list of parent clock trees from which this clock tree is generated, if any.</p> <p>Valid values: list cts_clock_tree</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>cts_clock_tree_source_driver</b>	
	<p>Specifies the base_pin which is assumed to drive this clock tree. It is either a single base_pin (in which case all arcs to that base_pin shall be used when timing the clock tree root) or a pair of base_pins (in which case only arcs from the first specified pin to the second will be considered).</p> <p>By default this is generated from clock tree extraction</p> <p>Valid values: base_pin   {base_pin base_pin}</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
<b>cts_clock_tree_source_group</b>	
	<p>Specifies the clock tree source group to which this clock tree belongs.</p> <p>Valid values: list cts_clock_tree_source_group</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>cts_clock_tree_source_group_clock_trees</b>	

	A list of the clock trees relevant to this source group. Valid values: list cts_clock_trees <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes
<b>cts_clock_tree_source_input_max_transition_time</b>	
	The slew which will be assumed at the input of the root driver. Valid values: double <b>Type:</b> double <b>Allowed -index values:</b> delay_corner <b>Default:</b> 0 <b>Edit:</b> Yes
<b>cts_clock_tree_source_max_capacitance</b>	
	The maximum capacitive load which this clock tree is permitted to drive. Valid values: double   auto Auto: from clock tree extraction <b>Type:</b> string <b>Default:</b> auto <b>Edit:</b> Yes
<b>cts_clock_tree_source_output_max_transition_time</b>	
	If non-zero, the slew which will be assumed at the output of the root driver. This overrides the value from SDC. Valid values: double <b>Type:</b> double <b>Allowed -index values:</b> delay_corner <b>Default:</b> 0 <b>Edit:</b> Yes
<b>cts_delay_cells</b>	

	<p>Specifies the delay cells available for CTS. If none are specified CCOpt will not use delay cells.</p> <p>Setting this attribute to the string 'auto' means that CCOpt will choose delay cells from the libraries to use.</p> <p>Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names.</p> <p>If set explicitly, CCOpt will ignore any dont_use settings for the cells specified.</p> <p>Different delay cells may be specified for any combination of clock tree and power domain, or by omitting those arguments a global setting can be applied.</p> <p>Some examples follow:</p> <p>To specify delay cells for all clock trees and power domains:</p> <pre>set_db cts_delay_cells {delayAX* delayBX*}</pre> <p>To specify delay cells for a particular clock tree and all power domains:</p> <pre>set_db clock_tree:&lt;clk&gt;.cts_delay_cells {delayX1 delayX2}</pre> <p>To specify delay cells for a particular clock tree and power domain:</p> <pre>set_db clock_tree:&lt;clk&gt;.cts_delay_cells -index {power_domain &lt;pd&gt;} {delayX2 delayX3}</pre> <p>Valid values: a list of library cell names, or a list of patterns to expand to library cell names, or the string 'auto'</p> <p><b>Type:</b> string</p> <p><b>Allowed -index values:</b> power_domain</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
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cts\_inverter\_cells

<p>Specifies the inverter cells available for CTS. If none are specified CCOpt will choose inverters from the libraries.</p> <p>Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names.</p> <p>If set explicitly, CCOpt will ignore any dont_use settings for the cells specified.</p> <p>Different inverter cells may be specified for any combination of clock tree and power domain.</p> <p>To use different inverters for each net type set the cts_inverter_cells_top and cts_inverter_cells_leaf attributes .</p> <p>Some examples follow:</p> <p>To specify inverter cells for all clock trees and all power domains:</p> <pre>set_db cts_inverter_cells {invAX* invBX*}</pre> <p>To specify inverter cells for a particular clock tree and all power domains:</p> <pre>set_db clock_tree:&lt;clk&gt;.cts_inverter_cells {invX20 invX18}</pre> <p>To specify inverter cells for a particular clock tree and power domain:</p> <pre>set_db clock_tree:&lt;clk&gt;.cts_inverter_cells -index {power_domain &lt;pd&gt;} {invX12 invX8}</pre> <p>Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> string  <b>Allowed -index values:</b> power_domain  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
<p><b>cts_inverter_cells_leaf</b></p> <p>Specifies the inverter cells available for CTS to use on leaf nets. If none are specified CCOpt will use the same inverters as on trunk nets (as specified in the cts_inverter_cells attribute).</p> <p>Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names.</p> <p>If set explicitly, CCOpt will ignore any dont_use settings for the cells specified.</p> <p>Different leaf inverter cells may be specified for any combination of clock tree and power domain.</p> <p>Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> string  <b>Allowed -index values:</b> power_domain  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
<p><b>cts_inverter_cells_top</b></p>

	<p>Specifies the inverter cells available for CTS to use on top nets. If none are specified CCOpt will use the same inverters as on trunk nets (as specified in the cts_inverter_cells attribute). Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names. If set explicitly, CCOpt will ignore any dont_use settings for the cells specified. Different top inverter cells may be specified for any combination of clock tree and power domain. Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> power_domain</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>cts_logic_cells</b>	
	<p>Specifies the clock logics for CTS. If none are specified CCOpt will choose clock logics from the libraries. Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names. If set explicitly, CCOpt will ignore any dont_use settings for the cells specified. Different logic cells may be specified for any combination of clock tree and power domain. Some examples follow:</p> <p>To specify logic cells for all clock trees and all power domains:  <code>set_db cts_logic_cells {and* mux*}</code></p> <p>To specify logic cells for a particular clock tree and all power domains:  <code>set_db clock_tree:&lt;clk&gt; .cts_logic_cells {andX20 andX18}</code></p> <p>To specify logic cells for a particular clock tree and power domain:  <code>set_db clock_tree:&lt;clk&gt; .cts_logic_cells -index {power_domain &lt;pd&gt;} {andX12 andX8}</code></p> <p>Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> power_domain</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>cts_route_type_leaf</b>	

	<p>Specifies the route type. Setting this attribute binds an existing user-defined route_type to one or more types of clock tree nets. Binding a route_type to a type of clock tree nets means that all nets of that type (including the nets created by CTS) will be routed according to the specification of that route_type.</p> <p>In the most common usage, the route_type is bound to one of the three types of clock tree nets (top, trunk, or leaf) with the optional -net_type argument. Omitting the -net_type argument causes the route_type to be bound to all three types of clock tree nets. The optional -clock_tree &lt;pattern&gt; argument limits the binding to the clock trees whose name matches &lt;pattern&gt;. Omitting the -clock_tree argument causes the binding to apply to all clock trees.</p> <p>For a route_type to be used in CTS, it must be bound to at least one net type. If net type is not bound to any route_type, a default route_type will be created for that net type at the start of CTS.</p> <p>Valid values: names of route_types created with create_route_type</p> <p><b>Type:</b> string <b>Default:</b> default <b>Edit:</b> Yes</p>
cts_route_type_top	<p>Specifies the route type. Setting this attribute binds an existing user-defined route_type to one or more types of clock tree nets. Binding a route_type to a type of clock tree nets means that all nets of that type (including the nets created by CTS) will be routed according to the specification of that route_type.</p> <p>In the most common usage, the route_type is bound to one of the three types of clock tree nets (top, trunk, or leaf) with the optional -net_type argument. Omitting the -net_type argument causes the route_type to be bound to all three types of clock tree nets. The optional -clock_tree &lt;pattern&gt; argument limits the binding to the clock trees whose name matches &lt;pattern&gt;. Omitting the -clock_tree argument causes the binding to apply to all clock trees.</p> <p>For a route_type to be used in CTS, it must be bound to at least one net type. If net type is not bound to any route_type, a default route_type will be created for that net type at the start of CTS.</p> <p>Valid values: names of route_types created with create_route_type</p> <p><b>Type:</b> string <b>Default:</b> default <b>Edit:</b> Yes</p>
cts_route_type_trunk	

	<p>Specifies the route type. Setting this attribute binds an existing user-defined route_type to one or more types of clock tree nets. Binding a route_type to a type of clock tree nets means that all nets of that type (including the nets created by CTS) will be routed according to the specification of that route_type.</p> <p>In the most common usage, the route_type is bound to one of the three types of clock tree nets (top, trunk, or leaf) with the optional -net_type argument. Omitting the -net_type argument causes the route_type to be bound to all three types of clock tree nets. The optional -clock_tree &lt;pattern&gt; argument limits the binding to the clock trees whose name matches &lt;pattern&gt;. Omitting the -clock_tree argument causes the binding to apply to all clock trees.</p> <p>For a route_type to be used in CTS, it must be bound to at least one net type. If net type is not bound to any route_type, a default route_type will be created for that net type at the start of CTS.</p> <p>Valid values: names of route_types created with create_route_type</p> <p><b>Type:</b> string  <b>Default:</b> default  <b>Edit:</b> Yes</p>
<b>cts_source_latency</b>	
	<p>Specifies a delay value between the global clock source and this clock tree. This additional delay will be included in all timing analysis involving skew groups for which this clock tree is a source. The default is 0.</p> <p>Valid values: double</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> delay_corner  <b>Default:</b> 0  <b>Edit:</b> Yes</p>
<b>cts_target_max_transition_time</b>	
	<p>The target slew used for clock tree synthesis. This attribute specifies a maximum slew time that the clock tree synthesis algorithm will allow in this clock tree, in library units. 'default' means 'auto' in primary half corner and 'ignore' in other half corners. If set to 'auto', CTS picks an appropriate value based on the collection of allowed buffer sizes and library parameters, although this may not give optimal quality of results. If set to 'ignore', CTS does not constrain the corner.</p> <p>Valid values: default   auto   ignore   double</p> <p><b>Type:</b> string  <b>Allowed -index values:</b> delay_corner power_domain  <b>Default:</b> top default trunk default leaf default  <b>Edit:</b> Yes</p>
<b>cts_target_max_transition_time_leaf</b>	

	<p>The target slew used for clock tree synthesis. This attribute specifies a maximum slew time that the clock tree synthesis algorithm will allow in this clock tree, in library units. 'default' means 'auto' in primary half corner and 'ignore' in other half corners. If set to 'auto', CTS picks an appropriate value based on the collection of allowed buffer sizes and library parameters, although this may not give optimal quality of results. If set to 'ignore', CTS does not constrain the corner.</p> <p>Valid values: default   auto   ignore   double</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> delay_corner power_domain</p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p>
<p>cts_target_max_transition_time_sdc</p>	
	<p>If non-zero, the target slew used for clock tree synthesis, overriding the SDC. This attribute specifies a maximum slew time that the clock tree synthesis algorithm will allow, in library units obtained from SDC.</p> <p>Valid values: double</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> delay_corner</p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
<p>cts_target_max_transition_time_top</p>	
	<p>The target slew used for clock tree synthesis. This attribute specifies a maximum slew time that the clock tree synthesis algorithm will allow in this clock tree, in library units. 'default' means 'auto' in primary half corner and 'ignore' in other half corners. If set to 'auto', CTS picks an appropriate value based on the collection of allowed buffer sizes and library parameters, although this may not give optimal quality of results. If set to 'ignore', CTS does not constrain the corner.</p> <p>Valid values: default   auto   ignore   double</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> delay_corner power_domain</p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p>
<p>cts_target_max_transition_time_trunk</p>	

	<p>The target slew used for clock tree synthesis. This attribute specifies a maximum slew time that the clock tree synthesis algorithm will allow in this clock tree, in library units. 'default' means 'auto' in primary half corner and 'ignore' in other half corners. If set to 'auto', CTS picks an appropriate value based on the collection of allowed buffer sizes and library parameters, although this may not give optimal quality of results. If set to 'ignore', CTS does not constrain the corner.</p> <p>Valid values: default   auto   ignore   double</p> <p><b>Type:</b> string</p> <p><b>Allowed -index values:</b> delay_corner power_domain</p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p>
<b>cts_top_fanout_threshold</b>	
	<p>Minimum number of transitive fanout in the clock tree for a net to be routed as a top net. Nets with at least this many sinks in their transitive fanout in the clock tree will have the special routing rules applied to them.</p> <p>Valid values: integer</p> <p><b>Type:</b> string</p> <p><b>Default:</b> unset</p> <p><b>Edit:</b> Yes</p>
<b>insts</b>	
	<p>instances in the clock tree</p> <p><b>Type:</b> obj(inst)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>name</b>	
	<p>name of clock_tree</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>nets</b>	
	<p>nets in the clock tree</p> <p><b>Type:</b> obj(net)</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>obj_type</b>	

	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum ( <a href="#">clock_tree</a> ) <b>Default:</b> "" <b>Edit:</b> No
sinks	
	sinks (pins or ports) of the clock tree <b>Type:</b> <a href="#">obj(pin)*</a> <a href="#">obj(port)*</a> <b>Default:</b> "" <b>Edit:</b> No
source	
	The source pin for this cts_clock_tree. Valid values: pin <b>Type:</b> <a href="#">obj(pin)*</a> <a href="#">obj(port)*</a> <b>Default:</b> "" <b>Edit:</b> No

## clock\_tree\_source\_group

### Parent Objects

[clock\\_tree](#), [root](#)

### Definition

clock tree source group

Attribute	Description
clock_trees	clock_tree_source_group member clock_trees <b>Type:</b> <a href="#">obj(clock_tree)*</a> <b>Default:</b> "" <b>Edit:</b> Yes
name	

	<p>name of clock_tree_source_group <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (clock_tree_source_group) <b>Default:</b> "" <b>Edit:</b> No</p>

## constraint\_mode

### Parent Objects

[analysis\\_view](#), [design](#), [root](#)

### Definition

Associates a list of SDC constraint files with a specified constraint mode name, for multi-mode multi-corner analysis. This constraint mode name can be referred to later when creating analysis views. Use the `create_constraint_mode` and `update_constraint_mode` commands to create and modify constraint\_modes.

Attribute	Description
ilm_sdc_files	<p>Specifies an optional list of constraint files to use when using ILM mode <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No</p>
is_active	<p>Indicates that the constraint_mode is associated with an analysis_view that is used in the active analysis_view. <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No</p>
is_dynamic	

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	Indicates that the constraint_mode is associated with an analysis_view that is used in the active dynamic analysis_view. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_hold	Indicates that the constraint_mode is associated with an analysis_view that is active for hold analysis. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_leakage	Indicates that the constraint_mode is associated with an analysis_view that is used in the active leakage analysis_view. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_setup	Indicates that the constraint_mode is associated with an analysis_view that is active for setup analysis. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
name	Provides the name of this constraint_mode object as specified by create_constraint_mode. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (constraint_mode)</a> <b>Default:</b> "" <b>Edit:</b> No
sdc_files	

	<p>Specifies an optional list of constraint files to associate with the mode</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
tcl_vars	<p>Specifies an optional list of user-specified Tcl variable name and value pairs - e.g: {{my_var1 true} {my_var2 0.1}} - which are set before the constraint files are read, and can be used inside the constraint files.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## delay\_corner

### Parent Objects

[analysis\\_view](#), [design](#), [root](#)

### Definition

The delay\_corner object provides references to rc\_corner objects which define the interconnect corner and timing\_condition-to-domain bindings which define device operating corners - providing the majority of the configuration information needed to drive delay calculation. An analysis\_view object will reference the delay\_corner and combine it with a constraint\_mode to complete the configuration. Use the create\_delay\_corner and update\_delay\_corner commands to create and modify delay\_corner objects.

Attribute	Description
default_early_timing_condition	<p>Specifies the timing condition to be used for early path analysis if one has not been explicitly specified for a given power domain.</p> <p><b>Type:</b> <a href="#">obj(timing_condition)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
default_late_timing_condition	

	<p>Specifies the timing condition to be used for late path analysis if one has not been explicitly specified for a given power domain.</p> <p><b>Type:</b> <a href="#">obj(timing_condition)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>early_irdrop_files</b>	
	<p>Specifies a file with instance-specific voltage data for early path analysis. Instance voltage data can be either exported from power rail analysis tools such as Voltus, or specified with set_instance_voltage constraints</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>early_pg_net_voltages</b>	
	<p>Specifies the power/ground net voltages to use for early analysis</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>early_rc_corner</b>	
	<p>Specifies the associated rc_corner object for early path analysis</p> <p><b>Type:</b> <a href="#">obj(rc_corner)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>early_temperature_files</b>	
	<p>Specifies a file with instance-specific temperature data for early path analysis</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>early_timing_condition</b>	
	<p>Provides the early_timing_condition object associated with the specified power_domain index. If no power_domain index is given, the default early_timing_condition will be returned.</p> <p><b>Type:</b> <a href="#">obj(timing_condition)</a></p> <p><b>Allowed -index values:</b> power_domain</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>early_timing_condition_string</b>	

**Stylus Common UI Database Object Information**  
**Database Objects--delay\_corner**

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	<p>Specifies the list of power_domain to timing_condition bindings for early path analysis - using &lt;power_domain&gt;@&lt;timing_condition&gt; list syntax, for example 'defaultTC PD1@TC1 PD2@TC2'.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_active	<p>Indicates that the delay_corner is associated with an analysis_view that is used in the active analysis_view</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_dynamic	<p>Indicates that the delay_corner is associated with an analysis_view that is used in the active dynamic analysis_view</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_hold	<p>Indicates that the delay_corner is associated with an analysis_view that is active for hold analysis</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_leakage	<p>Indicates that the delay_corner is associated with an analysis_view that is used in the active leakage analysis_view</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_setup	<p>Indicates that the delay_corner is associated with an analysis_view that is active for setup analysis</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_si_enabled	

**Stylus Common UI Database Object Information**  
Database Objects--delay\_corner

	Indicates that analysis_views associated with this delay_corner should have SI analysis performed on them <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
<b>late_irdrop_files</b>	
	Specifies a file with instance-specific voltage data for late path analysis. Instance voltage data can be either exported from power rail analysis tools such as Voltus, or specified with set_instance_voltage constraints <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
<b>late_pg_net_volts</b>	
	Specifies the power/ground net voltages to use for late analysis <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
<b>late_rc_corner</b>	
	Specifies the associated rc_corner object for late path analysis <b>Type:</b> <a href="#">obj(rc_corner)</a> <b>Default:</b> "" <b>Edit:</b> No
<b>late_temperature_files</b>	
	Specifies a file with instance-specific temperature data for late path analysis <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
<b>late_timing_condition</b>	
	Provides the late timing_condition object associated with the specified power_domain index. If no power_domain index is given, the default late timing_condition will be returned. <b>Type:</b> <a href="#">obj(timing_condition)</a> <b>Allowed -index values:</b> power_domain <b>Default:</b> "" <b>Edit:</b> No
<b>late_timing_condition_string</b>	

	Specifies the list of power_domain to timing_condition bindings for late path analysis - using <power_domain>@<timing_condition> list syntax, for example 'defaultTC PD1@TC1 PD2@TC2'. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
name	
	Provides the name of this delay_corner object as specified by create_delay_corner. This name can be referenced by other commands to refer to this object <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
obj_type	
	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (delay_corner) <b>Default:</b> "" <b>Edit:</b> No
pg_net_voltages	
	Specifies the power/ground net voltages to use for both early/late analysis <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No

## **density\_shape**

### **Parent Objects**

[place\\_blockage](#)

### **Definition**

Rectangle with metal/cut or placement density information

Attribute	Description
density	

	Density value (range: 0.0-1.0 <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (density_shape)</a> <b>Default:</b> "" <b>Edit:</b> No
rect	Rectangle. For cellDensity, the coordinates are local to cell, not relative to the design. <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No

# design

## Parent Objects

[hinst](#), [inst](#), [module](#), [pin\\_group](#), [pin\\_guide](#), [root](#), [port](#)

## Definition

top cell

Attribute	Description
analysis_views	Returns the information about the analysis views in the design. <b>Type:</b> <a href="#">obj(analysis_view)*</a> <b>Default:</b> "" <b>Edit:</b> No
area	

	The area of all the insts contained inside this design and below it. This does not include phys_insts. Use 'get_db \$design .boundary.area' if you want the area of the physical design boundary. <b>Type:</b> <a href="#">area</a> <b>Default:</b> "" <b>Edit:</b> No
bbox	Bounding box of the design boundary, <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No
boundaries	All the boundary objects (fence, region, etc.) in the design. <b>Type:</b> <a href="#">obj(boundary)</a> * <b>Default:</b> "" <b>Edit:</b> No
boundary	Polygon that define the shape of the floorplan boundary <b>Type:</b> <a href="#">polygon</a> * <b>Default:</b> "" <b>Edit:</b> No
bumps	List of bumps in the cell <b>Type:</b> <a href="#">obj(bump)</a> * <b>Default:</b> "" <b>Edit:</b> No
bus_guides	List of bus guide objects. <b>Type:</b> <a href="#">obj(bus_guide)</a> * <b>Default:</b> "" <b>Edit:</b> No
bus_sink_groups	

	A group of sinks (loads) that some floorplan and routing commands use to control adding buffers and routing for a bus. See 'help *bus_sink*' for a list of commands related to this object. <b>Type:</b> <a href="#">obj(bus_sink_group)</a> * <b>Default:</b> {} <b>Edit:</b> No
<b>busses</b>	
	The Verilog bus definitions for ports or nets in the top Verilog module. <b>Type:</b> <a href="#">obj(bus)</a> * <b>Default:</b> "" <b>Edit:</b> No
<b>constraint_modes</b>	
	Returns the information about the constraint modes in the design. <b>Type:</b> <a href="#">obj(constraint_mode)</a> * <b>Default:</b> "" <b>Edit:</b> No
<b>core_bbox</b>	
	Rectangle that defines the core row area <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No
<b>core_site</b>	
	The site object to use during floorplan creation <b>Type:</b> <a href="#">obj(site)</a> <b>Default:</b> "" <b>Edit:</b> No
<b>core_to_bottom</b>	
	Distance between core edge and its die/io box <b>Type:</b> <a href="#">coord</a> <b>Default:</b> "" <b>Edit:</b> No
<b>core_to_left</b>	
	Distance between core edge and its die/io box <b>Type:</b> <a href="#">coord</a> <b>Default:</b> "" <b>Edit:</b> No

core_to_right	<p>Distance between core edge and its die/io box  <b>Type:</b> coord  <b>Default:</b> ""  <b>Edit:</b> No</p>
core_to_top	<p>Distance between core edge and its die/io box  <b>Type:</b> coord  <b>Default:</b> ""  <b>Edit:</b> No</p>
delay_corners	<p>Returns the information about the delay corners in the design.  <b>Type:</b> obj(delay_corner)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
dont_touch	<p>This attribute defines the user preservation status of the design during optimization. This setting will apply to all insts within the design unless overridden at a lower level hinst or on the inst object itself. The dont_touch_effective attribute on each child inst and hinst will return the resolved value.</p> <p>Use 'help inst dont_touch' to see the enum value definitions.</p> <p><b>Type:</b> enum  <b>Enum Values:</b> none false true delete_ok const_prop_size_delete_ok const_prop_delete_ok size_delete_ok size_ok size_same_height_ok size_same_footprint_ok  <b>Default:</b> none  <b>Edit:</b> Yes</p>
dont_touch_effective	<p>This attribute defines the effective preservation status of the design during optimization from the dont_touch_sources values. If the read_only source is 'true' then the effective value for the hinst is 'true'. Otherwise, the user value has precedence.</p> <p>See help on inst dont_touch attribute for details on possible values.</p> <p><b>Type:</b> enum  <b>Enum Values:</b> none false true delete_ok const_prop_size_delete_ok const_prop_delete_ok size_delete_ok size_ok size_same_height_ok size_same_footprint_ok  <b>Default:</b> false  <b>Edit:</b> No</p>

dont_touch_sources	
	<p>Dictionary of {source &lt;value&gt;} pairs contributing to the dont_touch_effective attribute for this object :</p> <pre>{user &lt;value&gt;} {read_only &lt;value&gt;} user # This hinst dont_touch value read_only # The design is read_only (set_module_view -top_read_only true)</pre> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>
dont_use_cells	
	<p>List of cell names (wildcards supported) to disallow for this design during optimization. This can be overridden at a lower hinst level. Overrides any library dont_use values.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
dont_use_cells_effective	
	<p>The resolved list of all cell names to disallow during optimization for the design based on the library dont_use and the dont_use_cells and use_cells attributes of this design. The precedence is: use_cells of this hinst), then dont_use_cells of this design.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>
early_clk_cell_derate_factor	
	<p>Returns the derating factor for early clock paths specified through the set_timing_derate command with the -early parameter.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
early_data_cell_derate_factor	
	<p>Returns the derating factor for early paths specified through the set_timing_derate command with the -early parameter.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
early_fall_cell_check_derate_factor	

	Returns the early cell check derating factor specified through the set_timing_derate command with the -fall parameter. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
early_fall_clk_cell_derate_factor	Returns the early clock path derating factor specified through the set_timing_derate command with the -fall parameter. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
early_fall_data_cell_derate_factor	Returns the early data cell check derating factor specified through the set_timing_derate command with the -fall parameter. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
early_rise_cell_check_derate_factor	Returns the early cell check derating factor specified through the set_timing_derate command with the -rise and -cell_check parameter. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
early_rise_clk_cell_derate_factor	Returns the early clock cell check derating factor specified through the set_timing_derate command with the -rise parameter. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
early_rise_data_cell_derate_factor	

	Returns the early data cell check derating factor specified through the set_timing_derate command with the -rise parameter.  <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
gcell_grids	All the gcell_grid objects in the design.  <b>Type:</b> <a href="#">obj(gcell_grid)*</a> <b>Default:</b> "" <b>Edit:</b> No
gcells	The gcells for the current_design. The gcells are only created after global route has occurred.  <b>Type:</b> <a href="#">obj(gcell)*</a> <b>Default:</b> "" <b>Edit:</b> No
groups	List of groups  <b>Type:</b> <a href="#">obj(group)</a> <b>Default:</b> "" <b>Edit:</b> No
gui_lines	All the gui_line objects in the design.  <b>Type:</b> <a href="#">obj(gui_line)*</a> <b>Default:</b> "" <b>Edit:</b> No
gui_polygons	All the gui_polygon objects in the design.  <b>Type:</b> <a href="#">obj(gui_polygon)*</a> <b>Default:</b> "" <b>Edit:</b> No
gui_rects	

	All the gui_rect objects in the design. <b>Type:</b> <a href="#">obj(gui_rect)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>gui_shapes</b>	
	All the gui_shape objects in the design. <b>Type:</b> <a href="#">obj(gui_rect)* obj(gui_line)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>gui_texts</b>	
	All the gui_text objects in the design. <b>Type:</b> <a href="#">obj(gui_text)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>hinsts</b>	
	all hinsts inside this design <b>Type:</b> <a href="#">obj(hinst)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>hnets</b>	
	all hnets inside this design <b>Type:</b> <a href="#">obj(hnet)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>hpins</b>	
	all hpins inside this design <b>Type:</b> <a href="#">obj(hpin)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>insts</b>	
	all the logical insts inside this design. Does not include physical-insts. <b>Type:</b> <a href="#">obj(inst)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>io_bbox</b>	

	Rectangle that defines the IO area <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No
io_constraints	
	List of io_constraints. <b>Type:</b> <a href="#">obj(io_constraint)*</a> <b>Default:</b> "" <b>Edit:</b> No
is_clock_synthesized	
	Design status: Clock synthesized <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_core_to_io	
	Indicates whether core2* attributes are measured between core edge (core_bbox) and design boundary (box) or between core edge and io box edge (io_bbox) <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_detail_routed	
	Design status: detail routed, true if route_design was run. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_io_placed	
	Design status: Is IO placed <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_placed	
	Design status: Placed <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No

is_proto_model_committed	
	<p>Indicates that the design has committed FlexModels</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_proto_model_specified	
	<p>Indicates that the design has specified FlexModels</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_rc_extracted	
	<p>Design status: Parasitic extracted</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_routed	
	<p>Design status: routed. true if design has global routes from place_design/route_early_global or detail routes from route_design.</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_scan_optimized	
	<p>Design status: Scan optimized</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
late_cell_check_derate_factor	
	<p>Returns the derating factor for late paths specified through the set_timing_derate command with the -late parameter.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
late_clk_cell_derate_factor	

	<p>Returns the derating factor for late clock paths specified through the set_timing_derate command with the -late parameter.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
late_data_cell_derate_factor	<p>Returns the derating factor for late data paths specified through the set_timing_derate command with the -late parameter.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
late_fall_cell_check_derate_factor	<p>Returns the late cell check derating factor specified through the set_timing_derate command with the -fall parameter.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
late_fall_clk_cell_derate_factor	<p>Returns the late clock cell check derating factor specified through the set_timing_derate command with the -fall parameter.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
late_fall_data_cell_derate_factor	<p>Returns the late data cell check derating factor specified through the set_timing_derate command with the -fall parameter.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
late_rise_cell_check_derate_factor	

	<p>Returns the late cell check derating factor specified through the set_timing_derate command with the -rise parameter.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
late_rise_clk_cell_derate_factor	<p>Returns the late clock cell check derating factor specified through the set_timing_derate command with the -rise parameter.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
late_rise_data_cell_derate_factor	<p>Returns the late data cell check derating factor specified through the set_timing_derate command with the -rise parameter.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
local_hinsts	<p>List of hinsts in the current level of this design (e.g. from inside the design looking down at the hinsts at this level)</p> <p><b>Type:</b> obj(hinst)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
local_hnets	<p>List of hnets in the current level of this design (e.g. from inside the design looking down at the hnets at this level)</p> <p><b>Type:</b> obj(hnet)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
local_hpins	

	<p>List of hpins in the current level of this design (e.g. from inside the design looking down at the hpins of hinsts at this level)</p> <p><b>Type:</b> <a href="#">obj(hpin)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>local_insts</b>	
	<p>List of insts in the current level of this design (e.g. from inside the design looking down at the insts at this level)</p> <p><b>Type:</b> <a href="#">obj(inst)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>local_pins</b>	
	<p>List of pins in the current level of this design (e.g. from inside the design looking down at the pins of the insts at this level)</p> <p><b>Type:</b> <a href="#">obj(pin)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>markers</b>	
	<p>All the marker objects in the design.</p> <p><b>Type:</b> <a href="#">obj(marker)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>modules</b>	
	<p>all modules inside this design</p> <p><b>Type:</b> <a href="#">obj(module)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>name</b>	
	<p>Name of cell</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>net_groups</b>	

	List of net groups <b>Type:</b> <a href="#">obj(net_group)</a> * <b>Default:</b> "" <b>Edit:</b> No
nets	All the nets inside this design, including logical Verilog nets, physical-only nets, Verilog supply0/supply1, and Verilog 1'b0/1'b1 nets. <b>Type:</b> <a href="#">obj(net)</a> * <b>Default:</b> "" <b>Edit:</b> No
num_core_rows	Number of rows within the core area <b>Type:</b> <a href="#">int</a> <b>Default:</b> "" <b>Edit:</b> No
num_insts	Number of instances in the cell <b>Type:</b> <a href="#">int</a> <b>Default:</b> "" <b>Edit:</b> No
num_nets	Number of canonical (flat) nets in the cell <b>Type:</b> <a href="#">int</a> <b>Default:</b> "" <b>Edit:</b> No
num_pg_nets	Number of physical nets in the cell <b>Type:</b> <a href="#">int</a> <b>Default:</b> "" <b>Edit:</b> No
num_phys_insts	Number of physical instances in the cell <b>Type:</b> <a href="#">int</a> <b>Default:</b> "" <b>Edit:</b> No

oa_design_lib	Library name for the design in OpenAccess cellview <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
oa_design_view	View name for the design in OpenAccess cellview <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (design) <b>Default:</b> "" <b>Edit:</b> No
package_components	List of other chips in the package <b>Type:</b> obj(package_component)* <b>Default:</b> "" <b>Edit:</b> No
package_objects	List of objects in the package <b>Type:</b> obj(package_object)* <b>Default:</b> "" <b>Edit:</b> No
partitions	all partitions inside this design <b>Type:</b> obj(partition)* <b>Default:</b> "" <b>Edit:</b> No
pg_nets	

	<p>List of power ground nets in the design. This include physical-only PG nets, and Verilog supply0/supply1 nets. Note that Verilog nets assigned to 1'b0/1'b1 are returned by the nets attribute, not the pg_nets attribute.</p> <p><b>Type:</b> obj(net)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>pg_pins</b>	
	<p>All PG pins inside this design.</p> <p><b>Type:</b> obj(pg_pin)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>pg_ports</b>	
	<p>List of power/ground terminals in the cell</p> <p><b>Type:</b> obj(port)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>phys_insts</b>	
	<p>List of physical instances in the cell</p> <p><b>Type:</b> obj(inst)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>phys_ports</b>	
	<p>List of physical (unused) signal terminals in the cell</p> <p><b>Type:</b> obj(port)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>pin_blockages</b>	
	<p>List of partition pin blockage objects</p> <p><b>Type:</b> obj(pin_blockage)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>pin_groups</b>	
	<p>List of all the pin groups</p> <p><b>Type:</b> obj(pin_group)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

pin_guides	
	<p>List of all the pin guide object  <b>Type:</b> <a href="#">obj(pin_guide)</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
pin_to_corner_tracks	
	<p>List of distance constraints (in tracks) of pins from design/partition corners where the lower left corner is listed first and the remaining corners are listed in clockwise order.  <b>Type:</b> <a href="#">string</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
pins	
	<p>Short-cut for [get_db current_design .pins]  <b>Type:</b> <a href="#">obj(pin)</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
place_blockages	
	<p>List of placement blockages.  <b>Type:</b> <a href="#">obj(place_blockage)</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
port_shapes	
	<p>These are all the individual physical_pin shapes of the top-level ports including signal and PG ports.  <b>Type:</b> <a href="#">obj(port_shape)</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
ports	
	<p>ports of design. Does not include pg_ports, unless PG port is explicitly in the Verilog netlist.  <b>Type:</b> <a href="#">obj(port)</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
power_domains	

	List of power domains (pd) in the design <b>Type:</b> <a href="#">obj(power_domain)</a> * <b>Default:</b> "" <b>Edit:</b> No
power_modes	
	List of the power mode names in the design. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
read_db_design_name	
	The design name of the restored design. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
read_db_tool_name	
	The tool name save the restored design in current session. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
read_db_tool_version	
	The tool version number save the restored design in current session. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
read_only	

	<p>This attribute is set by set_module_view to identify if the top_level is read only or not. It means the partition cannot be optimized, and cells inside will not be moved. Setting this attribute will set the dont_touch_effective attribute on all insts and hinsts within the top level partition unless overridden at a lower level partition. It cannot be overridden by other hinst or inst values.</p> <p><b>Supported values:</b></p> <ul style="list-style-type: none"> <li>false: The top level is allowed to be optimized.</li> <li>true: The top level is read_only.</li> <li>none: No constraint.</li> </ul> <p><b>Type:</b> enum  <b>Enum Values:</b> none false true  <b>Default:</b> none  <b>Edit:</b> No</p>
resize_blockages	
	<p>List of resize_blockage objects</p> <p><b>Type:</b> obj(resize_blockage)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
route_blockages	
	<p>List of routing blockages</p> <p><b>Type:</b> obj(route_blockage)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
route_halo_bottom_layer	
	<p>The bottom layer for which routing halo will be created</p> <p><b>Type:</b> obj(layer)  <b>Default:</b> ""  <b>Edit:</b> No</p>
route_halo_to_boundary	
	<p>Specifies routing halo inside the design boundary (honored by the signal router). Only positive values are used and indicate the halo is inside of the design boundary.</p> <p><b>Type:</b> coord  <b>Default:</b> no_value  <b>Edit:</b> Yes</p>
route_halo_top_layer	

	<p>The top layer for which routing halo will be created  <b>Type:</b> <a href="#">obj(layer)</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
row_flip	<p>Specification of floorplan row creation, none = no flipping; first = first row is flipped, other rows alternate; second = first row is not flipped, other rows alternate  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> none second first  <b>Default:</b> ""  <b>Edit:</b> No</p>
row_spacing	<p>Specification of the floorplan row spacing  <b>Type:</b> <a href="#">coord</a>  <b>Default:</b> no_value  <b>Edit:</b> Yes</p>
row_spacing_type	<p>Indicates whether the rowSpacing is applied between each row (1) or between each pair of rows (2)  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> 0 1 2  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
rows	<p>List of rows  <b>Type:</b> <a href="#">obj(row)*</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
setup_views	<p>Returns the information about the setup analysis views in the design.  <b>Type:</b> <a href="#">obj(analysis_view)*</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
symmetry	

	<p>The allowed orientations for this design. This value only affects the SYMMETRY value written out by write_lef_abstract. none means r0 only (no SYMMETRY statement), x means ok to flip about X axis (SYMMETRY X), y means ok to flip about Y axis (SYMMETRY Y), xy means ok to flip about X or Y axis (SYMMETRY X Y), any means all orientations are allowed (SYMMETRY X Y R90). Modifications are not saved and are only valid for the current session.</p> <p><b>Type:</b> enum  <b>Enum Values:</b> none x y xy any  <b>Default:</b> any  <b>Edit:</b> Yes</p>
texts	
	<p>All the text objects in the design.</p> <p><b>Type:</b> obj(text)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
top_sdps	
	<p>List of all top level structured data path (sdp) objects.</p> <p><b>Type:</b> obj(sdp)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
track_patterns	
	<p>All the track_pattern objects in the design.</p> <p><b>Type:</b> obj(track_pattern)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
trim_grids	
	<p>All the trim_grid objects in the design from the LEF TRIMMETALTRACK statement.</p> <p><b>Type:</b> obj(trim_grid)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
use_cells	
	<p>List of cell names to allow for this design during optimization. This can be overridden at a lower hinst level. All lib_cells of each base_cell will be allowed. Overrides cells in the dont_use_cells list and any library dont_use values.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>

write_lec_dft_constraints	<p>This attribute is a TCL dict and holds the LEC dft pin constraints from the last LEC run by Genus. It is passed forward through write_design. The write_do_lec command will automatically include this constraints in the do file.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
write_lec_directory_naming_style	<p>The directory name where 'write_do_lec' will write verification files when the 'write_lec_files' attribute is 'true'. The directory will be created if it does not already exist, and will overwrite an existing directory of the same name. A %s in the string is replaced with the design name (e.g. it will overwrite the directory for the same design but not for a different design). A %d in the string is replaced with a unique integer to avoid overwriting any existing directory.</p> <p><b>Type:</b> string  <b>Default:</b> fv/invs/%s  <b>Edit:</b> Yes</p>

## flexible\_htree

### Parent Objects

[pin](#), [root](#)

### Definition

flexible\_htree

Attribute	Description
cts_flexible_htree_adjust_sink_grid_for_aspect_ratio	<p>If true adjust the sink grid for the aspect ratio of the sink grid box.          Valid values: boolean</p> <p><b>Type:</b> bool  <b>Default:</b> true  <b>Edit:</b> Yes</p>
cts_flexible_htree_final_cell	

	<p>The library cell to use for the H-tree sinks.          Valid values: string  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
<b>cts_flexible_htree_grid_step</b>	
	<p>The grid step used in flexible H-tree synthesis.  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> auto  <b>Edit:</b> No</p>
<b>cts_flexible_htree_hv_balance</b>	
	<p>Specifies whether horizontal and vertical wires can only be balanced against other wires of the same orientation (true), or whether any wire can be balanced against any other wire (false).          Valid values: true false  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> true  <b>Edit:</b> Yes</p>
<b>cts_flexible_htree_image_directory</b>	
	<p>Name of the directory to which images generated by the H-tree synthesis algorithm are written.          Valid values: string          Color coding of images:          White Unobstructed edges of the synthesis grid          Red Grid points that are blocked for trunk cell placement in all modules          Orange Grid points that are blocked for final cell placement in all modules          Red orange Grid points that are blocked for trunk and final cell placement in all modules          Yellow circle The grid point of the source          Yellow points Candidate grid points of H-tree sinks          Yellow rectangle The sink area containing target grid point candidates of H-sinks, adjusted to the synthesis grid          Brown If specified, the sink grid box adjusted to the synthesis grid          Green/blue The edges of the synthesized H-tree          Purple H-tree repeaters  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
<b>cts_flexible_htree_inverting</b>	

	<p>Specifies whether the flexible H-tree will invert its input.          Valid values: boolean  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes</p>
<b>cts_flexible_htree_layer_density</b>	
	<p>The assumed layer density used to compute the parasitics for timing estimates of H-tree nets during H-tree synthesis based on the non default rule for top nets.          Valid values: Any float in the range 0 to 1.  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 1  <b>Edit:</b> Yes</p>
<b>cts_flexible_htree_max_driver_distance</b>	
	<p>If specified, ignore DRVs and use the given value as the maximum length of the nets connecting H-tree drivers.          Valid values: float  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> auto  <b>Edit:</b> Yes</p>
<b>cts_flexible_htree_max_root_distance</b>	
	<p>If specified, ignore DRVs and use the given value as the maximum length of the net connecting the root and the first driver of the H-tree. This value overrides the attribute <code>cts_max_driver_distance</code> of this net and can only be specified if <code>-max_driver_distance</code> is also specified.          Valid values: float  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> auto  <b>Edit:</b> Yes</p>
<b>cts_flexible_htree_mode</b>	
	<p>The driver insertion mode for the H-tree.          If set to 'drv', the algorithm inserts drivers to avoid DRVs. It also minimizes the insertion delay of the H-tree if the power weight is less than 1.0.          If set to 'distance', the attributes '<code>cts_max_driver_distance</code>' and '<code>cts_max_root_distance</code>' determine the maximum net lengths allowed. Transitions and delays are not computed in this case.          Valid values: drv distance branch_point  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes</p>

cts\_flexible\_htree OMIT\_symmetry

Controls the omission of symmetry features to balance a flexible H-tree.  
Symmetry drivers are drivers that are added to balance pin capacitances at branch points. For example, if buffer pairs are inserted at branch points, one of these buffers may not drive any fanout and is inserted to match other buffer pairs at the same level of the flexible H-tree. Omitting symmetry drivers can reduce the power of the H-tree but increase its skew.

Similarly, symmetry branches are branches that are needed to balance the wire load at branch points. They are added to match other branchpoints at the same level of the flexible H-tree.

By default, symmetry branches and drivers are added.

Possible values for this attribute:

false Add symmetry branches and drivers

true Omit both symmetry drivers and branches

drivers Omit symmetry drivers

branches Omit symmetry branches

{drivers branches} Omit both symmetry drivers and branches

{ } Add symmetry branches and drivers

**Type:** string

**Default:** auto

**Edit:** Yes

cts\_flexible\_htree\_partition\_boundary\_inverting

Specifies whether the clock phase is inverting with regard to the root pin when entering partitions.

Valid values: boolean

**Type:** bool

**Default:** false

**Edit:** Yes

cts\_flexible\_htree\_partition\_groups

	<p>The groups in which partition are clustered in channelless designs. Nested lists imply allowed crossings between groups. Each group has zero or one input port and each partition must only be specified once.</p> <p>Optionally, a maximum pre-route net length from the boundary of a partition group can be specified. This argument must be specified as the second parameter of a nested partition group.</p> <p>Optionally, the next argument specifies the clock phase when entering the partition group in relation to the root pin of the H-tree. Allowed values are 'inverting' and 'non-inverting'. If no value is specified, the clock phase is unconstrained. The clock phase is unconstrained when crossing the boundaries of partitions within the same group. All specified clock phases must be either inverting or non-inverting.</p> <p>Example:</p> <pre> {{A} {{C D} 50 non_inverting {{E F}} {{G}}}}</pre> <ul style="list-style-type: none"> <li>- The H-tree starts in partition A and descends into group C/D.</li> <li>- From partition group C/D, the tree descends into groups E/F and G.</li> <li>- Any clustering of sinks inside the C/D and E/F groups are allowed, potentially crossing internal partition boundaries several times.</li> <li>- Partition A has no clock input port and one clock output port</li> <li>- Partition group C/D has one clock input port and two clock output ports</li> <li>- Partition group E/F and G have one clock input port and no clock output port</li> <li>- The maximum net length from the entry point into partition group C/D is 50um (pre-route)</li> <li>- The clock phase is non-inverting when entering partition group C/D. The clock phase is unconstrained when entering other partition groups.</li> </ul> <p>Valid values: string</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
<b>cts_flexible_htree_power_weight</b>	
	<p>The power versus insertion delay trade-off. The value specifies the weight that is put on the optimization of power related attributes , in particular the number of repeaters in the H-tree, during the synthesis of a flexible H-tree.</p> <p>Valid values: Any float in the range 0 to 1.</p> <p><b>Type:</b> double  <b>Default:</b> 1  <b>Edit:</b> Yes</p>
<b>cts_flexible_htree_root</b>	
	<p>The pin under which the H-tree is created. This pin must be part of a clock tree at the time of synthesis.</p> <p>Valid values: pin</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>

cts_flexible_htree_sink_grid	
	<p>Specifies the columns and rows of a grid of H-tree sinks.  Valid values: {columns rows}</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
cts_flexible_htree_sink_grid_box	
	<p>The box describing the area that the grid of H-tree sinks should cover. This attribute only has an effect if the cts_flexible_htree_sink_grid attribute of the flexible H-tree is set.  Valid values: {xmin ymin xmax ymax}</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
cts_flexible_htree_sink_grid_exclusion_areas	
	<p>Boxes describing zones that should not be covered by the grid of H-tree sinks. This attribute only has an effect if the cts_flexible_htree_sink_grid attribute of the flexible H-tree is set.  Valid values: list {xmin ymin xmax ymax}</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
cts_flexible_htree_sink_grid_sink_area	
	<p>The approximate size of the rectangle describing valid locations for final cells (given by -final_cell) per H-tree sink in the grid. This attribute only has an effect if the cts_flexible_htree_sink_grid attribute of the flexible H-tree is set.  Valid values: {width height}</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
cts_flexible_htree_sink_instance_prefix	
	<p>Prefix used for instance names of final cells (given by -final_cell). The name of the cell will be &lt;prefix&gt;_&lt;htree_name&gt;_&lt;id&gt;, where id is a running index.  Valid values: string</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
cts_flexible_htree_sinks	

	<p>Specifies H-tree sinks as approximate rectangular areas for locations of final cells (given by -final_cell) or pins to wire to.</p> <p>Valid values: list {pin   {xmin ymin xmax ymax}}</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>cts_flexible_htree_stop_at_sdc_clock_roots</b>	
	<p>If specified, stop searching for parts of the clock tree through SDC clock roots when defining generated clock trees for H-tree sinks.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>cts_flexible_htree_trunk_cell</b>	
	<p>The library cell to use inside the H-tree.</p> <p>Valid values: string</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>insts</b>	
	<p>instances in the clock tree</p> <p><b>Type:</b> <a href="#">obj(inst)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>name</b>	
	<p>name of flexible_htree</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>nets</b>	
	<p>nets in the clock tree</p> <p><b>Type:</b> <a href="#">obj(net)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>obj_type</b>	

	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> enum (flexible_htree) <b>Default:</b> "" <b>Edit:</b> No</p>
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# flow

## Parent Objects

[root](#)

## Definition

flow

Attribute	Description
end_steps	<p>List of steps for the flow</p> <p><b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes</p>
feature_values	<p>Feature values for instances of this flow.</p> <p><b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes</p>
features	<p>Features defined for this flow.</p> <p><b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes</p>
name	<p>The name of the flow</p> <p><b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes</p>

**Stylus Common UI Database Object Information**  
Database Objects--flow

obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (flow) <b>Default:</b> "" <b>Edit:</b> No
owner	Owner of this flow <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes
run_count	Number of times this flow has been run. <b>Type:</b> string <b>Default:</b> 0 <b>Edit:</b> Yes
skip_metric	Do not create a metric snapshot for the flow <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes
start_steps	List of steps for the flow <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes
steps	List of steps for the flow <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes
tool	The tool to run this flow <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes

## tool\_options

The tool options for the tool for this flow

**Type:** [string](#)

**Default:** ""

**Edit:** Yes

# flow\_step

## Parent Objects

[root](#)

## Definition

flow step

Attribute	Description
begin_tcl	<p>The Tcl body to run at the start of the step</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
body_tcl	<p>The Tcl body of the step. The initial value for this attribute is provided by the create_flow_step command.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
categories	<p>Metric categories to calculate for this flow step.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
check_tcl	

**Stylus Common UI Database Object Information**  
Database Objects--flow\_step

	A block of Tcl to run to perform step-specific static checks. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes
end_steps	
	A list of flows or flow_steps that will be run at the end of this step. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes
end_tcl	
	The Tcl body to run at the end of the step. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes
exclude_time_metric	
	Do not include cpu and wall time of this step in any parent steps <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes
feature_values	
	Feature values for instances of this flow step. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes
features	
	Features defined for this flow step. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes
name	
	The name of the step <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes
obj_type	

	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (flow_step)</a> <b>Default:</b> "" <b>Edit:</b> No
owner	
	Owner of this step. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes
run_count	
	An integer indicating how many times the step has been run. The value is initially zero, so it may be used as a Boolean indicating that the step has been run at all. <b>Type:</b> <a href="#">int</a> <b>Default:</b> no_value <b>Edit:</b> Yes
skip_db	
	Do not auto-save a db at the end of this step <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes
skip_metric	
	Do not auto-save a db at the end of this step <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
start_steps	
	A list of flows or flow_steps that will be run at the start of this step. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes
status	
	Flow step status <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes

# foreign\_cell

## Parent Objects

[base\\_cell](#), [root](#)

## Definition

LEF MACRO FOREIGN information

Attribute	Description
name	Name of the foreign cell (can be the same as the master if only a shift/offset is required) <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (foreign_cell)</a> <b>Default:</b> "" <b>Edit:</b> No
orient	Orientation of the foreign cell (non-R0 values are only allowed if the cell name is different from the master cell) <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> r0 r90 r180 r270 mx mx90 my my90 <b>Default:</b> "" <b>Edit:</b> No
point	Location (offset) of the foreign cell <b>Type:</b> <a href="#">point</a> <b>Default:</b> "" <b>Edit:</b> No

# gcell\_grid

## Parent Objects

[design](#), [root](#)

## Definition

Equivalent to DEF GCELLGRID statements

Attribute	Description
direction	<p>Specifies the location and direction of the first grid defined. x indicates vertical lines; y indicates horizontal lines.</p> <p><b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> y x <b>Default:</b> "" <b>Edit:</b> No</p>
num_grids	<p>Specifies the number of grid lines to create (number of rows or columns is numGrids-1)</p> <p><b>Type:</b> <a href="#">int</a> <b>Default:</b> "" <b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (gcell_grid)</a> <b>Default:</b> "" <b>Edit:</b> No</p>
start	<p>Specifies the coordinate of the first line</p> <p><b>Type:</b> <a href="#">coord</a> <b>Default:</b> "" <b>Edit:</b> No</p>
step	

	Specifies the spacing between the grids <b>Type:</b> <a href="#">coord</a> <b>Default:</b> "" <b>Edit:</b> No
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# group

## Parent Objects

[hinst](#), [inst](#), [design](#), [power\\_domain](#), [root](#),

## Definition

group of hinsts, insts, or groups

Attribute	Description
area	Area of the group as defined by the LEF MACRO SIZE or OVERLAP information <b>Type:</b> <a href="#">area</a> <b>Default:</b> "" <b>Edit:</b> No
constraint_type	Constraint type for the group <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> guide region fence cluster none <b>Default:</b> "" <b>Edit:</b> Yes
density	Group density (legal range: 0.0-1.0) <b>Type:</b> <a href="#">double</a> <b>Default:</b> no_value <b>Edit:</b> Yes
exclusive_group_gap	

	<p>This is the gap should be maintained between exclusive_groups (per safety island groups). The value is measured in microns. It can be set by command create_exclusive_groups -gap. It is only valid when the group's constraint_type is region or fence.</p> <p><b>Type:</b> coord  <b>Default:</b> 5  <b>Edit:</b> Yes</p>
exclusive_groups	
	<p>This attribute specifies a list of groups that are exclusive of this group. It can be used to implement safety islands in automotive application designs.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
is_floating	
	<p>Only affects groups with .constraint_type = fence or region. If true, the global placer can move the fence or region. The .rects value must also be set, and is currently restricted to a single rect. The global placer will not change the size of the rect, but may move it.</p> <p><b>Type:</b> bool  <b>Default:</b> false  <b>Edit:</b> Yes</p>
members	
	<p>List of group's members</p> <p><b>Type:</b> obj(hinst)* obj(inst)* obj(group)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
name	
	<p>Name of group</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>
obj_type	
	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> enum (group)  <b>Default:</b> ""  <b>Edit:</b> No</p>
parent	

	The parent group if is a sub-group <b>Type:</b> <a href="#">obj(group)</a> <b>Default:</b> "" <b>Edit:</b> No
<b>power_domain</b>	
	The Power Domain (if group is a power domain) <b>Type:</b> <a href="#">obj(power_domain)</a> <b>Default:</b> "" <b>Edit:</b> No
<b>rects</b>	
	List of non-overlapping rectangles that defines the shape of the group <b>Type:</b> <a href="#">rect*</a> <b>Default:</b> "" <b>Edit:</b> No

## gui\_line

### Parent Objects

[design](#), [root](#)

### Definition

A line that can be displayed on the GUI, and is not output to DEF.

Attribute	Description
arrow	Draw arrow in the middle of the line with direction from start point to end point. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
gui_layer_name	

	Normally a GUI-only layer name that is not a tech-file layer. If the name is the same as a tech-file layer, it will be drawn on the GUI with other shapes on that layer, but it will not be output to DEF. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (gui_line)</a> <b>Default:</b> "" <b>Edit:</b> No
pixel_width	Number of pixels in the border of the object. <b>Type:</b> <a href="#">int</a> <b>Default:</b> "" <b>Edit:</b> No
points	2 points for line <b>Type:</b> <a href="#">point*</a> <b>Default:</b> "" <b>Edit:</b> No

## gui\_polygon

### Parent Objects

[design](#), [root](#)

### Definition

The polygon shape that can be displayed on the GUI, and is not output to DEF.

Attribute	Description
gui_layer_name	

	Normally a GUI-only layer name that is not a tech-file layer. If the name is the same as a tech-file layer, it will be drawn on the GUI with other shapes on that layer, but it will not be output to DEF. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (gui_polygon)</a> <b>Default:</b> "" <b>Edit:</b> No
pixel_width	Number of pixels in the border of the object. <b>Type:</b> <a href="#">int</a> <b>Default:</b> "" <b>Edit:</b> No
points	point list for poly <b>Type:</b> <a href="#">point*</a> <b>Default:</b> "" <b>Edit:</b> No

## gui\_rect

### Parent Objects

[design](#), [root](#)

### Definition

A rect that can be displayed on the GUI, and is not output to DEF.

Attribute	Description
gui_layer_name	

	Normally a GUI-only layer name that is not a tech-file layer. If the name is the same as a tech-file layer, it will be drawn on the GUI with other shapes on that layer, but it will not be output to DEF. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (gui_rect)</a> <b>Default:</b> "" <b>Edit:</b> No
pixel_width	Number of pixels in the border of the object. <b>Type:</b> <a href="#">int</a> <b>Default:</b> "" <b>Edit:</b> No
rect	Rectangle that defines the gui_rect shape. <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No

## gui\_text

### Parent Objects

[design](#), [root](#)

### Definition

A text that can be displayed on the GUI, and is not output to DEF.

Attribute	Description
gui_layer_name	

	GUI layer name <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
height	
	Text height <b>Type:</b> <a href="#">coord</a> <b>Default:</b> "" <b>Edit:</b> No
label	
	Text string <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
location	
	Text location (lower left) <b>Type:</b> <a href="#">point</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	
	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (gui_text)</a> <b>Default:</b> "" <b>Edit:</b> No

## hinst

### Parent Objects

[partition](#), [inst](#), [module](#), [design](#), [hpin](#), [boundary](#), [root](#), [group](#), [hport](#)

### Definition

Hierarchical instance

Attribute	Description
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area	The area of all the insts contained inside this hinst and below it. <b>Type:</b> <a href="#">area</a> <b>Default:</b> "" <b>Edit:</b> No
base_name	The name at the base of a hierarchical name. So the base_name of i1/i2/i3 is i3. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
bbox	Bounding box of all the insts inside this hinst. <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No
boundary	The placement boundary (e.g. fence, region, group, cluster) for this hinst if it exists. <b>Type:</b> <a href="#">obj(boundary)</a> <b>Default:</b> "" <b>Edit:</b> No
dont_touch	This attribute defines the user preservation status of the hinst during optimization. Setting this attribute will set the dont_touch attribute on the parent module of this hinst and all hinsts of the same module. This setting will apply to all insts within the hinst unless overridden at a lower level hinst or on the inst object itself. The dont_touch_effective attribute on each child inst and hinst will return the resolved value. Use 'help inst dont_touch' to see the enum value definitions but note that map_size_ok is only allowed at the instance level. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> none false true delete_ok const_prop_size_delete_ok const_prop_delete_ok size_delete_ok size_ok size_same_height_ok size_same_footprint_ok <b>Default:</b> none <b>Edit:</b> Yes
dont_touch_effective	

	<p>This attribute defines the effective preservation status of this hinst during optimization from the dont_touch_sources values. If the partition source is 'true' or the ilm source is 'true', then the effective value for the hinst is 'true'. Otherwise, the user value has precedence. If the user value is false, then the parent value is returned.</p> <p>See help on inst dont_touch attribute for details on possible values.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> none false true delete_ok const_prop_size_delete_ok const_prop_delete_ok size_delete_ok size_ok size_same_height_ok size_same_footprint_ok</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> No</p>
	<p>dont_touch_hports</p>
	<p>This attribute defines the user preservation status for the hports of this hinst during optimization.</p> <p><b>Supported values:</b></p> <ul style="list-style-type: none"> <li>none: Unconstrained</li> <li>false: Can add/remove ports</li> <li>true: Cannot add/remove ports</li> <li>delete_ok: Can delete ports (if they have no fanout)</li> <li>add_ok: We cannot delete, or change the polarity or any hport but can add or duplicate hports</li> <li>invert_ok: We cannot delete, duplicate, or add but can change the polarity of any hport</li> <li>add_invert_ok: We cannot delete any hport but can add, duplicate, and change the polarity</li> </ul> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> none false true delete_ok add_ok invert_ok add_invert_ok</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p>
	<p>dont_touch_sources</p>
	<p>Dictionary of {source &lt;value&gt;} pairs contributing to the dont_touch_effective attribute for this object :</p> <pre>{user &lt;value&gt;} {parent &lt;value&gt;} {read_only_effective &lt;value&gt;} user # This hinst dont_touch value parent # The effective dont_touch value from an hinst above (the closest hinst above that is not false) read_only_effective # True when this hinst is read_only because it is an ilm or set_module_view set it or a parent partition to read_only. Local read_only value overrides parent read_only value</pre> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p>dont_use_cells</p>

	<p>List of cell names (wildcards supported) to disallow for this hinst during optimization. Setting on an hinst sets the attribute on the module of the hinst (setting on the hinst is just for convenience). If a cell is added to this list that is already in the .use_cells list, it will be removed from the .use_cells list so that the lists are non-overlapping.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>dont_use_cells_effective</b>	
	<p>The resolved list of all cell names to disallow during optimization for this hinst, based on the library dont_use and the dont_use_cells and use_cells attributes of this hinst or the closest parent hinst with a non-empty list. The precedence is: union of the use_cells of this hinst (or closest parent if empty), then dont_use_cells of this hinst (or closest parent if empty), then the library dont_use setting. When there are multiple hinsts that share the same module, the dont_touch_effective is calculated for the master hinst and the other (clone) hinsts inherit.</p> <p>A cell C is in the don't use cell effective list for a hinst H if and only if.</p> <ol style="list-style-type: none"> <li>(1) Walk from the hinst H up in the parent hierarchy (including H) to find the closest parent hinst where C is referred to in use cell list or don't use cell list.</li> <li>(2) If such a hinst is found and if it occurs as use cell in hinst then it is not in the effective don't use list. If it occurs in the don't_use cell list of hinst then it is in the effective don't use list.</li> <li>(3) If such a hinst is not found the library don't use determines if the cell is in the effective don't use list or not.</li> </ol> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>escaped_name</b>	
	<p>The full hierarchical name including escaped chars (if any). It follows DEF escaping syntax, so bus-bit chars [], or a hierarchy char \ that is not a bus-bit or hierarchy char has a \ in front of it. So i1/i2 is a two-level hierarchical name while i1\i2 is single level name, and a[0] is a bus-bit, while a\[0\] is a scalar.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>group</b>	
	<p>The parent group</p> <p><b>Type:</b> <a href="#">obj(group)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>hinsts</b>	

	<p>List of all the hinsts at the current level and below this hinst  <b>Type:</b> <a href="#">obj(hinst)</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>hnets</b>	
	<p>List of all the hnets at the current level and below this hinst  <b>Type:</b> <a href="#">obj(hnet)</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>hpins</b>	
	<p>List of all the hpins at the current level and below this hinst  <b>Type:</b> <a href="#">obj(hpin)</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>hports</b>	
	<p>List of all the hports of this hinst (e.g. from inside the hinst looking up at the hinst boundary).  <b>Type:</b> <a href="#">obj(hport)</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>ilm_inst</b>	
	<p>Specifies the inst object of this ilm when it is under unflatten view. This attribute is only valid when the ilm is under flatten view.  <b>Type:</b> <a href="#">obj(inst)</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>insts</b>	
	<p>List of all the insts at the current level and below this hinst  <b>Type:</b> <a href="#">obj(inst)</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>is_ilm</b>	

	<p>This attribute is true if the hinst is an ILM. It will affect the read_only_effective and dont_touch_effective of this hinst and all hinsts within it, as well as the dont_touch_effective of all insts within it. It cannot be overridden by other hinst or inst values.</p> <p><b>Type:</b> <code>bool</code>  <b>Default:</b> false  <b>Edit:</b> No</p>
<b>local_hinsts</b>	
	<p>List of hinsts in the current level of this hinst (e.g. from inside the hinst looking down at the hinsts at this level)</p> <p><b>Type:</b> <code>obj(hinst)*</code>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>local_hnets</b>	
	<p>List of hnets in the current level of this hinst (e.g. from inside the hinst looking down at the hnets at this level)</p> <p><b>Type:</b> <code>obj(hnet)*</code>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>local_hpins</b>	
	<p>List of hpins in the current level of this hinst (e.g. from inside the hinst looking down at the hpins of hinsts at this level)</p> <p><b>Type:</b> <code>obj(hpin)*</code>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>local_insts</b>	
	<p>List of insts in the current level of this hinst (e.g. from inside the hinst looking down at the insts at this level)</p> <p><b>Type:</b> <code>obj(inst)*</code>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>local_pins</b>	
	<p>List of pins in the current level of this hinst (e.g. from inside the hinst looking down at the pins of the insts at this level)</p> <p><b>Type:</b> <code>obj(pin)*</code>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>module</b>	

	<p>The module cell that corresponds to the hInst</p> <p><b>Type:</b> <a href="#">obj(module)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
name	<p>The same as .escaped_name without any \ escape chars. This name is commonly used to avoid problems with \ escape chars in Tcl scripts unless you carefully use list operators. Like SDC commands, 'get_db insts i1/i2' will first try to match i1/i2, and if not found then match i1Vi2 so that flattening hierarchical names (e.g. with ungroup) does not require changing the names in Tcl scripts.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (hinst)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
parent	<p>The parent of the hinst, which is either another hinst, or the design object.</p> <p><b>Type:</b> <a href="#">obj(hinst)* obj(design)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
partition	<p>The partition of hInst</p> <p><b>Type:</b> <a href="#">obj(partition)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
power_domain	<p>Power domain of the hierarchical inst if in a group</p> <p><b>Type:</b> <a href="#">obj(power_domain)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
power_dynamic	

	The sum of the power_dynamic value for all the insts inside this hinst. A value of no_value is treated as 0. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>power_internal</b>	
	The sum of the power_internal value for all the insts inside this hinst. A value of no_value is treated as 0. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>power_leakage</b>	
	The sum of the power_leakage value for all the insts inside this hinst. A value of no_value is treated as 0. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>power_switching</b>	
	The sum of the power_switching value for all the insts inside this hinst. A value of no_value is treated as 0. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>power_toggle_rate</b>	
	The average of the power_toggle_rate value for all the insts inside this <hinst/design>. A value of no_value is treated as 0 <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>power_total</b>	
	The sum of the power_total value for all the insts inside this hinst. A value of no_value is treated as 0. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>read_only</b>	

	<p>This attribute is true if the hinst is a read_only. This is set by the set_module_view command. When true, this hinst cannot be optimized and cells inside will not be moved. This attribute will affect the dont_touch_effective and place_status_effective attributes on all insts and hinsts within this hinst. It cannot be overridden by other hinst or inst values.</p> <p><b>Supported values:</b></p> <ul style="list-style-type: none"> <li>false: This hinst is allowed to be optimized</li> <li>true: The hinst read_only due to partition or ILM status</li> <li>none: No constraint.</li> </ul> <p><b>Type:</b> enum  <b>Enum Values:</b> none false true  <b>Default:</b> none  <b>Edit:</b> No</p>
read_only_effective	<p>This attribute defines the read_only status of this hinst. This can be true when the local .read_only attribute is true or if a parent .read_only attribute is true. The hinst cannot be optimized and cells inside will not be moved.</p> <p><b>Supported values:</b></p> <ul style="list-style-type: none"> <li>false: This hinst is allowed to be optimized</li> <li>true: The hinst read_only due to local or parent read_only partition</li> </ul> <p><b>Type:</b> bool  <b>Default:</b> false  <b>Edit:</b> No</p>
use_cells	<p>List of base_cell names to allow for this hinst during optimization. Setting on an hinst sets the attribute on the module of the hinst (setting on the hinst is just for convenience). All lib_cells of each base_cell will be allowed. If a cell is added to this list that is already in the .dont_use_cells list, it will be removed from the .dont_use_cells list so that the lists are non-overlapping.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>

## hnet

### Parent Objects

[hinst](#), [design](#), [hpin](#), [pin](#), [net](#), [root](#), [hport](#), [port](#)

## Definition

Hierarchical net

Attribute	Description
base_name	<p>The name at the base of a hierarchical name. So the base_name of i1/i2/i3 is i3.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>
constant	<p>Returns if this hnet has a constant logic value in the Verilog (supply0/supply1 or assigned 1'b0/1'b1). If it is no_constant, and it is connected to a net, you must check the net .constant value to see if the net is constant for other reasons. A supply0/1 hnet will cause its net to have .use = power or ground.</p> <p><b>Type:</b> enum  <b>Enum Values:</b> 0 1 no_constant  <b>Default:</b> ""  <b>Edit:</b> No</p>
dont_touch	<p>This attribute defines the preservation status of an hnet during optimization. Setting this will preserve all connections on the hnet at the level of hierarchy where the hnet exists (i.e. will stop at the hpins and hports connected to this hnet).</p> <p><b>Supported values:</b>      false: Unconstrained      true: Cannot touch      delete_ok: Can delete (if net has no sinks)</p> <p><b>Type:</b> enum  <b>Enum Values:</b> false true delete_ok  <b>Default:</b> false  <b>Edit:</b> Yes</p>
drivers	<p>local to this hinst: pins, hpins that are output or bider, and hports. Ports that are input or bidir</p> <p><b>Type:</b> obj(pin)* obj(hpin)* obj(port)* obj(hport)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
escaped_name	

	<p>The full hierarchical name including escaped chars (if any). It follows DEF escaping syntax, so bus-bit chars [], or a hierarchy char \ that is not a bus-bit or hierarchy char has a \ in front of it. So i1/i2 is a two-level hierarchical name while i1\i2 is single level name, and a[0] is a bus-bit, while a\[0\] is a scalar.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
loads	
	<p>local to this hinst: pins, hpins that are input or bider, and hports. Ports that are output or bidir</p> <p><b>Type:</b> <a href="#">obj(pin)* obj(hpin)* obj(port)* obj(hport)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
name	
	<p>The same as .escaped_name without any \ escape chars. This name is commonly used to avoid problems with \ escape chars in Tcl scripts unless you carefully use list operators. Like SDC commands, 'get_db insts i1/i2' will first try to match i1/i2, and if not found then match i1\i2 so that flattening hierarchical names (e.g. with ungroup) does not require changing the names in Tcl scripts.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
net	
	<p>canonical (flat) net associated with the hierarchical net</p> <p><b>Type:</b> <a href="#">obj(net)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
num_drivers	
	<p>number of local drivers</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
num_loads	
	<p>number of local loads</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obj_type	

	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (hnet) <b>Default:</b> "" <b>Edit:</b> No
--	---

# hpin

## Parent Objects

[arc](#), [partition](#), [hinst](#), [design](#), [hnet](#), [clock](#), [root](#), [hport](#)

## Definition

Hierarchical instance pin

Attribute	Description
base_name	<p>The name at the base of a hierarchical name. So the base_name of i1/i2/i3 is i3.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>
constant	<p>Returns if this hpin has a constant logic value due to a 1'b0 or 1'b1 asserted directly on the hpin in the Verilog. If it is no_constant, and it is connected to a net, you must check the net .constant value to see if the net is constant for other reasons.</p> <p><b>Type:</b> enum  <b>Enum Values:</b> 0 1 no_constant  <b>Default:</b> ""  <b>Edit:</b> No</p>
depth	<p>Depth constraint of the hpin in microns. The edit_pin command can be used to set it. It is only valid for partition .hpins affected by pin assignment commands.</p> <p><b>Type:</b> coord  <b>Default:</b> ""  <b>Edit:</b> No</p>
direction	

	<p>Direction of pin.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> internal in out inout</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
dont_touch	<p>The preservation status of an hpin during optimization. A preserved hpin means the logical function of the hpin must be preserved to maintain a simulation or test-point hpin in the netlist. However, the name does not need to be preserved.</p> <p><b>Supported values:</b></p> <ul style="list-style-type: none"> <li>false: Unconstrained</li> <li>true: Cannot add/remove ports</li> <li>delete_ok: Can delete ports (if they have no fanout)</li> <li>add_ok: We cannot delete, or change the polarity or any hport but can add or duplicate hports</li> <li>invert_ok: We cannot delete, duplicate, or add but can change the polarity of any hport</li> <li>add_invert_ok: We cannot delete any hport but can add, duplicate, and change the polarity</li> <li>none: No user setting; will inherit from the module/hinst</li> </ul> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> none false true delete_ok add_ok invert_ok add_invert_ok</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p>
dont_touch_effective	<p>This attribute defines the effective preservation status of an hpin during optimization based on the .dont_touch_sources. If the local hpin .dont_touch is not "none", it will be used. Otherwise, the hinst .dont_touch_effective is used if not "none" or "false". If not, then the hinst .dont_touch_hports is used.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> none false true delete_ok add_ok invert_ok add_invert_ok</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> No</p>
dont_touch_sources	

	<p>Dictionary of {source value&gt;} pairs contributing to the dont_touch_effective attribute for this object : {user &lt;value&gt;} {power_intent &lt;value&gt;}{hinst_dont_touch_hports &lt;value&gt;}{hinst_dont_touch_effective}.</p> <p>user # This pins dont_touch value          power_intent # Value set by committing UPF/CPF          hinst_dont_touch_effective # The hinst.dont_touch_effective value          hinst_dont_touch_hports # The hinst.dont_touch_hports value</p> <p><b>Type:</b> string  <b>Default:</b> {user none} {power_intent false}  <b>Edit:</b> No</p>
escaped_name	<p>The full hierarchical name including escaped chars (if any). It follows DEF escaping syntax, so bus-bit chars [], or a hierarchy char \ that is not a bus-bit or hierarchy char has a \ in front of it. So i1/i2 is a two-level hierarchical name while i1\i2 is single level name, and a[0] is a bus-bit, while a\[0\] is a scalar.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>
hinst	<p>The hinst for this hpin.</p> <p><b>Type:</b> obj(hinst)  <b>Default:</b> ""  <b>Edit:</b> No</p>
hnet	<p>The hnet connected to this hpin (above the hinst for this hpin).</p> <p><b>Type:</b> obj(hnet)  <b>Default:</b> ""  <b>Edit:</b> No</p>
hport	<p>The hport is the internal view of this hpin from inside the hinst.</p> <p><b>Type:</b> obj(hport)  <b>Default:</b> ""  <b>Edit:</b> No</p>
location	

	<p>Location of the hpin. The edit_pin command can be used to change a partition .hpins location.</p> <p><b>Type:</b> point  <b>Default:</b> ""  <b>Edit:</b> No</p>
name	<p>The same as .escaped_name without any \ escape chars. This name is commonly used to avoid problems with \ escape chars in Tcl scripts unless you carefully use list operators. Like SDC commands, 'get_db insts i1/i2' will first try to match i1/i2, and if not found then match i1Vi2 so that flattening hierarchical names (e.g. with ungroup) does not require changing the names in Tcl scripts.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>
net	<p>The canonical (flat) net attached to this hpin.</p> <p><b>Type:</b> obj(net)  <b>Default:</b> ""  <b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> enum (hpin)  <b>Default:</b> ""  <b>Edit:</b> No</p>
place_status	<p>The place_status of the hpin. This is only valid for partition .hpins affected by pin assignment commands.</p> <p><b>Type:</b> enum  <b>Enum Values:</b> unplaced placed fixed cover  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
side	<p>Side constraint of the hpin. The edit_pin command can be used to set this value. It is only valid for partition .hpins affected by pin assignment commands.</p> <p><b>Type:</b> enum  <b>Enum Values:</b> north west south east up none  <b>Default:</b> ""  <b>Edit:</b> No</p>

## width

	Width constraint of the hpin in microns. The edit_pin command can be used to set it. This is only valid for partition .hpins affected by pin assignment commands. <b>Type:</b> <a href="#">coord</a> <b>Default:</b> "" <b>Edit:</b> No
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# hport

## Parent Objects

[arc](#), [hinst](#), [hnet](#), [hpin](#), [clock](#), [root](#)

## Definition

hierarchical terminal

Attribute	Description
base_name	The name without the leading hinst hierarchy (e.g. p3 for h1/h2/p3). <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
direction	Direction of pin. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> internal in out inout <b>Default:</b> "" <b>Edit:</b> No
escaped_name	The escaped name of the hport. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
hinst	

	The hinst for this hport. <b>Type:</b> <a href="#">obj(hinst)</a> <b>Default:</b> "" <b>Edit:</b> No
hnet	The hnet connected to this hport (inside the hinst of this hport). <b>Type:</b> <a href="#">obj(hnet)</a> <b>Default:</b> "" <b>Edit:</b> No
hpin	The hpin is the external view from outside the hinst for this hport. <b>Type:</b> <a href="#">obj(hpin)</a> <b>Default:</b> "" <b>Edit:</b> No
name	The fully qualified path name of the hport (e.g. h1/h2/p3). <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (hport)</a> <b>Default:</b> "" <b>Edit:</b> No

## inst

### Parent Objects

[flexible\\_htree](#), [io\\_constraint](#), [place\\_blockage](#), [group](#), [hinst](#), [sdp](#), [design](#), [partition](#), [clock\\_tree](#), [root](#), [pg\\_pin](#), [route\\_blockage](#), [pin](#), [inst\\_obs\\_shape](#)

### Definition

instance

Attribute	Description
arcs	<p>Returns a list of arc objects that are associated with this inst</p> <p><b>Type:</b> <a href="#">obj(arc)</a>*</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
area	<p>area of inst</p> <p><b>Type:</b> <a href="#">area</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
base_cell	<p>cell of inst</p> <p><b>Type:</b> <a href="#">obj(base_cell)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
base_name	<p>The name at the base of a hierarchical name. So the base_name of i1/i2/i3 is i3.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
bbox	<p>Bounding box of the overlap rects that define the placement area used by this inst.</p> <p><b>Type:</b> <a href="#">rect</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
clock_gating_integrated_cell	<p>clock_gating_integrated_cell</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
cts_CANNOT_clone_reasons	<p>A list of reasons to explain why the inst could not be cloned.</p>

This attribute will not be set if attributes cts\_clone\_clock\_gates/cts\_clone\_clock\_logic are false.

The attribute returns a list of reasons why the inst cannot be cloned.

The reasons why a inst cannot be cloned can be divided into three categories:

1. The inst is marked as dont\_touch
2. Reasons specific to the clock node
3. General reasons

The possible dont\_touch reasons are:

dont\_touch.add\_port\_driver Set if inst was added above an output port or below an input port via attribute cts\_add\_port\_driver

dont\_touch.add\_driver\_cell Set if inst was added below the root via attribute cts\_add\_driver\_cell

dont\_touch.clock\_root Set during clock tree extraction if identified as having the root pin

dont\_touch.clock\_sink Set on inst if any pin is a clock sink in a clock tree

dont\_touch.clock\_tree\_generator\_path Set if nodes and wires are in clock tree generator paths

dont\_touch.clock\_wire Set on inst if clock input wire is user dont\_touch

dont\_touch.clockgate\_no\_power\_domain Set if clock gate / clock logic is a clocknode in a no clock gate / clock logic power domain

dont\_touch.drives\_multi\_driver\_net Set if inst drives wires with other drivers

dont\_touch.external\_skew\_group\_pin Set if a pin on the inst is a skew group sink, source or ignore pin for a skew group created by the user

dont\_touch.flexible\_htree Set if inst was added to a flexible H-tree

dont\_touch.internal\_skew\_group\_pin Set if a pin on the inst is a skew group sink, source or ignore pin for a skew group created by CCOpt

dont\_touch.neg\_edge\_clock\_gate Set if a clock gate gates the falling edge

dont\_touch.non\_flop\_clock\_gating Set by SetDontTouchBlackBoxGating

dont\_touch.non\_standard\_inputs\_clock\_gate Set if inst is a clock gate with 'non-standard' inputs, to avoid disconnecting them

dont\_touch.observability\_clock\_gate Set if inst is a clock gate with an observability output pin

dont\_touch.output\_wire Set if inst drives a net that is dont\_touch

dont\_touch.placer.lock Set if inst is user locked or locked by DEF

dont\_touch.power\_management Set if inst is a power management inst

dont\_touch.prevent\_assign Set if inst is necessary to prevent an assign

dont\_touch.sdc Set if constrained by SDC timing

dont\_touch.sdc\_path\_group Set if there is an SDC path group start / endpoint on one of the pins of this inst

dont\_touch.sub\_block Set if inst is in dont\_touch module

dont\_touch.unmergeable\_composite\_clock\_gate Set if some of the clock gate is dont\_touch

dont\_touch.user Set by user

Contact Cadence Support if any of the following reasons are listed:

dont\_touch.cannot\_understand\_clock\_gate Set if clock gate not recognized

dont\_touch.composite\_clock\_gate\_enable\_test\_or\_gate

The possible reasons specific to the clock node are:

	<p>PowerManagement Set if inst is a power management inst          PowerManagementInconsistency Set if a disconnection of the inst from the netlist would cause a power management inconsistency          PreservedUMPB Set if clock node is a User Module Port Bit which is preserved          Contact Cadence Support if any of the following reasons are listed:          ClockGatesAlways Set if inst is clock gate, considered always dont_touch          ClockLogicAlways Set if inst is clock logic, considered always dont_touch          NodeIsRoot Set if the clock node is the clock root          NoRoot Set if the clock node has no root          RootIgnored Set if the clock root is ignored          SpineCell Set if cell is a clock spine inst and is marked as dont_touch          The possible general reasons are:          DrivesAcrossPowerDomains The inst drives across power domain boundaries          NodeHasSGConstraints The inst has user mode skew group constraints in default mode          ClockDriverCannotCloneInverter          ClockDriverCreatedByBuffLongNets Set if the inst was created by 'Buffering long nets'.          ClockDriverInverterCloningDisabled The inst is an inverter and cloning inverters is disabled.          UncloneableClockSource Set if the inst carries the -source of an SDC clock          UncloneableIODelayReference Set if the inst is associated with an I/O timing constraint          UncloneablePLLReference Set if the inst is associated with a PLL constraint          UncloneablePLLFeedback Set if the inst is analyzed as a PLL feedback          UncloneablePLLOutput Set if the inst is analyzed as a PLL output          UnsupportedNodeType Set if the inst is not a supported type. Supported types are: clock gate, clock logic and clock driver.          SingleOrZeroFanoutNode Set if the inst has fewer than two fanout.          Contact Cadence Support if any of the following reasons are listed:          NoCellInst          ClockLogicMultiOutputCell          InIgnoredTree          IsUncloneable          NonIntegratedClockGate          NotTreeViewNode          OutputPinCellPinNull          ClockDriverNeedToKeep          Valid values: list string</p> <p><b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
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#### cts\_CANNOT\_MERGE\_REASONs

	<p>A list of reasons to explain why the inst could not be merged.          The attribute returns a list of reasons why the inst cannot be merged. These attributes are set on clock gates and clock logic instances.</p>
--	--

For clock gates, the merge is driven by the enable function. If two clock gates share the same enable function, potentially they may be merged together. The reasons explains why potentially mergeable clock gates could not in fact be merged.

For clock logic, the merge is driven by the logical expression, or logic function, at the clock output pin. If two clock logic express the same logic function, at least potentially they may be merged. The reasons lists why the potential merge could not be realized.

User configuration disabled merging:

ClockGateMergingDisabledOnTree Merging disabled: attribute ccopt/cts\_merge\_clock\_gates is false

ClockLogicMergingDisabledOnTree Merging disabled: attribute ccopt/cts\_merge\_clock\_logic is false

IsDontTouch The instance cannot be merged as it is marked dont\_touch

Attributes of a clock node rendered it unmergeable:

GloballyUnique The clock node has no potential candidate with which it might merge

UniqueUnderParent There are potential merge candidates, but not on the same clock net

HasSkewGroupConstraints The instance carries a skew group source, sink or ignore pin

UndrivenEnablePins The clock gate has a floating enable input

UndrivenRetentionPins The clock gate has a floating retention input

UndrivenTestPins The clock gate has a floating test enable input

DifferentSplitOnInputs The multi-input clock logic has different skew groups at its clock inputs

SiblingsNotMergeable Could not merge because all other candidates were unmergeable

Otherwise mergeable clock nodes may have incompatibilities that prevent merging:

DifferentSkewGroupForInputs Two clock nodes have different skew groups at their clock inputs

DifferentSkewGroupForOutputs Two clock nodes have different skew groups at their clock output

DifferentCellFamilies Two clock nodes belong to incompatible cell families

DifferentNumberOfInputPins Two clock nodes have different numbers of input pins

DifferentNonStandardInputs Two clock gates have non-standard\* inputs which are non-equivalent

MismatchingNonClockInputs Two clock nodes have non-clock inputs which receive non-equivalent signals

MismatchingClockInputs Two clock nodes have clock inputs which receive non-equivalent signals

MismatchingPowerDomains Two clock nodes are in incompatible power domains

NotLogicalClones Two clock nodes have outputs which are not logically equivalent

DifferentNumberOfParents Two clock nodes have different numbers of clock-carrying inputs

DifferentOutputPowerContext Two clock nodes have outputs with different power domain/voltage

DifferentInputPowerContext Two clock nodes have inputs with different power domain/voltage

IncompatibleRestrictedRegions Two clock nodes have incompatible restricted regions

DifferentAnnotations Two clock nodes have different annotations on its pins

(\*) Non-standard inputs on a clock gate are inputs besides the clock, enable, test enable

and retention inputs.

Valid values: list string

**Type:** string

**Default:** ""

**Edit:** Yes

#### cts\_node\_type

node type of instance within cts graph

**Type:** string

**Default:** ""

**Edit:** No

#### cts\_original\_names

Specifies for a clockgate or clocklogic which has been merged or is a clone a list of names from the original netlist which are equivalent to the clockgate/clocklogic.

For example:

If A and B are merged to form C then original\_names for C is { A B }.

If D\_clone is a clone of D then original\_names for D\_clone is { D }.

If E is a clone of C then original\_names for E is { A B } (remembering C was a merger of A and B).

Valid values: list string

**Type:** string

**Default:** ""

**Edit:** Yes

#### delta\_temperature

temperature of the inst

**Type:** string

**Default:** ""

**Edit:** No

#### dont\_merge\_multibit

This attribute denotes whether the instance can be merged during multibit optimization. This is enabled only when the root attribute 'use\_multibit\_cells' is set to true.

##### Supported values:

true: Cannot merge

false: Can be merged

**Type:** bool

**Default:** false

**Edit:** Yes

#### dont\_split\_multibit

	<p>This attribute denotes whether the instance can be split (unmerged) during multibit optimization. This is enabled only when the root attribute 'use_multibit_cells' is set to true.</p> <p><b>Supported values:</b></p> <ul style="list-style-type: none"> <li>true: Cannot split</li> <li>false: Can be split</li> </ul> <p><b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes</p>
dont_touch	<p>This attribute defines the user preservation status of an instance during optimization.</p> <p><b>Supported values:</b></p> <ul style="list-style-type: none"> <li>none (default): Unconstrained</li> <li>false: Can be mapped, sized, deleted, and constants can be propagated through it</li> <li>const_prop_size_delete_ok: Can be resized or deleted and constants can be propagated through it</li> <li>const_prop_delete_ok: Can be deleted and constants can be propagated through it</li> <li>size_delete_ok: Can be resized or deleted if no fanout</li> <li>delete_ok: Can be deleted if it has no fanout, but cannot be resized</li> <li>size_ok: Can only be resized</li> <li>size_same_height_ok: Can only be resized to a cell of the same height</li> <li>size_same_footprint_ok: Can only be resized to a cell of the same footprint that has exactly the same pin shapes</li> <li>map_size_ok: Can be mapped or sized (but not deleted). Applies only to sequential instances so cannot be applied on the module or hinst object.</li> </ul> <p>true: Cannot be touched</p> <p><b>Type:</b> enum <b>Enum Values:</b> none false true delete_ok const_prop_size_delete_ok const_prop_delete_ok size_delete_ok size_ok size_same_height_ok size_same_footprint_ok map_size_ok <b>Default:</b> none <b>Edit:</b> Yes</p>
dont_touch_effective	<p>This attribute defines the effective (most pessimistic) preservation status of an instance during optimization based on the 'sources'.</p> <p><b>Type:</b> enum <b>Enum Values:</b> none false true delete_ok const_prop_size_delete_ok const_prop_delete_ok size_delete_ok size_ok size_same_height_ok size_same_footprint_ok map_size_ok <b>Default:</b> "" <b>Edit:</b> No</p>
dont_touch_sources	

	<p>Dictionary of {source &lt;value&gt;} pairs contributing to the dont_touch_effective attribute for this object:</p> <pre>{user &lt;value&gt;} {lib &lt;value&gt;} {parent &lt;value&gt;} {scan &lt;value&gt;} user # This inst dont_touch value lib # The base_cell dont_touch value parent # The effective dont_touch value from an hinst above (the closest hinst above that is not false) scan # Is this inst part of a scan-chain (value is either size_ok or none). There is an additional inst attribute that holds this information.</pre> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>
early_cell_check_derate_factor	<p>Returns the derating factor on timing check values for early paths (e.g Hold checks)</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
early_clk_cell_derate_factor	<p>Returns the derating factor for instances on early clock paths</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
early_data_cell_derate_factor	<p>Returns the derating factor for instances on early data paths</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
early_fall_cell_check_derate_factor	<p>Returns the early cell check derating factor for falling arrivals</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
early_fall_clk_cell_derate_factor	

	Returns the early derating factor for falling delays through clock tree instances <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>early_fall_data_cell_derate_factor</b>	
	Returns the early derating factor for falling delays through data path instances <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>early_rise_cell_check_derate_factor</b>	
	Returns the early cell check derating factor for rising arrivals <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>early_rise_clk_cell_derate_factor</b>	
	Returns the early derating factor for rise delays through clock tree instances <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>early_rise_data_cell_derate_factor</b>	
	Returns the early derating factor for rising delays through data path instances <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>escaped_name</b>	
	The full hierarchical name including escaped chars (if any). It follows DEF escaping syntax, so bus-bit chars [], or a hierarchy char \ that is not a bus-bit or hierarchy char has a \ in front of it. So i1/i2 is a two-level hierarchical name while i1\i2 is single level name, and a[0] is a bus-bit, while a\[0\] is a scalar. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No

group	
	<p>The floorplan group that contains this inst. The instances in a group will be placed close together.</p> <p><b>Type:</b> <a href="#">obj(group)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
hierarchical_level	
	<p>Returns hierarchical level for an Instance</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_always_on	
	<p>Returns true if the associated library cell is recognized as always on type cell</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_black_box	
	<p>Returns a value of true if the cell is a black box cell.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_buffer	
	<p>This inst is a buffer.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_clock_gating_check	
	<p>Returns true if a clock gating check is performed by this instance. The clock gating check may be inferred from logic in netlist, asserted by SDC constraints, or may be due to this instance being an integrated clock gating cell</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

is_combinational	
	<p>Returns a value of true if the instance is a combinational cell (not a sequential cell).</p> <p><b>Type:</b> bool</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_disable_timing	
	<p>Returns true if set_disable_timing has been set on this cell instance</p> <p><b>Type:</b> bool</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_fixed_mask	
	<p>Indicates the base_cell of the inst has FIXEDMASK keyword in LEF, so mask-shifting is not allowed, except for the layers with LAYERMASKSHIFT keyword.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_flop	
	<p>Returns true if the library cell is recognized as flip-flop/register type cell</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_genus_clock_gate	
	<p>Set by the tool in the iSpatial flow to indicate that this integrated clock gating instance was added by Genus clock gating</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
is_inside_ilm	
	<p>This attribute denotes whether the inst is the child of a parent hinst that has an ILM specified for it</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_integrated_clock_gating	

	<p>Returns true if this instance's library cell has the Liberty clock_gating_integrated_cell set to true</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>is_interface_timing</b>	
	<p>Returns a value of true if this instance's library cell has the Liberty interface_timing attribute set to true</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>is_inverter</b>	
	<p>This inst is an inverter.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>is_isolation</b>	
	<p>This inst is an isolation.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>is_isolation_cell</b>	
	<p>Returns true if the associated library cell is recognized as isolation type cell</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>is_jtag</b>	
	<p>The inst is a JTAG element.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>is_latch</b>	

	Returns true if the associated library cell is recognized as latch type cell <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_level_shifter	Returns true if the associated library cell is recognized as level shifter type cell <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_macro	Returns a value of true if the associated library cell has the Liberty attribute is_macro_cell is set true <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_master_slave_flop	Returns true if the Liberty clock_on_also attribute is specified for the associated library cell <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_master_slave_lssd_flop	Returns true if this cell has been recognized as a master/slave LSSD device <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_memory	Returns true or false depending on whether the associated library cell of the inst is recognized as a Liberty memory cell. Cells which include a Liberty memory group definition are recognized as memory cells. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_negative_level_sensitive	

	Returns a value of true if the associated library cell is identified as a negative level-sensitive latch. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_pad	Returns a value of true if the associated library cell's Liberty is_pad attribute is set to true <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_physical	is physical only of inst <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_place_halo	Indicates that the instance has a placement halo. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
is_positive_level_sensitive	Returns a value of true if the associated library cell is identified as a positive level-sensitive latch. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_power_switch	Returns true if the associated library cell is recognized as power switch type cell <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_retention	

	Returns true if the associated library cell is recognized as retention type cell <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_sequential	Returns a value of true if the library cell is a latch or flip-flop, or if the cell has sequential timing checks. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_spare	The inst is a spare instance. These are used by post-mask ECO flows. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
is_tristate	Returns a value of true if the associated library cell definition includes the Liberty attribute three_state set to true . <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
late_cell_check_derate_factor	Returns the derating factor on timing check values for late paths (e.g Setup checks) <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
late_clk_cell_derate_factor	Returns the derating factor for instances on late clock paths <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
late_data_cell_derate_factor	

	Returns the derating factor for instances on late data paths <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>late_fall_cell_check_derate_factor</b>	
	Returns the late cell check derating factor for falling arrivals <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>late_fall_clk_cell_derate_factor</b>	
	Returns the late derating factor for falling delays through clock tree instances <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>late_fall_data_cell_derate_factor</b>	
	Returns the late derating factor for falling delays through data path instances <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>late_rise_cell_check_derate_factor</b>	
	Returns the late cell check derating factor for rising arrivals <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>late_rise_clk_cell_derate_factor</b>	
	Returns the late derating factor for rise delays through clock tree instances <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>late_rise_data_cell_derate_factor</b>	

	<p>Returns the late derating factor for rising delays through data path instances</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
leakage_power	<p>Returns the leakage power of the instance from library cell</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
level_shifter_type	<p>Returns the Level Shifter type for associated library cell. The supported values are LH, HL and HL_LH.</p> <p><b>Type:</b> <code>string</code></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
lib_cells	<p>Returns a list of library cell objects associated with this instance. You can use -index to refine this list to lib_cells associated with a specific view</p> <p><b>Type:</b> <code>obj(lib_cell)*</code></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
litho_halo	<p>A litho_halo on an inst forces parallelrouting away from the block boundary to meet lithography DRC rules on a few routing layers but allows perpendicular access to pins. It is only allowed if LEF LITHOMACROHALO values exists for some routing layers. See the LEF manual for figures and more details of this DRC rule. It cannot be added to standard cells (cells with a CLASS CORE SITE).</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
location	

	<p>The location of the inst. It is always the lower-left corner of the inst bounding-box, independent of the inst orientation.</p> <p><b>Type:</b> <a href="#">point</a>  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
mask_shift	<p>Digit encoded value indicates the mask shifting for the instance contents (0 = unshifted, for other shift cases refer to the DEF COMP + MASKSHIFT documentation).</p> <p><b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
name	<p>The same as .escaped_name without any \ escape chars. This name is commonly used to avoid problems with \ escape chars in Tcl scripts unless you carefully use list operators. Like SDC commands, 'get_db insts i1/i2' will first try to match i1/i2, and if not found then match i1\i2 so that flattening hierarchical names (e.g. with ungroup) does not require changing the names in Tcl scripts.</p> <p><b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (inst)</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
orient	<p>Instance placement orientation.</p> <p><b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> r0 r90 r180 r270 mx mx90 my my90  <b>Default:</b> r0  <b>Edit:</b> Yes</p>
overlap_rects	<p>List of rectangles that define the shape of instance</p> <p><b>Type:</b> <a href="#">rect*</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
parent	

	<p>The parent of the inst, which is either a hinst for an instance within hierarchy or the design object for an instance at the top level.</p> <p><b>Type:</b> <a href="#">obj.design</a>* <a href="#">obj.hinst</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>partition</b>	
	<p>If this inst is a physical black_box, this partition will carry the pin constraints and related data for the blackbox. Otherwise it is empty.</p> <p><b>Type:</b> <a href="#">obj.partition</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>peak_current</b>	
	<p>Peak current value of the inst</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>pg_pins</b>	
	<p>List of pg_pins for this inst. These are declared as power or ground pins in the .lib or LEF/OA library, and separated from the signal pins of the inst.</p> <p><b>Type:</b> <a href="#">obj(pg_pin)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>pins</b>	
	<p>The pins of this inst.</p> <p><b>Type:</b> <a href="#">obj.pin</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>place_halo_bbox</b>	
	<p>Bounding box of the inst placement halo. For a rectilinear block this might include area that is not covered by the place halo.</p> <p><b>Type:</b> <a href="#">rect</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>place_halo_bottom</b>	

	<p>Specifies an extra halo of space along the bottom edges of the inst that should not be used during placement. This area can still be used later during optimization and clock tree creation to add repeaters. It can only be used on blocks and cannot be added to standard-cells. See the padding attributes on the base_cell to add extra space to standard-cells.</p> <p><b>Type:</b> coord</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<p>place_halo_left</p>	
	<p>Specifies an extra halo of space along the left edges of the inst that should not be used during placement. This area can still be used later during optimization and clock tree creation to add repeaters. It can only be used on blocks and cannot be added to standard-cells. See the padding attributes on the base_cell to add extra space to standard-cells.</p> <p><b>Type:</b> coord</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<p>place_halo_polygon</p>	
	<p>Specifies the polygon shape of the inst placement halo.</p> <p><b>Type:</b> point</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<p>place_halo_right</p>	
	<p>Specifies an extra halo of space along the right edges of the inst that should not be used during placement. This area can still be used later during optimization and clock tree creation to add repeaters. It can only be used on blocks and cannot be added to standard-cells. See the padding attributes on the base_cell to add extra space to standard-cells.</p> <p><b>Type:</b> coord</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<p>place_halo_top</p>	
	<p>Specifies an extra halo of space along the top edges of the inst that should not be used during placement. This area can still be used later during optimization and clock tree creation to add repeaters. It can only be used on blocks and cannot be added to standard-cells. See the padding attributes on the base_cell to add extra space to standard-cells.</p> <p><b>Type:</b> coord</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<p>place_status</p>	

	<p>This attribute is the placement status of an instance during placement and optimization. The placer will look at both place_status and place_status_cts and use the more restrictive value. When this attribute is explicitly set by the user, it will reset the place_status_cts attribute so the user intent has precedence.</p> <p><b>Supported values:</b></p> <ul style="list-style-type: none"> <li>unplaced: Unconstrained</li> <li>placed: Is placed but can be moved</li> <li>soft_fixed: Is fixed, but can move a short distance to legalize it</li> <li>fixed: Is fixed and can only be moved by the user, will not be moved by placement or optimization commands.</li> <li>cover: Is fixed and cannot be moved by any commands, you must change the place_status to move it.</li> </ul> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> unplaced placed fixed cover soft_fixed</p> <p><b>Default:</b> unplaced</p> <p><b>Edit:</b> Yes</p>
place_status_cts	<p>This attribute is the CTS placement status of an instance during placement and optimization. The placer will look at both place_status and place_status_cts and use the more restrictive value.</p> <p><b>Supported values:</b></p> <ul style="list-style-type: none"> <li>unset: Unconstrained</li> <li>soft_fixed: For future use</li> <li>fixed: Cannot be moved</li> </ul> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> unset fixed soft_fixed</p> <p><b>Default:</b> unset</p> <p><b>Edit:</b> Yes</p>
place_status_effective	<p>This attribute is the effective placement status for the instance. It is the worst case of the instance place_status, instance place_status_cts, and hinst parent read only attribute (closest hinst above that is not set to none). See place_status for the description of possible values.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> unplaced placed fixed cover soft_fixed</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
power_domain	

	The power_domain for the inst. <b>Type:</b> obj(power_domain) <b>Default:</b> "" <b>Edit:</b> No
<b>power_dynamic</b>	
	The switching + internal power of this inst computed by report_power. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>power_frequency_domain</b>	
	signifies Frequency of the inst with which it is constrained, sdc/twf file has clock frequency related information for the instances <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
<b>power_internal</b>	
	The internal power of this inst computed by report_power. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>power_internal_density</b>	
	Internal power density of the inst which is inst power internal / inst area <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
<b>power_leakage</b>	
	The leakage power of this inst computed by report_power. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>power_leakage_density</b>	
	Leakage power density of the inst which is inst power leakage / inst area <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No

power_loading_capacitance	<p>Loading capacitance of the inst, it signifies the output net cap + pin cap of the next instance it is connecting to.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
power_ref_clock	<p>The reference clock for toggle and activity calculations. By default this is the fastest clock for multi clock domains but can be modified by some power commands.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
power_switch_type	<p>Returns the switch cell type associated with library cell. The supported values are coarse_grain, fine_grain.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
power_switching	<p>The switching power of the nets driven by this inst computed by report_power.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
power_switching_density	<p>Switching power density of the inst which is power switching / inst area</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
power_toggle_rate	<p>The average number of toggles read from VCD,TCF,SAIF, etc. or from propagation that occur in 1 second on all the pins of this inst. no_value is returned if it cannot be computed.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
power_total	

**Stylus Common UI Database Object Information**  
**Database Objects--inst**

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	The switching + internal + leakage power of this inst computed by report_power. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>power_total_density</b>	
	Total power density of the inst which is inst power total / inst area <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
<b>rail_domain_voltage_drop</b>	
	Worst Effective drop (VDD-VSS) of the inst in elapse or timing/switching window. Values are loaded in GUI after user loads the voltus state directory <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
<b>rail_ground_voltage_drop</b>	
	Ground bounce for ground rail of the inst, Values are loaded in GUI after user loads the voltus state directory <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
<b>rail_power_voltage_drop</b>	
	Voltage drop for power rail of the inst, Values are loaded in GUI after user loads the voltus state directory <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
<b>rail_reff</b>	
	signifies equivalent resistance for the instance pin from the voltage source, values are loaded in GUI after user load the effective resistance state directory. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
<b>rail_rlp</b>	

	<p>signifies least resistance path value of the inst from a voltage source to a pin of the instance, values are loaded in GUI after user load the voltus state directory. It is enabled when enable_rlp_analysis option of set_rail_analysis_config is turned on</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>route_halo_bottom_layer</b>	
	<p>The bottom layer for the routing halo.</p> <p><b>Type:</b> <a href="#">obj(layer)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>route_halo_polygon</b>	
	<p>Specifies the polygon shape of the inst routing halo.</p> <p><b>Type:</b> <a href="#">point</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>route_halo_size</b>	
	<p>Specifies the size of a routing halo around the inst. A value of 0 means there is no route_halo. It is used to keep routes away from the block edges to reduce cross-coupling to wires inside the block. A route_halo can only be added to blocks and is not allowed on standard-cells. The router will only route through the halo to reach pins on the boundary of the block. The value applies to all sides of the block and only positive values are allowed.</p> <p><b>Type:</b> <a href="#">coord</a></p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p>
<b>route_halo_top_layer</b>	
	<p>The top layer of the routing halo.</p> <p><b>Type:</b> <a href="#">obj(layer)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>sdp</b>	
	<p>The parent sdp group which the instance belongs to.</p> <p><b>Type:</b> <a href="#">obj(sdp)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>std_cell_main_rail_name</b>	

	Returns the rail name associated with pg pin for which std_cell_main_rail is enabled. <b>Type:</b> string <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
transition_density	
	Transition density of the inst <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
use_cells	
	This attribute is the list of allowable cells that this instance can be resized to. Wildcards are supported. If set, any parent (hinst) .dont_use_cells_effective values are ignored. This attribute only applies to operations on mapped designs. The .dont_touch_effective values size_same_height_ok and size_same_footprint_ok will filter this list further based on height and footprint, respectively. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes

## io\_constraint

### Parent Objects

[design](#), [root](#)

### Definition

IO object for block (term) or chip design (inst) constraints

Attribute	Description
area	
	Area of the instance as defined by the LEF MACRO SIZE or OVERLAP information <b>Type:</b> area <b>Default:</b> "" <b>Edit:</b> No

**Stylus Common UI Database Object Information**  
Database Objects--io\_constraint

bbox	
	Bounding box of the inst overlap rects. This is only correct if type = inst. <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> Yes
indent	
	Indent of instance from the boundary of the design <b>Type:</b> <a href="#">coord</a> <b>Default:</b> no_value <b>Edit:</b> Yes
inst	
	The IO instance (null/0x0 for block design case) <b>Type:</b> <a href="#">obj(inst)* obj(bump)*</a> <b>Default:</b> "" <b>Edit:</b> No
is_assigned	
	Indicates that the IO location has been set by the IO placer <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
is_corner	
	Indicates that the IO refers to a corner cell <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
is_gap_fixed	
	Indicates that the IO spacing constraint is applied <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
is_ground	
	Indicates that the IO is a Ground <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes

**Stylus Common UI Database Object Information**  
Database Objects--io\_constraint

is_offset_fixed	Indicates that the IO offset constraint is applied <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
is_power	Indicates that the IO is a Power <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
name	IO name <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (io_constraint)</a> <b>Default:</b> "" <b>Edit:</b> No
offset	IO relative location from left (North & South) or bottom (East & West) die edge <b>Type:</b> <a href="#">coord</a> <b>Default:</b> no_value <b>Edit:</b> Yes
order	IO order per side. Order is left-to-right (North & South) or bottom-to-top (East & West) <b>Type:</b> <a href="#">int</a> <b>Default:</b> "" <b>Edit:</b> Yes
row	IO row/ring number (0 is outermost IO row) <b>Type:</b> <a href="#">int</a> <b>Default:</b> 0 <b>Edit:</b> Yes

side	
	Side constraint of IO <b>Type:</b> enum <b>Enum Values:</b> north west south east none <b>Default:</b> "" <b>Edit:</b> Yes
spacing	
	Spacing between IO and previous IO (left or below) <b>Type:</b> coord <b>Default:</b> no_value <b>Edit:</b> Yes
term	
	The IO terminal (only used when 'type = term') <b>Type:</b> obj(port) <b>Default:</b> "" <b>Edit:</b> Yes
type	
	Type of IO (endSpace indicates from last IO to corner, inst indicates real instance case, obs indicates obstruction between IOs, term indicates block design case) <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No

## layer

### Parent Objects

[marker](#), [bump\\_pin](#), [layer\\_shape](#), [text](#), [port](#), [via\\_def](#), [pin\\_blockage](#), [special\\_wire](#), [what\\_if\\_wire](#), [what\\_if\\_via](#), [trim\\_grid](#), [base\\_pin](#), [partition](#), [design](#), [track\\_pattern](#), [root](#), [layer\\_rule](#), [pin\\_guide](#), [virtual\\_wire](#), [port\\_shape](#), [via\\_def\\_rule](#), [route\\_blockage](#), [patch\\_wire](#), [antenna\\_data](#), [inst](#), [wire](#), [bus\\_guide](#), [net](#), [pin](#), [route\\_type](#), [inst\\_obs\\_shape](#)

### Definition

A layer from the LEF or OA technology file.

Attribute	Description
antenna_model_1	<p>The antenna model object for Oxide1  <b>Type:</b> <a href="#">obj(antenna_model)</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
antenna_model_2	<p>The antenna model object for Oxide2  <b>Type:</b> <a href="#">obj(antenna_model)</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
antenna_model_3	<p>The antenna model object for Oxide3  <b>Type:</b> <a href="#">obj(antenna_model)</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
antenna_model_4	<p>The antenna model object for Oxide4  <b>Type:</b> <a href="#">obj(antenna_model)</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
area	<p>Layer minimum area from LEF/OpenAccess. If AREA rule is not specified in LEF, the value of -1 in dbu will be returned.  <b>Type:</b> <a href="#">area</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
backside	<p>Indicates that the layer is a backside (underside of the die) layer.  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
cut_index	

	An index into the cut layers used by vias in the routing. It is 1 for the cut-layer above the first routing layer, 2 for the cut-layer above the second routing layer, etc. It is 0 for the cut-layer just below the first routing layer. The cut_index is -1 for any other layer, including LEF cut layers with TYPE MIMCAP, TSV or BACKSIDE. In OpenAccess, the cut layers are determined by the LEFDefaultRouteSpec validVias list. <b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No
<b>density_step_x</b>	
	Layer density window step from LEF/OpenAccess <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
<b>density_step_y</b>	
	Layer density window step from LEF/OpenAccess <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
<b>density_window_x</b>	
	Layer density window length from LEF/OpenAccess <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
<b>density_window_y</b>	
	Layer density window width from LEF/OpenAccess <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
<b>direction</b>	
	Layer pref. direction from LEF/OpenAccess <b>Type:</b> enum <b>Enum Values:</b> horizontal vertical unassigned diag45 diag135 <b>Default:</b> "" <b>Edit:</b> No
<b>fill_active_spacing</b>	

	Layer fill minimum spacing from LEF/OpenAccess <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
<b>fill_gap_spacing</b>	
	Layer fill to fill spacing from LEF/OpenAccess <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
<b>max_density</b>	
	Layer fill maximum density from LEF/OpenAccess <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>max_width</b>	
	Layer maximum wire width from LEF/OpenAccess <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
<b>mfg_grid</b>	
	Manufacturing grid <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
<b>min_density</b>	
	Layer fill minimum density from LEF/OpenAccess <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>min_spacing</b>	
	Layer minimum spacing from LEF/OpenAccess <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
<b>min_width</b>	

	<p>Layer minimum wire width from LEF/OpenAccess  <b>Type:</b> <a href="#">coord</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
name	
	<p>Layer name from LEF/OpenAccess technology file definition.  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
num_masks	
	<p>Indicates how many masks will be used for the layer (1 = single mask, 2 = double-patterning, 3 = triple-patterning)  <b>Type:</b> <a href="#">int</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
obj_type	
	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a>  <b>Type:</b> <a href="#">enum (layer)</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
offset_x	
	<p>Layer offset X from LEF/OpenAccess  <b>Type:</b> <a href="#">coord</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
offset_y	
	<p>Layer offset Y from LEF/OpenAccess  <b>Type:</b> <a href="#">coord</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
pitch_x	
	<p>Layer wire pitch X from LEF/OpenAccess  <b>Type:</b> <a href="#">coord</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>

pitch_y	
	<p>Layer wire pitch Y from LEF/OpenAccess  <b>Type:</b> coord  <b>Default:</b> ""  <b>Edit:</b> No</p>
route_index	
	<p>An index into the routing layers. It is 1 for the first LEF TYPE ROUTING layer in the technology file, 2 for the second routing layer, etc. It is 0 for the layer just below the first routing layer (e.g a poly layer or non-routing metal layer that may have pin shapes in some cells). The route_index is -1 for any non-routing layers, or LEF routing layers with LEF TYPE MIMCAP or TYPE BACKSIDE. In OpenAccess, the routing layers are determined by the LEFDefaultRouteSpec validLayers list.  <b>Type:</b> int  <b>Default:</b> ""  <b>Edit:</b> No</p>
spacing_tables	
	<p>A list of all the LEF spacing-table rules for this layer in the LEF SPACINGTABLE syntax. All SPACINGTABLE and LEF58_SPACINGTABLE property values are returned.  <b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>
type	
	<p>The layer type (routing, cut, etc.) from the LEF LAYER TYPE statements or OA tech for this layer.  <b>Type:</b> enum  <b>Enum Values:</b> invalid masterslice cut overlap routing implant tsv mimcap passivation poly_routing nwell pwell stacked_die cut_mimcap above_die_edge below_die_edge diffusion ignore trim_poly trim_metal region cut_region routing_region trim_metal_region  <b>Default:</b> ""  <b>Edit:</b> No</p>
width	
	<p>Layer wire width from LEF/OpenAccess  <b>Type:</b> coord  <b>Default:</b> ""  <b>Edit:</b> No</p>
wrong_way_min_width	

	<p>min width in the non-preferred direction (from LEF LAYER MINWIDTH WRONGDIRECTION). A value of 0 indicates that there is no special value assigned for a wrong direction behavior.</p> <p><b>Type:</b> coord</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
wrong_way_spacing	<p>min spacing in the non-preferred direction (from LEF LAYER SPACING WRONGDIRECTION). A value of 0 indicates that there is no special value assigned for a wrong direction behavior.</p> <p><b>Type:</b> coord</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
wrong_way_width	<p>min width in the non-preferred direction (from LEF LAYER WIDTH WRONGDIRECTION). A value of 0 indicates that there is no special value assigned for a wrong direction behavior.</p> <p><b>Type:</b> coord</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
wsp_oa_width_spacing_pattern	<p>A list of Tcl dict style parameters that match the OA widthSpacingPattern parameters like this: {name &lt;string&gt; is_from_lib &lt;bool&gt; offset &lt;coord&gt;}. The 'name' and 'offset' match the corresponding OA parameters, and 'is_from_lib &lt;bool&gt;' is true if it is from the OA tech graph and false if it is from the cellview.</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
wsp_oa_width_spacing_snap_pattern_def	<p>A list of Tcl dict style parameters that match the OA widthSpacingSnapPatternDef parameters like this: {name &lt;string&gt; is_from_lib &lt;bool&gt; offset &lt;coord&gt; offset_reference &lt;string&gt; wire_type &lt;name&gt; purpose &lt;name&gt;}. The 'name', 'offset', 'wire_type', and 'purpose' match the corresponding OA parameters. 'offset_reference' indicates whether the 'offset' is from the lower-left corner of the boundary or the origin. 'is_from_lib &lt;bool&gt;' is true if it is from the OA tech graph and false if it is from the cellview.</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
wsp_offset	

	<p>Offset from lower-left corner of the core box to the first track. For a horizontal routing layer track, this is a Y offset.</p> <p><b>Type:</b> <a href="#">coord</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>wsp_pattern</b>	
	<p>This is set by add_tracks or by reading an OA design with widthSpacingPatterns defined. It is a list of {width pitch repeat} values that created the tracks. For example, {1.5 2.5 1} {1.0 2.0 3} means a track of 1.5 width, 2.5 track-to-track pitch repeated 1 time, and then a track with width 1.0, track-to-track pitch 2.0 repeated 3 times, then the full pattern repeats. If this is not an SADP layer, there is no width assigned to the track, and a width value of 0.0 is returned. For a horizontal routing layer, the width and pitch are Y values.</p> <p><b>Type:</b> <a href="#">string*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>wsp_pattern_masks</b>	
	<p>A list of mask values for each track in the wsp_pattern after the pattern repeat sections are expanded.</p> <p><b>Type:</b> <a href="#">int*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## layer\_rule

### Parent Objects

[route\\_rule](#)

### Definition

Layer Rule

Attribute	Description
layer	

	The layer of laye rule <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (layer_rule)</a> <b>Default:</b> "" <b>Edit:</b> No
spacing	min spacing (from NONDEFUALTRULE LAYER SPACING, LEF LAYER SPACING or SPACINGTABLE) <b>Type:</b> <a href="#">coord</a> <b>Default:</b> "" <b>Edit:</b> No
width	wire width (from NONDEFUALTRULE LAYER WIDTH or LEF LAYER WIDTH) <b>Type:</b> <a href="#">coord</a> <b>Default:</b> "" <b>Edit:</b> No

## layer\_shape

### Parent Objects

[base\\_cell](#), [physical\\_pin](#)

### Definition

layer shape

Attribute	Description
is_ignore_pg_net	

	Indicates that Power/Ground routing is ignored when checking for DRC violations (including shorts) involving the current shape (equivalent to LEF MACRO OBS LAYER EXCEPTPGNET});,isExceptPGNet,, <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
layer	The layer of blockage <b>Type:</b> obj(layer) <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (layer_shape) <b>Default:</b> "" <b>Edit:</b> No
shapes	List of shapes that define the blockage area <b>Type:</b> obj(shape)* <b>Default:</b> "" <b>Edit:</b> No
spacing	LEF OBS SPACING equivalent min_spacing value, zero if not specified in LEF. <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No

## lib\_arc

### Parent Objects

[lib\\_cell](#), [arc](#), [root](#), [lib\\_pin](#)

### Definition

cte library timing arc

Attribute	Description
aocv_weight	<p>Returns the AOCV stage weight for this library arc. By default, all library cells and library arcs have default stage weight of 1.0. The aocv_weight property is specified as a user-defined library attribute in the Liberty timing library explicitly - or, by asserting it via command. You can use -index to return a value for a specific view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
base_name	<p>Returns the simple name for this library timing arc in the form:          inputPin_outputPin_uniqueIntegerSuffix</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
from_lib_pin	<p>Returns a lib_pin object for beginning pin of this timing arc. You can use -index to return a value for a specific view.</p> <p><b>Type:</b> <a href="#">obj(lib_pin)*</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
full_name	<p>Returns the unique name for this library arc in the form:          librarySet/libraryName/libraryCell/inputPin_outputPin_uniqueIntegerSuffix. You can use -index to return a value for a specific view.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_disabled	

	<p>Returns a value of true if this library timing arc has been explicitly disabled by the user via a set_disable_timing constraint. You can use -index to return a value for a specific view.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
lib_cell	<p>Returns the parent library cell object for this library arc. You can use -index to return a value for a specific view.</p> <p><b>Type:</b> <a href="#">obj(lib_cell)</a>*</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
mode	<p>If this timing arc is defined as part of a Liberty mode group, this attribute will return the name of the group. You can use -index to return a value for a specific view.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
name	<p>Returns an identifier for this library arc in the form:          libraryName/libraryCell/inputPin_outputPin_uniqueIntegerSuffix</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (lib_arc)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
sdf_cond	

	Returns the value of the Liberty sdf_cond attribute if specified for this arc. You can use -index to return a value for a specific view. <b>Type:</b> <a href="#">string</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
sense	Returns the Liberty timing_sense value associated with this arc. This value is one of: positive_unate, negative_unate, or non_unate. You can use -index to return a value for a specific view. <b>Type:</b> <a href="#">string</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
timing_type	Returns the Liberty timing_type associated with this arc. You can consult the Liberty documentation for the list of possible values for this attribute. You can use -index to return a value for a specific view. <b>Type:</b> <a href="#">string</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
to_lib_pin	Returns a lib_pin object for terminating pin of this timing arc. You can use -index to return a value for a specific view. <b>Type:</b> <a href="#">obj(lib_pin)*</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
when	Returns the value of the Liberty 'when' attribute if specified for this arc. You can use -index to return a value for a specific view. <b>Type:</b> <a href="#">string</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
when_end	

	Returns the value of the Liberty 'when_end' attribute if specified for this arc. You can use -index to return a value for a specific view.  <b>Type:</b> <a href="#">string</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
when_start	Returns the value of the Liberty 'when_start' attribute if specified for this arc. You can use -index to return a value for a specific view.  <b>Type:</b> <a href="#">string</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No

## lib\_cell

### Parent Objects

[inst](#), [base\\_cell](#), [lib\\_arc](#), [root](#), [library](#), [lib\\_pin](#)

### Definition

cte lib cell

Attribute	Description
aocv_weight	Returns the AOCV stage weight specified for the library cell either explicitly in the library or as a user-defined library attribute  <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
area	

	Returns the area of the library cell as specified by the Liberty timing library <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>async_clear_pins</b>	
	Returns a list of lib_pins that have both the is_async and is_clear attributes set to true <b>Type:</b> <a href="#">obj(lib_pin)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>async_preset_pins</b>	
	Returns a list of lib_pins that have both the is_async and is_clear attributes set to true <b>Type:</b> <a href="#">obj(lib_pin)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>base_cell</b>	
	Returns a pointer the base_cell object associated with this library cell. You can use chaining to reach the attributes of the base_cell <b>Type:</b> <a href="#">obj(base_cell)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>base_name</b>	
	The base_name of the cell. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
<b>bit_width</b>	
	Returns the bit width of the cell <b>Type:</b> <a href="#">int</a> <b>Default:</b> "" <b>Edit:</b> No
<b>clock_gating_integrated_cell</b>	

**Stylus Common UI Database Object Information**  
Database Objects--lib\_cell

	<p>clock_gating_integrated_cell <b>Type:</b> <a href="#">string</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No</p>
clock_pins	<p>Returns a list of lib_pins which have the attribute is_clock equal to true <b>Type:</b> <a href="#">obj(lib_pin)</a>* <b>Default:</b> "" <b>Edit:</b> No</p>
data_pins	<p>Returns a list of lib_pins which have the attribute is_data equal to true <b>Type:</b> <a href="#">obj(lib_pin)</a>* <b>Default:</b> "" <b>Edit:</b> No</p>
fall_input_switching_degrade_factor	<p>Returns user or library defined value for controlling the arrival sensitivity window for simultaneous rising inputs to this cell type <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No</p>
hierarchical_name	<p>hierarchical_name <b>Type:</b> <a href="#">string</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No</p>
is_always_on	<p>Returns a value of true if the lib_cell is identified as always on type <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No</p>
is_black_box	

	Returns a value of true if the cell is a black box cell. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_buffer	Returns a value of true if the lib_cell is identified as a buffer type <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_combinational	Returns a value of true if the library cell is a combinational cell (not a sequential cell). <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_disable_timing	Returns true if set_disable_timing has been set on this library cell <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_exist	Returns true if library cell present in view. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_fall_edge_triggered	Returns a value of true if the library cell is triggered by the falling edge of the clock. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_flop	

	Returns true if the library cell is recognized as flip-flop/register type cell <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_integrated_clock_gating	Returns true if the library cell has the Liberty clock_gating_integrated_cell set to true <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_interface_timing	Returns a value of true if a library cell has the Liberty interface_timing attribute set to true <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_inverter	Returns a value of true if the lib_cell is identified as an inverter type <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_isolation_cell	Returns a value of true if the lib_cell is identified as an isolation cell type <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_latch	Returns true if the library cell is recognized as latch type cell <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_level_shifter	

	Returns a value of true if the lib_cell is identified as a level shifter type <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>is_macro</b>	
	Returns a value of true if the Liberty attribute is_macro_cell is set true <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>is_master_slave_flop</b>	
	Returns true if the lib_cell is recognized as a master/slave flip-flop <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
<b>is_master_slave_lssd_flop</b>	
	Returns true if this cell has been recognized as a master/slave LSSD device <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
<b>is_memory</b>	
	Returns true or false depending on whether the associated library cell is recognized as a Liberty memory cell. Cells which include a Liberty memory group definition are recognized as memory cells. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>is_negative_level_sensitive</b>	
	Returns a value of true if the library cell is identified as a negative level-sensitive latch. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>is_pad</b>	

	<p>Returns a value of true if Liberty attribute is_pad is set to true  <b>Type:</b> <a href="#">bool</a>  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
is_pll	<p>Returns a value of true if the Liberty library is_pll_cell attribute is set to true for this library cell.  <b>Type:</b> <a href="#">bool</a>  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
is_positive_level_sensitive	<p>Returns a value of true if the library cell is identified as a positive level-sensitive latch.  <b>Type:</b> <a href="#">bool</a>  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
is_power_switch	<p>Returns a value of true if the lib_cell is identified as power switch type  <b>Type:</b> <a href="#">bool</a>  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
is_retention	<p>Returns a value of true if the lib_cell is identified as an retention cell type  <b>Type:</b> <a href="#">bool</a>  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
is_rise_edge_triggered	<p>Returns a value of true if the library cell is triggered by the rising edge of the clock.  <b>Type:</b> <a href="#">bool</a>  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
is_sequential	

	Returns a value of true if the library cell is a latch or flip-flop, or if the cell has sequential timing checks.  <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_tristate	Returns a value of true if the library cell definition includes the Liberty attribute three_state set to true.  <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
latch_enable_pins	Returns a list of lib_pin objects which function as the enable/gate pin of a latch  <b>Type:</b> <a href="#">obj(lib_pin)*</a> <b>Default:</b> "" <b>Edit:</b> No
leakage	Returns a cell_leakage_power property for a lib cell  <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
leakage_power	Returns the leakage power of the library cell as specified by the Liberty timing library  <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
level_shifter_type	Returns the Level Shifter type for a given lib_cell. The supported values are LH, HL and HL_LH.  <b>Type:</b> <a href="#">string</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No

lib_arcs	
	Returns a list of lib_arc objects contained with the lib_cell <b>Type:</b> <a href="#">obj(lib_arc)</a> * <b>Default:</b> "" <b>Edit:</b> No
lib_pins	
	Returns a list of lib_pin objects for the lib_cell <b>Type:</b> <a href="#">obj(lib_pin)</a> * <b>Default:</b> "" <b>Edit:</b> No
library	
	Returns the parent library object for the lib_cell <b>Type:</b> <a href="#">obj(library)</a> * <b>Default:</b> "" <b>Edit:</b> No
name	
	Returns the unique name of the library cell in the form lib_cell:librarySetName/libraryName/libraryCellName <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	
	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (lib_cell)</a> <b>Default:</b> "" <b>Edit:</b> No
pg_lib_pins	
	Returns a list of the power and ground lib_pin objects of the lib_cell <b>Type:</b> <a href="#">obj(lib_pin)</a> * <b>Default:</b> "" <b>Edit:</b> No
power_switch_type	

	<p>Returns the switch cell type associated with library cell. The supported values are coarse_grain, fine_grain.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p><b>rise_input_switching_derate_factor</b></p> <p>Returns user or library defined value for controlling the arrival sensitivity window for simultaneous rising inputs to this cell type</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p><b>std_cell_main_rail_name</b></p> <p>Returns the rail name associated with pg pin for which std_cell_main_rail is enabled.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p><b>timing_model_type</b></p> <p>Returns the Liberty model type for a given cell or instance. The supported values are abstracted , extracted , and qtm .</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## lib\_pin

### Parent Objects

[lib\\_cell](#), [pin](#), [lib\\_arc](#), [root](#), [port](#)

### Definition

cte lib pin

Attribute	Description
base_name	<p>Returns the simple name of this library pin. The base_name of BUFFERX1/A is 'A'.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
base_pin	<p>Returns the related base_pin object of this library pin. Use chaining to access the base_pin attributes</p> <p><b>Type:</b> <a href="#">obj(base_pin)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
capacitance	<p>Returns the capacitance for the library pin.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
capacitance_max_fall	<p>Returns the maximum value of the falling capacitance range.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
capacitance_max_rise	<p>Returns the maximum value of the rising capacitance range.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
capacitance_min_fall	

	Returns the minimum value of the falling capacitance range. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
capacitance_min_rise	Returns the minimum value of the rising capacitance range. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
cell_name	Returns the name of the lib_cell of the lib_pin mentioned. <b>Type:</b> string <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
direction	Returns the direction of the library pin: in , out , inout or internal. Internal is for a lib_pin that is not visible in the netlist, but is used internally by the timer to model timing arcs and constraints. These lib_pins will not appear in the GUI, or Verilog, but may appear in timing reports. <b>Type:</b> enum <b>Enum Values:</b> internal in out inout <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
drive_resistance_fall	Specifies the driving resistance of the cell for falling transitions <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
drive_resistance_rise	

	<p>Specifies the driving resistance of the cell for falling transitions</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
fanout_load	<p>Returns the fanout load value of the library pin.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
from_lib_arcs	<p>Returns the list of lib_arc objects that begin from this library pin</p> <p><b>Type:</b> <a href="#">obj(lib_arc)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
full_name	<p>Returns a unique reference for the library cell of the form: libset/lib_name/cell_name/pin_name</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
function	<p>Returns the function property for a lib pin</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
input_signal_level	<p>Returns the rail name associated with input library pin.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
input_signal_level_high	

	Returns partial high voltage swing of an input pin. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>input_signal_level_low</b>	
	Returns partial low voltage swing of an input pin. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>input_signal_level_voltage</b>	
	Returns rail voltage of signal which is driving the input pin. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>is_always_on</b>	
	Returns a value of true if the Liberty library is_always_on attribute is set to true for this library pin. <b>Type:</b> bool <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>is_async</b>	
	Returns a value of true if the library pin is an asynchronous preset pin, or an asynchronous clear pin. <b>Type:</b> bool <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>is_clear</b>	
	Returns a value of true if the pin is an asynchronous clear pin. <b>Type:</b> bool <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No

is_clock	
	<p>Returns a value of true if the library pin definition includes clock:true .</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Allowed -index values:</b> <code>analysis_view</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_clock_gate_clock	
	<p>Returns a value of true if the pin has the Liberty attribute <code>clock_gate_clock_pin</code> set to true</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Allowed -index values:</b> <code>analysis_view</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_clock_gate_enable	
	<p>Returns a value of true if the pin has the Liberty attribute <code>clock_gate_enable_pin</code> set to true</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Allowed -index values:</b> <code>analysis_view</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_data	
	<p>Returns a value of true if the library pin is the data pin of a flip-flop.</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Allowed -index values:</b> <code>analysis_view</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_exist	
	<p>Returns a value of true if the library pin exists in view.</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Allowed -index values:</b> <code>analysis_view</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_fall_edge_triggered_clock	
	<p><code>is_fall_edge_triggered_clock</code></p> <p><b>Type:</b> <code>bool</code></p> <p><b>Allowed -index values:</b> <code>analysis_view</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

is_fall_edge_triggered_data	Returns a value of true if the library pin is the data pin of a falling edge triggered device. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_isolated	Returns a value of true if the Liberty library is_isolated attribute is set to true for this library pin. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_isolation_cell_clock	Returns true if a clock lib pin is part of an isolation cell, <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_isolation_cell_data	Returns a value of true if the Liberty library is_isolation_cell_data attribute is set to true for this library pin. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_isolation_cell_enable	Returns a value of true if the Liberty library is_isolation_cell_enable attribute is set to true for this library pin. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_level_shifter_data	

	Returns a value of true if the Liberty library is_level_shifter_data attribute is set to true for this library pin. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_level_shifter_enable	Returns a value of true if the Liberty library is_level_shifter_enable attribute is set to true for this library pin. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_negative_level_sensitive_clock	Returns a value of true if the library pin is an enable pin of an active low level-sensitive device. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_negative_level_sensitive_data	Returns a value of true if the pin is a data pin of an active low level-sensitive device. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_pad	Returns the pad value of a pin <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_pll_feedback_pin	

	<p>Returns a value of true if the Liberty library is_pll_feedback_pin attribute is set to true for this library pin.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_pll_output_pin	<p>Returns a value of true if the Liberty library is_pll_output_pin attribute is set to true for this library pin.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_pll_reference_pin	<p>Returns a value of true if the Liberty library is_pll_reference_pin attribute is set to true for this library pin.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_positive_level_sensitive_clock	<p>Returns a value of true if the library pin is an enable pin of an active high level-sensitive device.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_positive_level_sensitive_data	<p>Returns a value of true if the pin is a data pin of an active high level-sensitive device.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_power_switch_enable	

	<p>Returns a value of true if the Liberty library is_power_switch_enable attribute is set to true for this library pin.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_preset	<p>Returns a value of true if the pin is a preset pin.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_retention_cell_enable	<p>Returns a value of true if the Liberty library is_retention_cell_enable attribute is set to true for this library pin.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_rise_edge_triggered_clock	<p>Returns a value of true if the library pin is the clock pin of a rising edge triggered device.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_rise_edge_triggered_data	<p>Returns a value of true if the library pin is the data pin of a rising edge triggered device.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_tristate	<p>Returns a value of true if the library pin definition includes three_state:true .</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

is_tristate_enable	Returns a value of true if the library pin is part of a Liberty three_state_enable logical expression  <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_tristate_output	Returns a value of true if the library pin definition includes three_state:true .  <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
lib_cell	Returns the lib_cell parent object of this lib_pin  <b>Type:</b> <a href="#">obj(lib_cell)*</a> <b>Default:</b> "" <b>Edit:</b> No
max_capacitance	Returns the maximum capacitance limit for the library pin.  <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
max_fanout	Returns the maximum fanout value for the library pin.  <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
max_transition	

	<p>Returns the maximum transition time limit specified for a given library pin. If the limit is not specified for a library pin, then the limit specified at the corresponding library level will be used.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>min_capacitance</b>	
	<p>Returns the minimum capacitance limit for the library pin.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>min_fanout</b>	
	<p>Returns the minimum fanout value for the library pin.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>min_transition</b>	
	<p>Returns the minimum transition time limit specified for a given library pin. If the limit is not specified for a library pin, then the limit specified at the corresponding library level will be used.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>name</b>	
	<p>Returns the name of the library pin in the form: &lt;library_name&gt;/&lt;cell_name&gt;/&lt;pin_name&gt;</p> <p><b>Type:</b> string</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>obj_type</b>	

	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (lib_pin)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
output_signal_level	<p>Returns the rail name associated with output library pin.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
output_signal_level_high	<p>Returns partial high voltage swing of an output pin.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
output_signal_level_low	<p>Returns partial low voltage swing of an output pin.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
related_ground_pin_rail_voltage	<p>Returns rail voltage of associated ground pin for the given pin.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
related_power_pin_rail_voltage	<p>Returns rail voltage of associated power pin for the given pin.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slew_threshold_percent_fall_high	

	<p>Specifies the upper threshold point used to model a falling transition on this pin. This value is typically inherited from the library-level specification. This value is specified as a percentage.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_threshold_percent_fall_low</b>	
	<p>Specifies the lower threshold point used to model a falling transition on this pin. This value is typically inherited from the library-level specification. This value is specified as a percentage.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_threshold_percent_rise_high</b>	
	<p>Specifies the upper threshold point used to model a rising transition on this pin. This value is typically inherited from the library-level specification. This value is specified as a percentage.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_threshold_percent_rise_low</b>	
	<p>Specifies the lower threshold point used to model a rising transition on this pin. This value is typically inherited from the library-level specification. This value is specified as a percentage.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>to_lib_arcs</b>	
	<p>Returns the list of lib_arc objects that terminate at this pin</p> <p><b>Type:</b> obj(lib_arc)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

# library

## Parent Objects

[timing\\_condition](#), [lib\\_cell](#), [library\\_set](#), [root](#)

## Definition

cte lib

Attribute	Description
base_name	Returns the simple name of the library as defined by the Liberty library() group name <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
cap_scale_in_ff	Returns the capacitance scaling of the library in femtofarads <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No
default_power_rail	Returns the power rail defined by the Liberty default_power_rail attribute <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
default_wireload	Returns the wire-load model defined by the Liberty default_wire_load attribute <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
files	

	Returns the list of library files associated with this library <b>Type:</b> string <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
has_cells_having_power_ground_pins	Returns a value of true if the library cells in this library have power/ground pin modeling <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
hierarchical_name	hierarchical_name <b>Type:</b> string <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
input_threshold_pct_fall	Specifies the delay threshold for a falling input signal. This value is specified as a percentage. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
input_threshold_pct_rise	Specifies the delay threshold for a rising input signal. This value is specified as a percentage. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_exist	Returns a value of true if library is present in view. <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
leakage_power_scale_in_nw	

	Returns the leakage power scaling used in this library in units of nanoWatts <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>lib_cells</b>	
	Returns a list of library cell objects contained within this library <b>Type:</b> obj(lib_cell)* <b>Default:</b> "" <b>Edit:</b> No
<b>name</b>	
	Returns an identifier for this library of the form: library_set/library_name <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
<b>nominal_process</b>	
	Returns the nominal process of the library as specified by the Liberty nom_process attribute <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>nominal_temperature</b>	
	Returns the nominal temperature of the library as specified by the Liberty nom_temperature attribute <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>nominal_voltage</b>	
	Returns the nominal voltage of the library as specified by the Liberty nom_voltage attribute <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>obj_type</b>	
	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (library) <b>Default:</b> "" <b>Edit:</b> No

output_threshold_pct_fall	<p>Specifies the delay threshold for a falling output signal. This value is specified as a percentage.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
output_threshold_pct_rise	<p>Specifies the delay threshold for a rising output signal. This value is specified as a percentage.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
power_rails	<p>Returns the power rails defined for this library</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slew_derate_from_library	<p>Specifies the multiplier used to translate between the transition time range used during characterization and the transition time range used in the timing library tables. A characterization range of 30% and library range of 10% would result in a derate value of 0.5.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slew_lower_threshold_pct_fall	<p>Specifies the lower threshold point used to model a falling transition on this pin. This value is specified as a percentage.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slew_lower_threshold_pct_rise	

	<p>Specifies the lower threshold point used to model a rising transition on this pin. This value is specified as a percentage.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_upper_threshold_pct_fall</b>	
	<p>Specifies the upper threshold point used to model a falling transition on this pin.. This value is specified as a percentage.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_upper_threshold_pct_rise</b>	
	<p>Specifies the upper threshold point used to model a rising transition on this pin. This value is specified as a percentage.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>wireload_models</b>	
	<p>Returns a list of the wireload models defined in the library</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## library\_set

### Parent Objects

[timing\\_condition](#), [root](#)

## Definition

Specifies a group of library files to be treated as a single entity so that higher-level descriptions (delay\_corners) can simply refer to the library configuration by name. All non-physical libraries used by the timing must be part of a library\_set - including Liberty, AOCV, SOCV, and signal integrity library formats. Use the create\_library\_set command to define new library\_sets and the update\_library\_set command to update the attributes of existing library\_sets.

Attribute	Description
aocv_files	<p>Specifies the list of optional AOCV derating library files associated with the library_set</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
libraries	<p>Specifies the list of timing library objects that result from the import of the library_files</p> <p><b>Type:</b> <a href="#">obj(library)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
library_files	<p>Specifies the list of Liberty timing library files associated with the library_set</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
name	<p>Provides the name of this library_set object as specified by create_library_set.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (library_set)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
si_files	

	Specifies the list of optional signal integrity (.cdb) library files associated with the library_set <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
<b>socv_files</b>	
	Specifies the list of optional SOCV variation library files associated with the library_set <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No

## marker

### Parent Objects

[design](#), [root](#)

### Definition

A violation marker. All markers have a .bbox and .originator set, and optionally .polygon for polygon shapes. Other attributes depend on the marker. Markers created by internal check or report commands will have .originator != external and have a .layer, .type, .subtype, .message, and .message\_id defined by those commands. Markers created with `read_markers` or `create_marker` will have .originator == external and will have .layer, .user\_type, .user\_subtype, .user\_originator, and .message based on the external input.

Attribute	Description
bbox	Bounding box of the marker shape. <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No
layer	The layer of marker <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> No
message	

	The message attached to the marker <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
<b>message_id</b>	
	The message ID used internally for this message <b>Type:</b> <a href="#">int</a> <b>Default:</b> "" <b>Edit:</b> No
<b>obj_type</b>	
	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (marker)</a> <b>Default:</b> "" <b>Edit:</b> No
<b>originator</b>	
	The originator of the marker from an internal command, or 'external' if the marker is from create_marker or read_markers. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> unknown check external check_place route_litho route_design pg_ccopt <b>Default:</b> "" <b>Edit:</b> No
<b>polygon</b>	
	Polygon boundary for the marker if it is not a rectangle. The first point is not repeated as the last point in the list. <b>Type:</b> <a href="#">polygon</a> <b>Default:</b> "" <b>Edit:</b> No
<b>subtype</b>	
	The marker subtype if it was created be an internal check or report command (when .originator != external). <b>Type:</b> <a href="#">string</a> <b>Default:</b> {} <b>Edit:</b> No
<b>type</b>	

	The marker type if it was created by an internal check or report command (when .originator != external). <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> none drc antenna connectivity floorplan overlap density ir_drop xtalk ac_limit mixed_signal electrical place route_litho busplanning msv ccopt <b>Default:</b> "" <b>Edit:</b> No
<b>user_originator</b>	
	The originator given by the user for external markers from create_marker or read_marker (when .originator == external). <b>Type:</b> <a href="#">string</a> <b>Default:</b> {} <b>Edit:</b> No
<b>user_subtype</b>	
	The type given by the user for external markers from create_marker or read_marker (when .originator == external). <b>Type:</b> <a href="#">string</a> <b>Default:</b> {} <b>Edit:</b> No
<b>user_type</b>	
	The type given by the user for external markers from create_marker or read_marker (when .originator == external). <b>Type:</b> <a href="#">string</a> <b>Default:</b> {} <b>Edit:</b> No

# module

## Parent Objects

[hinst](#), [design](#), [root](#)

## Definition

Cell module

Attribute	Description
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allow_ilm_eco	<p>The attribute is only valid when the module is an ILM. If true, optimizer can optimize the ILM boundary interface logic to improve timing</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
design	<p>The design that contains this module.</p> <p><b>Type:</b> <a href="#">obj.design</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
dont_touch	<p>This attribute defines the user preservation status of the module during optimization. Setting this attribute will set the dont_touch attribute on all hinsts of the same module. This setting will apply to all insts within the hinst unless overridden at a lower level hinst or on the inst object itself. The dont_touch_effective attribute on each child inst and hinst will return the resolved value.</p> <p>Use 'help inst dont_touch' to see the enum value definitions.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none false true delete_ok const_prop_size_delete_ok      const_prop_delete_ok size_delete_ok size_ok size_same_height_ok      size_same_footprint_ok</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p>
dont_touch_hports	

	<p>This attribute defines the user preservation status for the module object hports during optimization.</p> <p><b>Supported values:</b></p> <ul style="list-style-type: none"> <li>none: Unconstrained</li> <li>false: Can add/remove ports</li> <li>true: Cannot add/remove ports</li> <li>delete_ok: Can delete ports (if they have no fanout)</li> <li>add_ok: We cannot delete, or change the polarity or any hport but can add or duplicate hports</li> <li>invert_ok: We cannot delete, duplicate, or add but can change the polarity of any hport</li> <li>add_invert_ok: We cannot delete any hport but can add, duplicate, and change the polarity</li> </ul> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none false true delete_ok add_ok invert_ok add_invert_ok</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p>
	<p>dont_use_cells</p>
	<p>List of cell names (wildcards supported) to disallow for this module during optimization. Setting this applies to all hinsts sharing the module. Overrides any library dont_use values</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
	<p>dont_use_cells_effective</p>
	<p>The resolved list of all cell names to disallow during optimization for hinsts of this module, based on the library dont_use and the dont_use_cells and use_cells attributes of this module or the closest parent hinst with a non-empty list. The precedence is: use_cells of this hinst (or closest parent if empty), then dont_use_cells of this hinst (or closest parent if empty), then the library dont_use setting.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p>hinsts</p>
	<p>The hinsts that are derived from (instantiate) this module.</p> <p><b>Type:</b> <a href="#">obj(hinst)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p>is_ilm</p>

	<p>This attribute is true if the module is a ILM. This attribute will affect the read_only_effective and dont_touch_effective attribute on all insts and hinsts within the hinsts of this module. It cannot be overridden by other hinst or inst values.</p> <p><b>Supported values:</b></p> <p>false: This module is not an ILM true: This module is an ILM</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> No</p>
name	
	<p>Name of cell</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (module)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
use_cells	<p>List of cell names to allow for this module during optimization. Setting this applies to all hinsts sharing the module. All lib_cells of each base_cell will be allowed. Overrides cells in the dont_use_cells list and any library dont_use values.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>

## net

### Parent Objects

[flexible\\_htree](#), [bus](#), [resistor](#), [port](#), [special\\_wire](#), [hpin](#), [hnet](#), [what\\_if\\_wire](#), [via](#), [what\\_if\\_via](#), [design](#), [clock\\_tree](#), [net\\_group](#), [bump](#), [root](#), [power\\_domain](#), [virtual\\_wire](#), [pg\\_pin](#), [patch\\_wire](#), [wire](#), [pin](#), [special\\_via](#), [route\\_type](#)

### Definition

canonical net

Attribute	Description
annotated_capacitance_max	<p>Returns maximum annotated capacitance of the net for late path analysis. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
annotated_capacitance_min	<p>Returns the minimum annotated capacitance of the net for early path analysis. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
annotated_resistance_max	<p>Returns the maximum annotated resistance of the net for late path analysis. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
annotated_resistance_min	<p>Returns the minimum annotated resistance of the net for early path analysis. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
arcs	<p>Returns a list of arc objects that are associated with this net.</p> <p><b>Type:</b> <a href="#">obj(arc)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
base_name	

	<p>The name at the base of a hierarchical name. So the base_name of i1/i2/i3 is i3.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
bbox	<p>Bounding box of all the wires, vias, pins, and ports of the net. Does not include special wires or special vias.</p> <p><b>Type:</b> <a href="#">rect</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
bottom_preferred_layer	<p>The preferred lowest routing layer. This attribute is a soft limit; that is, NanoRoute might use a layer below the specified layer if necessary to complete routing.</p> <p><b>Type:</b> <a href="#">obj(layer)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
bus	<p>The bus for this net.</p> <p><b>Type:</b> <a href="#">obj(bus)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
capacitance_max	<p>Returns the total capacitance of the net used for late path analysis. You can use -index to return the capacitance for specific views.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
capacitance_min	<p>Returns the total capacitance of the net for early path analysis. You can use -index to return the capacitance for specific views.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
constant	

	<p>Returns if this net has a 1'b0 or 1'b1 on any hpin or hnet, or a supply0/supply1 for any hnet. It does not include timing set_case_analysis assertions, or propagation through cells, or the effects of a constant driver on the net.</p> <p><b>Type:</b> <code>enum</code></p> <p><b>Enum Values:</b> 0 1 no_constant</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>coupling_capacitance_max</b>	
	<p>Returns the maximum value of coupling capacitance of a net over all the views.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>coupling_capacitance_min</b>	
	<p>Returns the minimum value of coupling capacitance of a net over all the views.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>cts_net_type</b>	
	<p>For a net, return the CTS net type.</p> <p>Will be one of:</p> <ul style="list-style-type: none"> <li>. "top" - A clock net that has fanout above cts_top_fanout_transitive_count.</li> <li>. "trunk" - A CTS clock net that is not a "top" net nor a "leaf" net.</li> <li>. "leaf" - A CTS clock net that has fanout to only clock sinks.</li> <li>. "unknown" - A CTS clock net that has not been analyzed.</li> <li>. "" - Not a CTS clock net.</li> </ul> <p>See also the get_clock_tree_nets command.</p> <p><b>Type:</b> <code>string</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>dont_touch</b>	

	<p>This attribute defines the preservation status of an net during optimization. Setting this attribute will preserve all connections on this net. When set, this overrides any setting on hnets of this net. Also, note that the .use attribute for the net can also cause the net to be preserved.</p> <p><b>Supported values:</b></p> <ul style="list-style-type: none"> <li>false: Unconstrained</li> <li>true: Cannot touch</li> <li>delete_ok: Can delete (if they have no sinks)</li> </ul> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> false true delete_ok</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
driver_pins	<p>These are the drivers of the net that are pins (no port drivers are returned). Pins that have direction = out or inout are considered drivers.</p> <p><b>Type:</b> obj(pin)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
driver_ports	<p>These are the drivers of the net that are ports (no pin drivers are returned). Ports that have direction = in or inout are considered drivers.</p> <p><b>Type:</b> obj(port)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
drivers	<p>Ports and pins that drive the net. These are pins that have direction = out or inout, and ports that have direction = in or inout.</p> <p><b>Type:</b> obj(pin)* obj(port)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
early_fall_clk_net_delta_derate_factor	<p>Returns the early derating factor for falling SI/delta delays on data path nets. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
early_fall_clk_net_derate_factor	

	Returns the early derating factor for falling static delays on clock path nets. You can use -index to return the derate factor for specific views. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
early_fall_data_net_delta_derate_factor	Returns the early derating factor for falling SI/delta delays on clock path nets. You can use -index to return the derate factor for specific views. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
early_fall_data_net_derate_factor	Returns the early derating factor for falling static delays on data path nets. You can use -index to return the derate factor for specific views. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
early_rise_clk_net_delta_derate_factor	Returns the early derating factor for rising SI/delta delays on data path nets. You can use -index to return the derate factor for specific views. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
early_rise_clk_net_derate_factor	Returns the early derating factor for rising static delays on clock path nets. You can use -index to return the derate factor for specific views. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
early_rise_data_net_delta_derate_factor	

	<p>Returns the early derating factor for rising SI/delta delays on clock path nets. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
early_rise_data_net_derate_factor	<p>Returns the early derating factor for rising static delays on data path nets. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
escaped_name	<p>The full hierarchical name including escaped chars (if any). It follows DEF escaping syntax, so bus-bit chars [], or a hierarchy char \ that is not a bus-bit or hierarchy char has a \ in front of it. So i1/i2 is a two-level hierarchical name while i1\i2 is single level name, and a[0] is a bus-bit, while a\[0\] is a scalar.</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
frequency	<p>Reports the frequency of the net.</p> <p><b>Type:</b> double</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
has_detailed_parasitics	<p>Returns a value of true if the net, or one of its parts, has detailed parasitics associated with it from either RC extraction or SPEF annotation.</p> <p><b>Type:</b> bool</p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
hnets	

	<p>List of hNets which make up this net.</p> <p><b>Type:</b> <a href="#">obj(hnet)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_avoid_detour_route	<p>Avoids detours of roughly more than a few gcell grids on the specified nets (affects global routing only).</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
is_clock	<p>Indicates that net is a clock according to timing constraints and tracing. It is only valid if the timing-graph has been created.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_custom_route	<p>Indicates that the net has Virtuoso/OA custom routing constraints that NR does not support, so NR should not route this net.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_early_global_routed	<p>Indicate that the net is from early global route</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
is_edit	<p>Indicate that the wire/via on the net has been modified. This attribute only works when "set_db edit_wire_create_is_edit_flag 1". Please look up for more details by "help edit_wire_create_is_edit_flag".</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
is_external	

	Indicates that net is connected to a to a top-level port. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_fixed_bump	Indicates that net is fixed to bump connection. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_ground	Indicate that the net is ground net <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_ideal	Returns true if the net is part of an ideal network due to the assertion or propagation of the set_ideal_network constraint. You can use -index to return the is_ideal value for specific views. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
is_ilm	Specify if a top level net is connecting to ILM (Interface Logic Model) modules and some or all terms (either drive or sink) of the net are inside ILM module. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_physical_only	Indicates that the net is a physical only net that does not get written to logical Verilog netlist. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_power	

	<p>Indicate that the net is power net</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p><code>is_trunk_pattern_route</code></p>
	<p>Indicates that the net is routed with a trunk pattern</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p><code>late_fall_clk_net_delta_derate_factor</code></p>
	<p>Returns the late derating factor for falling SI/delta delays on data path nets. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> <code>analysis_view</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p><code>late_fall_clk_net_derate_factor</code></p>
	<p>Returns the late derating factor for falling static delays on clock path nets. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> <code>analysis_view</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p><code>late_fall_data_net_delta_derate_factor</code></p>
	<p>Returns the late derating factor for falling SI/delta delays on clock path nets. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> <code>analysis_view</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p><code>late_fall_data_net_derate_factor</code></p>
	<p>Returns the late derating factor for falling static delays on data path nets. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> <code>analysis_view</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

late_rise_clk_net_delta_derate_factor	<p>Returns the late derating factor for rising SI/delta delays on data path nets. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
late_rise_clk_net_derate_factor	<p>Returns the late derating factor for rising static delays on clock path nets. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
late_rise_data_net_delta_derate_factor	<p>Returns the late derating factor for rising SI/delta delays on clock path nets. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
late_rise_data_net_derate_factor	<p>Returns the late derating factor for rising static delays on data path nets. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
load_pins	<p>These are the loads of the net that are pins (no port loads are returned). Pins that have direction = in or inout are considered loads.</p> <p><b>Type:</b> obj(pin)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
load_ports	

	<p>These are the loads of the net that are ports (no pin loads are returned). Ports that have direction = out or inout are considered loads.</p> <p><b>Type:</b> <a href="#">obj(port)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
loads	<p>Ports and pins that are loads for the net. These are pins that have direction = in or inout, and ports that have direction = out or inout.</p> <p><b>Type:</b> <a href="#">obj(pin)</a>* <a href="#">obj(port)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
mask	<p>Indicates mask number for multiple mask layer usage. Refer to layer .numMask attributes for valid range, 0 indicates unconstrained. Layers that do not support the specified value will be treated as unconstrained. (Legal range: 0-3).</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
max_voltage	<p>Max voltage for the net, determined by the max net voltage of all active hold views. Net voltage is determined using the following procedure: voltage from net's driver pin, associated power from CPF related_power_pins command or Liberty related_pg_pin attribute or LEF SUPPLYSENSITIVITY statement; power domain operating voltage; or default system voltage.</p> <p><b>Type:</b> <a href="#">voltage</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
min_voltage	<p>Min voltage for the net, determined by the min net voltage of all active setup views. Net voltage is determined using the following procedure: voltage from net's driver pin, associated power from CPF related_power_pins command or Liberty related_pg_pin attribute or LEF SUPPLYSENSITIVITY statement; power domain operating voltage; or default system voltage.</p> <p><b>Type:</b> <a href="#">voltage</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
name	

	<p>The same as .escaped_name without any \ escape chars. This name is commonly used to avoid problems with \ escape chars in Tcl scripts unless you carefully use list operators. Like SDC commands, 'get_db insts i1/i2' will first try to match i1/i2, and if not found then match i1\i2 so that flattening hierarchical names (e.g. with ungroup) does not require changing the names in Tcl scripts.</p> <p><b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No</p>
<b>num_connections</b>	
	<p>Number of connections to the net (number of pins + number of ports)</p> <p><b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No</p>
<b>num_drivers</b>	
	<p>Number of drivers for the net. These are pins that have direction = out or inout, and ports that have direction = in or inout.</p> <p><b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No</p>
<b>num_loads</b>	
	<p>Number of loads for the net. These are pins that have direction = in or inout, and ports that have direction = out or inout.</p> <p><b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No</p>
<b>obj_type</b>	
	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> enum (net) <b>Default:</b> "" <b>Edit:</b> No</p>
<b>patch_wires</b>	
	<p>List of patch_wire</p> <p><b>Type:</b> obj(patch_wire)* <b>Default:</b> "" <b>Edit:</b> No</p>
<b>pin_capacitance_max</b>	

	<p>Returns the portion of the net's total capacitance which comes the library max pin capacitance values. This is used for late path delay calculation. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>pin_capacitance_max_fall</b>	
	<p>pin_capacitance_max_fall</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>pin_capacitance_max_rise</b>	
	<p>pin_capacitance_max_rise</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>pin_capacitance_min</b>	
	<p>Returns the portion of the net's total capacitance which comes the library min pin capacitance values. This is used for early path delay calculation. You can use -index to return the derate factor for specific views.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>pin_capacitance_min_fall</b>	
	<p>pin_capacitance_min_fall</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>pin_capacitance_min_rise</b>	

	pin_capacitance_min_rise <b>Type:</b> double <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
power_duty_cycle	  <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
power_ref_clock	The static probability of the signal to stay high during one clock cycle. It is a value between 0.0 and 1.0. no_value is returned if it cannot be computed. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
power_switching	The switching power of this net computed by report_power. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
power_toggle_per_clock	The number of toggles per clock cycle. It is computed from power_toggle_rate * <period of power_ref_clock>. It can be as high as 2.0 for a clock, and is between 0 and 1 for a signal net. If there is more than one output pin, then it is the average of all the output pin power_toggle_rates. no_value is returned if no value can be computed. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
power_toggle_rate	The average number of toggles read from VCD, TCF, SAIF, etc. or from propagation that occur in 1 second on the net. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
power_toggle_rate_max	

	<p>The average number of toggles read from VCD, TCF, SAIF, etc. or from propagation that occur in 1 second on the net.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>power_toggle_rate_source</b>	
	<p>The source of the power_toggle_rate value. The enum values mean:  <b>asserted</b>: the value is user-specified by direct assertion or from a switching activity file.  <b>clock</b>: the value is derived from the clock waveform.  <b>computed</b>: the value is computed by propagating internal switching activity.  <b>constant</b>: the value is driven by a constant value (e.g. from set_case_analysis or tie-offs).  <b>default</b>: the value is not user-specified, but determined from the root power_default_toggle_rate attribute.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>preferred_extra_space</b>	
	<p>Gives additional spacing to the specified net in units of routing-pitch. Use this attribute to give critical nets extra space to reduce coupling. Legal range: 0-3</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
<b>resistance_max</b>	
	<p>Returns the maximum resistance of the net for late path analysis. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>resistance_min</b>	
	<p>Returns the minimum resistance of the net for early path analysis. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>route_rule</b>	

	Routing rule for this net (NDR) <b>Type:</b> <a href="#">obj(route_rule)</a> <b>Default:</b> "" <b>Edit:</b> Yes
<b>shield_nets</b>	
	1 or 2 shield nets. Must be power or ground nets <b>Type:</b> <a href="#">obj(net)</a> <b>Default:</b> "" <b>Edit:</b> No
<b>si_post_route_repair</b>	
	Specifies that antenna violations should not be corrected by the routing as the violation will be corrected in a different level of the design hierarchy. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
<b>skip_antenna_repair</b>	
	Specifies that antenna violations should not be corrected by the routing as the violation will be corrected in a different level of the design hierarchy. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
<b>skip_routing</b>	
	Specifies that Nanoroute should not route or re-route the net. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
<b>special_vias</b>	
	List of special vias. <b>Type:</b> <a href="#">obj(special_via)</a> * <b>Default:</b> "" <b>Edit:</b> No
<b>special_wires</b>	
	List of special_wires (DEF SPECIALNETS equivalent) <b>Type:</b> <a href="#">obj(special_wire)</a> * <b>Default:</b> "" <b>Edit:</b> No

top_preferred_layer	
	<p>The preferred highest routing layer. This attribute is a soft limit. The router considers it high cost to go above this layer, but might still use a higher layer in order to avoid DRC violations.</p> <p><b>Type:</b> <a href="#">obj(layer)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
use	
	<p>Indicates how this net is used. The enum values correspond to DEF and OpenAccess enum names. By default nets are 'signal'. Power/ground nets get marked 'power' or 'ground' when they are created. The clock tree creation commands set any net added for the clock tree to 'clock'. In practice the other values like 'scan' or 'tieoff' are not used anymore.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> signal analog clock ground power scan tieoff</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
vias	
	<p>List of vialnsts.</p> <p><b>Type:</b> <a href="#">obj(via)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
virtual_wires	
	<p>List of virtual_wire</p> <p><b>Type:</b> <a href="#">obj(virtual_wire)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
weight	
	<p>Net weight.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 2</p> <p><b>Edit:</b> Yes</p>
what_if_vias	
	<p>List of 'what if' vias.</p> <p><b>Type:</b> <a href="#">obj(what_if_via)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
what_if_wires	

	<p>List of 'what if' wires  <b>Type:</b> <a href="#">obj(what_if_wire)*</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>wire_capacitance_max</b>	
	<p>Returns the portion of the net's total capacitance which comes extracted or annotated wire capacitance values. This is used for late path delay calculation. You can use -index to return the derate factor for specific views.  <b>Type:</b> <a href="#">double</a>  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>wire_capacitance_max_fall</b>	
	<p>Returns the wire capacitance of the net for the maximum value of the falling capacitance range.  <b>Type:</b> <a href="#">double</a>  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>wire_capacitance_max_rise</b>	
	<p>Returns the wire capacitance of the net for the maximum value of the rising capacitance range.  <b>Type:</b> <a href="#">double</a>  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>wire_capacitance_min</b>	
	<p>Returns the portion of the net's total capacitance which comes extracted or annotated wire capacitance values. This is used for early path delay calculation. You can use -index to return the derate factor for specific views.  <b>Type:</b> <a href="#">double</a>  <b>Allowed -index values:</b> analysis_view  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>wire_capacitance_min_fall</b>	

	<p>Returns the wire capacitance of the net for the minimum value of the falling capacitance range.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>wire_capacitance_min_rise</b>	
	<p>Returns the wire capacitance of the net for the minimum value of the rising capacitance range.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>wires</b>	
	<p>List of wires</p> <p><b>Type:</b> <a href="#">obj(wire)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## net\_group

### Parent Objects

[design](#), [bus\\_guide](#), [pin\\_guide](#), [root](#)

### Definition

Net Group

Attribute	Description
<b>exclude_net</b>	<p>Indicates group net exclude type(all_layer, same_layer, inclusive, all_layer_in_guided_area)</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> all_layer_in_guided_area all_layer same_layer inclusive</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>

**Stylus Common UI Database Object Information**  
Database Objects--net\_group

is_compact	
	Indicate whether the nets in the group are assigned tightly together. By default, nets which are part of a group and associated to a guide can be spread inside the guide based on the area available and alignment to targets <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes
is_guided	
	Indicates if net group is guided <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes
is_optimize_order	
	Indicates whether net order will be optimized <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes
is_spread	
	Indicates whether member nets distributed evenly <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes
keep_out_space	
	Minimum spacing with pin of foreign nets (Unit: track) <b>Type:</b> int <b>Default:</b> 0 <b>Edit:</b> Yes
name	
	Group name <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
nets	

	<p>List of member nets to this net group  <b>Type:</b> obj(net)  <b>Default:</b> ""  <b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a>  <b>Type:</b> enum (net_group)  <b>Default:</b> ""  <b>Edit:</b> No</p>

## obj\_type

### Parent Objects

[attribute](#), [root](#)

### Definition

Attribute	Description
accept_user_defined_attributes	<p>Specifies whether new attributes can be added by user.  <b>Type:</b> bool  <b>Default:</b> ""  <b>Edit:</b> No</p>
attributes	<p>list of attribute for this obj_type  <b>Type:</b> obj(attribute)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
help	<p>Specifies the help text for the object  <b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>

name	
	obj_type name like inst, lib_cell, etc. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (obj_type) <b>Default:</b> "" <b>Edit:</b> No

## opcond

### Parent Objects

[timing\\_condition](#), [root](#)

### Definition

An opcond represents a named operating condition which is defined by specific process, voltage, and temperature values. Opcond objects may preexist within a Liberty library or "virtual" opconds may be created using the `create_opcond` command. Virtual opconds can also be modified by using the `update_opcond` command.

Attribute	Description
base_name	The base name of the opcond without any leading library_set or library names (e.g. op1 for libset1/lib1/op1). <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
is_virtual	

	Indicates that this opcond object is a virtual opcond created by the create_opcond command vs. an opcond that is created by reading a Liberty timing library file.  <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
name	The full name of the opcond. The opcond name from a Liberty file includes the library_set and library names (e.g. libset1/lib1/op1) while the full name from create_opcond is just the opcond name (e.g. op1).  <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a>  <b>Type:</b> <a href="#">enum (opcond)</a> <b>Default:</b> "" <b>Edit:</b> No
process	Specifies the Process value of the opcond  <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No
temperature	Specifies the Temperature value of the opcond in Celsius.  <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No
tree_type	

	<p>The Liberty tree_type model. It is an enum with these choices: none means there is no tree_type value given; best_case_tree models each load pin is close to the driver, so wire capacitance is incurred, but wire resistance is ignored; balanced_tree models when all load pins are on equal branches, so each load pin has an equal portion of the total wire cap and resistance; worst_case_tree models when the load pin is at the extreme end of the wire, so each load pin incurs the full wire capacitance and resistance</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none best_case_tree balanced_tree worst_case_tree</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
voltage	
	<p>Specifies the Voltage value of the opcond in units of the library it came from.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## package\_component

### Parent Objects

[design](#)

### Definition

pkg component

Attribute	Description
cell_name	<p>The name of other chip cell in the package</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
inst_name	<p>The name of other chips in the package</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (package_component)</a> <b>Default:</b> "" <b>Edit:</b> No
pt	Location of the other chips in the package <b>Type:</b> <a href="#">point</a> <b>Default:</b> "" <b>Edit:</b> No
ref_design	Another identifying name of the chip in the package <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
size	Size of the cell <b>Type:</b> <a href="#">point</a> <b>Default:</b> "" <b>Edit:</b> No

## package\_object

### Parent Objects

[design](#), [root](#)

### Definition

pkg object

Attribute	Description
die_net_name	

**Stylus Common UI Database Object Information**  
Database Objects--package\_object

	the name of die net which this package object connected to <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
layer_name	The package layer that this package object belongs to <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
name	The name of this package object <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (package_object)</a> <b>Default:</b> "" <b>Edit:</b> No
package_net_name	the name of package net which this package object connected to <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
pt	Location of the package object <b>Type:</b> <a href="#">point</a> <b>Default:</b> "" <b>Edit:</b> No
size	Size of the package object <b>Type:</b> <a href="#">point</a> <b>Default:</b> "" <b>Edit:</b> No
type	

	the type of this package object <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> bga_ball bond_finger bond_wire route flight_line component other <b>Default:</b> "" <b>Edit:</b> No
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# partition

## Parent Objects

[hinst](#), [inst](#), [design](#), [pin\\_group](#), [pin\\_guide](#), [root](#)

## Definition

Partition Object

Attribute	Description
base_pins	List of partition pins. It is valid only if partition is in non-committed state, i.e. partition module is instantiated as hinst. Otherwise it is set to NULL. <b>Type:</b> <a href="#">obj(base_pin)*</a> <b>Default:</b> "" <b>Edit:</b> No
clones	List of clone inst/hinsts. The obj_type returned will be inst if the partition is committed or a blackbox, otherwise the obj_type will be hinst. <b>Type:</b> <a href="#">obj(inst)* obj(hinst)*</a> <b>Default:</b> "" <b>Edit:</b> No
core_to_bottom	Spacing between the partition boundary and core design area of the partition module <b>Type:</b> <a href="#">coord</a> <b>Default:</b> no_value <b>Edit:</b> Yes
core_to_left	

**Stylus Common UI Database Object Information**  
**Database Objects--partition**

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	<p>Spacing between the partition boundary and core design area of the partition module</p> <p><b>Type:</b> coord</p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p>
core_to_right	<p>Spacing between the partition boundary and core design area of the partition module</p> <p><b>Type:</b> coord</p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p>
core_to_top	<p>Spacing between the partition boundary and core design area of the partition module</p> <p><b>Type:</b> coord</p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p>
hpins	<p>Hierarchical instance pin of the partition. It is only valid if the partition is uncommitted and still an hinst.</p> <p><b>Type:</b> obj(hpin)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_black_box	<p>Specifies if partition is a blackbox</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_committed	<p>Specifies if partition is committed</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
master	<p>The master inst/hInst. The obj_type returned will be inst if the partition is committed or a blackbox, otherwise the objType will be hInst.</p> <p><b>Type:</b> obj(inst)* obj(hinst)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

min_pitch_bottom	
	<p>Specifies the pin pitch (in tracks)  <b>Type:</b> int  <b>Default:</b> 0  <b>Edit:</b> Yes</p>
min_pitch_left	
	<p>Specifies the pin pitch (in tracks)  <b>Type:</b> int  <b>Default:</b> 0  <b>Edit:</b> Yes</p>
min_pitch_right	
	<p>Specifies the pin pitch (in tracks)  <b>Type:</b> int  <b>Default:</b> 0  <b>Edit:</b> Yes</p>
min_pitch_top	
	<p>Specifies the pin pitch (in tracks)  <b>Type:</b> int  <b>Default:</b> 0  <b>Edit:</b> Yes</p>
name	
	<p>name of the partition  <b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>
obj_type	
	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a>  <b>Type:</b> enum (partition)  <b>Default:</b> ""  <b>Edit:</b> No</p>
pin_bottom_layers	
	<p>List of bottom layers to use for the partition  <b>Type:</b> obj(layer)*  <b>Default:</b> ""  <b>Edit:</b> Yes</p>

pin_left_layers	<p>List of left layers to use for the partition  <b>Type:</b> <a href="#">obj(layer)</a>*  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
pin_right_layers	<p>List of right layers to use for the partition  <b>Type:</b> <a href="#">obj(layer)</a>*  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
pin_to_corner_tracks	<p>Minimum number of routing tracks between pins and each corner. It is a list of int values, where the first value is for the lower-left corner, and the remaining corners are listed in clockwise order.  <b>Type:</b> <a href="#">int</a>*  <b>Default:</b> ""  <b>Edit:</b> No</p>
pin_top_layers	<p>List of top layers to use for the partition  <b>Type:</b> <a href="#">obj(layer)</a>*  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
place_halo_bottom	<p>Specifies extra spacing around the partition that should not be used for placement  <b>Type:</b> <a href="#">coord</a>  <b>Default:</b> no_value  <b>Edit:</b> Yes</p>
place_halo_left	<p>Specifies extra spacing around the partition that should not be used for placement  <b>Type:</b> <a href="#">coord</a>  <b>Default:</b> no_value  <b>Edit:</b> Yes</p>
place_halo_right	

**Stylus Common UI Database Object Information**  
**Database Objects--partition**

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	<p>Specifies extra spacing around the partition that should not be used for placement</p> <p><b>Type:</b> <a href="#">coord</a></p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p>
place_halo_top	<p>Specifies extra spacing around the partition that should not be used for placement</p> <p><b>Type:</b> <a href="#">coord</a></p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p>
rail_width	<p>Specifies the cell rail width</p> <p><b>Type:</b> <a href="#">coord</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
read_only	<p>This attribute is set by set_module_view to identify if a partition is read only or not. It means the partition cannot be optimized, and cells inside will not be moved. Setting this attribute will set the dont_touch_effective attribute on all insts and hinsts within the partition unless overridden at a lower level partition. It cannot be overridden by other hinst or inst values.</p> <p><b>Supported values:</b></p> <ul style="list-style-type: none"> <li>false: This partition is allowed to be optimized, even if a partition or design above has read_only = true.</li> <li>true: The partition is read_only.</li> <li>none: No constraint. This partition inherits any read_only from a partition or design above.</li> </ul> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none false true</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> No</p>
reserved_layers	<p>List of metal layers which are used for routing in the partition and generating partition pins. Any metal layers that are not specified, usually the top-most metal layers, are allowed to route over the partition</p> <p><b>Type:</b> <a href="#">obj(layer)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
route_halo_bottom_layer	

	The bottom partition layer for which routing halo will be created <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> Yes
route_halo_to_boundary	
	Specifies routing halo around the partition (honored by signal router). Positive values indicate the halo is outside the partition. Negative values indicate the halo is inside of the boundary of the partition and will be pushed into the partition when the partition is committed. <b>Type:</b> <a href="#">coord</a> <b>Default:</b> no_value <b>Edit:</b> Yes
route_halo_top_layer	
	The top partition layer for which routing halo will be created <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> Yes

## patch\_wire

### Parent Objects

[net](#)

### Definition

DEF NETS RECT wire

Attribute	Description
has_trim_metal	Indicate the path wire has trim metal or not <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
layer	

**Stylus Common UI Database Object Information**  
Database Objects--patch\_wire

	<p>The layer of patch <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> No</p>
location	
	<p>Reference point to symbolic location <b>Type:</b> <a href="#">point</a> <b>Default:</b> "" <b>Edit:</b> No</p>
mask	
	<p>Indicates mask number for multiple mask layer usage. Refer to layer's .numMask attribute for legal range, 0 indicates uncolored. <b>Type:</b> <a href="#">int</a> <b>Default:</b> 0 <b>Edit:</b> Yes</p>
net	
	<p>The net that the patch belongs to <b>Type:</b> <a href="#">obj(net)</a> <b>Default:</b> "" <b>Edit:</b> No</p>
obj_type	
	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (patch_wire)</a> <b>Default:</b> "" <b>Edit:</b> No</p>
rect	
	<p>Rectangle that defines the patch_wire shape <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No</p>
route_rule	
	<p>The non-default rule corresponding to the wire, wires with the default routing rule will return NULL (0x0). <b>Type:</b> <a href="#">obj(route_rule)</a> <b>Default:</b> "" <b>Edit:</b> No</p>

status	
	<p>Wiring status (equivalent to DEF NETS regular wiring status)</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> unknown routed fixed cover noshield</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
trim_metal_color	
	<p>Color of this patch wire trim metal</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
trim_metal_rect	
	<p>The trim_metal rect if the patch_wire has a trim_metal shape attached. This only occurs for some advanced node layers that use self-aligned patterning. {0 0 0} is returned if there is no trim_metal attached.</p> <p><b>Type:</b> <a href="#">rect</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## path\_group

### Parent Objects

[timing\\_path](#)

### Definition

cte path group

Attribute	Description
name	<p>The name of the path_group.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obj_type	

	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (path_group)</a> <b>Default:</b> "" <b>Edit:</b> No
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## pg\_base\_pin

### Parent Objects

[base\\_cell](#), [root](#), [pg\\_pin](#)

### Definition

A power or ground pin for a base\_cell.

Attribute	Description
base_cell	<p>The base_cell of this pg_base_pin. <b>Type:</b> <a href="#">obj(base_cell)</a>* <b>Default:</b> "" <b>Edit:</b> No</p>
base_name	<p>The base name of this pg_base_pin without the base_cell name (e.g. vdd). <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No</p>
direction	

	<p>The pin direction from .lib if available, otherwise from LEF/OA. It can be in, out, inout or internal. Internal means it is an internal pin from a .lib file for the timing model, and is not part of the netlist. If there is no .lib for this cell, then the direction comes from the LEF PIN DIRECTION or equivalent OA oaTermType. The LEF DIRECTION values (and equivalent oaTermType values) are mapped this way: INPUT = in, OUTPUT = out, OUTPUT TRISTATE = out, INOUT = inout, FEEDTHRU = inout, and the oaTermType unknown = inout.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> in out inout internal</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_always_on	<p>This pg_base_pin is an always on power pin. This attribute can be set by liberty files.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
name	<p>The name of this pg_base_pin with the base_cell name (e.g. and2/vdd).</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> enum (pg_base_pin)</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
pg_type	<p>The type of the power or ground pin from liberty data. PG pins with no liberty entry will have "invalid".</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> primary_power primary_ground backup_power backup_ground internal_power internal_ground pwell nwell deep_pwell deep_nwell invalid</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
physical_direction	

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**Database Objects--pg\_base\_pin**

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	<p>Direction of this pin.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> input output inout unknown feedthrough tristate</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>physical_pins</b>	
	<p>Physical pins for the pg_base_pin. One logical pg_base_pin can have multiple physical_pins (equivalent to separate LEF or DEF PORT statements for one LEF or DEF PIN). Each physical_pin normally has one shape, but may have multiple shapes that are all strongly connected to each other. By default, at least one shape of each physical_pin should be connected to the power-mesh.</p> <p><b>Type:</b> <a href="#">obj(physical_pin)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>taper_rule</b>	
	<p>The taper route_rule for the pg_pin. By default, if tapered routing is needed to access the pin, the default route_rule will be used unless this attribute is set (see LEF MACRO PIN TAPERRULE).</p> <p><b>Type:</b> <a href="#">obj(route_rule)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>tied_to</b>	
	<p>If this pg_base_pin is a substrate bias-pin (e.g. pg_type is nwell or pwell), and it is internally tied-to a "master" PG pin, this specifies the PG pin name (e.g. an nwell pin might have tied_to = vdd if it is internally connected to the vdd pin).</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>use</b>	
	<p>Indicates how this pg_base_pin is used from the LEF USE value or OA equivalent. Only power or ground enum values make sense in normal usage, but if there are conflicts between Liberty and LEF/OA definitions, you may have pg_base_pins that are marked in LEF/OA with the other values.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> signal analog power ground clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

# pg\_pin

## Parent Objects

[inst](#), [design](#), [root](#)

## Definition

Power or ground pin information

Attribute	Description
base_name	<p>The base name for this pg_pin without the base_cell name (e.g. vdd).</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
escaped_name	<p>The escaped name of this pg_pin.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
inst	<p>The inst containing this pg_pin.</p> <p><b>Type:</b> <a href="#">obj(inst)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
name	<p>The pg_pin name including the inst path (e.g. i1/i2/vdd)</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
net	

	The net connected to this pg_pin. <b>Type:</b> <a href="#">obj(net)</a> <b>Default:</b> "" <b>Edit:</b> No
<b>obj_type</b>	
	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (pg_pin)</a> <b>Default:</b> "" <b>Edit:</b> No
<b>pg_base_pin</b>	
	The corresponding pg_base_pin on the base_cell for this pg_pin. <b>Type:</b> <a href="#">obj(pg_base_pin)</a> <b>Default:</b> "" <b>Edit:</b> No

## physical\_pin

### Parent Objects

[pg\\_base\\_pin](#), [base\\_pin](#), [port](#)

### Definition

physical pin

Attribute	Description
class	
	Physical pin class <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> undefined none core bump <b>Default:</b> "" <b>Edit:</b> No
layer_shapes	

	<p>List of layer_shapes that define the terminal pin geometries.</p> <p><b>Type:</b> <a href="#">obj(layer_shape)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (physical_pin)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
port_number	<p>The port number for geometries under the physical_pin.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
shape_vias	<p>List of shape_vias that define the terminal pin geometries.</p> <p><b>Type:</b> <a href="#">obj(shape_via)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## pin

### Parent Objects

[clock](#), [skew\\_group](#), [hinst](#), [arc](#), [hnet](#), [timing\\_point](#), [design](#), [bus\\_sink\\_group](#), [clock\\_tree](#), [root](#), [timing\\_path](#), [inst](#), [net](#)

### Definition

Instance terminal

Attribute	Description
actual_latency_early_fall_max	

	<p>Returns the computed early falling clock latency to this clock pin. If the analysis mode is set to best-case/worst-case, the value will be the Setup capture latency. When operating in OCV mode, the max qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>actual_latency_early_fall_min</b>	
	<p>Returns the computed early falling clock latency to this clock pin. If the analysis mode is set to best-case/worst-case, the value will be the Hold launch latency. When operating in OCV mode, the min qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>actual_latency_early_rise_max</b>	
	<p>Returns the computed early rising clock latency to this clock pin. If the analysis mode is set to best-case/worst-case, the value will be the Setup capture latency. When operating in OCV mode, the max qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>actual_latency_early_rise_min</b>	

	<p>Returns the computed early rising clock latency to this clock pin. If the analysis mode is set to best-case/worst-case, the value will be the Hold launch latency. When operating in OCV mode, the min qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
actual_latency_late_fall_max	<p>Returns the computed late falling clock latency to this clock pin. If the analysis mode is set to best-case/worst-case, the value will be the Setup launch latency. When operating in OCV mode, the max qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
actual_latency_late_fall_min	<p>Returns the computed late falling clock latency to this clock pin. If the analysis mode is set to best-case/worst-case, the value will be the Hold capture latency. When operating in OCV mode, the min qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
actual_latency_late_rise_max	

	<p>Returns the computed late rising clock latency to this clock pin. If the analysis mode is set to best-case/worst-case, the value will be the Setup launch latency. When operating in OCV mode, the max qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
actual_latency_late_rise_min	<p>Returns the computed late rising clock latency to this clock pin. If the analysis mode is set to best-case/worst-case, the value will be the Hold capture latency. When operating in OCV mode, the min qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
arrival_max_fall	<p>Returns the latest falling arrival time to the specified pin across all concurrent MMMC views. You can use -index to determine the worst arrival for a specific view. You can also use -index to get the latest arrival time related to a specific clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
arrival_max_rise	<p>Returns the latest rising arrival time to the specified pin across all concurrent MMMC views. You can use -index to determine the worst arrival for a specific view. You can also use -index to get the latest arrival time related to a specific clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
arrival_mean_max_fall	

	<p>In SOCV analysis mode, this returns the mean value of the latest falling arrival time to the specified pin across all concurrent MMMC views. You can use -index to determine the latest arrival for a specific view. You can also use -index to get the worst arrival time related to a specific clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
arrival_mean_max_rise	<p>In SOCV analysis mode, this returns the mean value of the latest rising arrival time to the specified pin across all concurrent MMMC views. You can use -index to determine the latest arrival for a specific view. You can also use -index to get the worst arrival time related to a specific clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
arrival_mean_min_fall	<p>In SOCV analysis mode, this returns the mean value of the earliest falling arrival time to the specified pin across all concurrent MMMC views. You can use -index to determine the earliest arrival for a specific view. You can also use -index to get the earliest arrival time related to a specific clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
arrival_mean_min_rise	<p>In SOCV analysis mode, this returns the mean value of the earliest rising arrival time to the specified pin across all concurrent MMMC views. You can use -index to determine the earliest arrival for a specific view. You can also use -index to get the earliest arrival time related to a specific clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
arrival_min_fall	

	<p>Returns the earliest falling arrival time to the specified pin across all concurrent MMMC views. You can use -index to determine the worst arrival for a specific view. You can also use -index to get the earliest arrival time related to a specific clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>arrival_min_rise</b>	
	<p>Returns the earliest falling arrival time to the specified pin across all concurrent MMMC views. You can use -index to determine the worst arrival for a specific view. You can also use -index to get the worst arrival time related to a specific clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>arrival_sigma_max_fall</b>	
	<p>In SOCV analysis mode, this returns the variation component of the latest falling arrival time to the specified pin across all concurrent MMMC views. You can use -index to determine the latest arrival for a specific view. You can also use -index to get the worst arrival time related to a specific clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>arrival_sigma_max_rise</b>	
	<p>In SOCV analysis mode, this returns the variation component of the latest rising arrival time to the specified pin across all concurrent MMMC views. You can use -index to determine the latest arrival for a specific view. You can also use -index to get the worst arrival time related to a specific clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>arrival_sigma_min_fall</b>	

	<p>In SOCV analysis mode, this returns the variation component of the earliest falling arrival time to the specified pin across all concurrent MMMC views. You can use -index to determine the earliest arrival for a specific view. You can also use -index to get the earliest arrival time related to a specific clock.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> <code>analysis_view clock</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>arrival_sigma_min_rise</b>	
	<p>In SOCV analysis mode, this returns the mean value of the earliest rising arrival time to the specified pin across all concurrent MMMC views. You can use -index to determine the earliest arrival for a specific view. You can also use -index to get the earliest arrival time related to a specific clock.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> <code>analysis_view clock</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>arrival_window</b>	
	<p>Returns a list of the earliest and latest, rising and falling arrival times per clock phase at the pin across all concurrent MMMC views. You can use -index to make the arrival times specific to a given view</p> <p><b>Type:</b> <code>string</code></p> <p><b>Allowed -index values:</b> <code>analysis_view clock</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>base_name</b>	
	<p>The name at the base of a hierarchical name. So the <code>base_name</code> of <code>i1/i2/i3</code> is <code>i3</code>.</p> <p><b>Type:</b> <code>string</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>base_pin</b>	
	<p>pointer to equivalent base pin</p> <p><b>Type:</b> <code>obj(base_pin)</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>capacitance_max_fall</b>	

	<p>Returns the maximum value of the falling capacitance range of the corresponding library pin. You can use -index to return the value from a specific analysis view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
capacitance_max_rise	
	<p>Returns the maximum value of the rising capacitance range of the corresponding library pin. You can use -index to return the value from a specific analysis view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
capacitance_min_fall	
	<p>Returns the minimum value of the falling capacitance range of the corresponding library pin. You can use -index to return the value from a specific analysis view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
capacitance_min_rise	
	<p>Returns the minimum value of the rising capacitance range of the corresponding library pin. You can use -index to return the value from a specific analysis view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
cell_name	
	<p>Returns the name of the instance of the instance pin mentioned.</p> <p><b>Type:</b> string</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
clocks	

	<p>Returns a list of all of the clock objects arriving at the pin. You can use -index to return the value from a specific analysis view.</p> <p><b>Type:</b> <a href="#">obj(clock)</a>*</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
constant	<p>Returns if this pin has a constant logic value of 1'b0 or 1'b1 directly on the pin in the Verilog. If it is no_constant, and it is connected to a net, you must also check the net .constant value to see if the net driving the pin is constant.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> 0 1 no_constant</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
constant_value	<p>Returns a constant value of 0 or 1 if logic state has been asserted or propagated to this pin. You can use -index to return the value from a specific analysis view.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
cts_add_port_driver	<p>Specifies a cell type so that a cell inst can be added above an output port or below an input port.</p> <p>The port is specified by the argument pin.</p> <p>If the pin specified is not a design IO pin or it is not in the clock network then CCOpt will emit a warning and will not add cell insts at that position.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
cts_assign_clock_tree	

	<p>Can be used to make sure a clock tree sink pin gets driven by a particular clock tree. The clock tree can alternatively be specified as the tree's root pin, in case extraction renames the clock trees defined from a single SDC clock.</p> <p>By default CCOpt automatically selects appropriate pins.</p> <p>Valid values: cts_clock_tree   list of pins</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>cts_case_analysis</b>	
	<p>Specifies a constant value to be used as pin signal when analyzing timing within CTS. Only applies to input pins of cells in the clock tree. If set to 'none' (the default), CTS will consider the input as non-constant.</p> <p>Valid values: 0 1 none</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p>
<b>cts_clock_tree</b>	
	<p>The clock tree to which this object belongs. Flops do not belong to a clock tree, but their clock pins do.</p> <p>Valid values: cts_clock_tree</p> <p><b>Type:</b> <a href="#">obj(clock_tree)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>cts_clock_trees</b>	
	<p>A list of clock trees the pin is contained within. This includes parents of generated clock trees and all relevant parents when clock trees overlap.</p> <p>Valid values: list cts_clock_tree</p> <p><b>Type:</b> <a href="#">obj(clock_tree)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>cts_flexible_htree</b>	
	<p>The flexible HTree, if any, associated with the given object.</p> <p><b>Type:</b> <a href="#">obj(flexible_htree)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>cts_is_sdc_clock_root</b>	

	<p>Specifies whether the given pin is the root (source pin) of an SDC clock. The <code>create_clock_tree_spec</code> populates this attribute with the location of the SDC clock root (source) pins. This attribute controls the behavior of clock tree definition commands <code>create_clock_tree</code> and <code>create_generated_clock_tree</code>, when the <code>-stop_at_sdc_clock_roots</code> argument is specified. In such a case, pins and ports for which this attribute is true will be treated as being SDC clock root pins.</p> <p>Valid values: true false</p> <p><b>Type:</b> <code>bool</code>  <b>Default:</b> false  <b>Edit:</b> Yes</p>
<b>cts_net_unbufferable_reasons</b>	
	<p>This attribute contains a list of reasons why CCOpt was not able to buffer the clock net attached to the specified pin.</p> <p>Valid values: string</p> <p><b>Type:</b> <code>string</code>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>cts_node_type</b>	
	<p>node type of pin within cts graph</p> <p><b>Type:</b> <code>string</code>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>cts_pin_insertion_delay</b>	
	<p>The insertion delay under this pin.</p> <p>Valid values: double   auto</p> <p><b>Type:</b> <code>string</code>  <b>Allowed -index values:</b> <code>delay_corner</code>  <b>Default:</b> auto  <b>Edit:</b> Yes</p>
<b>cts_routing_trunk_override</b>	
	<p>Prefer trunk routing rules for this pin. Only applies to clock tree sinks.</p> <p>Valid values: true false</p> <p><b>Type:</b> <code>bool</code>  <b>Default:</b> false  <b>Edit:</b> Yes</p>
<b>cts_sink_type</b>	

	<p>The type of sink this pin represents.      Valid values are as follows:</p> <ul style="list-style-type: none"> <li>auto The sink type will be automatically determined by CCOpt.</li> <li>through Through pin. Trace the clock tree through this pin.</li> <li>stop Stop pin. When defining clock trees, CCOpt stops searching for parts of the clock tree at stop pins.</li> <li>ignore Ignore pin. CCOpt stops searching for parts of the clock tree at ignore pins and it does not attempt to balance the insertion delay of ignore pins.</li> <li>exclude Exclude pin. Exclude this pin from the clock tree.</li> </ul> <p>Valid values: auto through stop ignore exclude</p> <p><b>Type:</b> string  <b>Default:</b> auto  <b>Edit:</b> Yes</p>
<b>cts_sink_type_effective</b>	
	<p>Indicates how CCOpt will treat a given pin, taking into account both its cts_sink_type_implicit, and any cts_sink_type settings.</p> <p>Setting a non-default value for the cts_sink_type attribute will override the cts_sink_type_implicit attribute.</p> <p><b>Type:</b> string  <b>Default:</b> auto  <b>Edit:</b> No</p>
<b>cts_sink_type_implicit</b>	
	<p>Indicates the type of sink that CCOpt classified this pin as. Note that the cts_sink_type attribute can override these internal classifications.</p> <p>Possible values are:</p> <ul style="list-style-type: none"> <li>exclude Indicates that this pin is a sink which represents a non-clock pin.</li> <li>ignore Indicates that CCOpt has determined not to search for more clock tree through this pin. Additionally, this pin will not be balanced.</li> <li>stop Indicates that CCOpt has determined not to search for more clock tree through this pin. An empty value for this attribute indicates either that this pin is either not a sink, or that it is a sink that is not implicitly exclude or ignore or stop.</li> </ul> <p><b>Type:</b> string  <b>Default:</b> exclude  <b>Edit:</b> No</p>
<b>cts_sink_type_reasons</b>	

	<p>The reasons why this pin has the given cts_sink_type.      This attribute is configured by the create_clock_tree_spec command in order to record the reasons that the cts_sink_type attribute has been configured for the given pin.</p> <p>This attribute is a list of values. Valid values are as follows:</p> <ul style="list-style-type: none"> <li>auto The cts_sink_type attribute is set to 'auto'</li> <li>implicit The pin is an implicit sink (flop/latch)</li> <li>user The user has set the cts_sink_type attribute</li> <li>design_io This pin is a design I/O</li> <li>multiple_outputs This pin is on an instance with multiple outputs, and the cts_spec_config_trace_through_to attribute has not been set</li> <li>set_disable_timing SDC set_disable_timing stops the clock at this pin</li> <li>set_case_analysis SDC set_case_analysis stops the clock at this pin</li> <li>generated_clock_tree This pin is the generator input to an SDC generated clock</li> <li>no_sdc_clock The SDC clock is stopped at this pin for other reasons</li> <li>ilm The create_clock_tree_spec command has detected an ILM below this pin</li> </ul> <p>Valid values: auto implicit user design_output multiple_outputs set_disable_timing set_case_analysis generated_clock_tree no_sdc_clock ilm</p> <p><b>Type:</b> string  <b>Default:</b> auto  <b>Edit:</b> Yes</p>
cts_skew_groups_active	<p>Returns the list of active skew groups for this pin.      For sink pins, this attribute lists both skew groups that pass through this pin and skew groups for which this sink is an endpoint.      For non-sink pins, shows skew groups that pass through this pin.      Valid values: list skew_groups</p> <p><b>Type:</b> obj(skew_group)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
cts_skew_groups_active_sink	<p>Returns the list of skew groups for which this pin is an active sink.      For sink pins, this attribute lists the skew groups for which this sink is an endpoint. Skew groups that pass through this pin are not included.      For non-sink pins, this attribute always returns null.      Valid values: list skew_groups</p> <p><b>Type:</b> obj(skew_group)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
cts_skew_groups_ignore	

	<p>The list of skew groups for which paths through this pin are ignored. Valid values: list skew_groups <b>Type:</b> <a href="#">obj(skew_group)</a>* <b>Default:</b> "" <b>Edit:</b> No</p>
cts_skew_groups_sink	
	<p>The list of skew groups for which this pin is a sink. Valid values: list skew_groups <b>Type:</b> <a href="#">obj(skew_group)</a>* <b>Default:</b> "" <b>Edit:</b> No</p>
cts_skew_groups_source_pin	
	<p>The list of skew groups for which this clock tree or pin is specified as a source. Valid values: list skew_groups <b>Type:</b> <a href="#">obj(skew_group)</a>* <b>Default:</b> "" <b>Edit:</b> No</p>
cts_spec_config_trace_through_to	

	<p>Clock tree definition will, by default, not continue through certain types of cell arc (for instance, the clock to Q arc in a DFF). This attribute allows you to override this default behavior, permitting the clock tree to trace through such a cell.</p> <p>The attribute should be configured on the input pin at which the clock arrives. The value of the attribute specifies the output pin to which the clock should propagate. The specified output pin must be another pin on the same instance. The output pin may be specified either by its fully qualified name (i.e. inclusive of the instance name), or else simply by its local (cell-relative) name.</p> <p>There must be a pre-existing (library-defined) chain of one or more delay arcs that connect the input and output pins together. It is not possible to use trace_through_to to synthesize delay arcs.</p> <p>If multiple input pins are annotated on a given instance, the value of trace_through_to at each of those pins must select the same output pin: i.e. the configuration must identify a single clock output for the instance. If multiple clock outputs are required then trace_through_to should not be used: instead define a generated clock tree at each of the clock-carrying outputs.</p> <p>If the configuration of trace_through_to settings for a given instance does not meet these requirements, a warning will be issued and the settings for that instance will be ignored.</p> <p>Note: if both trace_through_to and library_trace_through_to are applicable at a given netlist instance pin, the trace_through_to value takes precedence.</p> <p>Valid values: pin</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>cts_top_fanout_count_override</b>	
	<p>The number of clock sinks this sink counts for when applying the top routing rules.</p> <p>Note that this attribute is only valid for sink pins, and it returns auto for non-sink pins.</p> <p>For a sink pin, a non-auto value means that this sink is counted as though it were multiple sinks, for the purposes of determining which nets should have top routing. An auto value for a sink pin means that the sink counts as a single sink.</p> <p>Valid values: integer &gt; 0</p> <p><b>Type:</b> string</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p>
<b>cts_top_fanout_transitive_count</b>	

	<p>The number of clock sinks in the transitive fanout of the pin as counted for applying the top routing rules.</p> <p>This attribute is very similar to the cts_transitive_fanout attribute but counts sink fanout using the cts_top_fanout_count_override attribute instead of always counting sinks as a single item of fanout.</p> <p>Requesting this attribute for a pin not in the clock tree will result in an error.</p> <p>Valid values: integer</p> <p><b>Type:</b> int <b>Default:</b> 0 <b>Edit:</b> No</p>
<b>cts_transitive_fanout</b>	
	<p>The number of clock sinks in the transitive fanout of the pin, within the clock tree.</p> <p>Requesting this attribute for a pin not in the clock tree will result in an error.</p> <p>Valid values: int</p> <p><b>Type:</b> int <b>Default:</b> 0 <b>Edit:</b> No</p>
<b>cts_virtual_delay_early_fall</b>	
	<p>The amount of virtual delay that has been applied under this pin.</p> <p>Valid values: double</p> <p><b>Type:</b> double <b>Allowed -index values:</b> delay_corner <b>Default:</b> 0 <b>Edit:</b> Yes</p>
<b>cts_virtual_delay_early_rise</b>	
	<p>The amount of virtual delay that has been applied under this pin.</p> <p>Valid values: double</p> <p><b>Type:</b> double <b>Allowed -index values:</b> delay_corner <b>Default:</b> 0 <b>Edit:</b> Yes</p>
<b>cts_virtual_delay_late_fall</b>	
	<p>The amount of virtual delay that has been applied under this pin.</p> <p>Valid values: double</p> <p><b>Type:</b> double <b>Allowed -index values:</b> delay_corner <b>Default:</b> 0 <b>Edit:</b> Yes</p>

cts_virtual_delay_late_rise	<p>The amount of virtual delay that has been applied under this pin.      Valid values: double  <b>Type:</b> <a href="#">double</a>  <b>Allowed -index values:</b> delay_corner  <b>Default:</b> 0  <b>Edit:</b> Yes</p>
delay_max_fall	<p>Returns the maximum falling delay. You can use -index to return the value from a specific analysis view.  <b>Type:</b> <a href="#">double</a>  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
delay_max_rise	<p>Returns the maximum rising delay. You can use -index to return the value from a specific analysis view.  <b>Type:</b> <a href="#">double</a>  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
delay_min_fall	<p>Returns the minimum falling delay. You can use -index to return the value from a specific analysis view.  <b>Type:</b> <a href="#">double</a>  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
delay_min_rise	<p>Returns the minimum rising delay. You can use -index to return the value from a specific analysis view.  <b>Type:</b> <a href="#">double</a>  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
direction	

	<p>Pin's direction from the corresponding base_pin. It can be in, out, inout or internal. Internal means it is an internal pin from a .lib file for the timing model, and is not part of the netlist.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> internal in out inout</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
dont_touch	<p>The preservation status of a pin during optimization. A preserved pin means the logical function of the pin must be preserved to maintain a simulation or test-point pin in the netlist. However, the name does not need to be preserved.</p> <p><b>Supported values:</b></p> <ul style="list-style-type: none"> <li>false: Unconstrained</li> <li>true: Cannot add/remove ports</li> <li>delete_ok: Can delete ports (if they have no fanout)</li> <li>invert_ok: We cannot delete, duplicate, or add but can change the polarity</li> <li>none: No user setting; will inherit from the module/hinst</li> </ul> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> none false true delete_ok invert_ok</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p>
effective_stack_via_rule	<p>The stack_via_rule that is expected to be used by the router for connecting to this pin. This value is derived from the other pin and base_pin attributes related to stack via.</p> <p><b>Type:</b> obj(stack_via_rule)</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
escaped_name	<p>The full hierarchical name including escaped chars (if any). It follows DEF escaping syntax, so bus-bit chars [], or a hierarchy char \ that is not a bus-bit or hierarchy char has a \ in front of it. So i1/i2 is a two-level hierarchical name while i1\i2 is single level name, and a[0] is a bus-bit, while a\[0\] is a scalar.</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
fanout_load	

	Returns the fanout load for the pin. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
<b>from_arcs</b>	
	Returns a list of arc objects for which this pin is the starting pin of the timing arc. <b>Type:</b> obj(arc)* <b>Default:</b> "" <b>Edit:</b> No
<b>hierarchical_level</b>	
	Returns hierarchical level for an Instance Pin. <b>Type:</b> int <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
<b>hnet</b>	
	pointer to the hnet connected to the pin <b>Type:</b> obj(hnet) <b>Default:</b> "" <b>Edit:</b> No
<b>hold_uncertainty</b>	
	Returns the most conservative uncertainty of all possible uncertainty assertions associated with the pin. You can use -index to return the value from a specific analysis view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
<b>initial_name</b>	
	This will be used for verification of initial input netlist (post-synthesis) to any other netlist generated during Innovus flow. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes
<b>input_signal_level</b>	

	Returns the rail name associated with input pin. <b>Type:</b> <a href="#">string</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
<b>input_signal_level_voltage</b>	
	Returns rail voltage of signal which is driving the input pin. <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
<b>inst</b>	
	pointer to the inst containing the pin <b>Type:</b> <a href="#">obj(inst)</a> <b>Default:</b> "" <b>Edit:</b> No
<b>is_always_on</b>	
	Returns a value of true if the pin is always on type pin. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
<b>is_async</b>	
	Returns a value of true if the pin is an asynchronous clear or preset pin. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
<b>is_clear</b>	
	Returns a value of true if the pin is an asynchronous clear pin. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
<b>is_clock</b>	

	<p>Returns a value of true if the pin has the Liberty pin attribute: clock .</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>is_clock_gating</b>	
	<p>Returns a value of true if the pin is defined as a pin of a clock gating cell. You can use -index to return the value from a specific analysis view.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>is_clock_gating_clock</b>	
	<p>Returns a value of true if the pin is defined as a clock pin of a clock gating cell.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>is_clock_gating_enable</b>	
	<p>Returns a value of true if the pin corresponds to the enable pin of a clock gating cell.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>is_clock_used_as_clock</b>	
	<p>Returns a value of true if the pin lies in the clock network and at least one of the clocks arriving at the pin is used as a clock in the downstream network of the pin. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>is_clock_used_as_data</b>	

	<p>Returns a value of true if the pin lies in the clock source path and at least one of the clocks arriving on the pin is used as data in the downstream network of the pin. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>is_data</b>	
	<p>Returns a value of true if the pin is a data pin (that is, is not a clock pin).</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>is_disable_timing</b>	
	<p>Returns a value of true if the pin's timing has been disabled. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>is_fall_edge_triggered_clock</b>	
	<p>Returns a value of true if the pin is a clock pin of a flop, and is triggered by the falling edge of a clock.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>is_fall_edge_triggered_data</b>	
	<p>Returns a value of true if the pin corresponds to the data pin of a fall edge triggered device.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>is_hierarchical</b>	

**Stylus Common UI Database Object Information**  
Database Objects--pin

	<p>is_hierarchical <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No</p>
is_initial_phase_inverted	<p>This indicates if the initial RTL phase has been inverted. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes</p>
is_inside_partition	<p>Returns whether pin is in partition or not. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No</p>
is_internal_disable	<p>Returns the internal disabled assertion on endpoints. Such endpoints will have no timing computed on them. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No</p>
is_isolation_cell_clock	<p>Returns true if a clock pin is part of an isolation cell, <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No</p>
is_isolation_cell_data	<p>Returns a value of true if the pin is isolation data pin type. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No</p>
is_isolation_cell_enable	

	<p>Returns a value of true if the pin is isolation enable pin type.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_latency_network_pin	<p>Returns a value of true if the pin has latency phase propagated to it.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_level_shifter_data	<p>Returns a value of true if the pin is level shifter data pin type.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_level_shifter_enable	<p>Returns a value of true if the pin is level shifter enable pin type.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_multiple_clock_fanin_point	<p>Returns a value of true if multiple clock phases converge at the pin. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_mux_select_pin	<p>Returns the is_mux_select_pin property for a pin. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

is_negative_level_sensitive_clock	
	<p>Returns a value of true if the library pin is an enable pin of an active low level-sensitive device.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_negative_level_sensitive_data	
	<p>Returns a value of true if the pin is a data pin of an active low level-sensitive device.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_owner	
	<p>Returns true if client is the owner for pin in distributed STA.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_positive_level_sensitive_clock	
	<p>Returns a value of true if the library pin is an enable pin of an active high level-sensitive device.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_positive_level_sensitive_data	
	<p>Returns a value of true if the pin is a data pin of an active high level-sensitive device.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_power_mode_disabled	

	<p>Returns true if power mode is disabled</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Allowed -index values:</b> <code>analysis_view</code></p> <p><b>Default:</b> <code>""</code></p> <p><b>Edit:</b> No</p>
is_preset	<p>Returns a value of true if the pin is a preset pin.</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Allowed -index values:</b> <code>analysis_view clock</code></p> <p><b>Default:</b> <code>""</code></p> <p><b>Edit:</b> No</p>
is_propagated_clock	<p>Returns a value of true if there is an explicit <code>set_propagated_clock</code> assertion at the pin. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Allowed -index values:</b> <code>analysis_view clock</code></p> <p><b>Default:</b> <code>""</code></p> <p><b>Edit:</b> No</p>
is_rise_edge_triggered_clock	<p>Returns a value of true if the pin is a clock pin of a flop, and is triggered by the rising edge of a clock.</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Allowed -index values:</b> <code>analysis_view clock</code></p> <p><b>Default:</b> <code>""</code></p> <p><b>Edit:</b> No</p>
is_rise_edge_triggered_data	<p>Returns a value of true if the pin corresponds to the data pin of a rise edge-triggered device.</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Allowed -index values:</b> <code>analysis_view clock</code></p> <p><b>Default:</b> <code>""</code></p> <p><b>Edit:</b> No</p>
is_shared	<p>Returns true if pin is shared across clients in distributed STA</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Allowed -index values:</b> <code>analysis_view clock</code></p> <p><b>Default:</b> <code>""</code></p> <p><b>Edit:</b> No</p>

is_special	
	<p>pin is belong DEF SPECIALNETS section</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
is_tristate	
	<p>Returns a value of true if the pin has the three_state attribute in the Liberty timing library.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_tristate_enable	
	<p>Returns a value of true if the pin is the source pin of timing arcs with either the three_state_enable or three_state_disable attribute in the Liberty timing library.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_tristate_output	
	<p>Returns a value of true if the pin corresponds to a three-state output pin.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_valid_for_reports	
	<p>Returns the pin is valid for reporting.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
latch_time_given	

	<p>In latch-based analysis, this returns the value by which the arrival time on this pin is adjusted to account for time borrowed at the previous stage. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
layer	
	<p>pin layer</p> <p><b>Type:</b> <a href="#">obj(layer)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
lib_pins	
	<p>Returns a list of library pin (lib_pin) objects which are associated with this pin.</p> <p><b>Type:</b> <a href="#">obj(lib_pin)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
location	
	<p>pin location</p> <p><b>Type:</b> <a href="#">point</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
max_capacitance	
	<p>Returns the maximum capacitance limit for the pin. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
max_fanout	
	<p>Returns the maximum fanout load that the pin can drive. This value is set using set_max_fanout or the default_max_fanout library attribute. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

max_time_borrow	<p>In latch-based analysis, returns the maximum time that a path arriving at this latch input can borrow from the next stage - as specified by set_max_time_borrow. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
max_transition	<p>Returns the maximum transition time limit specified for the pin. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
min_capacitance	<p>Returns the minimum capacitance limit for the pin. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
min_fanout	<p>Returns the minimum fanout design rule limit of the corresponding library pin. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
min_transition	<p>Returns the minimum transition time limit specified for the pin. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
name	

	<p>The same as .escaped_name without any \ escape chars. This name is commonly used to avoid problems with \ escape chars in Tcl scripts unless you carefully use list operators. Like SDC commands, 'get_db insts i1/i2' will first try to match i1/i2, and if not found then match i1\i2 so that flattening hierarchical names (e.g. with ungroup) does not require changing the names in Tcl scripts.</p> <p><b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No</p>
net	<p>pointer to the net connected to the pin</p> <p><b>Type:</b> obj(net) <b>Default:</b> "" <b>Edit:</b> No</p>
network_latency_fall_max	<p>Returns the maximum fall insertion delay specified by an explicit set_clock_latency at the pin. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No</p>
network_latency_fall_min	<p>Returns the minimum fall insertion delay specified by an explicit set_clock_latency at the pin. You can use -index to return the value for a specific analysis view and/or clock.</p> <p><b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No</p>
network_latency_rise_max	<p>Returns the maximum rise insertion delay specified by an explicit set_clock_latency at the pin. You can use -index to return the value for a specific analysis view and/or clock</p> <p><b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No</p>
network_latency_rise_min	

	Returns the minimum rise insertion delay specified by an explicit set_clock_latency at the pin. You can use -index to return the value for a specific analysis view and/or clock <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (pin) <b>Default:</b> "" <b>Edit:</b> No
output_signal_level	Returns the rail name associated with output pin. <b>Type:</b> string <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
power_domain	The parent power domain of the pin (equivalent to Design Browser effPD) <b>Type:</b> obj(power_domain) <b>Default:</b> "" <b>Edit:</b> No
power_rail_voltage_inout_input_max	Reports power rail voltage for input part of bidi pins/ports for maximum operating condition. You can use -index to return the value for a specific analysis view <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
power_rail_voltage_inout_input_min	Reports power rail voltage for input part of bidi pins/ports for minimum operating condition. You can use -index to return the value for a specific analysis view <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
power_rail_voltage_max	

	<p>Reports power rail voltage for maximum operating condition for bidirectional, input and output pins. For bidirectional pins, the power rail voltage for output signal is reported. You can use -index to return the value for a specific analysis view</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>power_rail_voltage_min</b>	
	<p>Reports power rail voltage for minimum operating condition for bidirectional, input and output pins. For bidirectional pins, the power rail voltage for output signal is reported. You can use -index to return the value for a specific analysis view</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>setup_uncertainty</b>	
	<p>Returns the most conservative uncertainty of all possible uncertainty assertions associated with the pin. You can use -index to return the value for a specific analysis view</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slack_max</b>	
	<p>Returns the worst slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slack_max_edge</b>	
	<p>Returns the data edge of the path responsible for the slack_max value. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slack_max_fall</b>	

	<p>Returns the worst falling slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_max_rise	<p>Returns the worst rising slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_mean_max	<p>In SOCV analysis, this returns the mean component of the worst slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_mean_max_fall	<p>In SOCV analysis, this returns the mean component of the worst falling slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_mean_max_rise	<p>In SOCV analysis, this returns the mean component of the worst rising slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_mean_min	

	<p>In SOCV analysis, this returns the mean component of the worst slack across all concurrent MMMC views for Hold-style early data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
slack_mean_min_fall	<p>In SOCV analysis, this returns the mean component of the worst falling slack across all concurrent MMMC views for Hold-style early data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
slack_mean_min_rise	<p>In SOCV analysis, this returns the mean component of the worst rising slack across all concurrent MMMC views for Hold-style early data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
slack_min	<p>Returns the worst slack across all concurrent MMMC views for Hold-style early data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
slack_min_edge	<p>Returns the data edge of the path responsible for the slack_min value. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> string  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
slack_min_fall	

	<p>Returns the worst falling slack across all concurrent MMMC views for Hold-style early data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_min_rise	<p>Returns the worst rising slack across all concurrent MMMC views for Hold-style early data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_sigma_max	<p>In SOCV analysis, this returns the variation component of the worst slack across all concurrent MMMC views for Setup-style late data path checks.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_sigma_max_fall	<p>In SOCV analysis, this returns the variation component of the worst falling slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_sigma_max_rise	<p>In SOCV analysis, this returns the variation component of the worst rising slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_sigma_min	

	<p>In SOCV analysis, this returns the variation component of the worst slack across all concurrent MMMC views for Hold-style early data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slack_sigma_min_fall</b>	
	<p>In SOCV analysis, this returns the variation component of the worst falling slack across all concurrent MMMC views for Hold-style early data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slack_sigma_min_rise</b>	
	<p>In SOCV analysis, this returns the variation component of the worst rising slack across all concurrent MMMC views for Hold-style early data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_max_fall</b>	
	<p>Returns the maximum slew time for falling transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_max_rise</b>	
	<p>Returns the maximum slew time for rising transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_mean_max_fall</b>	

	<p>In SOCV mode, returns the mean component of the maximum slew time for falling transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
slew_mean_max_rise	
	<p>In SOCV mode, returns the mean component of the maximum slew time for rising transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
slew_mean_min_fall	
	<p>In SOCV mode, returns the mean component of the minimum slew time for falling transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
slew_mean_min_rise	
	<p>In SOCV mode, returns the mean component of the minimum slew time for rising transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
slew_min_fall	
	<p>Returns the minimum slew time for falling transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>

slew_min_rise	<p>Returns the minimum slew time for rising transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slew_sigma_max_fall	<p>In SOCV mode, returns the variation component of the maximum slew time for falling transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slew_sigma_max_rise	<p>In SOCV mode, returns the variation component of the maximum slew time for rising transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slew_sigma_min_fall	<p>In SOCV mode, returns the variation component of the minimum slew time for falling transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slew_sigma_min_rise	

	<p>In SOCV mode, returns the variation component of the minimum slew time for rising transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>source_latency_early_fall_max</b>	
	<p>Returns the maximum early fall source insertion delay specified by an explicit set_clock_latency at the pin.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>source_latency_early_fall_min</b>	
	<p>Returns the minimum early fall source insertion delay specified by an explicit set_clock_latency at the pin. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>source_latency_early_rise_max</b>	
	<p>Returns the maximum early rise source insertion delay specified by an explicit set_clock_latency at the pin. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>source_latency_early_rise_min</b>	
	<p>Returns the minimum early rise source insertion delay specified by an explicit set_clock_latency at the pin. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

source_latency_late_fall_max	<p>Returns the maximum late fall source insertion delay specified by an explicit set_clock_latency at the pin. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
source_latency_late_fall_min	<p>Returns the minimum late fall source insertion delay specified by an explicit set_clock_latency at the pin. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
source_latency_late_rise_max	<p>Returns the maximum late rise source insertion delay specified by an explicit set_clock_latency at the pin. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
source_latency_late_rise_min	<p>Returns the minimum late rise source insertion delay specified by an explicit set_clock_latency at the pin. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
stack_via_rule	

	<p>This value serves as a pin-specific override to use this stack_via_rule when connecting to this pin. If set, it must match one of the elements from the stack_via_rule_list attribute of the corresponding base_pin. The interpretation of this value depends on this pin's stack_via_rule_required attribute.</p> <p>stack_via_rule == {} &amp;&amp; stack_via_rule_required == false: stack_via_rule does not affect the choice.</p> <p>stack_via_rule == stackrule1 &amp;&amp; stack_via_rule_required == false: Router will prefer stackrule1, but it may select another (or possibly none) if necessary to avoid design rule violations.</p> <p>stack_via_rule == {} &amp;&amp; stack_via_rule_required == true: The required stack_via_rule is empty, so the router will not use any stack_via_rule for connecting to this pin (even ignoring stack_via_required on the base_pin if necessary).</p> <p>stack_via_rule == stackrule1 &amp;&amp; stack_via_rule_required == true: Router will use stackrule1, even if it leads to design rule violations.</p> <p><b>Type:</b> <a href="#">obj(stack_via_rule)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>stack_via_rule_required</b>	
	<p>Specifies whether the router must use this pin's stack_via_rule value. If false, the stack_via_rule value will be preferred by the router, if true the stack_via_rule value is required by the router. See the stack_via_rule attribute for more details.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_case_computed_value</b>	
	<p>Returns the case computed value</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>timing_case_logic_value</b>	
	<p>Returns the case logic value</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>to_arcs</b>	

	Returns a list of arc objects where the current pin is the termination point of the arc <b>Type:</b> obj(arc)* <b>Default:</b> "" <b>Edit:</b> No
<b>user_constant_value</b>	
	Returns constant values from netlist or constraints. You can use -index to return the value for a specific view. <b>Type:</b> int <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No

## pin\_blockage

### Parent Objects

[design](#), [root](#)

### Definition

Pin blockage objects

Attribute	Description
layer	The layer that is being blocked <b>Type:</b> obj(layer) <b>Default:</b> "" <b>Edit:</b> No
name	Partition pin blockage name <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
obj_type	

	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (pin_blockage)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
rect	<p>Rectangle that define the pin_blockage shape.</p> <p><b>Type:</b> <a href="#">rect</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## pin\_group

### Parent Objects

[design](#), [pin\\_guide](#), [root](#)

### Definition

Pin group

Attribute	Description
base_pins	<p>List of base pins associated with the group</p> <p><b>Type:</b> <a href="#">obj(base_pin)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
exclude_pin	<p>Indicates group pin exclude type(all_layer, same_layer, inclusive, all_layer_in_guided_area)</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> all_layer_in_guided_area all_layer same_layer inclusive</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
is_compact	

**Stylus Common UI Database Object Information**  
Database Objects--pin\_group

	Indicate whether the pins in the group are assigned tightly together. By default, pins which are part of a group and associated to a guide can be spread inside the guide based on the area available and alignment to targets <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
is_guided	Indicates if pin group is guided <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_spread	Indicates whether member pins distributed evenly <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
keep_out_space	Minimum spacing with foreign pins (Unit: track) <b>Type:</b> <a href="#">int</a> <b>Default:</b> "" <b>Edit:</b> No
name	Name of pin group <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (pin_group)</a> <b>Default:</b> "" <b>Edit:</b> No
optimize_order	Name of pin group <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No

parent	The parent of the pin_group. It can be a design, a partition (if not committed yet), or base_cell for a black_box. <b>Type:</b> obj.design)* obj(partition)* obj(base_cell)* <b>Default:</b> "" <b>Edit:</b> No
pin_spacing	Minimum spacing between adjacent pins (Unit: track) <b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No

## pin\_guide

### Parent Objects

[design](#), [root](#)

### Definition

Pin guide

Attribute	Description
area	Area of the pin guide as defined by the LEF MACRO SIZE or OVERLAP information <b>Type:</b> area <b>Default:</b> "" <b>Edit:</b> No
layer_priority	layer priority <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
layers	

	layers where pin_guide is present <b>Type:</b> obj(layer)* <b>Default:</b> "" <b>Edit:</b> No
name	
	Name of pin guide <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
net_group	
	net_group, if pin_guide is based on net_group otherwise NULL <b>Type:</b> obj(net_group) <b>Default:</b> "" <b>Edit:</b> No
obj_type	
	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (pin_guide) <b>Default:</b> "" <b>Edit:</b> No
parent	
	The parent of the pin_guide. It can be a design, a partition (if not committed yet), or base_cell for a black_box. <b>Type:</b> obj.design)* obj(partition)* obj(base_cell)* <b>Default:</b> "" <b>Edit:</b> No
pin_group	
	pin_group, if pin_guide is based on pin_group otherwise NULL <b>Type:</b> obj(pin_group) <b>Default:</b> "" <b>Edit:</b> No
rects	
	The rects that define the location of the pin_guide. <b>Type:</b> rect* <b>Default:</b> "" <b>Edit:</b> No

# place\_blockage

## Parent Objects

[design](#), [root](#)

## Definition

Placement blockage(hard, soft, partial).

Attribute	Description
density	<p>The max placement density percent allowed inside this place_blockage. It must be in the range of 5 to 100, in steps of 5. It is only valid if the type = partial or soft. For example, a partial placement percentage of 75 percent means that up to 75 percent of placement density is allowed in the area. If the type is not partial or soft, a value of 0 is returned.</p> <p><b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> Yes</p>
inst	<p>The instance that the placement blockage is associated with (equivalent to DEF BLOCKAGES + COMPONENT)</p> <p><b>Type:</b> <a href="#">obj(inst)</a> <b>Default:</b> "" <b>Edit:</b> No</p>
is_no_flop	<p>Flip-flops and latches cannot be placed inside this place_blockage. Only has an effect if type = partial.</p> <p><b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes</p>
is_pushdown	<p>This place_blockage has been pushed down from a higher level in the design hierarchy.</p> <p><b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes</p>

**Stylus Common UI Database Object Information**  
Database Objects--place\_blockage

name	
	Name of placement blockage <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes
obj_type	
	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (place_blockage)</a> <b>Default:</b> "" <b>Edit:</b> No
rects	
	List of non-overlapping rectangles that defines the shape of place_blockage <b>Type:</b> <a href="#">rect*</a> <b>Default:</b> "" <b>Edit:</b> Yes
shapes	
	List of shapes of this placement blockage <b>Type:</b> <a href="#">obj(shape)*</a> <a href="#">obj(density_shape)*</a> <b>Default:</b> "" <b>Edit:</b> No
type	
	The type of blockage. hard = no cells allowed, macro_only = standard-cells are allowed but blocks are not allowed, partial = allow cells until reach the .density limit, soft = most logic cells are not allowed, but 'repeater' cells like inverters, buffers, level-shifters, isolation cells, and clock-gating cells are allowed. See the set_selective_blockage_gate command for other methods to control what is allowed inside a soft place_blockage. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> macro_only hard soft partial <b>Default:</b> "" <b>Edit:</b> Yes

# port

## Parent Objects

[bus](#), [bump\\_pin](#), [clock](#), [io\\_constraint](#), [skew\\_group](#), [hnet](#), [timing\\_point](#), [design](#), [bus\\_sink\\_group](#), [clock\\_tree](#), [timing\\_path](#), [root](#), [bump](#), [port\\_shape](#), [net](#)

## Definition

External logical ports of the design. See [pg\\_ports](#) for power/ground ports

Attribute	Description
actual_latency_early_fall_max	<p>Returns the computed early falling clock latency to this clock port. If the analysis mode is set to best-case/worst-case, the value will be the Setup capture latency. When operating in OCV mode, the max qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
actual_latency_early_fall_min	<p>Returns the computed early falling clock latency to this clock port. If the analysis mode is set to best-case/worst-case, the value will be the Hold launch latency. When operating in OCV mode, the min qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
actual_latency_early_rise_max	

	<p>Returns the computed early rising clock latency to this clock port. If the analysis mode is set to best-case/worst-case, the value will be the Setup capture latency. When operating in OCV mode, the max qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
actual_latency_early_rise_min	<p>Returns the computed early rising clock latency to this clock port. If the analysis mode is set to best-case/worst-case, the value will be the Hold launch latency. When operating in OCV mode, the min qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
actual_latency_late_fall_max	<p>Returns the computed late falling clock latency to this clock port. If the analysis mode is set to best-case/worst-case, the value will be the Setup launch latency. When operating in OCV mode, the max qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
actual_latency_late_fall_min	

	<p>Returns the computed late falling clock latency to this clock port. If the analysis mode is set to best-case/worst-case, the value will be the Hold capture latency. When operating in OCV mode, the min qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
actual_latency_late_rise_max	<p>Returns the computed late rising clock latency to this clock port If the analysis mode is set to best-case/worst-case, the value will be the Setup launch latency. When operating in OCV mode, the max qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
actual_latency_late_rise_min	<p>Returns the computed late rising clock latency to this clock port. If the analysis mode is set to best-case/worst-case, the value will be the Hold capture latency. When operating in OCV mode, the min qualification is ignored. If there are multiple arrival times from different clock phases - the most conservative latency value is reported. You can use the -index function to return latencies with respect to a specific clock. When operating in concurrent MMMC mode, the worst latency across all views is reported. You can use the -index function to filter latencies based on view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
antenna_data	<p>List of antenna data for the terminal</p> <p><b>Type:</b> obj(antenna_data)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

aocv_early_input_stage_weight	<p>Returns the number of external path stages to consider in AOCV early analysis of paths from this port.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
aocv_early_output_stage_weight	<p>Returns the number of external path stages to consider in AOCV early analysis of paths to this port.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
aocv_late_input_stage_weight	<p>Returns the number of external path stages to consider in AOCV late analysis of paths from this port.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
aocv_late_output_stage_weight	<p>Returns the number of external path stages to consider in AOCV late analysis of paths to this port.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
arrival_max_fall	<p>Returns the latest falling arrival time to the specified port across all concurrent MMMC views. You can use -index to determine the worst arrival for a specific view. You can also use -index to get the latest arrival time related to a specific clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
arrival_max_rise	

	<p>Returns the latest rising arrival time to the specified port across all concurrent MMMC views. You can use -index to determine the worst arrival for a specific view. You can also use -index to get the latest arrival time related to a specific clock.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
arrival_mean_max_fall	<p>In SOCV analysis mode, this returns the mean value of the latest falling arrival time to the specified port across all concurrent MMMC views. You can use -index to determine the latest arrival for a specific view. You can also use -index to get the worst arrival time related to a specific clock.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
arrival_mean_max_rise	<p>In SOCV analysis mode, this returns the mean value of the latest rising arrival time to the specified port across all concurrent MMMC views. You can use -index to determine the latest arrival for a specific view. You can also use -index to get the worst arrival time related to a specific clock.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
arrival_mean_min_fall	<p>In SOCV analysis mode, this returns the mean value of the earliest falling arrival time to the specified port across all concurrent MMMC views. You can use -index to determine the earliest arrival for a specific view. You can also use -index to get the earliest arrival time related to a specific clock.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
arrival_mean_min_rise	

	<p>In SOCV analysis mode, this returns the mean value of the earliest rising arrival time to the specified port across all concurrent MMMC views. You can use -index to determine the earliest arrival for a specific view. You can also use -index to get the earliest arrival time related to a specific clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>arrival_min_fall</b>	
	<p>Returns the earliest falling arrival time to the specified port across all concurrent MMMC views. You can use -index to determine the worst arrival for a specific view. You can also use -index to get the earliest arrival time related to a specific clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>arrival_min_rise</b>	
	<p>Returns the earliest falling arrival time to the specified port across all concurrent MMMC views. You can use -index to determine the worst arrival for a specific view. You can also use -index to get the worst arrival time related to a specific clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>arrival_sigma_max_fall</b>	
	<p>In SOCV analysis mode, this returns the variation component of the latest falling arrival time to the specified port across all concurrent MMMC views. You can use -index to determine the latest arrival for a specific view. You can also use -index to get the worst arrival time related to a specific clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>arrival_sigma_max_rise</b>	

	<p>In SOCV analysis mode, this returns the variation component of the latest rising arrival time to the specified port across all concurrent MMMC views. You can use -index to determine the latest arrival for a specific view. You can also use -index to get the worst arrival time related to a specific clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>arrival_sigma_min_fall</b>	
	<p>In SOCV analysis mode, this returns the variation component of the earliest falling arrival time to the specified port across all concurrent MMMC views. You can use -index to determine the earliest arrival for a specific view. You can also use -index to get the earliest arrival time related to a specific clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>arrival_sigma_min_rise</b>	
	<p>In SOCV analysis mode, this returns the mean value of the earliest rising arrival time to the specified port across all concurrent MMMC views. You can use -index to determine the earliest arrival for a specific view. You can also use -index to get the earliest arrival time related to a specific clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>arrival_window</b>	
	<p>Returns a list of the earliest and latest, rising and falling arrival times per clock phase at the port across all concurrent MMMC views. You can use -index to make the arrival times specific to a given view</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>base_name</b>	
	<p>The name at the base of a hierarchical name. So the base_name of i1/i2/i3 is i3.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

bus	
	<p>Bus of port  <b>Type:</b> <a href="#">obj(bus)</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
clocks	
	<p>Returns a list of all of the clock objects arriving at the port. You can use -index to return the value from a specific analysis view.  <b>Type:</b> <a href="#">obj(clock)*</a>  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
constant_value	
	<p>Returns a constant value of 0 or 1 if logic state has been asserted or propagated to this pin. You can use -index to return the value from a specific analysis view.  <b>Type:</b> <a href="#">int</a>  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
cts_add_port_driver	
	<p>Specifies a cell type so that a cell inst can be added above an output port or below an input port.  The port is specified by the argument pin.  If the pin specified is not a design IO pin or it is not in the clock network then CCOpt will emit a warning  and will not add cell insts at that position.  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
cts_assign_clock_tree	

	<p>Can be used to make sure a clock tree sink pin gets driven by a particular clock tree. The clock tree can alternatively be specified as the tree's root pin, in case extraction renames the clock trees defined from a single SDC clock.</p> <p>By default CCOpt automatically selects appropriate pins.</p> <p>Valid values: cts_clock_tree   list of pins</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>cts_case_analysis</b>	
	<p>Specifies a constant value to be used as pin signal when analyzing timing within CTS. Only applies to input pins of cells in the clock tree. If set to 'none' (the default), CTS will consider the input as non-constant.</p> <p>Valid values: 0 1 none</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p>
<b>cts_clock_tree</b>	
	<p>The clock tree to which this object belongs. Flops do not belong to a clock tree, but their clock pins do.</p> <p>Valid values: cts_clock_tree</p> <p><b>Type:</b> <a href="#">obj(clock_tree)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>cts_clock_trees</b>	
	<p>A list of clock trees the pin is contained within. This includes parents of generated clock trees and all relevant parents when clock trees overlap.</p> <p>Valid values: list cts_clock_tree</p> <p><b>Type:</b> <a href="#">obj(clock_tree)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>cts_is_sdc_clock_root</b>	

	<p>Specifies whether the given pin is the root (source pin) of an SDC clock. The <code>create_clock_tree_spec</code> populates this attribute with the location of the SDC clock root (source) pins. This attribute controls the behavior of clock tree definition commands <code>create_clock_tree</code> and <code>create_generated_clock_tree</code>, when the <code>-stop_at_sdc_clock_roots</code> argument is specified. In such a case, pins and ports for which this attribute is true will be treated as being SDC clock root pins.</p> <p>Valid values: true false</p> <p><b>Type:</b> <code>bool</code>  <b>Default:</b> false  <b>Edit:</b> Yes</p>
<b>cts_net_unbufferable_reasons</b>	
	<p>This attribute contains a list of reasons why CCOpt was not able to buffer the clock net attached to the specified pin.</p> <p>Valid values: string</p> <p><b>Type:</b> <code>string</code>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>cts_node_type</b>	
	<p>node type of port within cts graph</p> <p><b>Type:</b> <code>string</code>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>cts_pin_insertion_delay</b>	
	<p>The insertion delay under this pin.</p> <p>Valid values: double   auto</p> <p><b>Type:</b> <code>string</code>  <b>Allowed -index values:</b> <code>delay_corner</code>  <b>Default:</b> auto  <b>Edit:</b> Yes</p>
<b>cts_pin_insertion_delay_wire</b>	
	<p>The wire component of the insertion delay under this pin.</p> <p>Valid values: double   auto</p> <p><b>Type:</b> <code>string</code>  <b>Allowed -index values:</b> <code>delay_corner</code>  <b>Default:</b> auto  <b>Edit:</b> Yes</p>

cts_routing_trunk_override	
	<p>Prefer trunk routing rules for this pin. Only applies to clock tree sinks.      Valid values: true false</p> <p><b>Type:</b> bool  <b>Default:</b> false  <b>Edit:</b> Yes</p>
cts_sink_type	
	<p>The type of sink this pin represents.      Valid values are as follows:</p> <ul style="list-style-type: none"> <li>auto The sink type will be automatically determined by CCOpt.</li> <li>through Through pin. Trace the clock tree through this pin.</li> <li>stop Stop pin. When defining clock trees, CCOpt stops searching for parts of the clock tree at stop pins.</li> <li>ignore Ignore pin. CCOpt stops searching for parts of the clock tree at ignore pins and it does not attempt to balance the insertion delay of ignore pins.</li> <li>exclude Exclude pin. Exclude this pin from the clock tree.</li> </ul> <p>Valid values: auto through stop ignore exclude</p> <p><b>Type:</b> string  <b>Default:</b> auto  <b>Edit:</b> Yes</p>
cts_sink_type_effective	
	<p>Indicates how CCOpt will treat a given pin, taking into account both its cts_sink_type_implicit, and any cts_sink_type settings.</p> <p>Setting a non-default value for the cts_sink_type attribute will override the cts_sink_type_implicit attribute.</p> <p><b>Type:</b> string  <b>Default:</b> auto  <b>Edit:</b> No</p>
cts_sink_type_implicit	

	<p>Indicates the type of sink that CCOpt classified this pin as. Note that the cts_sink_type attribute can override these internal classifications.</p> <p>Possible values are:</p> <ul style="list-style-type: none"> <li>exclude Indicates that this pin is a sink which represents a non-clock pin.</li> <li>ignore Indicates that CCOpt has determined not to search for more clock tree through this pin. Additionally, this pin will not be balanced.</li> <li>stop Indicates that CCOpt has determined not to search for more clock tree through this pin.</li> <li>An empty value for this attribute indicates either that this pin is either not a sink, or that it is a sink that is not implicitly exclude or ignore or stop.</li> </ul> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> exclude</p> <p><b>Edit:</b> No</p>
<b>cts_sink_type_reasons</b>	
	<p>The reasons why this pin has the given cts_sink_type.</p> <p>This attribute is configured by the <code>create_clock_tree_spec</code> command in order to record the reasons that the <code>cts_sink_type</code> attribute has been configured for the given pin.</p> <p>This attribute is a list of values. Valid values are as follows:</p> <ul style="list-style-type: none"> <li>auto The <code>cts_sink_type</code> attribute is set to 'auto'</li> <li>implicit The pin is an implicit sink (flop/latch)</li> <li>user The user has set the <code>cts_sink_type</code> attribute</li> <li>design_io This pin is a design I/O</li> <li>multiple_outputs This pin is on an instance with multiple outputs, and the <code>cts_spec_config_trace_through_to</code> attribute has not been set</li> <li>set_disable_timing SDC <code>set_disable_timing</code> stops the clock at this pin</li> <li>set_case_analysis SDC <code>set_case_analysis</code> stops the clock at this pin</li> <li>generated_clock_tree This pin is the generator input to an SDC generated clock</li> <li>no_sdc_clock The SDC clock is stopped at this pin for other reasons</li> <li>ilm The <code>create_clock_tree_spec</code> command has detected an ILM below this pin</li> </ul> <p>Valid values: auto implicit user design_output multiple_outputs set_disable_timing set_case_analysis generated_clock_tree no_sdc_clock ilm</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p>
<b>cts_skew_group_pin_insertion_delay_wire</b>	

	<p>The wire component of the insertion delay under this pin for a specific skew group.          Valid values: double   auto</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> delay_corner skew_group</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p>
	<p><b>cts_skew_groups_active</b></p>
	<p>Returns the list of active skew groups for this pin.          For sink pins, this attribute lists both skew groups that pass through this pin and skew groups for which this sink is an endpoint.          For non-sink pins, shows skew groups that pass through this pin.          Valid values: list skew_groups</p> <p><b>Type:</b> <a href="#">obj(skew_group)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p><b>cts_skew_groups_active_sink</b></p>
	<p>Returns the list of skew groups for which this pin is an active sink.          For sink pins, this attribute lists the skew groups for which this sink is an endpoint. Skew groups that pass through this pin are not included.          For non-sink pins, this attribute always returns null.          Valid values: list skew_groups</p> <p><b>Type:</b> <a href="#">obj(skew_group)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p><b>cts_skew_groups_ignore</b></p>
	<p>The list of skew groups for which paths through this pin are ignored.          Valid values: list skew_groups</p> <p><b>Type:</b> <a href="#">obj(skew_group)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p><b>cts_skew_groups_sink</b></p>
	<p>The list of skew groups for which this pin is a sink.          Valid values: list skew_groups</p> <p><b>Type:</b> <a href="#">obj(skew_group)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

<p><b>cts_skew_groups_source_pin</b></p>	<p>The list of skew groups for which this clock tree or pin is specified as a source.          Valid values: list skew_groups  <b>Type:</b> obj(skew_group)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
<p><b>cts_spec_config_trace_through_to</b></p>	<p>Clock tree definition will, by default, not continue through certain types of cell arc (for instance, the clock to Q arc in a DFF). This attribute allows you to override this default behavior, permitting the clock tree to trace through such a cell.          The attribute should be configured on the input pin at which the clock arrives. The value of the attribute specifies the output pin to which the clock should propagate. The specified output pin must be another pin on the same instance. The output pin may be specified either by its fully qualified name (i.e. inclusive of the instance name), or else simply by its local (cell-relative) name.          There must be a pre-existing (library-defined) chain of one or more delay arcs that connect the input and output pins together. It is not possible to use trace_through_to to synthesize delay arcs.          If multiple input pins are annotated on a given instance, the value of trace_through_to at each of those pins must select the same output pin: i.e. the configuration must identify a single clock output for the instance. If multiple clock outputs are required then trace_through_to should not be used: instead define a generated clock tree at each of the clock-carrying outputs.          If the configuration of trace_through_to settings for a given instance does not meet these requirements, a warning will be issued and the settings for that instance will be ignored.          Note: if both trace_through_to and library_trace_through_to are applicable at a given netlist instance pin, the trace_through_to value takes precedence.          Valid values: pin  <b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
<p><b>cts_top_fanout_count_override</b></p>	

	<p>The number of clock sinks this sink counts for when applying the top routing rules.          Note that this attribute is only valid for sink pins, and it returns auto for non-sink pins.          For a sink pin, a non-auto value means that this sink is counted as though it were multiple sinks, for the purposes of determining which nets should have top routing. An auto value for a sink pin means that the sink counts as a single sink.          Valid values: integer &gt; 0</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p>
<b>cts_top_fanout_transitive_count</b>	
	<p>The number of clock sinks in the transitive fanout of the pin as counted for applying the top routing rules.          This attribute is very similar to the cts_transitive_fanout attribute but counts sink fanout using the          cts_top_fanout_count_override attribute instead of always counting sinks as a single item of fanout.          Requesting this attribute for a pin not in the clock tree will result in an error.          Valid values: integer</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> No</p>
<b>cts_transitive_fanout</b>	
	<p>The number of clock sinks in the transitive fanout of the pin, within the clock tree.          Requesting this attribute for a pin not in the clock tree will result in an error.          Valid values: int</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> No</p>
<b>cts_virtual_delay_early_fall</b>	
	<p>The amount of virtual delay that has been applied under this pin.          Valid values: double</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> delay_corner</p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
<b>cts_virtual_delay_early_rise</b>	

	<p>The amount of virtual delay that has been applied under this pin.          Valid values: double  <b>Type:</b> <a href="#">double</a>  <b>Allowed -index values:</b> delay_corner  <b>Default:</b> 0  <b>Edit:</b> Yes</p>
cts_virtual_delay_late_fall	<p>The amount of virtual delay that has been applied under this pin.          Valid values: double  <b>Type:</b> <a href="#">double</a>  <b>Allowed -index values:</b> delay_corner  <b>Default:</b> 0  <b>Edit:</b> Yes</p>
cts_virtual_delay_late_rise	<p>The amount of virtual delay that has been applied under this pin.          Valid values: double  <b>Type:</b> <a href="#">double</a>  <b>Allowed -index values:</b> delay_corner  <b>Default:</b> 0  <b>Edit:</b> Yes</p>
delay_max_fall	<p>Returns the maximum falling delay. You can use -index to return the value from a specific analysis view.  <b>Type:</b> <a href="#">double</a>  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
delay_max_rise	<p>Returns the maximum rising delay. You can use -index to return the value from a specific analysis view.  <b>Type:</b> <a href="#">double</a>  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
delay_min_fall	

	<p>Returns the minimum falling delay. You can use -index to return the value from a specific analysis view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
delay_min_rise	<p>Returns the minimum rising delay. You can use -index to return the value from a specific analysis view.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
depth	<p>Depth constraint of the port in microns. Pin assignment commands will create a pin shape for this port that extends 'depth' microns inside the design edge. The edit_pin command can be used to set it.</p> <p><b>Type:</b> <a href="#">coord</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
design	<p>The design of this port</p> <p><b>Type:</b> <a href="#">obj.design</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
direction	<p>Direction of the port from the Verilog netlist.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> in out inout</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
drive_resistance_fall_max	

	<p>Returns the falling linear drive resistance at the port for late timing paths. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> <code>analysis_view clock</code></p> <p><b>Default:</b> <code>""</code></p> <p><b>Edit:</b> No</p>
<b>drive_resistance_fall_min</b>	
	<p>Returns the falling linear drive resistance at the port for early timing paths. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> <code>analysis_view clock</code></p> <p><b>Default:</b> <code>""</code></p> <p><b>Edit:</b> No</p>
<b>drive_resistance_rise_max</b>	
	<p>Returns the rising linear drive resistance at the port for late timing paths.. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> <code>analysis_view clock</code></p> <p><b>Default:</b> <code>""</code></p> <p><b>Edit:</b> No</p>
<b>drive_resistance_rise_min</b>	
	<p>Returns the rising linear drive resistance at the port for early timing paths. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> <code>analysis_view clock</code></p> <p><b>Default:</b> <code>""</code></p> <p><b>Edit:</b> No</p>
<b>driver_from_pin_fall_max</b>	
	<p>Returns the driving cell input pin specified for max falling delays at the port. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <code>obj(lib_pin)*</code></p> <p><b>Default:</b> <code>""</code></p> <p><b>Edit:</b> No</p>
<b>driver_from_pin_fall_min</b>	

	Returns the driving cell input pin specified for min falling delays at the port. You can use -index to return the value for a specific view.  <b>Type:</b> <a href="#">obj(lib_pin)</a> * <b>Default:</b> "" <b>Edit:</b> No
driver_from_pin_rise_max	Returns the driving cell input pin specified for max rising delays at the port. You can use -index to return the value for a specific view.  <b>Type:</b> <a href="#">obj(lib_pin)</a> * <b>Default:</b> "" <b>Edit:</b> No
driver_from_pin_rise_min	Returns the driving cell input pin specified for min rising delays at the port. You can use -index to return the value for a specific view.  <b>Type:</b> <a href="#">obj(lib_pin)</a> * <b>Default:</b> "" <b>Edit:</b> No
driver_ignore_drc	driver_ignore_drc <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driver_input_slew_fall_to_fall_max	Returns the driver input pin slew used for the max fall-to-fall delay. You can use -index to return the value for a specific view.  <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driver_input_slew_fall_to_fall_min	Returns the driver input pin slew used for the min fall-to-fall delay. You can use -index to return the value for a specific view.  <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No

driver_input_slew_fall_to_rise_max	Returns the driver input pin slew used for the max fall-to-rise delay. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driver_input_slew_fall_to_rise_min	Returns the driver input pin slew used for the min fall-to-rise delay. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driver_input_slew_rise_to_fall_max	Returns the driver input pin slew used for the max rise-to-fall delay. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driver_input_slew_rise_to_fall_min	Returns the driver input pin slew used for the min rise-to-fall delay. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driver_input_slew_rise_to_rise_max	Returns the driver input pin slew used for the max rise-to-rise delay. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driver_input_slew_rise_to_rise_min	

	Returns the driver input pin slew used for the min rise-to-rise delay. You can use -index to return the value for a specific view. <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driver_pin_fall_max	Returns the driving cell output pin specified for max falling delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> <a href="#">obj(lib_pin)*</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
driver_pin_fall_min	Returns the driving cell output pin specified for min falling delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> <a href="#">obj(lib_pin)*</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
driver_pin_rise_max	Returns the driving cell output pin specified for max rising delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> <a href="#">obj(lib_pin)*</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
driver_pin_rise_min	Returns the driving cell output pin specified for min rising delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> <a href="#">obj(lib_pin)*</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
driving_cell_fall_max	

	Returns the name of the library cell used to compute max falling delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driving_cell_fall_min	Returns the name of the library cell used to compute min falling delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driving_cell_from_pin_fall_max	Returns the driving cell input pin specified for max falling delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driving_cell_from_pin_fall_min	Returns the driving cell input pin specified for min falling delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driving_cell_from_pin_rise_max	Returns the driving cell input pin specified for max rising delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driving_cell_from_pin_rise_min	

	Returns the driving cell input pin specified for min rising delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driving_cell_library_fall_max	
	Returns the driving cell library specified for max falling delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driving_cell_library_fall_min	
	Returns the driving cell library specified for min falling delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driving_cell_library_rise_max	
	Returns the driving cell library specified for max rising delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driving_cell_library_rise_min	
	Returns the driving cell library specified for min rising delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driving_cell_pin_fall_max	

	Returns the driving cell output pin specified for max falling delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driving_cell_pin_fall_min	Returns the driving cell output pin specified for min falling delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driving_cell_pin_rise_max	Returns the driving cell output pin specified for max rising delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driving_cell_pin_rise_min	Returns the driving cell output pin specified for min rising delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driving_cell_rise_max	Returns the name of the library cell used to compute max rising delays at the port. You can use -index to return the value for a specific view. <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
driving_cell_rise_min	

	<p>Returns the name of the library cell used to compute max rising delays at the port. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>escaped_name</b>	
	<p>The full hierarchical name including escaped chars (if any). It follows DEF escaping syntax, so bus-bit chars [], or a hierarchy char \ that is not a bus-bit or hierarchy char has a \ in front of it. So i1/i2 is a two-level hierarchical name while i1\i2 is single level name, and a[0] is a bus-bit, while a\[0] is a scalar.</p> <p><b>Type:</b> <code>string</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>external_capacitance_max</b>	
	<p>Returns the total max external loading on the port from all sources - including set_load assertions or wireload models. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>external_capacitance_min</b>	
	<p>Returns the total min external loading on the port from all sources - including set_load assertions or wireload models. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>external_fanout_load</b>	
	<p>Returns the external fanout load specified by set_fanout_load. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> <code>double</code></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>external_wireload_model</b>	

	Returns the wireload model used to model external connections to the port. You can use -index to return the value for a specific view.  <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
hdl_name	This is the original RTL name for this port.  <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes
hnet	hnet of this port  <b>Type:</b> <a href="#">obj(hnet)</a> <b>Default:</b> "" <b>Edit:</b> No
hold_uncertainty	Returns the most conservative uncertainty of all possible uncertainty Hold assertions associated with the port. You can use -index to return the value from a specific analysis view.  <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
input_slew_max_fall	Returns the slowest falling transition on the port as specified by set_input_transition. You can use -index to return the value from a specific analysis view.  <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
input_slew_max_rise	Returns the slowest rising transition on the port as specified by set_input_transition. You can use -index to return the value from a specific analysis view.  <b>Type:</b> <a href="#">double</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
input_slew_min_fall	

	<p>Returns the fastest falling transition on the port as specified by set_input_transition. You can use -index to return the value from a specific analysis view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
input_slew_min_rise	<p>Returns the fastest rising transition on the port as specified by set_input_transition. You can use -index to return the value from a specific analysis view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_clock_used_as_clock	<p>Returns a value of true if the port lies in the clock network and at least one of the clocks arriving at the pin is used as a clock in the downstream network of the pin. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> bool</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_clock_used_as_data	<p>Returns a value of true if the port lies in the clock source path and at least one of the clocks arriving on the pin is used as data in the downstream network of the pin. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> bool</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_disable_timing	<p>Returns a value of true if the port's timing has been disabled. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> bool</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_ideal_driver	

	Returns true if the port is an ideal driver due to the set_ideal_latency or set_ideal_transition constraint. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
<b>is_ideal_network</b>	
	Returns true if the port is part of an ideal network due to the set_ideal_network constraint. You can use -index to return the value for a specific analysis view. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
<b>is_inside_partition</b>	
	Returns whether port is inside partition or not. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
<b>is_internal_disable</b>	
	Return is_internal_disable property for a pin. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
<b>is_owner</b>	
	Returns true if client is the owner for pin in distributed STA. <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
<b>is_power_mode_disabled</b>	
	Returns true if power mode is disabled <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>is_propagated_clock</b>	

	Returns a value of true if there is an explicit set_propagated_clock assertion at the port. You can use -index to return the value for a specific analysis view.  <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
is_shared	Returns true if pin is shared across clients in distributed STA.  <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
is_special	Indicates that the port is Special(not set for base_cell terms)  <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
is_valid_for_reports	Return whether a pin is valid for reporting or not  <b>Type:</b> <a href="#">bool</a> <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
layer	Layer of the port. For ports with more than one shape, it is the layer of the first shape (which is the same shape used for the .location value).  <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> No
location	Location of port. For port with only one shape, it is the center of the port shape edge abutting the design boundary. The edit_pin command can be used to set it. For ports that have more than one shape, the location will overlap the first shape of the port.  <b>Type:</b> <a href="#">point</a> <b>Default:</b> "" <b>Edit:</b> Yes
max_capacitance	

	<p>max_capacitance</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
max_fanout	<p>Returns the maximum fanout load that the port can drive. . You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
max_transition	<p>Returns the maximum transition time limit specified for the port. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
min_capacitance	<p>Returns the minimum capacitance limit for the port. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
min_fanout	<p>Returns the minimum fanout value for the port.</p> <p><b>Type:</b> int</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
min_transition	<p>Returns the minimum transition time limit specified for the port.</p> <p><b>Type:</b> double</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
name	

	<p>The same as .escaped_name without any \ escape chars. This name is commonly used to avoid problems with \ escape chars in Tcl scripts unless you carefully use list operators. Like SDC commands, 'get_db insts i1/i2' will first try to match i1/i2, and if not found then match i1\i2 so that flattening hierarchical names (e.g. with ungroup) does not require changing the names in Tcl scripts.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>
net	<p>The canonical (flat) net connected to the terminal</p> <p><b>Type:</b> obj(net)  <b>Default:</b> ""  <b>Edit:</b> No</p>
network_latency_fall_max	<p>Returns the maximum fall insertion delay specified by an explicit set_clock_latency at the port. You can use -index to return the value for a specific analysis view.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
network_latency_fall_min	<p>Returns the minimum fall insertion delay specified by an explicit set_clock_latency at the port. You can use -index to return the value for a specific analysis view and/or clock.</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
network_latency_rise_max	<p>Returns the maximum rise insertion delay specified by an explicit set_clock_latency at the port. You can use -index to return the value for a specific analysis view and/or clock</p> <p><b>Type:</b> double  <b>Allowed -index values:</b> analysis_view clock  <b>Default:</b> ""  <b>Edit:</b> No</p>
network_latency_rise_min	

	Returns the minimum rise insertion delay specified by an explicit set_clock_latency at the port. You can use -index to return the value for a specific analysis view and/or clock <b>Type:</b> double <b>Allowed -index values:</b> analysis_view clock <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (port) <b>Default:</b> "" <b>Edit:</b> No
physical_pins	List of ports <b>Type:</b> obj(physical_pin)* <b>Default:</b> "" <b>Edit:</b> No
pin_edge	If this port is for a design, and the port is assigned (has place_status of placed/fixed/cover), the edge value indicates along which edge of the boundary polygon the port is assigned. The edge number starts from the lowest Y, then left-most X vertex, starting with 0, and then counting clock-wise. See the set_pin_constraint command document for a figure showing the edge numbering. If the port is not assigned, or not for a design, the value of -1 is returned. <b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No
place_status	Placement Status of terminal (not for base_cell terms) <b>Type:</b> enum <b>Enum Values:</b> unplaced placed fixed cover soft_fixed <b>Default:</b> "" <b>Edit:</b> Yes
power_domain	The power domain of the terminal (equivalent to Design Browser effPD) <b>Type:</b> obj(power_domain) <b>Default:</b> "" <b>Edit:</b> No
power_rail_voltage_max	

	<p>power_rail_voltage_max</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
power_rail_voltage_min	<p>power_rail_voltage_min</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
related_ground_pin	<p>Specifies which ground pin drives this signal pin. It must be one of the ground pins defined for this cell. It can be set by CPF, Liberty, or LEF/OA, with CPF having highest precedence, then Liberty, then LEF/OA. It is often only set when there is more than one ground pin for the cell.</p> <p><b>Type:</b> <a href="#">obj(port)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
related_power_pin	<p>Specifies which power pin drives this signal pin. It must be one of the power pins defined for this cell. It can be set by CPF, Liberty, or LEF/OA, with CPF having highest precedence, then Liberty, then LEF/OA. It is often only set when there is more than one power pin for the cell.</p> <p><b>Type:</b> <a href="#">obj(port)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
setup_uncertainty	<p>Returns the most conservative uncertainty of all possible uncertainty assertions associated with the port. You can use -index to return the value for a specific analysis view</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
shape	

	<p>Terminal shape</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none ring abutment feed_through</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
side	<p>Side constraint of the port. The edit_pin command can be used to set this value.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> north west south east up none</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_max	<p>Returns the worst slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_max_edge	<p>Returns the edge (rise or fall) of the worst slack-causing path at the specified port in late mode.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_max_fall	<p>Returns the worst falling slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_max_rise	

	<p>Returns the worst rising slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_mean_max	<p>In SOCV analysis, this returns the mean component of the worst slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_mean_max_fall	<p>In SOCV analysis, this returns the mean component of the worst falling slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_mean_max_rise	<p>In SOCV analysis, this returns the mean component of the worst rising slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_mean_min	<p>In SOCV analysis, this returns the mean component of the worst slack across all concurrent MMMC views for Hold-style early data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

slack_mean_min_fall	<p>In SOCV analysis, this returns the mean component of the worst falling slack across all concurrent MMMC views for Hold-style early data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_mean_min_rise	<p>In SOCV analysis, this returns the mean component of the worst rising slack across all concurrent MMMC views for Hold-style early data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_min	<p>Returns the worst slack across all concurrent MMMC views for hold-style late data path checks</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_min_edge	<p>Returns the edge (rise or fall) of the worst slack-causing path at the specified port in early mode.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_min_fall	<p>Returns the worst hold slack for a falling signal at the port endpoint.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_min_rise	

	<p>Returns the worst hold slack for a rising signal at the port endpoint.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_sigma_max	<p>In SOCV analysis, this returns the variation component of the worst slack across all concurrent MMMC views for Setup-style late data path checks.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_sigma_max_fall	<p>In SOCV analysis, this returns the variation component of the worst falling slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_sigma_max_rise	<p>In SOCV analysis, this returns the variation component of the worst rising slack across all concurrent MMMC views for Setup-style late data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_sigma_min	<p>In SOCV analysis, this returns the variation component of the worst slack across all concurrent MMMC views for Hold-style early data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_sigma_min_fall	

	<p>In SOCV analysis, this returns the variation component of the worst falling slack across all concurrent MMMC views for Hold-style early data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slack_sigma_min_rise</b>	
	<p>In SOCV analysis, this returns the variation component of the worst rising slack across all concurrent MMMC views for Hold-style early data path checks. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_max_fall</b>	
	<p>Returns the maximum slew time for falling transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_max_rise</b>	
	<p>Returns the maximum slew time for rising transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_mean_max_fall</b>	
	<p>In SOCV mode, returns the mean component of the maximum slew time for falling transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_mean_max_rise</b>	

	<p>In SOCV mode, returns the mean component of the maximum slew time for rising transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_mean_min_fall</b>	
	<p>In SOCV mode, returns the mean component of the minimum slew time for falling transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_mean_min_rise</b>	
	<p>In SOCV mode, returns the mean component of the minimum slew time for rising transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_min_fall</b>	
	<p>Returns the minimum slew time for falling transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_min_rise</b>	
	<p>Returns the minimum slew time for rising transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_sigma_max_fall</b>	

	<p>In SOCV mode, returns the variation component of the maximum slew time for falling transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_sigma_max_rise</b>	
	<p>In SOCV mode, returns the variation component of the maximum slew time for rising transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_sigma_min_fall</b>	
	<p>In SOCV mode, returns the variation component of the minimum slew time for falling transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>slew_sigma_min_rise</b>	
	<p>In SOCV mode, returns the variation component of the minimum slew time for rising transitions across all concurrent MMMC views. You can use -index to return the value for a specific view.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>source_latency_early_fall_max</b>	
	<p>Returns the maximum early fall source insertion delay specified by an explicit set_clock_latency at the port.</p> <p><b>Type:</b> double</p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

source\_latency\_early\_fall\_min

Returns the minimum early fall source insertion delay specified by an explicit set\_clock\_latency at the port. You can use -index to return the value for a specific view and/or clock.  
**Type:** double  
**Allowed -index values:** analysis\_view clock  
**Default:** ""  
**Edit:** No

source\_latency\_early\_rise\_max

Returns the maximum early rise source insertion delay specified by an explicit set\_clock\_latency at the port. You can use -index to return the value for a specific view and/or clock.  
**Type:** double  
**Allowed -index values:** analysis\_view clock  
**Default:** ""  
**Edit:** No

source\_latency\_early\_rise\_min

Returns the minimum early rise source insertion delay specified by an explicit set\_clock\_latency at the port. You can use -index to return the value for a specific view and/or clock.  
**Type:** double  
**Allowed -index values:** analysis\_view clock  
**Default:** ""  
**Edit:** No

source\_latency\_late\_fall\_max

Returns the maximum late fall source insertion delay specified by an explicit set\_clock\_latency at the port. You can use -index to return the value for a specific view and/or clock.  
**Type:** double  
**Allowed -index values:** analysis\_view clock  
**Default:** ""  
**Edit:** No

source\_latency\_late\_fall\_min

	<p>Returns the minimum late fall source insertion delay specified by an explicit set_clock_latency at the port. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>source_latency_late_rise_max</b>	
	<p>Returns the maximum late rise source insertion delay specified by an explicit set_clock_latency at the port. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>source_latency_late_rise_min</b>	
	<p>Returns the minimum late rise source insertion delay specified by an explicit set_clock_latency at the port. You can use -index to return the value for a specific view and/or clock.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>timing_case_computed_value</b>	
	<p>Returns the case computed value</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>timing_case_logic_value</b>	
	<p>Returns the case logic value</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Allowed -index values:</b> analysis_view clock</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>type</b>	

	<p>Terminal type  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> normal_term clock_term latch_q_term f_fq_term d_term d_q_term tri_state_term power_term ground_term feed_term r_s_term async_control_term gated_clock_term analog_term  <b>Default:</b> ""  <b>Edit:</b> No</p>
width	
	<p>Width constraint of the port in microns. The edit_pin command can be used to set it.  <b>Type:</b> <a href="#">coord</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>

## port\_shape

### Parent Objects

[design](#), [root](#)

### Definition

This corresponds to one of a port's .physical\_pins.layer\_shapes.shapes, but is directly accessible from the design and root objects. It carries a link to the port object, that a layer\_shape object does not have. This allows GUI operations that need both the layer\_shape and the port object together as one object like delete\_obj or wire-editing commands.

Attribute	Description
layer	<p>Layer of this port shape  <b>Type:</b> <a href="#">obj(layer)</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
mask	

**Stylus Common UI Database Object Information**  
Database Objects--port\_shape

	<p>The mask number for this port_shape if this layer has multiple masks. 0 means it is uncolored. Refer to layer .num_masks for legal range.</p> <p><b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No</p>
name	<p>Name of the port for this port_shape. Note that all the port_shapes for one port will have the same name.</p> <p><b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> enum (port_shape) <b>Default:</b> "" <b>Edit:</b> No</p>
polygon	<p>Points of the polygon of the port_shape for type rect or polygon.</p> <p><b>Type:</b> point* <b>Default:</b> "" <b>Edit:</b> No</p>
port	<p>The port this port shape belongs to.</p> <p><b>Type:</b> obj(port) <b>Default:</b> "" <b>Edit:</b> No</p>
rect	<p>Bounding box of the port_shape for type rect or polygon.</p> <p><b>Type:</b> rect <b>Default:</b> "" <b>Edit:</b> No</p>
type	

Type of port_shape (rect polygon). <b>Type:</b> enum <b>Enum Values:</b> rect polygon <b>Default:</b> "" <b>Edit:</b> No
--

## power\_domain

### Parent Objects

hinst, inst, design, pin, root, group, port

### Definition

Power domain

Attribute	Description
available_supply_nets	Specifies the power nets physically available for this power domain to use for secondary power pin connections. <b>Type:</b> obj(net)* <b>Default:</b> "" <b>Edit:</b> No
base_domains	Specifies the base power domains (always-on domains) that supply the power to this switchable power domain through power switch cells. <b>Type:</b> obj(power_domain)* <b>Default:</b> "" <b>Edit:</b> No
core_to_bottom	Distance between the power domain edge and its core box <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
core_to_left	

**Stylus Common UI Database Object Information**  
Database Objects--power\_domain

	Distance between the power domain edge and its core box <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
core_to_right	
	Distance between the power domain edge and its core box <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
core_to_top	
	Distance between the power domain edge and its core box <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
extend_power_bottom	
	Maximum search distance for power connections <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
extend_power_edges	
	List of maximum search distances for power extension connections in clockwise order starting with the vertical edge at the lower-left corner (smallest Y, then smallest X) <b>Type:</b> coord* <b>Default:</b> "" <b>Edit:</b> No
extend_power_left	
	Maximum search distance for power connections <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
extend_power_right	
	Maximum search distance for power connections <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No

**Stylus Common UI Database Object Information**  
Database Objects--power\_domain

extend_power_top	Maximum search distance for power connections <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
gap_bottom	Minimum spacing to other power domains or rows <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
gap_edges	List of minimum spacing values to other power domains or rows in clockwise order starting with the vertical edge at the lower-left corner (smallest Y, then smallest X) <b>Type:</b> coord* <b>Default:</b> "" <b>Edit:</b> No
gap_left	Minimum spacing to other power domains or rows <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
gap_right	Minimum spacing to other power domains or rows <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
gap_top	Minimum spacing to other power domains or rows <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
group	

	<p>The group of PD  <b>Type:</b> <a href="#">obj(group)</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
is_always_on	<p>Indicates that the power domain is always on  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
is_default	<p>The power domain is the default power domain or not.  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
is_power_domain_macro_only	<p>Indicates whether the domain member has only hardmacro members.  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
is_virtual	<p>Specifies the power domain is a virtual domain, meaning that this domain does not have any inst member.  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> No</p>
name	<p>Name of the power domain  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a>  <b>Type:</b> <a href="#">enum (power_domain)</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>

power_switch_rule_name	Indicates the domain's power switch rule name. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
primary_ground_net	Specifies the main ground rail net of the power domain. <b>Type:</b> <a href="#">obj(net)</a> <b>Default:</b> "" <b>Edit:</b> No
primary_power_net	Specifies the main power rail net of the power domain. <b>Type:</b> <a href="#">obj(net)</a> <b>Default:</b> "" <b>Edit:</b> No
shutoff_condition	Indicates the power domain's shutoff condition. It is a logic expression with pin or hpin names. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No

## preferred\_cell\_stripe

### Parent Objects

### Definition

preferred cell stripe

Attribute	Description
name	

	name of preferred_cell_stripe <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (preferred_cell_stripe) <b>Default:</b> "" <b>Edit:</b> No

## rc\_corner

### Parent Objects

[delay\\_corner](#), [root](#)

### Definition

The rc\_corner object represents a specific interconnect parasitic corner. It contains configuration information for controlling the extraction of the parasitics and possible scaling. Parasitic files are annotated or exported with respect to an rc\_corner object name. The rc\_corner object is typically referenced from one or many higher-level delay\_corner objects. Use the `create_rc_corner` command to define new rc\_corners and the `update_rc_corner` command to update the attributes of existing rc\_corners.

Attribute	Description
cap_table_file	Specifies the layer capacitance table file associated with the rc_corner. This is not recommended for designs below 32nm. See the <code>write_cap_table</code> command for more details on the file. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
is_active	

## Stylus Common UI Database Object Information

### Database Objects--rc\_corner

	Indicates that the rc_corner is associated with an analysis_view that is used in the active analysis_view <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_dynamic	Indicates that the rc_corner is associated with an analysis_view that is used in the active dynamic analysis_view <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_hold	Indicates that the rc_corner is associated with an analysis_view that is used in the active hold analysis_view <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_leakage	Indicates that the rc_corner is associated with an analysis_view that is used in the active leakage analysis_view <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_setup	Indicates that the rc_corner is associated with an analysis_view that is used in the active setup analysis_view <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
name	Provides the name of this rc_corner object as specified by create_rc_corner. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
obj_type	

	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (rc_corner)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
post_route_cap	<p>Specifies scaling factor(s) to be used for capacitances in post_route flow steps. 1 to 3 values may be specified to control each extraction effort level. Example: {lowEffortFactor}, {lowEffortFactor mediumEffortFactor}, {lowEffortFactor mediumEffortFactor highEffortFactor}. A scaling value of 1.0 is assumed for any effort level without an explicit setting.</p> <p><b>Type:</b> <a href="#">double*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
post_route_clock_cap	<p>Specifies scaling factor(s) to be used for clock network capacitances in post_route flow steps. 1 to 3 values may be specified to control each extraction effort level. Example: {lowEffortFactor}, {lowEffortFactor mediumEffortFactor}, {lowEffortFactor mediumEffortFactor highEffortFactor}. A scaling value of 1.0 is assumed for any effort level without an explicit setting.</p> <p><b>Type:</b> <a href="#">double*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
post_route_clock_res	<p>Specifies scaling factor(s) to be used for clock network resistances in post_route flow steps. 1 to 3 values may be specified to control each extraction effort level. Example: {lowEffortFactor}, {lowEffortFactor mediumEffortFactor}, {lowEffortFactor mediumEffortFactor highEffortFactor}. A scaling value of 1.0 is assumed for any effort level without an explicit setting.</p> <p><b>Type:</b> <a href="#">double*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
post_route_cross_cap	<p>Specifies scaling factor(s) to be used for coupling-capacitances in post_route flow steps. 1 to 3 values may be specified to control each extraction effort level. Example: {lowEffortFactor}, {lowEffortFactor mediumEffortFactor}, {lowEffortFactor mediumEffortFactor highEffortFactor}. A scaling value of 1.0 is assumed for any effort level without an explicit setting.</p> <p><b>Type:</b> <a href="#">double*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

**Stylus Common UI Database Object Information**  
Database Objects--rc\_corner

post_route_res	Specifies scaling factor(s) to be used for resistances in post_route flow steps. 1 to 3 values may be specified to control each extraction effort level. Example: {lowEffortFactor}, {lowEffortFactor mediumEffortFactor}, {lowEffortFactor mediumEffortFactor highEffortFactor}. A scaling value of 1.0 is assumed for any effort level without an explicit setting. <b>Type:</b> double* <b>Default:</b> "" <b>Edit:</b> No
pre_route_cap	Specifies a scaling factor to be used for capacitances in pre_route flow steps. Defaults to 1.0 if not given. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
pre_route_clock_cap	Specifies a scaling factor to be used for clock network capacitances in pre_route flow steps. Defaults to 1.0 if not given. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
pre_route_clock_res	Specifies a scaling factor to be used for clock network resistance in pre_route flow steps. Defaults to 1.0 if not given. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
pre_route_res	Specifies a scaling factor to be used for resistances in pre_route flow steps. Defaults to 1.0 if not given. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
qrc_tech_file	Specifies the QRC technology file associated with the rc_corner <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No

## temperature

Specifies the temperature, in units of Celsius, to use to derate resistance values for this rc\_corner. Use this parameter when you want to override the default temperature specified in the capacitance table or the QRC technology file. By default, the RC extractor uses the temperature of 25 degrees Celsius, unless it is specified by the capacitance table or the QRC technology file. Note, the opcond temperature is not used for RC extraction, the temperature for RC extraction must be set with this attribute if you want to override the techfile or capturable settings.

**Type:** [double](#)

**Default:** ""

**Edit:** No

## via\_variation\_file

Specifies the via layer file so that all the VIA resistance in SPEF could be mapped to have own variation multiplier.

**Type:** [string](#)

**Default:** ""

**Edit:** No

# resize\_blockage

## Parent Objects

[design](#), [root](#)

## Definition

resize blkg

Attribute	Description
is_resizeable	<p>Specifies that the size blockage can be resized, however alignment and the minimum space between the objects in the blockage area will be maintained during floorplan resize.(1 = resizable).</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
name	

	Name of the size blockage <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (resize_blockage)</a> <b>Default:</b> "" <b>Edit:</b> No
rect	Rectangle that defines the resize_blockage shape. <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No

## root

### Parent Objects

### Definition

root

Attribute	Description
add_endcaps_avoid_two_sites_cell_abut	
	avoid 2 sites boundary cell abut to incorner cell in N10 <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_avoid_two_sites_cell_abut</a>
add_endcaps_bottom_edge	

	<p>EndCaps with n-well at the bottom edge</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_endcaps_bottom_edge</a></p>
<b>add_endcaps_boundary_tap</b>	
	<p>New flow to add cap cell and tap cell together</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_endcaps_boundary_tap</a></p>
<b>add_endcaps_cells</b>	
	<p>Specify endCaps cell candidates for N10 that has defined in LEF</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_endcaps_cells</a></p>
<b>add_endcaps_create_rows</b>	
	<p>Create rows for endtap cell techSites which do not have rows in the floor plan</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_endcaps_create_rows</a></p>
<b>add_endcaps_flip_y</b>	
	<p>Flips the orientation of the endcap instances in Y direction if the site symmetry allows it.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_endcaps_flip_y</a></p>
<b>add_endcaps_incremental_left_edge</b>	
	<p>EndCap lists with n-well at the left edge</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_endcaps_incremental_left_edge</a></p>
<b>add_endcaps_incremental_right_edge</b>	

	EndCap list with n-well at the right edge <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_incremental_right_edge</a>
add_endcaps_left_bottom_corner	
	EndCap with n-well at the left bottom corner <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_bottom_corner</a>
add_endcaps_left_bottom_corner_even	
	EndCap with n-well at the left bottom corner, even sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_bottom_corner_even</a>
add_endcaps_left_bottom_corner_neighbor	
	The cell to be abutted with the left side of leftBottomCorner in R0 orientation <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_bottom_corner_neighbor</a>
add_endcaps_left_bottom_corner_odd	
	EndCap with n-well at the left bottom corner, odd sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_bottom_corner_odd</a>
add_endcaps_left_bottom_edge	
	EndCap with n-well at the left bottom edge <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_bottom_edge</a>
add_endcaps_left_bottom_edge_even	

	EndCap with n-well at the left bottom edge, even sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_bottom_edge_even</a>
add_endcaps_left_bottom_edge_neighbor	
	The cell to be abutted with the right edge of leftBottomEdge in R0 orientation <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_bottom_edge_neighbor</a>
add_endcaps_left_bottom_edge_odd	
	EndCap with n-well at the left bottom edge, odd sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_bottom_edge_odd</a>
add_endcaps_left_edge	
	EndCap with n-well at the left edge <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_edge</a>
add_endcaps_left_edge_bottom_border	
	EndCaps with n-well at the left edge, poly at the bottom boundary <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_edge_bottom_border</a>
add_endcaps_left_edge_even	
	EndCap with n-well at the left edge, even sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_edge_even</a>
add_endcaps_left_edge_odd	

	EndCap with n-well at the left edge, odd sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_edge_odd</a>
add_endcaps_left_edge_top_border	
	EndCaps with n-well at the left edge, poly at the top boundary <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_edge_top_border</a>
add_endcaps_left_top_corner	
	EndCap with n-well at the left top corner <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_top_corner</a>
add_endcaps_left_top_corner_even	
	EndCap with n-well at the left top corner, even sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_top_corner_even</a>
add_endcaps_left_top_corner_neighbor	
	The cell to be abutted with the left side of leftTopCorner in R0 orientation <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_top_corner_neighbor</a>
add_endcaps_left_top_corner_odd	
	EndCap with n-well at the left top corner, odd sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_left_top_corner_odd</a>
add_endcaps_left_top_edge	

	<p>EndCap with n-well at the left top edge  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_endcaps_left_top_edge</a></p>
<b>add_endcaps_left_top_edge_even</b>	
	<p>EndCap with n-well at the left top edge, even sites  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_endcaps_left_top_edge_even</a></p>
<b>add_endcaps_left_top_edge_neighbor</b>	
	<p>The cell to be abutted with the right edge of leftTopEdge in R0 orientation  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_endcaps_left_top_edge_neighbor</a></p>
<b>add_endcaps_left_top_edge_odd</b>	
	<p>EndCap with n-well at the left top edge, odd sites  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_endcaps_left_top_edge_odd</a></p>
<b>add_endcaps_prefix</b>	
	<p>Prefix of EndCap cells  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_endcaps_prefix</a></p>
<b>add_endcaps_right_bottom_corner</b>	
	<p>EndCap with n-well at the right bottom corner  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_endcaps_right_bottom_corner</a></p>
<b>add_endcaps_right_bottom_corner_even</b>	

	<p>EndCap with n-well at the right bottom corner, even sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_bottom_corner_even</a></p>
add_endcaps_right_bottom_corner_neighbor	<p>The cell to be abutted with the right side of rightBottomCorner in R0 orientation <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_bottom_corner_neighbor</a></p>
add_endcaps_right_bottom_corner_odd	<p>EndCap with n-well at the right bottom corner, odd sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_bottom_corner_odd</a></p>
add_endcaps_right_bottom_edge	<p>EndCap with n-well at the right bottom edge <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_bottom_edge</a></p>
add_endcaps_right_bottom_edge_even	<p>EndCap with n-well at the right bottom edge, even sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_bottom_edge_even</a></p>
add_endcaps_right_bottom_edge_neighbor	<p>The cell to be abutted with the left edge of rightBottomEdge in R0 orientation <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_bottom_edge_neighbor</a></p>
add_endcaps_right_bottom_edge_odd	

	EndCap with n-well at the right bottom edge, odd sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_bottom_edge_odd</a>
add_endcaps_right_edge	
	EndCap with n-well at the right edge <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_edge</a>
add_endcaps_right_edge_bottom_border	
	EndCaps with n-well at the right edge, poly at the bottom boundary <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_edge_bottom_border</a>
add_endcaps_right_edge_even	
	EndCap with n-well at the right edge, even sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_edge_even</a>
add_endcaps_right_edge_odd	
	EndCap with n-well at the right edge, odd sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_edge_odd</a>
add_endcaps_right_edge_top_border	
	EndCaps with n-well at the right edge, poly at the top boundary <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_edge_top_border</a>
add_endcaps_right_top_corner	

	EndCap with n-well at the right top corner <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_top_corner</a>
add_endcaps_right_top_corner_even	
	EndCap with n-well at the right top corner, even sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_top_corner_even</a>
add_endcaps_right_top_corner_neighbor	
	The cell to be abutted with the right side of rightTopCorner in R0 orientation <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_top_corner_neighbor</a>
add_endcaps_right_top_corner_odd	
	EndCap with n-well at the right top corner, odd sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_top_corner_odd</a>
add_endcaps_right_top_edge	
	EndCap with n-well at the right top edge <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_top_edge</a>
add_endcaps_right_top_edge_even	
	EndCap with n-well at the right top edge, even sites <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_top_edge_even</a>
add_endcaps_right_top_edge_neighbor	

	The cell to be abutted with the left edge of rightTopEdge in R0 orientation <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_top_edge_neighbor</a>
add_endcaps_right_top_edge_odd	EndCap with n-well at the right top edge, odd sites <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_right_top_edge_odd</a>
add_endcaps_top_bottom_edge	EndCaps with n-well at the both top and bottom edges <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_top_bottom_edge</a>
add_endcaps_top_edge	EndCaps with n-well at the top edge <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_top_edge</a>
add_endcaps_use_even_odd_sites	use even or odd poly sites <b>Type:</b> enum <b>Enum Values:</b> none even odd <b>Default:</b> none <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_endcaps_use_even_odd_sites</a>
add_fillers_avoid_abutment_patterns	illegal abutment patterns <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_fillers_avoid_abutment_patterns</a>
add_fillers_cell_name_style	

	Add physical cells into hierarchical modules, or as top level cells (flat) <b>Type:</b> enum <b>Enum Values:</b> hier flat <b>Default:</b> hier <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_fillers_cell_name_style</a>
<b>add_fillers_cells</b>	
	List of filler cells <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_fillers_cells</a>
<b>add_fillers_check_different_cells</b>	
	Check violations between different cell types <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_fillers_check_different_cells</a>
<b>add_fillers_check_drc</b>	
	DRC checking after filler insertion <b>Type:</b> bool <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_fillers_check_drc</a>
<b>add_fillers_create_rows</b>	
	Create rows for filler cell techSites which do not have rows in the floor plan <b>Type:</b> bool <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_fillers_create_rows</a>
<b>add_fillers_distribute_Implant_evenly</b>	
	distribute implant evenly for fillers <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_fillers_distribute_Implant_evenly</a>
<b>add_fillers_eco_mode</b>	

	<p>Fillers inserted in eco flow</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_eco_mode</a></p>
<b>add_fillers_honor_preroute_as_obs</b>	
	<p>Filler command honors place_detail_preroute_as_obs value</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_honor_preroute_as_obs</a></p>
<b>add_fillers_horizontal_exception_cell</b>	
	<p>List of exceptional cells for horizontal stack checking</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_horizontal_exception_cell</a></p>
<b>add_fillers_horizontal_max_length</b>	
	<p>specify instance max length (in micron) aligned in horizontal direction</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_horizontal_max_length</a></p>
<b>add_fillers_horizontal_repair_cell</b>	
	<p>List of filler cells to fix horizontal max length violation</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_horizontal_repair_cell</a></p>
<b>add_fillers_keep_fixed</b>	
	<p>'FIXED' fillers are kept</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_keep_fixed</a></p>
<b>add_fillers_no_single_site_gap</b>	

	<p>Filler command fit 1-site gap</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_no_single_site_gap</a></p>
<b>add_fillers_prefix</b>	
	<p>Prefix of filler cells</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_prefix</a></p>
<b>add_fillers_preserve_user_order</b>	
	<p>Instruct tool to insert fillers by the user defined order</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_preserve_user_order</a></p>
<b>add_fillers_scheme</b>	
	<p>Instruct tool to select locationFirst cellFirst scheme</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> locationFirst cellFirst</p> <p><b>Default:</b> locationFirst</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_scheme</a></p>
<b>add_fillers_swap_cell</b>	
	<p>swap cell pairs</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_swap_cell</a></p>
<b>add_fillers_vertical_stack_exception_cell</b>	
	<p>List of exceptional cells for vertical stack checking</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_vertical_stack_exception_cell</a></p>
<b>add_fillers_vertical_stack_left_edge_exception_cell</b>	

	<p>List of cells only check right edge for vertical stack violation</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_vertical_stack_left_edge_exception_cell</a></p>
add_fillers_vertical_stack_max_length	<p>specify instance max length (in micron) aligned in vertical direction</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_vertical_stack_max_length</a></p>
add_fillers_vertical_stack_repair_cell	<p>List of filler cells to fix vertical stack violation</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_vertical_stack_repair_cell</a></p>
add_fillers_vertical_stack_repair_edge	<p>specify the edge to use of vertical repair cell</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> left right</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_vertical_stack_repair_edge</a></p>
add_fillers_vertical_stack_right_edge_exception_cell	<p>List of cells only check left edge for vertical stack violation</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_vertical_stack_right_edge_exception_cell</a></p>
add_fillers_with_drc	<p>call second add_fillers without drc checking</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_fillers_with_drc</a></p>
add_fillers_y_flip_type	

	Defines first or last cell with certain cell size should be y-flipped <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_fillers_y_flip_type</a>
<b>add_reinforce_pg_respect_clock_routes</b>	
	Specifies whether to honor pre-existing clock net check during stripe generation <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_reinforce_pg_respect_clock_routes</a>
<b>add_reinforce_pg_respect_signal_routes</b>	
	Specifies whether to honor pre-existing signals check during stripe generation <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_reinforce_pg_respect_signal_routes</a>
<b>add_rings_avoid_short</b>	
	Specifies whether to avoid short violation <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_rings_avoid_short</a>
<b>add_rings_break_core_ring_io_list</b>	
	Specifies io instance names for which core ring wires are broken <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_rings_break_core_ring_io_list</a>
<b>add_rings_continue_on_no_selection</b>	
	Continues w/o selection <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_rings_continue_on_no_selection</a>
<b>add_rings_detailed_log</b>	

	<p>Outputs detailed log file addring.log</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_rings_detailed_log</a></p>
<b>add_rings_extend_block_ring_search_distance</b>	
	<p>Specifies blockring extension search distance</p> <p><b>Type:</b> <code>double</code></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_rings_extend_block_ring_search_distance</a></p>
<b>add_rings_extend_core_ring_search_distance</b>	
	<p>Specifies corering extension search distance</p> <p><b>Type:</b> <code>double</code></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_rings_extend_core_ring_search_distance</a></p>
<b>add_rings_extend_merge_with_pre_wires</b>	
	<p>Specifies whether to merge with prerouted wires</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_rings_extend_merge_with_pre_wires</a></p>
<b>add_rings_extend_over_row</b>	
	<p>Specifies whether to extend over row</p> <p><b>Type:</b> <code>bool</code></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_rings_extend_over_row</a></p>
<b>add_rings_extend_search_nets</b>	
	<p>Specifies search net names</p> <p><b>Type:</b> <code>string</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_rings_extend_search_nets</a></p>
<b>add_rings_extend_stripe_search_distance</b>	

	<p>Specifies stripe extension search distance  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 0.0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_rings_extend_stripe_search_distance</a></p>
<b>add_rings_gap_width_without_io</b>	
	<p>Specifies the max missing IO Pads area width between IO Pads  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 0.0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_rings_gap_width_without_io</a></p>
<b>add_rings_ignore_drc</b>	
	<p>Specifies whether to ignore DRC check during ring generation, it is always used for prototype flow  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_rings_ignore_drc</a></p>
<b>add_rings_ignore_rows</b>	
	<p>Specifies whether to ignore all rows  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_rings_ignore_rows</a></p>
<b>add_rings_max_via_size</b>	
	<p>the maximum size of a crossover via  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_rings_max_via_size</a></p>
<b>add_rings_orthogonal_only</b>	
	<p>vias connect to orthogonal targets only  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_rings_orthogonal_only</a></p>
<b>add_rings_skip_shared_inner_ring</b>	

	<p>Specifies whether to skip crossing trunks</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> horizontal vertical none</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_rings_skip_shared_inner_ring</a></p>
add_rings_skip_via_on_pin	<p>prevent vias from being generated on the specified type of pins</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> pad block cover standardcell physicalpin</p> <p><b>Default:</b> standardcell</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_rings_skip_via_on_pin</a></p>
add_rings_skip_via_on_wire_shape	<p>prevent vias from being generated on the specified wire shapes</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> blockring stripe followpin corewire blockwire iowire padring ring fillwire noshape</p> <p><b>Default:</b> noshape</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_rings_skip_via_on_wire_shape</a></p>
add_rings_spacing_from_block	<p>Specifies the spacing from block</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_rings_spacing_from_block</a></p>
add_rings_split_long_via	<p>Split vias longer than &lt;threshold&gt; into smaller vias with specified &lt;step&gt; and bottom/left end &lt;offset&gt; and vertical/horizontal &lt;length&gt;</p> <p><b>Type:</b> string</p> <p><b>Default:</b> 0 0 -1 -1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_rings_split_long_via</a></p>
add_rings_stacked_via_bottom_layer	

	lef layer name <b>Type:</b> string <b>Default:</b> bottomLayer <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_rings_stacked_via_bottom_layer</a>
<b>add_rings_stacked_via_top_layer</b>	
	lef layer name <b>Type:</b> string <b>Default:</b> topLayer <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_rings_stacked_via_top_layer</a>
<b>add_rings_target</b>	
	Specifies ring target <b>Type:</b> enum <b>Enum Values:</b> core_ring default first_ring pad_ring stripe <b>Default:</b> default <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_rings_target</a>
<b>add_rings_via_using_exact_crossover_size</b>	
	generate partial vias of the exact crossover size <b>Type:</b> bool <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_rings_via_using_exact_crossover_size</a>
<b>add_rings_wire_center_offset</b>	
	offset value is from wire center to domain/core boundary <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_rings_wire_center_offset</a>
<b>add_route_vias_auto</b>	
	enable auto via generation when design is loaded <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_route_vias_auto</a>
<b>add_route_vias_ndr_only</b>	

	<p>generate vias for non default rules only</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_route_vias_ndr_only</a></p>
	<p><b>add_stripes_allow_jog</b></p> <p>Specifies the allowed jog type.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none padcore_ring block_ring</p> <p><b>Default:</b> padcore_ring block_ring</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_allow_jog</a></p>
	<p><b>add_stripes_allow_non_preferred_dir</b></p> <p>Specifies whether to allow non-preferred direction to jog to target</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none blockring corering padring stripe</p> <p><b>Default:</b> padring</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_allow_non_preferred_dir</a></p>
	<p><b>add_stripes_area</b></p> <p>Specify the rectangular areas or rectilinear areas or a mix of them, the correct value should be {&lt;lx ly ux uy&gt;   &lt;x1 y1 x2 y2 x3 y3 ...&gt;}</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_area</a></p>
	<p><b>add_stripes_blocks_without_same_net</b></p> <p>Specifies the stripe break point.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none block_ring selected_block unassigned_bump overlap_ringpin outer_ring outside_ringmacro blocks_without_same_net</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_blocks_without_same_net</a></p>
	<p><b>add_stripes_break_at</b></p>

	<p>Specifies the stripe break point.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none block_ring selected_block unassigned_bump overlap_ringpin outer_ring outside_ringmacro blocks_without_same_net</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_break_at</a></p>
<b>add_stripes_continue_on_no_selection</b>	
	<p>Specifies whether to continue w/o selection</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_continue_on_no_selection</a></p>
<b>add_stripes_detailed_log</b>	
	<p>Specifies whether to output detailed log file pp.log</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_detailed_log</a></p>
<b>add_stripes_domain_offset_from_core</b>	
	<p>Specifies whether to use global offset for power domain stripes</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_domain_offset_from_core</a></p>
<b>add_stripes_extend_to_closest_target</b>	
	<p>Specifies the stripe to specified target</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> ring stripe same_dir_stripe area_boundary none</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_extend_to_closest_target</a></p>
<b>add_stripes_extend_to_first_ring</b>	

	<p>Specifies whether to extend stripe antennas to closest ring  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_extend_to_first_ring</a></p>
<b>add_stripes_ignore_block_check</b>	
	<p>Specifies whether to ignore block check  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_ignore_block_check</a></p>
<b>add_stripes_ignore_block_ring_during_break</b>	
	<p>Specifies whether to break stripe outside block  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_ignore_block_ring_during_break</a></p>
<b>add_stripes_ignore_drc</b>	
	<p>Specifies whether to ignore DRC check during stripe generation, it is always used for prototype flow  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_ignore_drc</a></p>
<b>add_stripes_ignore_non_default_domains</b>	
	<p>Specifies whether to break at non-default domain  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_ignore_non_default_domains</a></p>
<b>add_stripes_in_cell_only</b>	
	<p>Specifies whether to generate stripes only inside selected or specified cell  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_in_cell_only</a></p>
<b>add_stripes_mask_color_balance</b>	

	<p>same_color would correspond to interlace with groups and alternate_color would correspond to interlace within group</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> same_color alternate_color none</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripesmask_color_balance</a></p>
	<b>add_stripes_max_extension_distance</b>
	<p>Specifies maximum extension distance(default=max integer) when -extend_to_closest_target is specified.</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 2.14748e+09</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_max_extension_distance</a></p>
	<b>add_stripes_max_via_size</b>
	<p>the maximum size of a crossover via, the correct value should be {shape width% height% target_penetration%}</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_max_via_size</a></p>
	<b>add_stripes_merge_with_all_layers</b>
	<p>Specifies whether to merge a stripe on all layers</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_merge_with_all_layers</a></p>
	<b>add_stripes_mesh_via</b>
	<p>use mesh via to reduce memory</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_mesh_via</a></p>
	<b>add_stripes_offset_from_core</b>

	<p>Specifies whether to offset first or last stripe from the core area  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_offset_from_core</a></p>
<b>add_stripes_opt_stripe_for_routing_track</b>	
	<p>move stripe location to preserve routing resource  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> shift none  <b>Default:</b> none  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_opt_stripe_for_routing_track</a></p>
<b>add_stripes_orthogonal_offset</b>	
	<p>Specifies the offsets for edges orthogonally, the correct value should be {{edge1 orthogonal_offset1} {edge2 edge3 orthogonal_offset2} {edge4 edge5 ... orthogonal_offset3} ...}   [all orthogonal_offset]  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> {none}  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_orthogonal_offset</a></p>
<b>add_stripes_orthogonal_only</b>	
	<p>vias connect to orthogonal targets only  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_orthogonal_only</a></p>
<b>add_stripes_over_row_extension</b>	
	<p>Specifies whether to extend the stripe to cover followpin at the row end  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_over_row_extension</a></p>
<b>add_stripes_partial_set_through_domain</b>	

	<p>Specifies whether to go over power domain if domain contains the specified net</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_partial_set_through_domain</a></p>
<b>add_stripes_remove_floating_stapling</b>	
	<p>remove floating stapling stripe if there is no via connection</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_remove_floating_stapling</a></p>
<b>add_stripes_remove_floating_stripe_over_block</b>	
	<p>Specifies whether to remove stripe fragments start and end inside same block or ring macro</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_remove_floating_stripe_over_block</a></p>
<b>add_stripes_remove_stripe_under_ring</b>	
	<p>Specifies whether to remove those segments under rings.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_remove_stripe_under_ring</a></p>
<b>add_stripes_respect_signal_routes</b>	
	<p>Specifies whether to honor pre-existing signals check during stripe generation</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_respect_signal_routes</a></p>
<b>add_stripes_route_over_rows_only</b>	
	<p>Specifies whether to route stripe over rows within the boundary</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_route_over_rows_only</a></p>
<b>add_stripes_rows_without_stripes_only</b>	

	<p>Specifies whether to generate stripes over rows w/o stripes</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_rows_without_stripes_only</a></p>
	<p>add_stripes_same_size_stack_vias</p> <p>generate same-sized stacked vias</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_same_size_stack_vias</a></p>
	<p>add_stripes_skip_via_on_pin</p> <p>prevent vias from being generated on the specified type of pins</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> pad block cover standardcell physicalpin</p> <p><b>Default:</b> standardcell</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_skip_via_on_pin</a></p>
	<p>add_stripes_skip_via_on_wire_shape</p> <p>prevent vias from being generated on the specified wire shapes</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> blockring stripe followpin corewire blockwire iowire padring ring fillwire noshape</p> <p><b>Default:</b> noshape</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_skip_via_on_wire_shape</a></p>
	<p>add_stripes_spacing_from_block</p> <p>Specifies the spacing from block</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_spacing_from_block</a></p>
	<p>add_stripes_spacing_type</p>

	<p>Specify the type of intra spacing for add_stripes -spacing</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> edge_to_edge center_to_center</p> <p><b>Default:</b> edge_to_edge</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_spacing_type</a></p>
add_stripes_split_long_via	<p>Split vias longer than &lt;threshold&gt; into smaller vias with specified &lt;step&gt; and bottom/left end &lt;offset&gt; and vertical/horizontal &lt;length&gt;, the correct value should be {threshold step offset length}</p> <p><b>Type:</b> string</p> <p><b>Default:</b> 0 0 -1 -1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_split_long_via</a></p>
add_stripes_split_vias	<p>create multiple partial vias</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_split_vias</a></p>
add_stripes_split_wire_spacing	<p>Specifies the spacing between each split wire</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_split_wire_spacing</a></p>
add_stripes_split_wire_weight	<p>Deletes fewest IO wires to accommodate approximately n of 10 split stripe wires</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_split_wire_weight</a></p>
add_stripes_split_wire_width	

	<p>Specifies the width of each split wire  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 0.0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_split_wire_width</a></p>
<b>add_stripes_stacked_via_bottom_layer</b>	
	<p>lef layer name  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> bottomLayer  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_stacked_via_bottom_layer</a></p>
<b>add_stripes_stacked_via_top_layer</b>	
	<p>lef layer name  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> topLayer  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_stacked_via_top_layer</a></p>
<b>add_stripes_stapling_nets_style</b>	
	<p>Specify the stapling style if multiple nets are specified  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> end_to_end side_to_side side_to_side_full_nets  <b>Default:</b> end_to_end  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_stapling_nets_style</a></p>
<b>add_stripes_stapling_shift</b>	
	<p>shift stapling stripe to avoid the drc automatically  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_stapling_shift</a></p>
<b>add_stripes_stop_at_closest_target</b>	
	<p>Specifies the stripe to specified target when over_pins is enabled.  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> none block_ring core_ring stripe  <b>Default:</b> none  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_stripes_stop_at_closest_target</a></p>

add_stripes_stop_at_last_wire_for_area	Specifies whether to trim back stripe antennas to the closest wire or pin of the same net <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_stripes_stop_at_last_wire_for_area</a>
add_stripes_stripe_min_length	Specifies the minimum stripe length <b>Type:</b> <a href="#">string</a> <b>Default:</b> stripe_width <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_stripes_stripe_min_length</a>
add_stripes_stripe_min_width	Specifies the min width of remaining stripe after being trimmed <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_stripes_stripe_min_width</a>
add_stripes_switch_cell_name	Specifies the switch cells to be treated as rings <b>Type:</b> <a href="#">string</a> <b>Default:</b> none <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_stripes_switch_cell_name</a>
add_stripes_switch_layer_overlap_length	Specifies the overlap distance used for the via between a stripe layer and the layer being switched to <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_stripes_switch_layer_overlap_length</a>
add_stripes_trim_antenna_back_to_shape	

	<p>Specifies the distance between the end of antenna and blocked target</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> none block_ring core_ring pad_ring stripe</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_trim_antenna_back_to_shape</a></p>
add_stripes_trim_antenna_max_distance	<p>Specifies the distance between the end of antenna and blocked target</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_trim_antenna_max_distance</a></p>
add_stripes_trim_stripe	<p>Specifies if stripe is trimmed by the specified shape.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> none design_boundary core_boundary</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_trim_stripe</a></p>
add_stripes_use_exact_spacing	<p>Specifies whether to use exact spacing</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_use_exact_spacing</a></p>
add_stripes_use_point_to_point_route	<p>Specifies whether to use exact spacing</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_use_point_to_point_route</a></p>
add_stripes_use_stripe_width	<p>Specifies whether to use stripe width</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">add_stripes_use_stripe_width</a></p>

add_stripes_via_using_exact_crossover_size	
	generate partial vias of the exact crossover size <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_stripes_via_using_exact_crossover_size</a>
add_stripes_width_file	
	Specify the values of recommended width in the file name <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_stripes_width_file</a>
add_tieoffs_cells	
	Set tie cell lists for set_db command <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_tieoffs_cells</a>
add_tieoffs_create_hports	
	Add tie-cells in different hierarchy than tie-off pins when possible <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_tieoffs_create_hports</a>
add_tieoffs_honor_dont_touch	
	honor dont_touch attribute on nets, insts, cells and modules <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_tieoffs_honor_dont_touch</a>
add_tieoffs_honor_dont_use	
	honor dont_use attribute on cells. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_tieoffs_honor_dont_use</a>

add_tieoffs_max_distance	
	<p>distance between tie-cell and tie-pins should be less than given value  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 0.0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_tieoffs_max_distance</a></p>
add_tieoffs_max_fanout	
	<p>the number of tie-pins a tie-net can drive. A '0' means no-limit  <b>Type:</b> <a href="#">int</a>  <b>Default:</b> 0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_tieoffs_max_fanout</a></p>
add_tieoffs_module_prevention	
	<p>add tie cell for module instantiation port  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_tieoffs_module_prevention</a></p>
add_tieoffs_prefix	
	<p>Prefix of tie cell instances  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_tieoffs_prefix</a></p>
add_tieoffs_report_hports	
	<p>Report created ports when add_tieoffs_create_hports is set  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_tieoffs_report_hports</a></p>
add_well_taps_avoid_abutment	
	<p>Specifies whether the inserted taps should avoid horizontal and vertical abutment  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_well_taps_avoid_abutment</a></p>

add_well_taps_block_boundary_only	Specifies whether inserting termination cells on the core boundary <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_well_taps_block_boundary_only</a>
add_well_taps_bottom_tap_cell	Cell to be used as bottom tap for add_endcaps boundary cell insertion flow <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_well_taps_bottom_tap_cell</a>
add_well_taps_bottom_termination_cell	Specifies the list of bottom termination cells to be used <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_well_taps_bottom_termination_cell</a>
add_well_taps_cell	Cell to be used as well_taps <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_well_taps_cell</a>
add_well_taps_channel_offset	Specifies the offset value between taps and blockage in channel <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_well_taps_channel_offset</a>
add_well_taps_check_channel	Specifies whether checking blockage channel <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_well_taps_check_channel</a>

add_well_taps_column_cells	Specifies the list of cells which can be replaced by termination cell <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_well_taps_column_cells</a>
add_well_taps_create_rows	Create rows for welltap cell techSites which do not have rows in the floor plan <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_well_taps_create_rows</a>
add_well_taps_in_row_offset	Specifies the distance between the first wellTap in a row and the start of the row <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_well_taps_in_row_offset</a>
add_well_taps_insert_cells	Insert well-taps based on cell, layer and inertval <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_well_taps_insert_cells</a>
add_well_taps_rule	Specifies the well latch-up rule <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_well_taps_rule</a>
add_well_taps_site_offset	Specifies the offset value in number of sites that vertical taps need to be aware of <b>Type:</b> <a href="#">int</a> <b>Default:</b> 1 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">add_well_taps_site_offset</a>

add_well_taps_termination_align	
	<p>Specifies the termination cell align  <b>Type:</b> enum  <b>Enum Values:</b> left right center  <b>Default:</b> left  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_well_taps_termination_align</a></p>
add_well_taps_termination_cells	
	<p>Specifies the list of termination cells to be used  <b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_well_taps_termination_cells</a></p>
add_well_taps_top_tap_cell	
	<p>Cell to be used as top tap for add_endcaps boundary cell insertion flow  <b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_well_taps_top_tap_cell</a></p>
add_well_taps_top_termination_cell	
	<p>Specifies the list of top termination cells to be used  <b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_well_taps_top_termination_cell</a></p>
add_well_taps_vertical_boundary_spacing	
	<p>Specifies the spacing between center of tap cell and vertical boundary  <b>Type:</b> double  <b>Default:</b> -1.0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_well_taps_vertical_boundary_spacing</a></p>
add_well_taps_well_cut_cells	
	<p>Specifies the list of cells with the well cuts  <b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">add_well_taps_well_cut_cells</a></p>

analysis_views	Returns the information about the analysis views in the design. <b>Type:</b> <a href="#">obj(analysis_view)*</a> <b>Default:</b> "" <b>Edit:</b> No
analyze_proto_place_design	Runs cell placement <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">analyze_proto_place_design</a>
analyze_proto_read_timing_debug_report	Invokes timing debugger <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">analyze_proto_read_timing_debug_report</a>
analyze_proto_time_design	Invokes prototype timing analysis <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">analyze_proto_time_design</a>
analyze_proto_trial_route	Routes the design with specific setting <b>Type:</b> <a href="#">string</a> <b>Default:</b> off <b>Edit:</b> Yes <b>Reference:</b> <a href="#">analyze_proto_trial_route</a>
analyze_proto_trial_route_max_iteration	Specifies number of timing driven trialRoute iterations <b>Type:</b> <a href="#">int</a> <b>Default:</b> 4 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">analyze_proto_trial_route_max_iteration</a>
assign_pins_advanced_node_rule_support	

	If you use this parameter, all the pin related command will use design object shapes for deciding pin location which will give accurate result but will have larger runtime. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">assign_pins_advanced_node_rule_support</a>
assign_pins_allow_non_ndr_net_pins_on_ndr_tracks	A true value allows general pins to be placed on ndr tracks if available. Alternately, if the value is set to false, the ndr-track rule is followed strictly and the net's pins are placed on matching ndr tracks only. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">assign_pins_allow_non_ndr_net_pins_on_ndr_tracks</a>
assign_pins_allow_unconnected_in_abutted_edge	If you use this parameter, unconnected partition pin can be placed in abutted edge <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">assign_pins_allow_unconnected_in_abutted_edge</a>
assign_pins_blocked_boundary_macro_distance	This option blocks automatic pin assignment, from putting pins on the part of partition boundary facing block on layers with OBS, in the places where channel width between partition boundary and block is less than the value specified. For channel width below specified value, block all pins on boundary facing this channel on layers with OBS. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 3.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">assign_pins_blocked_boundary_macro_distance</a>
assign_pins_edit_in_batch	To enable/disable pin-editing in batch mode. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">assign_pins_edit_in_batch</a>
assign_pins_force_abutment_with_fixed	

	<p>For fixed abutted pins's connected pin, ignore soft constraints checks</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">assign_pins_force_abutment_with_fixed</a></p>
	<p><b>assign_pins_max_channel_width_as_abutted</b></p> <p>If you set this parameter value then all channel less than equal to specified value will be considered as abutted and abutment rules will be applied</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 3.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">assign_pins_max_channel_width_as_abutted</a></p>
	<p><b>assign_pins_max_distance_pair</b></p> <p>Ignores moving corresponding connected pins of 2-pin-connection nets where distance (in microns) between the pins is equal or greater than distance specified</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 50.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">assign_pins_max_distance_pair</a></p>
	<p><b>assign_pins_off_stripe</b></p> <p>Prevents the generation of pins on metal layers with respect to the power and ground stripe</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> below all none</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">assign_pins_off_stripe</a></p>
	<p><b>assign_pins_pin_to_stripe_distance</b></p> <p>Layer specific, keep distance (in microns) from pin to stripe</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">assign_pins_pin_to_stripe_distance</a></p>
	<p><b>assign_pins_pin_to_via_distance_non_preferred_direction</b></p>

	<p>Layer specific, keep distance (in microns) from pin to via-stack  <b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">assign_pins_pin_to_via_distance_non_preferred_direction</a></p>
<b>assign_pins_pin_to_via_distance_preferred_direction</b>	
	<p>Layer specific, keep distance (in microns) from pin to via-stack from the partition fence boundary  <b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">assign_pins_pin_to_via_distance_preferred_direction</a></p>
<b>assign_pins_promoted_macro_bottom_layer</b>	
	<p>Specifies the minimum metal layer name for promoting macro pins  <b>Type:</b> string  <b>Default:</b> 31  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">assign_pins_promoted_macro_bottom_layer</a></p>
<b>assign_pins_promoted_macro_top_layer</b>	
	<p>Specifies the maximum metal layer name for promoting macro pins  <b>Type:</b> string  <b>Default:</b> 31  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">assign_pins_promoted_macro_top_layer</a></p>
<b>assign_pins_restricted_boundary_macro_distance</b>	
	<p>This option blocks automatic pin assignment, from putting pins on the part of partition boundary facing block on layers with OBS, in the places where channel width between partition boundary and block is less than the value specified. For channel width below specified value: OBS area on the layer, channel length and channel width considered to allow suitable number of pins on boundary facing this channel.  <b>Type:</b> double  <b>Default:</b> 30.0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">assign_pins_restricted_boundary_macro_distance</a></p>
<b>assign_pins_strict_abutment</b>	

	To relax abutment violations, for placing multi partition pin of a net and non neighbor pins of a net on abutted edges <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">assign_pins_strict_abutment</a>
attributes	
	Short-cut for [get_db obj_types .attributes] <b>Type:</b> <a href="#">obj(attribute)*</a> <b>Default:</b> "" <b>Edit:</b> No
auto_file_dir	
	Represents the top-level directory to store files/sub-directories 'auto-generated' by the tool. <b>Type:</b> <a href="#">string</a> <b>Default:</b> ./ <b>Edit:</b> Yes <b>Reference:</b> <a href="#">auto_file_dir</a>
auto_file_prefix	
	Represents the prefix to be applied to all files/sub-directories 'auto-generated' by the tool. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">auto_file_prefix</a>
base_cells	
	All the base_cells from .lib, Verilog stubs, LEF or OA. <b>Type:</b> <a href="#">obj(base_cell)*</a> <b>Default:</b> "" <b>Edit:</b> No
base_pins	
	All the base_pins in all the base_cells. <b>Type:</b> <a href="#">obj(base_pin)*</a> <b>Default:</b> "" <b>Edit:</b> No
boundaries	

	<p>Short-cut to all the boundary objects (fence, region, etc.) in the design.</p> <p><b>Type:</b> <a href="#">obj(boundary)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
	<p><b>budget_abutted</b></p>
	<p>Assumes all partitions are abutted</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_abutted</a></p>
	<p><b>budget_accumulated</b></p>
	<p>To be used for flat constraints in case of nested partitions, in conjunction with set_db budget_use_accumulated</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_accumulated</a></p>
	<p><b>budget_boundary_model_path</b></p>
	<p>Directory path containing model files to be used with option useBoundaryCondition template</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_boundary_model_path</a></p>
	<p><b>budget_buffer_delay_adjustment</b></p>
	<p>User defined value for virtual buffer adjustment</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_buffer_delay_adjustment</a></p>
	<p><b>budget_buffer_delay_lib_cell</b></p>
	<p>user defined buffer which should be used for virtual buffer adjustment</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_buffer_delay_lib_cell</a></p>
	<p><b>budget_buffer_delay_selection_effort</b></p>

	<p>controls the tool effort for calculating the buffer delay adjustment internally</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> low high</p> <p><b>Default:</b> low</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_buffer_delay_selection_effort</a></p>
	<p><b>budget_constant_model</b></p>
	<p>Specifies the type of timing model created</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_constant_model</a></p>
	<p><b>budget_distribute_mmmc</b></p>
	<p>distributed multiple analysis views over multiple sessions</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_distribute_mmmc</a></p>
	<p><b>budget_drive_cell</b></p>
	<p>write boundary drive information</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_drive_cell</a></p>
	<p><b>budget_fix_top_level</b></p>
	<p>Fixes the top-level timing budget, and proportions the remaining timing budget only for the partitions</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_fix_top_level</a></p>
	<p><b>budget_fix_top_level_negative_path_only</b></p>

	Fixes the top-level timing budget, and proportions the remaining timing budget only for the partitions when the slack is negative <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">budget_fix_top_level_negative_path_only</a>
<b>budget_handle_complex_sdc</b>	handle sdc files with complex constructs and regular expressions in push down <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">budget_handle_complex_sdc</a>
<b>budget_ignore_dont_touch</b>	Specifies the handling of don't touch objects <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">budget_ignore_dont_touch</a>
<b>budget_include_latency</b>	Specifies whether the clock latency is included in the set_input_delay and set_output_delay constraints <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">budget_include_latency</a>
<b>budget_include_wire_loads_in_lib</b>	Include the wire loads in library model pin capacitance <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">budget_include_wire_loads_in_lib</a>
<b>budget_input_load</b>	write set_load for input pins <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">budget_input_load</a>

budget\_input\_transition

write input transition using set\_input\_transition  
**Type:** [bool](#)  
**Default:** false  
**Edit:** Yes  
**Reference:** [budget\\_input\\_transition](#)

budget\_justify\_lib

If true, generate justification files for libs  
**Type:** [bool](#)  
**Default:** false  
**Edit:** Yes  
**Reference:** [budget\\_justify\\_lib](#)

budget\_keep\_pin\_list\_for\_block\_ports

Preserve all fan-in and fan-out lists  
**Type:** [bool](#)  
**Default:** true  
**Edit:** Yes  
**Reference:** [budget\\_keep\\_pin\\_list\\_for\\_block\\_ports](#)

budget\_latency\_on\_clocks

write set\_clock\_latency on clocks  
**Type:** [bool](#)  
**Default:** false  
**Edit:** Yes  
**Reference:** [budget\\_latency\\_on\\_clocks](#)

budget\_local\_latency

Write user specific set\_clock\_latency constraints, provided through set\_partition\_user\_constraints\_file command, in partition constraint files  
**Type:** [bool](#)  
**Default:** false  
**Edit:** Yes  
**Reference:** [budget\\_local\\_latency](#)

budget\_local\_uncertainty

	<p>Use local uncertainty specified through set_partition_user_constraints_file command for partitions</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_local_uncertainty</a></p>
	<p><b>budget_make_negative_input_delay_zero</b></p> <p>To be backward compatible where negative set input delays were made zero</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_make_negative_input_delay_zero</a></p>
	<p><b>budget_master_clone</b></p> <p>controls the tool behaviour for master clones</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> master_only merged unique_view_per_hinst</p> <p><b>Default:</b> master_only</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_master_clone</a></p>
	<p><b>budget_no_false_paths_for_unconstrained_ports</b></p> <p>do not create false paths for unconstrained ports</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_no_false_paths_for_unconstrained_ports</a></p>
	<p><b>budget_no_hold_view</b></p> <p>Disable hold view budgeting</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_no_hold_view</a></p>
	<p><b>budget_no_setup_view</b></p> <p>Disable setup view budgeting</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_no_setup_view</a></p>

budget_override_net_cap	
	<p>Specifies the lump capacitance value.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 100.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_override_net_cap</a></p>
budget_pin_load	
	<p>write set_load with -pin_load information</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_pin_load</a></p>
budget_report_dir	
	<p>Alternate directory name for justify reports when -justify is given with create_timing_budget</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> budget_justify</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_report_dir</a></p>
budget_report_exception	
	<p>Enable justify exceptions info in create_timing_budget</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_report_exception</a></p>
budget_report_negative_slack_on_ports	
	<p>save warnings for ports having slack less than the specified value</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_report_negative_slack_on_ports</a></p>
budget_report_or_update_budget	
	<p>Enable the collection of data to use the update_timing_budget command</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_report_or_update_budget</a></p>

budget_snap_feedthru_budget_to	
	<p>Specifies the minimum delay value (in picoseconds) for the path from partition input port to partition output port.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_snap_feedthru_budget_to</a></p>
budget_snap_input_budget_to	
	<p>Specifies the minimum delay (in picoseconds) for the path from the partition input port to the internal register.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_snap_input_budget_to</a></p>
budget_snap_negative_only	
	<p>Considers the only negative slack paths when used with budget_snap_input_budget_to and budget_snap_output_budget_to.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_snap_negative_only</a></p>
budget_snap_output_budget_to	
	<p>Specifies the min delay (in picoseconds) for the path from the internal register to the partition output port.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_snap_output_budget_to</a></p>
budget_top_level	
	<p>Specifies the minimum % of total available budget set aside for the top level</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> -1.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_top_level</a></p>
budget_top_level_delay_per_length	

	<p>Specifies the top-level estimated delay (in picoseconds) per millimeter length.</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 180</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_top_level_delay_per_length</a></p>
<b>budget_top_level_min_delay_per_net</b>	
	<p>Specifies the top-level minimum delay-per-net value in picoseconds/millimeter units.</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 100</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_top_level_min_delay_per_net</a></p>
<b>budget_use_boundary_condition</b>	
	<p>Mechanism used for finding buffers to be used as driver/load</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> optimized template actual empty</p> <p><b>Default:</b> template</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_use_boundary_condition</a></p>
<b>budget_use_real_cell_for_timing_model</b>	
	<p>Use actual gate connected to the partition port to write out the model timing arc, else medium size buffer is used</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_use_real_cell_for_timing_model</a></p>
<b>budget_virtual_opt_engine</b>	
	<p>Specifies the virtual optimization engine to be used</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> none opt early_timing_engine proto</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_virtual_opt_engine</a></p>
<b>budget_write_constraints_for_clock_output_ports</b>	

	<p>Write constraints for clock output ports</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_write_constraints_for_clock_output_ports</a></p>
budget_write_false_path_for_hold	<p>write false path -hold for all I/Os in setup budgeting</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_write_false_path_for_hold</a></p>
budget_write_latency_per_clock	<p>write latency per clock instead of per port</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_write_latency_per_clock</a></p>
budget_write_virtual_io_clocks	<p>Write I/O Constraints using virtual clocks only</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">budget_write_virtual_io_clocks</a></p>
bumps	<p>Short-cut for [get_db current_design .bumps]</p> <p><b>Type:</b> <a href="#">obj(bump)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
bus_sink_groups	<p>A group of sinks (loads) that some floorplan and routing commands use to control adding buffers and routing for a bus. See 'help *bus_sink*' for a list of commands related to this object.</p> <p><b>Type:</b> <a href="#">obj(bus_sink_group)*</a></p> <p><b>Default:</b> {}</p> <p><b>Edit:</b> No</p>
busses	

	<p>Short-cut for [get_db current_design .busses]</p> <p><b>Type:</b> <a href="#">obj(bus)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
categories	
	<p>available categories of root attributes</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
ccopt_auto_limit_insertion_delay_factor	
	<p>CCOpt attempts to keep the insertion delays of each clock tree a fixed multiple of the longest insertion delay that would result from a global skew approach. This multiple can be modified by design timing and the presence of other clock trees, but will start at a fixed fraction above the global skew insertion delay. This attribute specifies that fixed fraction.</p> <p>Valid values: real</p> <p>See also:</p> <ul style="list-style-type: none"> <li>.ccopt_auto_limit_insertion_delay_factor_skew_group</li> </ul> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 1.5</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">ccopt_auto_limit_insertion_delay_factor</a></p>
ccopt_merge_clock_gates	
	<p>If set to true, clock gate merging is enabled. If this is false, merging of all clock gates is disabled, including clock gates which may have been cloned by CTS.</p> <p>Note that this attribute has no impact on 'ccopt_design -cts'. See also attribute <a href="#">cts_merge_clock_gates</a>.</p> <p>Valid values: true false</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">ccopt_merge_clock_gates</a></p>
ccopt_merge_clock_logic	

	<p>If set to true, clock logic merging is enabled. If this is false, merging of all clock logics is disabled, including clock logics which may have been cloned by CTS.</p> <p>Note that this attribute has no impact on 'ccopt_design -cts'. See also attribute <code>cts_merge_clock_logic</code>.</p> <p>Valid values: true false</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">ccopt_merge_clock_logic</a></p>
<b>check_ac_limit_avg_recovery</b>	
	<p>override QRC tech em_recover factor for all layers used in lavg limits.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_avg_recovery</a></p>
<b>check_ac_limit_check_thermal_aware_em</b>	
	<p>check thermal aware EM</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>check_ac_limit_current_file</b>	
	<p>Specify current file to provide currents for cell/instance's pin.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_current_file</a></p>
<b>check_ac_limit_current_scale_factor</b>	
	<p>Scale Signal EM current, syntax: -current_scale_factor { [rms &lt;rms_value&gt;] [peak &lt;peak_value&gt;] [avg &lt;avg_value&gt;] }</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_current_scale_factor</a></p>
<b>check_ac_limit_current_scale_table</b>	

	<p>Specifies the layer-based scale table for current</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_current_scale_table</a></p>
<b>check_ac_limit_default_freq_for_unconstrained_nets</b>	
	<p>Specifies the frequency for EM calculation when a net has no defined frequency or a defined frequency of 0Hz in the design.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_default_freq_for_unconstrained_nets</a></p>
<b>check_ac_limit_delta_temperature</b>	
	<p>maximum change in temperature allowed in units of Celsius. Used in the QRC tech for RMS limits. Default=5.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 5.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_delta_temperature</a></p>
<b>check_ac_limit_delta_temperature_layer_list</b>	
	<p>Specifies layer based delta temperature for EM RMS currnet limit analysis</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>check_ac_limit_detailed</b>	
	<p>Generates a detailed report containing information for all signal nets, including those without violations</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_detailed</a></p>
<b>check_ac_limit_effort_level</b>	

	<p>Enum_list legal values are: low, medium, high. Default: low.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> low medium high</p> <p><b>Default:</b> low</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_effort_level</a></p>
check_ac_limit_em_limit_scale_factor	<p>Scale Signal EM limit, syntax: -em_limit_scale_factor { [rms &lt;rms_value&gt;] [peak &lt;peak_value&gt;] [avg &lt;avg_value&gt;] }</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_em_limit_scale_factor</a></p>
check_ac_limit_em_limit_scale_table	<p>Specifies the layer-based scale table for em_limit</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_em_limit_scale_table</a></p>
check_ac_limit_em_res_width	<p>Specifies width used to get EM limit. enum_list legal values are: drawn, silicon. Default: drawn.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> drawn silicon</p> <p><b>Default:</b> drawn</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_em_res_width</a></p>
check_ac_limit_em_temperature	<p>Specifies the temperature used to lookup the temperature scaling factor. By default, no scaling is done.</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_em_temperature</a></p>
check_ac_limit_em_temperature_layer_list	

	Specifies layer based EM temperature for EM AVG current limit analysis <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes
check_ac_limit_em_threshold	
	The value is the ratio of signal current (avg/peak/rms) to the respective EM limit. Default: 1.0. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 1.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">check_ac_limit_em_threshold</a>
check_ac_limit_enable_seb	
	Enable SEB calculation <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
check_ac_limit_env_temperature	
	<b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes
check_ac_limit_extraction_tech_file	
	Specify qrcTechFile name. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">check_ac_limit_extraction_tech_file</a>
check_ac_limit_force_hold_view	
	<b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">check_ac_limit_force_hold_view</a>
check_ac_limit_handle_pin_obs_via	

	<p><b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">check_ac_limit_handle_pin_obs_via</a></p>
check_ac_limit_ict_em_models	<p>Specify ict EM file to provide EM rule if EM rule not exists in qrcTechFile.</p> <p><b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">check_ac_limit_ict_em_models</a></p>
check_ac_limit_lifetime	<p>Specifies the hours of operation used to lookup the lifetime scaling factor. By default, no scaling is done.</p> <p><b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">check_ac_limit_lifetime</a></p>
check_ac_limit_max_error	<p><b>Type:</b> <a href="#">int</a> <b>Default:</b> 10000 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">check_ac_limit_max_error</a></p>
check_ac_limit_method	<p>Specifies the current waveform calculation method, check one or more of lrms, lpeak, and lavg limits. enum_list legal values are: rms, peak, avg. Default: rms.</p> <p><b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">check_ac_limit_method</a></p>
check_ac_limit_min_peak_duty_ratio	

	<p>Do not check Ipeak for nets with duty ratio below &lt;duty_ratio&gt;. default = 0.05, range 0.0 to 1.0.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_min_peak_duty_ratio</a></p>
<b>check_ac_limit_min_peak_freq</b>	
	<p>Do not check Ipeak for nets with frequency below &lt;freq&gt; in units of hertz. default = 1e6.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_min_peak_freq</a></p>
<b>check_ac_limit_net_file</b>	
	<p>Specifies from file the net to check in signalEM analysis</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_net_file</a></p>
<b>check_ac_limit_nets</b>	
	<p>Specifies whether to check named or selected nets</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_nets</a></p>
<b>check_ac_limit_out_file</b>	
	<p>Specifies the report file for the violation data</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_out_file</a></p>
<b>check_ac_limit_peak_td_method</b>	

	<p>Specifies Td calculation method for Ipeak check. enum_list legal values are: effective_width_from_integration, effective_half_peak_width, max_equivalent_dc_peak, sum_half_peak_width. Default: effective_width_from_integration.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> effective_width_from_integration effective_half_peak_width max_equivalent_dc_peak sum_half_peak_width</p> <p><b>Default:</b> effective_width_from_integration</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_peak_td_method</a></p>
check_ac_limit_seb_lifetime	<p>Specifies the hours of operation. By default, it's 5 years.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 43800.0</p> <p><b>Edit:</b> Yes</p>
check_ac_limit_seb_table	<p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
check_ac_limit_seb_temperature	<p>Specifies the temperature of operation. By default, it's 110c.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> -273.0</p> <p><b>Edit:</b> Yes</p>
check_ac_limit_selected	<p>Specifies whether to check named or selected nets</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_selected</a></p>
check_ac_limit_skip_category_mode	<p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_skip_category_mode</a></p>
check_ac_limit_skip_net	

	<p>Specifies the net to be skipped in signalEM analysis</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_skip_net</a></p>
<b>check_ac_limit_skip_net_file</b>	
	<p>Specifies the net to be skipped in signalEM analysis</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_skip_net_file</a></p>
<b>check_ac_limit_toggle</b>	
	<p>Specifies the toggle rate for signal nets</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_toggle</a></p>
<b>check_ac_limit_use_db_freq</b>	
	<p>Uses the database frequency value as the effective frequency per net</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_use_db_freq</a></p>
<b>check_ac_limit_use_new_api</b>	
	<p>Signal EM support of new AAE API for bidirectional net</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>check_ac_limit_use_qrc_tech</b>	
	<p>Turn this on to force lrms checks to use the QRC tech file rather than the LEF tech. If either lpeak or lavg is also checked, then all checks will use the QRC tech file, including lrms.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_ac_limit_use_qrc_tech</a></p>
<b>check_ac_limit_use_rms_delta_t</b>	

	<p><b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes</p>
	<p>check_ac_limit_use_simulation</p>
	<p>use simulation-based EM analysis at 3 cases: [1] multi-pin; [2] multi-driver; [3] mesh structure</p> <p><b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes</p>
	<p>check_ac_limit_view</p>
	<p>Specifies the name of the view</p> <p><b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">check_ac_limit_view</a></p>
	<p>check_drc_area</p>
	<p>Specifies the coordinates of the area to verify</p> <p><b>Type:</b> <a href="#">rect</a> <b>Default:</b> 0.0 0.0 0.0 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">check_drc_area</a></p>
	<p>check_drc_check_only</p>
	<p>Specifies what kind of shapes to be checked.</p> <p><b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> all regular special selected_net cell default <b>Default:</b> default <b>Edit:</b> Yes <b>Reference:</b> <a href="#">check_drc_check_only</a></p>
	<p>check_drc_check_routing_halo</p>
	<p>Check routing halo.</p> <p><b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">check_drc_check_routing_halo</a></p>
	<p>check_drc_check_routing_halo_corner</p>

	<p>Check routing halo in the corner</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_drc_check_routing_halo_corner</a></p>
<p>check_drc_disable_rules</p>	
	<p>Disable the rule that from the provided rule list. the rule list as follow: (jog2jog_spacing   eol_spacing cut_spacing min_cut enclosure color min_step protrusion min_area out_of_die)</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> jog2jog_spacing eol_spacing cut_spacing min_cut enclosure color min_step protrusion min_area out_of_die</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_drc_disable_rules</a></p>
<p>check_drc_exclude_pg_net</p>	
	<p>Excludes the checking of power and ground nets.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_drc_exclude_pg_net</a></p>
<p>check_drc_ignore_cell_blockage</p>	
	<p>Ignore geometries of cell blockage.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_drc_ignore_cell_blockage</a></p>
<p>check_drc_ignore_trial_route</p>	
	<p>Ignore trial route when check drc.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_drc_ignore_trial_route</a></p>
<p>check_drc_inside_via_def</p>	

	<p>Check the cut spacing from the same via</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_drc_inside_via_def</a></p>
check_drc_layer_range	<p>Checks between the range of metal layers including cut layers in between</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_drc_layer_range</a></p>
check_drc_limit	<p>Specifies the maximum number of errors to report</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1000</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_drc_limit</a></p>
check_drc_max_wrong_way_halo	<p>Specifies the maximum wrong way halo</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> -1.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_drc_max_wrong_way_halo</a></p>
check_drc_ndr_spacing	<p>Specifies what kind of non-default rule spacing to be checked</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> true false auto</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_drc_ndr_spacing</a></p>
check_drc_report	<p>Specifies the report file that contains the violations information</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">check_drc_report</a></p>
check_drc_trim_length	

	Consider max length in the trim shape layer. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">check_drc_trim_length</a>
<b>check_drc_uncolored</b>	
	report color change violation when the dpt layer shape is free color. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">check_drc_uncolored</a>
<b>check_drc_use_min_spacing_on_block_obs</b>	
	Use min spacing to check for block OBS. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> true false auto <b>Default:</b> auto <b>Edit:</b> Yes <b>Reference:</b> <a href="#">check_drc_use_min_spacing_on_block_obs</a>
<b>clock_tree_source_groups</b>	
	list of <code>clock_tree_source_group</code> <b>Type:</b> <a href="#">obj(clock_tree_source_group)*</a> <b>Default:</b> "" <b>Edit:</b> No <b>Reference:</b> <a href="#">clock_tree_source_groups</a>
<b>clock_trees</b>	
	list of <code>clock_tree</code> <b>Type:</b> <a href="#">obj(clock_tree)*</a> <b>Default:</b> "" <b>Edit:</b> No <b>Reference:</b> <a href="#">clock_trees</a>
<b>clocks</b>	
	clocks <b>Type:</b> <a href="#">obj(clock)*</a> <b>Allowed -index values:</b> analysis_view <b>Default:</b> "" <b>Edit:</b> No
<b>cmd_file</b>	

	<p>cmd log file name of the program  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cmd_file</a></p>
cmd_file_line_length_limit	<p>Limits the number of characters printed to the .cmd file for any single command. As the variables are expanded by default when stored in the .cmd file the file can become quite large if a variable contains a very large list (examples of commands that can produce large lists are: get_db and get_computed_shapes). A value of -1 indicates that there is no limit on the number of characters per command output to the .cmd file  <b>Type:</b> <a href="#">int</a>  <b>Default:</b> 1000  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cmd_file_line_length_limit</a></p>
constraint_modes	<p>Returns the information about the constraint modes in the design.  <b>Type:</b> <a href="#">obj(constraint_mode)*</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
cts_allow_non_std_clock_gate_inputs	<p>If this attribute is set, CTS will allow the use of clock gates with non-standard pins. CCOpt considers the following pin types to be standard: clock pins, enable pins, test enable pins, retention pins and power gating pins. Before starting CTS CCOpt will emit a warning, indicating which pin(s) it considers non-standard.  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_allow_non_std_clock_gate_inputs</a></p>
cts_balance_mode	

	<p>Replace CCOpt mode setting cts_opt_type {full   cluster   trial}. If not full, causes CCOpt and CCOpt CTS to halt before final completion of the clock tree to facilitate clock tree inspection. The possible values for this attribute are as follows:</p> <ul style="list-style-type: none"> <li>- full - default value, a full CTS is performed.</li> <li>- cluster - a cluster-only CTS is performed. The clock tree has no balancing delay applied.</li> <li>- trial - The clock has only virtual (numeric annotation) balancing delays applied.</li> </ul> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> full</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_balance_mode</a></p>
<b>cts_buffer_cells</b>	
	<p>Specifies the buffer cells for CTS. If none are specified CCOpt will choose buffers from the libraries.</p> <p>Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names.</p> <p>If set explicitly, CCOpt will ignore any dont_use settings for the cells specified.</p> <p>Different buffer cells may be specified for any combination of clock tree and power domain.</p> <p>To use different buffers for each net type set the cts_buffer_cells_top and cts_buffer_cells_leaf attributes .</p> <p>Some examples follow:</p> <p>To specify buffer cells for all clock trees and all power domains:</p> <pre>set_db cts_buffer_cells {bufAX* bufBX*}</pre> <p>To specify buffer cells for a particular clock tree and all power domains:</p> <pre>set_db clock_tree:&lt;clk&gt;.cts_buffer_cells {bufX20 bufX18}</pre> <p>To specify buffer cells for a particular clock tree and power domain:</p> <pre>set_db clock_tree:&lt;clk&gt;.cts_buffer_cells -index {power_domain &lt;pd&gt;} {bufX12 bufX8}</pre> <p>Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> power_domain</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_buffer_cells</a></p>
<b>cts_buffer_cells_leaf</b>	

	<p>Specifies the buffer cells available for CTS to use on leaf nets. If none are specified CCOpt will use the same buffers as on trunk nets (as specified in the cts_buffer_cells attribute). Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names. If set explicitly, CCOpt will ignore any dont_use settings for the cells specified. Different leaf buffer cells may be specified for any combination of clock tree and power domain. Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> power_domain</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_buffer_cells_leaf</a></p>
cts_buffer_cells_top	<p>Specifies the buffers cells available for CTS to use on top nets. If none are specified CCOpt will use the same buffers as on trunk nets (as specified in the cts_buffer_cells attribute). Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names. If set explicitly, CCOpt will ignore any dont_use settings for the cells specified. Different top buffer cells may be specified for any combination of clock tree and power domain. Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> power_domain</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_buffer_cells_top</a></p>
cts_buffer_move_location_count	<p>When fixing slew by moving buffers, the number of destination locations to consider.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> 3</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_buffer_move_location_count</a></p>
cts_cell_halo_rows	

	<p>Specifies the clock halo in the y direction in rows for all clock cells.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_cell_halo_rows</a></p>
<b>cts_cell_halo_sites</b>	
	<p>Specifies the clock halo in the x direction in sites for all clock cells.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 4</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_cell_halo_sites</a></p>
<b>cts_cell_halo_x</b>	
	<p>Specifies the cell halo distance in the x direction. The default value of this attribute is auto. By default, CCOpt can automatically compute a cts_cell_halo_x in terms of cts_cell_density attribute.</p> <p>See also:</p> <ul style="list-style-type: none"> <li>. <a href="#">cts_cell_density</a></li> </ul> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> power_domain</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_cell_halo_x</a></p>
<b>cts_cell_halo_y</b>	
	<p>Specifies the cell halo distance in the y direction. The default value of this attribute is auto. By default, CCOpt can automatically compute a cts_cell_halo_y in terms of cts_cell_density attribute.</p> <p>See also:</p> <ul style="list-style-type: none"> <li>. <a href="#">cts_adjacent_rows_legal</a></li> </ul> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> power_domain</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_cell_halo_y</a></p>
<b>cts_clock_gate_movement_limit</b>	

	<p>Each clock gate is restricted to a Manhattan ball centered on its original location with CTS flow.</p> <p>The radius of the ball is a multiple of the clock gate height.</p> <p>This controls the default value of that multiple.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> 10</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_clock_gate_movement_limit</a></p>
<b>cts_clock_gating_cells</b>	
	<p>Specifies the clock gates for CTS. If none are specified CCOpt will choose clock gates from the libraries.</p> <p>Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names.</p> <p>If set explicitly, CCOpt will ignore any dont_use settings for the cells specified.</p> <p>Different clock gates may be specified for any combination of clock tree and power domain. Some examples follow:</p> <p>To specify clock gates for all clock trees and all power domains:</p> <pre>set_db cts_clock_gating_cells {cgAX* cgBX*}</pre> <p>To specify clock gates for a particular clock tree and all power domains:</p> <pre>set_db clock_tree:&lt;clk&gt;.cts_clock_gating_cells {cgX20 cgX18}</pre> <p>To specify clock gates for a particular clock tree and power domain:</p> <pre>set_db clock_tree:&lt;clk&gt;.cts_clock_gating_cells -index {power_domain &lt;pd&gt;} {cgX12 cgX8}</pre> <p>Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> power_domain</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_clock_gating_cells</a></p>
<b>cts_clock_source_cells</b>	

	<p>Specifies the cells available for CTS to size clock sources if the cts_size_clock_sources attribute is set to true. If none are specified the tool will choose cells from the libraries. Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names.</p> <p>If set explicitly, the tool will ignore any dont_use settings for the cells specified.</p> <p>Different cells may be specified for clock trees or power domains. Only clock sources that are buffers, inverters, logic and clock gating cells with a single output can be resized.</p> <p>Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> power_domain</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_clock_source_cells</a></p>
<b>cts_clock_tree_source_group_clock_trees</b>	
	<p>A list of the clock trees relevant to this source group.</p> <p>Valid values: list cts_clock_trees</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_clock_tree_source_group_clock_trees</a></p>
<b>cts_clock_tree_source_input_max_transition_time</b>	
	<p>The slew which will be assumed at the input of the root driver.</p> <p>Valid values: double</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Allowed -index values:</b> delay_corner</p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_clock_tree_source_input_max_transition_time</a></p>
<b>cts_delay_cells</b>	

	<p>Specifies the delay cells available for CTS. If none are specified CCOpt will not use delay cells.</p> <p>Setting this attribute to the string 'auto' means that CCOpt will choose delay cells from the libraries to use.</p> <p>Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names.</p> <p>If set explicitly, CCOpt will ignore any dont_use settings for the cells specified.</p> <p>Different delay cells may be specified for any combination of clock tree and power domain, or by omitting those arguments a global setting can be applied.</p> <p>Some examples follow:</p> <p>To specify delay cells for all clock trees and power domains:  <code>set_db cts_delay_cells {delayAX* delayBX*}</code></p> <p>To specify delay cells for a particular clock tree and all power domains:  <code>set_db clock_tree:&lt;clk&gt;.cts_delay_cells {delayX1 delayX2}</code></p> <p>To specify delay cells for a particular clock tree and power domain:  <code>set_db clock_tree:&lt;clk&gt;.cts_delay_cells -index {power_domain &lt;pd&gt;} {delayX2 delayX3}</code></p> <p>Valid values: a list of library cell names, or a list of patterns to expand to library cell names, or the string 'auto'</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> <a href="#">power_domain</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_delay_cells</a></p>
	<p><b>cts_detailed_cell_warnings</b></p>
	<p>If set to true, CCOpt outputs detailed cell warning diagnostics when it encounters issues with library cell selection, power domains and/or signal levels.</p> <p>Valid values: true false</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_detailed_cell_warnings</a></p>
	<p><b>cts_exit_if_no_placeable_area</b></p>

	<p>Specifies that CTS should exit if the design has zero placeable area. Setting this attribute may be useful to temporarily work-around problems with row definition and/or blockages causing placeable area to be zero. Valid values: true false</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_exit_if_no_placeable_area</a></p>
<b>cts_exit_if_skew_target_over_constrained</b>	
	<p>Specifies that CCOpt should exit as current skew targets are likely to lead to poor results. By default, CCOpt computes a minimum skew target which should not lead to excessive buffering, and does not allow any skew target to be set lower than this minimum. This attribute overrides that check, and allows any skew target to be used. Valid values: true false</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_exit_if_skew_target_over_constrained</a></p>
<b>cts_exit_if_transition_target_over_constrained</b>	
	<p>Specifies that CCOpt should exit, as with current slew targets it is likely to lead to runtime problems. By default, CCOpt computes a minimum slew target which should not lead to runtime problems, and does not allow any slew target to be set lower than this minimum. This attribute overrides that check, and allows any slew target to be used. Valid values: true false</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_exit_if_transition_target_over_constrained</a></p>
<b>cts_fix_clock_sinks</b>	
	<p>If set to true, we will DEF lock clock tree sinks after routing in addition to any clock node locking (fixed). If set to soft, we will DEF lock clock tree sinks after routing in addition to any clock node soft_locking (softFixed). Valid values: true false soft</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_fix_clock_sinks</a></p>

cts_flexible_htree OMIT_symmetry	<p>Controls the omission of symmetry features to balance a flexible H-tree. Symmetry drivers are drivers that are added to balance pin capacitances at branch points. For example, if buffer pairs are inserted at branch points, one of these buffers may not drive any fanout and is inserted to match other buffer pairs at the same level of the flexible H-tree. Omitting symmetry drivers can reduce the power of the H-tree but increase its skew. Similarly, symmetry branches are branches that are needed to balance the wire load at branch points. They are added to match other branchpoints at the same level of the flexible H-tree.</p> <p>By default, symmetry branches and drivers are added.</p> <p>Possible values for this attribute:</p> <ul style="list-style-type: none"> <li>false Add symmetry branches and drivers</li> <li>true Omit both symmetry drivers and branches</li> <li>drivers Omit symmetry drivers</li> <li>branches Omit symmetry branches</li> <li>{drivers branches} Omit both symmetry drivers and branches</li> <li>{ } Add symmetry branches and drivers</li> </ul> <p><b>Type:</b> string  <b>Default:</b> auto  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_flexible_htree OMIT_symmetry</a></p>
cts_flexible_htree_placement_legalization_effort	<p>The legalization effort for finding placement unblocked points on the synthesis grid for flexible H-trees. High placement legalization effort can avoid having to relax placement constraints when implementing H-trees but may lead to increased runtime.</p> <p>Valid values: low, high (default low)</p> <p><b>Type:</b> string  <b>Default:</b> low  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_flexible_htree_placement_legalization_effort</a></p>
cts_inst_name_prefix	<p>The name prefix of instances created by CTS. The default value is "CTS". The default names of instances are CTS_ *.</p> <p>Valid values: string</p> <p><b>Type:</b> string  <b>Default:</b> CTS  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_inst_name_prefix</a></p>
cts_inverter_cells	

	<p>Specifies the inverter cells available for CTS. If none are specified CCOpt will choose inverters from the libraries.</p> <p>Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names.</p> <p>If set explicitly, CCOpt will ignore any dont_use settings for the cells specified.</p> <p>Different inverter cells may be specified for any combination of clock tree and power domain.</p> <p>To use different inverters for each net type set the cts_inverter_cells_top and cts_inverter_cells_leaf attributes .</p> <p>Some examples follow:</p> <p>To specify inverter cells for all clock trees and all power domains:</p> <pre>set_db cts_inverter_cells {invAX* invBX*}</pre> <p>To specify inverter cells for a particular clock tree and all power domains:</p> <pre>set_db clock_tree:&lt;clk&gt;.cts_inverter_cells {invX20 invX18}</pre> <p>To specify inverter cells for a particular clock tree and power domain:</p> <pre>set_db clock_tree:&lt;clk&gt;.cts_inverter_cells -index {power_domain &lt;pd&gt;} {invX12 invX8}</pre> <p>Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> power_domain</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_inverter_cells</a></p>
cts_inverter_cells_leaf	<p>Specifies the inverter cells available for CTS to use on leaf nets. If none are specified CCOpt will use the same inverters as on trunk nets (as specified in the cts_inverter_cells attribute).</p> <p>Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names.</p> <p>If set explicitly, CCOpt will ignore any dont_use settings for the cells specified.</p> <p>Different leaf inverter cells may be specified for any combination of clock tree and power domain.</p> <p>Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> power_domain</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_inverter_cells_leaf</a></p>
cts_inverter_cells_top	

	<p>Specifies the inverter cells available for CTS to use on top nets. If none are specified CCOpt will use the same inverters as on trunk nets (as specified in the <code>cts_inverter_cells</code> attribute). Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names. If set explicitly, CCOpt will ignore any <code>dont_use</code> settings for the cells specified. Different top inverter cells may be specified for any combination of clock tree and power domain. Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> <code>power_domain</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_inverter_cells_top</a></p>
<b>cts_logic_cells</b>	
	<p>Specifies the clock logics for CTS. If none are specified CCOpt will choose clock logics from the libraries. Cell names may be specified as a Tcl list of names, or as a Tcl list of patterns to be expanded to match names. If set explicitly, CCOpt will ignore any <code>dont_use</code> settings for the cells specified. Different logic cells may be specified for any combination of clock tree and power domain. Some examples follow:</p> <p>To specify logic cells for all clock trees and all power domains:  <code>set_db cts_logic_cells {and* mux*}</code></p> <p>To specify logic cells for a particular clock tree and all power domains:  <code>set_db clock_tree:&lt;clk&gt;.cts_logic_cells {andX20 andX18}</code></p> <p>To specify logic cells for a particular clock tree and power domain:  <code>set_db clock_tree:&lt;clk&gt;.cts_logic_cells -index {power_domain &lt;pd&gt;} {andX12 andX8}</code></p> <p>Valid values: a list of library cell names, or a list of patterns to expand to library cell names</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> <code>power_domain</code></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_logic_cells</a></p>
<b>cts_manage_power_intent_violations</b>	

	<p>If this attribute is set, the CTS algorithm will work around power management illegalities in the clock tree, as opposed to failing with an error when it encounters them. This allows the clock tree to be synthesized, but any power management illegalities will remain in the exported design.</p> <p>Valid values: true false</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_manage_power_intent_violations</a></p>
cts_max_fanout	<p>The maximum fanout at any point in the clock tree.</p> <p>Valid values: integer ranged between 2 and 1000 inclusive</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 100</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_max_fanout</a></p>
cts_max_source_to_sink_net_length	<p>The maximum routing length in microns between driving source pin and driven sink pin on each net that clock tree synthesis should observe.</p> <p>This constraint can be applied to either a pin, a clock tree, or a net type.</p> <p>By default (if this attribute is not set) no explicit clock tree net length constraint is enforced. However, other clock tree constraints such as maximum slew (transition) and maximum capacitance will indirectly limit the maximum net length.</p> <p>Valid values: double</p> <p><b>Type:</b> string</p> <p><b>Default:</b> top auto trunk auto leaf auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_max_source_to_sink_net_length</a></p>
cts_max_source_to_sink_net_length_leaf	

	<p>The maximum routing length in microns between driving source pin and driven sink pin on each net that clock tree synthesis should observe. This constraint can be applied to either a pin, a clock tree, or a net type. By default (if this attribute is not set) no explicit clock tree net length constraint is enforced. However, other clock tree constraints such as maximum slew (transition) and maximum capacitance will indirectly limit the maximum net length.</p> <p>Valid values: double</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_max_source_to_sink_net_length_leaf</a></p>
cts_max_source_to_sink_net_length_top	<p>The maximum routing length in microns between driving source pin and driven sink pin on each net that clock tree synthesis should observe. This constraint can be applied to either a pin, a clock tree, or a net type. By default (if this attribute is not set) no explicit clock tree net length constraint is enforced. However, other clock tree constraints such as maximum slew (transition) and maximum capacitance will indirectly limit the maximum net length.</p> <p>Valid values: double</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_max_source_to_sink_net_length_top</a></p>
cts_max_source_to_sink_net_length_trunk	<p>The maximum routing length in microns between driving source pin and driven sink pin on each net that clock tree synthesis should observe. This constraint can be applied to either a pin, a clock tree, or a net type. By default (if this attribute is not set) no explicit clock tree net length constraint is enforced. However, other clock tree constraints such as maximum slew (transition) and maximum capacitance will indirectly limit the maximum net length.</p> <p>Valid values: double</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_max_source_to_sink_net_length_trunk</a></p>
cts_merge_clock_gates	

	<p>If set to true, clock gate merging is enabled. If this is false, merging of all clock gates is disabled, including clock gates which may have been cloned by CTS.</p> <p>Note that this attribute only impacts 'ccopt_design -cts'. See also attribute ccopt_merge_clock_gates.</p> <p>Valid values: true false</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_merge_clock_gates</a></p>
	<p>cts_merge_clock_logic</p>
	<p>If set to true, clock logic merging is enabled. If this is false, merging of all clock logics is disabled, including clock logics which may have been cloned by CTS.</p> <p>Note that this attribute only impacts 'ccopt_design -cts'. See also attribute ccopt_merge_clock_logic.</p> <p>Valid values: true false</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_merge_clock_logic</a></p>
	<p>cts_mixed_fanout_net_type</p>
	<p>Controls how CCOpt considers nets that have fanout consisting partially but not entirely of sinks. By default, having any sinks (eg. DFFs) will make the net be considered leaf, but when set to trunk, a net has to drive only sinks to be considered leaf. For example, a net driving a clock gate and a DFF would no longer count as a leaf net.</p> <p>Valid values: leaf trunk</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> leaf</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_mixed_fanout_net_type</a></p>
	<p>cts_move_clock_gates</p>

	<p>If this attribute is set, the CTS algorithm will move clock gates that appear in the clock tree. 'Logic' does not include clock gates, buffers, and inverters in a clock tree, which are always moved unless they are locked, or clock generators that are above the root of the clock tree. Usually, this will affect multiplexers used for selecting one of a number of clocks, or for switching between a test clock and the main clock. Setting this attribute may cause the clock tree to have a lower insertion delay, but might break datapath timing. During optimization, this is not a problem, because the timing will be automatically recovered during the optimization process.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_move_clock_gates</a></p>
cts_move_logic	<p>If this attribute is set, the CTS algorithm will move logic that appears in the clock tree. "Logic" does not include clock gates, buffers, and inverters in a clock tree, which are always moved unless they are locked, or clock generators that are above the root of the clock tree. Usually, this will affect multiplexers used for selecting one of a number of clocks, or for switching between a test clock and the main clock. Setting this attribute may cause the clock tree to have a lower insertion delay, but might break datapath timing. During optimization, this is not a problem, because the timing will be automatically recovered during the optimization process.</p> <p>Valid values: true false</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_move_logic</a></p>
cts_net_name_prefix	<p>The name prefix of nets created by CTS. The default value is "CTS". The default names of nets are CTS, CTS_1, CTS_2... ...</p> <p>Valid values: string</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> CTS</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_net_name_prefix</a></p>
cts_override_vias	

	<p>When specified, this attribute defines the vias to be used in RC extraction from routing estimates. The listed vias will be used in place of those configured on the routing rules for the clock network.</p> <p>The order of the list is irrelevant.</p> <p>The vias may also be overridden for each non-default rule (NDR). In this case, the name of the NDR is given as the first element in the list with subsequent entries being the via names. Multiple NDRs can be specified, e.g.</p> <p>{via1d {NDR1 via2d} {NDR2 via2d}} will override via1d in the default rule, and both via1d and via2d in NDR1 and NDR2.</p> <p>Valid values: list via_call</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_override_vias</a></p>
<b>cts_post_route_enable</b>	
	<p>Enable post-conditioning optimization after clock nets are routed.</p> <p>Valid values: true false</p> <p><b>Type:</b> bool  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_post_route_enable</a></p>
<b>cts_post_route_enable_routing_eco</b>	
	<p>If set to false, post-conditioning will skip its ECO-routing step.</p> <p>Valid values: true false</p> <p><b>Type:</b> bool  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_post_route_enable_routing_eco</a></p>
<b>cts_post_route_repair_drv</b>	
	<p>If set to false, post-conditioning will skip its DRV-fixing step.</p> <p>Valid values: true false</p> <p><b>Type:</b> bool  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_post_route_repair_drv</a></p>
<b>cts_post_route_repair_drv_by_buffering</b>	

	<p>If set, post-conditioning will fix DRVs by adding buffers.          Valid values: true false</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_post_route_repair_drv_by_buffering</a></p>
cts_post_route_repair_skew_by_buffering	<p>If set to true, post-conditioning will attempt skew-fixing using rebuffering.          Valid values: true false</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_post_route_repair_skew_by_buffering</a></p>
cts_primary_delay_corner	<p>This specifies the delay corner in which clock tree balancing applies the slew and insertion delay targets. If more than one timing corner is defined, this must be set before running CCOpt. By default, this is set to the first defined delay corner.          Valid values: corner name, or empty</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_primary_delay_corner</a></p>
cts_primary_reporting_skew_groups	<p>The primary skew groups used for reporting.          By default, the value is specified as auto that automatically takes the skew group with maximum number of sinks          as the primary reporting skew group. For invalid values, the default (auto) will be considered.          Valid values: a list of existing skew group names, auto or none</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_primary_reporting_skew_groups</a></p>
cts_primary_reporting_skew_groups_log_min_max_sinks	

	<p>If set to on, the sinks with the shortest and longest paths in each primary reporting skew group will be logged. If set to logv, they will be logged only to the logv file.          Valid values: on, off, logv</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> logv</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_primary_reporting_skew_groups_log_min_max_sinks</a></p>
<b>cts_repair_drv_by_buffering</b>	
	<p>If set, PRO will fix DRVs by adding buffers.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_repair_drv_by_buffering</a></p>
<b>cts_report_skew_groups_only_with_targets</b>	
	<p>The skew groups report (run using the <code>report_skew_groups</code> command) displays insertion delay, skew, and min/max path information for different combinations of skew group, timing corner, and early/late path.</p> <p>Set the <code>cts_report_skew_groups_only_with_targets</code> attribute to false (the default) to report on all skew group/timing corner/path combinations regardless of whether a skew target has been set.</p> <p>Set the <code>cts_report_skew_groups_only_with_targets</code> attribute to true to report only on skew group/timing corner/path combinations where a skew target has been set (either explicitly or using the 'auto' setting).</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_report_skew_groups_only_with_targets</a></p>
<b>cts_route_clock_tree_nets</b>	
	<p>Perform detailed routing, during the final implementation clock routing phase.</p> <p>Valid values: true or false</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_route_clock_tree_nets</a></p>
<b>cts_route_type_leaf</b>	

	<p>Specifies the route type. Setting this attribute binds an existing user-defined route_type to one or more types of clock tree nets. Binding a route_type to a type of clock tree nets means that all nets of that type (including the nets created by CTS) will be routed according to the specification of that route_type.</p> <p>In the most common usage, the route_type is bound to one of the three types of clock tree nets (top, trunk, or leaf) with the optional -net_type argument. Omitting the -net_type argument causes the route_type to be bound to all three types of clock tree nets. The optional -clock_tree &lt;pattern&gt; argument limits the binding to the clock trees whose name matches &lt;pattern&gt;. Omitting the -clock_tree argument causes the binding to apply to all clock trees.</p> <p>For a route_type to be used in CTS, it must be bound to at least one net type. If net type is not bound to any route_type, a default route_type will be created for that net type at the start of CTS.</p> <p>Valid values: names of route_types created with create_route_type</p> <p><b>Type:</b> string <b>Default:</b> default <b>Edit:</b> Yes <b>Reference:</b> <a href="#">cts_route_type_leaf</a></p>
<a href="#">cts_route_type_top</a>	<p>Specifies the route type. Setting this attribute binds an existing user-defined route_type to one or more types of clock tree nets. Binding a route_type to a type of clock tree nets means that all nets of that type (including the nets created by CTS) will be routed according to the specification of that route_type.</p> <p>In the most common usage, the route_type is bound to one of the three types of clock tree nets (top, trunk, or leaf) with the optional -net_type argument. Omitting the -net_type argument causes the route_type to be bound to all three types of clock tree nets. The optional -clock_tree &lt;pattern&gt; argument limits the binding to the clock trees whose name matches &lt;pattern&gt;. Omitting the -clock_tree argument causes the binding to apply to all clock trees.</p> <p>For a route_type to be used in CTS, it must be bound to at least one net type. If net type is not bound to any route_type, a default route_type will be created for that net type at the start of CTS.</p> <p>Valid values: names of route_types created with create_route_type</p> <p><b>Type:</b> string <b>Default:</b> default <b>Edit:</b> Yes <b>Reference:</b> <a href="#">cts_route_type_top</a></p>
<a href="#">cts_route_type_trunk</a>	

	<p>Specifies the route type. Setting this attribute binds an existing user-defined route_type to one or more types of clock tree nets. Binding a route_type to a type of clock tree nets means that all nets of that type (including the nets created by CTS) will be routed according to the specification of that route_type.</p> <p>In the most common usage, the route_type is bound to one of the three types of clock tree nets (top, trunk, or leaf) with the optional -net_type argument. Omitting the -net_type argument causes the route_type to be bound to all three types of clock tree nets. The optional -clock_tree &lt;pattern&gt; argument limits the binding to the clock trees whose name matches &lt;pattern&gt;. Omitting the -clock_tree argument causes the binding to apply to all clock trees.</p> <p>For a route_type to be used in CTS, it must be bound to at least one net type. If net type is not bound to any route_type, a default route_type will be created for that net type at the start of CTS.</p> <p>Valid values: names of route_types created with create_route_type</p> <p><b>Type:</b> string  <b>Default:</b> default  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_route_type_trunk</a></p>
cts_size_clock_gates	<p>When set to true (the default), the CTS algorithm sizes clock gates that appear in the clock tree. 'Logic' does not include clock gates, buffers, and inverters in a clock tree, which are always sized unless they are locked, or clock generators that are above the root of the clock tree. Usually, this affects multiplexers used for selecting one of a number of clocks, or for switching between a test clock and the main clock. Setting this attribute may cause the clock tree to have a lower insertion delay, but might change the cell types of logic gates in the clock tree, which in turn may require them to be moved slightly to find a legal location for the new cell.</p> <p><b>Type:</b> bool  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_size_clock_gates</a></p>
cts_size_clock_sources	<p>When set to true, CTS will try to size the clock source. Only clock sources that are buffers, inverters, logic and clock gating cells with a single output will be sized. The cells available for CTS to size clock sources can be set specified using the attribute 'cts_clock_source_cells'.</p> <p>Valid values: true false</p> <p><b>Type:</b> bool  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_size_clock_sources</a></p>

## cts\_size\_logic

When set to true (the default), the CTS algorithm sizes logic that appears in the clock tree. "Logic" does not include clock gates, buffers, and inverters in a clock tree, which are always sized unless they are locked, or clock generators that are above the root of the clock tree. Usually, this affects multiplexers used for selecting one of a number of clocks, or for switching between a test clock and the main clock. Setting this attribute may cause the clock tree to have a lower insertion delay, but might change the cell types of logic gates in the clock tree, which in turn may require them to be moved slightly to find a legal location for the new cell.

Valid values: true false

**Type:** [bool](#)

**Default:** true

**Edit:** Yes

**Reference:** [cts\\_size\\_logic](#)

## cts\_skew\_group\_report\_columns

A Tcl list of columns to include in skew group reports produced by the skew group report. You can use this attribute to specify the columns you would like to include in the skew group report, and the order in which the columns should appear.

Most of the legal values are straightforward. However, the set of legal values of the following form deserve further explanation:

`summaryType_summaryLocation[_event]`

These values let you report the delay value for other paths that go through the pin.

`summaryType` is one of: max (show the longest delay), min (show the shortest delay), or skew (show the skew, that is the difference between the longest and the shortest delay).

`summaryLocation` is one of: above (show the delay/skew above this pin), below (show the delay/skew below this pin), or through (show the delay/skew for paths through this pin).

`event` is one of: rise (show the delay/skew for the rise event at this pin), fall (show the delay/skew for the fall event at this pin), or both (show the delay/skew for both events at this pin).

Valid values:

capacitance

distance

event

fanout

increment

length

lib\_cell

load\_capacitance

location  
max\_above  
max\_above\_fall  
max\_above\_rise  
max\_below  
max\_below\_fall  
max\_below\_rise  
max\_through  
max\_through\_fall  
max\_through\_rise  
min\_above  
min\_above\_fall  
min\_above\_rise  
min\_below  
min\_below\_fall  
min\_below\_rise  
min\_through  
min\_through\_fall  
min\_through\_rise  
name  
net  
pin  
resistance  
skew\_above  
skew\_above\_fall  
skew\_above\_rise  
skew\_below  
skew\_below\_fall  
skew\_below\_rise  
skew\_through  
skew\_through\_fall  
skew\_through\_rise  
slew  
status  
time  
wire\_capacitance

**Type:** string

**Default:** name lib\_cell event increment time slew capacitance location distance fanout status

**Edit:** Yes

**Reference:** [cts\\_skew\\_group\\_report\\_columns](#)

[cts\\_skew\\_group\\_report\\_histogram\\_bin\\_size](#)

When set to a numeric value, that numeric value will be used as the histogram range size (in library units). For example, if the library time units are set to 1 nanosecond, a value of 0.010 for report\_skew\_groups\_histogram\_bin\_size will result in histogram ranges of 10 picoseconds.

When set to auto, the size of the histogram ranges are dependent on the skew targets that are set. If a skew target is set for a given half corner and skew group combination, then the histogram range size will be 10% of the skew target for that half corner and skew target combination. If no skew target is set for a half corner and skew group combination but a skew target is set for the primary half corner and skew group combination, then the histogram range size will be 10% of the skew target for the primary half corner and skew group combination.

In the event that no skew targets are set and report\_skew\_groups\_histogram\_bin\_size is set to auto, a default value of 10 picoseconds will be used for the histogram range size.

Valid values: auto | string

**Type:** [string](#)

**Default:** auto

**Edit:** Yes

**Reference:** [cts\\_skew\\_group\\_report\\_histogram\\_bin\\_size](#)

cts\_spec\_config\_base\_pin\_trace\_through\_to

Clock tree definition will, by default, not continue through certain types of cell arc (for instance, the clock to Q arc in a DFF). This attribute allows you to override this default behavior, permitting the clock tree to trace through all instances of such a cell.

This attribute serves the same function as `trace_through_to`, except that here the clock path is specified at the level of the library cell.

The attribute should be configured on the input library pin at which the clock will arrive. The value of the attribute specifies the output library pin to which the clock should propagate. The specified output pin must be another pin on the same library cell. The output pin may be specified either by its fully qualified name (i.e. inclusive of the cell name), or else simply by its local (cell-relative) name.

There must be a pre-existing (library-defined) chain of one or more delay arcs that connect the input and output pins together. It is not possible to use `library_trace_through_to` to synthesize delay arcs.

If multiple input pins are annotated on a given library cell, the value of `library_trace_through_to` at each of those pins must select the same output pin: i.e. the configuration must identify a single clock output for the cell. If multiple clock outputs are necessary then `library_trace_through_to` should not be used: instead for each instance of the library cell, define a generated clock tree at each of the clock-carrying outputs.

If the configuration of `library_trace_through_to` settings for a given library cell does not meet these requirements, a warning will be issued and the settings for that cell will be ignored.

All instances of the library cell will be affected by this setting. If both `trace_through_to` and `library_trace_through_to` are applicable at a given instance pin, the `trace_through_to` value will take precedence.

Valid values: `base_pin`

**Type:** `string`

**Default:** `""`

**Edit:** Yes

**Reference:** [cts\\_spec\\_config\\_base\\_pin\\_trace\\_through\\_to](#)

`cts_spec_config_create_clock_tree_source_groups`

	<p>Causes <code>create_clock_tree_spec</code> to set up a clock tree source group for SDC clocks with multiple source pins. If this attribute is set to true, <code>create_clock_tree_spec</code> defines one clock tree for each source pin and then uses the <code>create_clock_tree_source_group</code> command to collect those clock trees together, so that CTS can distribute sinks between the clock trees.</p> <p><b>Type:</b> <code>bool</code>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_spec_config_create_clock_tree_source_groups</a></p>
<b>cts_spec_config_create_generator_skew_groups</b>	
	<p>This attribute will cause the <code>create_clock_tree_spec</code> command to create skew groups for sequential generators and their adjacent registers. Such skew groups will be specified with the same highest rank so that they can be balanced from the other normal skew groups that share some sinks of them. The adjacent registers of a generator are registers that have a datapath timing path to talk with the generator directly. When this attribute is set to true, one skew group will be created per sequential generator instance, master clock and generated clock tree triple. The resulting skew groups will by default be named in the pattern:</p> <pre>_clock_gen_&lt;master_clock_name&gt;_&lt;generator_local_name&gt; &lt;optional_number&gt;/&lt;constraint_mode_name&gt;.</pre> <p>For example, for a pair of generators, with the same local name "reg_clkgen", CCOpt creates generated clock trees from the same master clock named "fclk" in a constraint mode named "func" the skew groups emitted into the clock tree specification file would be named:</p> <pre>_clock_gen_fclk_reg_clkgen_1/func _clock_gen_fclk_reg_clkgen_2/func</pre> <p>The prefix for the names of such skew groups is controlled by the <code>cts_spec_config_create_generator_skew_groups_name_prefix</code> CCOpt attribute and defaults to "<code>_clock_gen</code>" (the start underscore is used to group such skew groups at the end of any skew group listing ordered by name).</p> <p><b>Type:</b> <code>bool</code>  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_spec_config_create_generator_skew_groups</a></p>
<b>cts_spec_config_create_generator_skew_groups_name_prefix</b>	
	<p>This attribute controls the skew group name prefix used for skew groups generated to balance generator flops with their adjacent flops. Default is "<code>_clock_gen</code>". The default has a start underscore at the beginning to cause listings of skew groups ordered by name to collect such skew groups together at the end of a list.</p> <p><b>Type:</b> <code>string</code>  <b>Default:</b> <code>_clock_gen</code>  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_spec_config_create_generator_skew_groups_name_prefix</a></p>

### cts\_target\_max\_capacitance

The target maximum capacitive load to allow during clock tree synthesis. This attribute specifies a maximum (combined pin and wire) capacitance that the clock tree synthesis algorithm will allow any given base\_pin to drive in a given clock tree when driving a given net\_type. It is specified in library units. It currently only constrains the primary delay corner capacitance values - other delay corners can be specified but will not be constrained. This attribute is applied in addition to the max\_capacitance constraints read from the liberty library data - the tightest (lowest) of the constraint specified by this attribute and the constraint present in the liberty data will be used. It also does not apply at the root pins of clock trees - to constrain those nets the cts\_clock\_tree\_source\_max\_capacitance CCOpt attribute should be used instead. Valid values: auto | double

**Type:** string

**Allowed -index values:** delay\_corner

**Default:** top auto trunk auto leaf auto

**Edit:** Yes

**Reference:** [cts\\_target\\_max\\_capacitance](#)

### cts\_target\_max\_capacitance\_leaf

The target maximum capacitive load to allow during clock tree synthesis. This attribute specifies a maximum (combined pin and wire) capacitance that the clock tree synthesis algorithm will allow any given base\_pin to drive in a given clock tree when driving a given net\_type. It is specified in library units. It currently only constrains the primary delay corner capacitance values - other delay corners can be specified but will not be constrained. This attribute is applied in addition to the max\_capacitance constraints read from the liberty library data - the tightest (lowest) of the constraint specified by this attribute and the constraint present in the liberty data will be used. It also does not apply at the root pins of clock trees - to constrain those nets the cts\_clock\_tree\_source\_max\_capacitance CCOpt attribute should be used instead. Valid values: auto | double

**Type:** string

**Allowed -index values:** delay\_corner

**Default:** auto

**Edit:** Yes

**Reference:** [cts\\_target\\_max\\_capacitance\\_leaf](#)

### cts\_target\_max\_capacitance\_top

The target maximum capacitive load to allow during clock tree synthesis. This attribute specifies a maximum (combined pin and wire) capacitance that the clock tree synthesis algorithm will allow any given base\_pin to drive in a given clock tree when driving a given net\_type. It is specified in library units. It currently only constrains the primary delay corner capacitance values - other delay corners can be specified but will not be constrained. This attribute is applied in addition to the max\_capacitance constraints read from the liberty library data - the tightest (lowest) of the constraint specified by this attribute and the constraint present in the liberty data will be used. It also does not apply at the root pins of clock trees - to constrain those nets the cts\_clock\_tree\_source\_max\_capacitance CCOpt attribute should be used instead. Valid values: auto | double

**Type:** [string](#)

**Allowed -index values:** delay\_corner

**Default:** auto

**Edit:** Yes

**Reference:** [cts\\_target\\_max\\_capacitance\\_top](#)

#### cts\_target\_max\_capacitance\_trunk

The target maximum capacitive load to allow during clock tree synthesis. This attribute specifies a maximum (combined pin and wire) capacitance that the clock tree synthesis algorithm will allow any given base\_pin to drive in a given clock tree when driving a given net\_type. It is specified in library units. It currently only constrains the primary delay corner capacitance values - other delay corners can be specified but will not be constrained. This attribute is applied in addition to the max\_capacitance constraints read from the liberty library data - the tightest (lowest) of the constraint specified by this attribute and the constraint present in the liberty data will be used. It also does not apply at the root pins of clock trees - to constrain those nets the cts\_clock\_tree\_source\_max\_capacitance CCOpt attribute should be used instead. Valid values: auto | double

**Type:** [string](#)

**Allowed -index values:** delay\_corner

**Default:** auto

**Edit:** Yes

**Reference:** [cts\\_target\\_max\\_capacitance\\_trunk](#)

#### cts\_target\_max\_transition\_time

	<p>The target slew used for clock tree synthesis. This attribute specifies a maximum slew time that the clock tree synthesis algorithm will allow in this clock tree, in library units. 'default' means 'auto' in primary half corner and 'ignore' in other half corners. If set to 'auto', CTS picks an appropriate value based on the collection of allowed buffer sizes and library parameters, although this may not give optimal quality of results. If set to 'ignore', CTS does not constrain the corner.</p> <p>Valid values: default   auto   ignore   double</p> <p><b>Type:</b> string</p> <p><b>Allowed -index values:</b> delay_corner power_domain</p> <p><b>Default:</b> top default trunk default leaf default</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_target_max_transition_time</a></p>
<p><a href="#">cts_target_max_transition_time_leaf</a></p>	
	<p>The target slew used for clock tree synthesis. This attribute specifies a maximum slew time that the clock tree synthesis algorithm will allow in this clock tree, in library units. 'default' means 'auto' in primary half corner and 'ignore' in other half corners. If set to 'auto', CTS picks an appropriate value based on the collection of allowed buffer sizes and library parameters, although this may not give optimal quality of results. If set to 'ignore', CTS does not constrain the corner.</p> <p>Valid values: default   auto   ignore   double</p> <p><b>Type:</b> string</p> <p><b>Allowed -index values:</b> delay_corner power_domain</p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_target_max_transition_time_leaf</a></p>
<p><a href="#">cts_target_max_transition_time_top</a></p>	

	<p>The target slew used for clock tree synthesis. This attribute specifies a maximum slew time that the clock tree synthesis algorithm will allow in this clock tree, in library units. 'default' means 'auto' in primary half corner and 'ignore' in other half corners. If set to 'auto', CTS picks an appropriate value based on the collection of allowed buffer sizes and library parameters, although this may not give optimal quality of results. If set to 'ignore', CTS does not constrain the corner.</p> <p>Valid values: default   auto   ignore   double</p> <p><b>Type:</b> string</p> <p><b>Allowed -index values:</b> delay_corner power_domain</p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_target_max_transition_time_top</a></p>
	<p><b>cts_target_max_transition_time_trunk</b></p> <p>The target slew used for clock tree synthesis. This attribute specifies a maximum slew time that the clock tree synthesis algorithm will allow in this clock tree, in library units. 'default' means 'auto' in primary half corner and 'ignore' in other half corners. If set to 'auto', CTS picks an appropriate value based on the collection of allowed buffer sizes and library parameters, although this may not give optimal quality of results. If set to 'ignore', CTS does not constrain the corner.</p> <p>Valid values: default   auto   ignore   double</p> <p><b>Type:</b> string</p> <p><b>Allowed -index values:</b> delay_corner power_domain</p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_target_max_transition_time_trunk</a></p>
	<p><b>cts_target_skew</b></p>

	<p>This specifies the target skew for clock tree balancing. This may be set to a numeric value, or one of 'auto', 'ignore' or 'default'. If set to 'auto' this indicates that an appropriate skew target should be computed. If set to 'ignore' this indicates that skew should not be balanced for this corner/path combination. If unspecified then the value of this attribute is 'default'. If the value of the attribute is 'default' the target skew for late delays in the primary delay corner is interpreted as 'auto' and as 'ignore' otherwise. Valid values: default   auto   ignore   double</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> delay_corner</p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_target_skew</a></p>
<b>cts_top_fanout_threshold</b>	
	<p>Minimum number of transitive fanout in the clock tree for a net to be routed as a top net. Nets with at least this many sinks in their transitive fanout in the clock tree will have the special routing rules applied to them. Valid values: integer</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> unset</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_top_fanout_threshold</a></p>
<b>cts_update_clock_latency</b>	
	<p>Determine whether to update IO latencies within ccopt_design. Valid values: true false</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">cts_update_clock_latency</a></p>
<b>cts_use_inverters</b>	

	<p>Specifies whether clock tree synthesis should prefer to use inverters rather than buffers when balancing the clock tree. If set to true, CTS will use inverters for the clock tree balancing process. If set to false, CTS will use the minimum number of levels of inverters required to maintain logical correctness. If set to auto (the default) CTS will use what it considers to be the best combination of buffers and inverters to get optimal quality of results.</p> <p>Valid values: auto true false</p> <p><b>Type:</b> string  <b>Default:</b> auto  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_use_inverters</a></p>
<b>cts_use_receiver_model_capacitance_for_drv</b>	
	<p>If true, CCOpt will use receiver model capacitance for drv.</p> <p><b>Type:</b> bool  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">cts_use_receiver_model_capacitance_for_drv</a></p>
<b>current_design</b>	
	<p>current design</p> <p><b>Type:</b> obj.design  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>dataflow_hinsts</b>	
	<p>specify hinst to be placed</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
<b>delay_corners</b>	
	<p>Returns the information about the delay corners in the design.</p> <p><b>Type:</b> obj(delay_corner)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>delaycal_accuracy_level</b>	

	set accuracy level for delay calculation <b>Type:</b> int <b>Default:</b> 0 <b>Edit:</b> Yes
<b>delaycal_advanced_node_pin_cap_settings</b>	
	Enable advanced node pin cap settings. <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">delaycal_advanced_node_pin_cap_settings</a>
<b>delaycal_advanced_pin_cap_mode</b>	
	Enable advanced receiver pin cap mode for base delay. <b>Type:</b> enum <b>Enum Values:</b> 0 1 2 <b>Default:</b> 0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">delaycal_advanced_pin_cap_mode</a>
<b>delaycal_combine_mmmc</b>	
	Specifies whether delay calculation runs are to be combined for delay calculation simulations <b>Type:</b> enum <b>Enum Values:</b> none early_late early_late_corner <b>Default:</b> early_late_corner <b>Edit:</b> Yes <b>Reference:</b> <a href="#">delaycal_combine_mmmc</a>
<b>delaycal_default_net_delay</b>	
	set default net delay. <b>Type:</b> string <b>Default:</b> 1000ps <b>Edit:</b> Yes <b>Reference:</b> <a href="#">delaycal_default_net_delay</a>
<b>delaycal_default_net_load</b>	
	set default net load. <b>Type:</b> string <b>Default:</b> 0.5pf <b>Edit:</b> Yes <b>Reference:</b> <a href="#">delaycal_default_net_load</a>

delaycal_degrade_slew_on_early_nets	Controls interconnect slew degradation for early paths. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">delaycal_degrade_slew_on_early_nets</a>
delaycal_early_irdrop_data_type	IRDrop EIV DB EivMethod for early corner <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> best_average worst best average worst_average <b>Default:</b> worst <b>Edit:</b> Yes <b>Reference:</b> <a href="#">delaycal_early_irdrop_data_type</a>
delaycal_enable_high_fanout	Enables the default net delay which will be annotated on high fanout nets <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">delaycal_enable_high_fanout</a>
delaycal_enable_quiet_receivers_for_hold	<b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">delaycal_enable_quiet_receivers_for_hold</a>
delaycal_enable_si	Enables SIAware delay calculation that also includes cross-talk induced delays. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> true false <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">delaycal_enable_si</a>
delaycal_enable_wire_load_model	

	<p>Enables support of Liberty wire-load models and related SDC commands.</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">delaycal_enable_wire_load_model</a></p>
<b>delaycal_equivalent_waveform_model</b>	
	<p>Controls the equivalent waveform model to be used</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> none no_propagation propagation</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">delaycal_equivalent_waveform_model</a></p>
<b>delaycal_equivalent_waveform_model_for_timing_check</b>	
	<p>Enable EWM for timing check delay.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>delaycal_equivalent_waveform_type</b>	
	<p>Equivalent waveform model type to be used</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> moments simulation</p> <p><b>Default:</b> moments</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">delaycal_equivalent_waveform_type</a></p>
<b>delaycal_honor_slew_propagate_constraint</b>	
	<p>Determines whether to propagate the slew from the disabled timing arcs to the output pin.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">delaycal_honor_slew_propagate_constraint</a></p>
<b>delaycal_ignore_net_load</b>	
	<p>Uses zero-cap, zero-resistance wire-load model for estimating delays.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">delaycal_ignore_net_load</a></p>
<b>delaycal_input_transition_delay</b>	

	set default input transition time. <b>Type:</b> <a href="#">string</a> <b>Default:</b> 0ps <b>Edit:</b> Yes <b>Reference:</b> <a href="#">delaycal_input_transition_delay</a>
<b>delaycal_irdrop_data_type</b>	
	IRDrop EIV DB EivMethod <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> best_average worst best average worst_average <b>Default:</b> worst <b>Edit:</b> Yes <b>Reference:</b> <a href="#">delaycal_irdrop_data_type</a>
<b>delaycal_irdrop_window_based</b>	
	Fetch window based EIV values from EIV DB <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> none late early both <b>Default:</b> both <b>Edit:</b> Yes <b>Reference:</b> <a href="#">delaycal_irdrop_window_based</a>
<b>delaycal_late_irdrop_data_type</b>	
	IRDrop EIV DB EivMethod for late corner <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> best_average worst best average worst_average <b>Default:</b> worst <b>Edit:</b> Yes <b>Reference:</b> <a href="#">delaycal_late_irdrop_data_type</a>
<b>delaycal_report_out_bound</b>	
	Generates a report that contains a list of index values (input transition) in the delay tables that are beyond the index range. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">delaycal_report_out_bound</a>
<b>delaycal_signoff_alignment_settings</b>	

	<p>Turn on/off signoff alignment settings</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>delaycal_slew_out_bound_limit_high</b>	
	<p>Limits the maximum slew used in the analysis to the specified value.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 3.40282e+38</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">delaycal_slew_out_bound_limit_high</a></p>
<b>delaycal_slew_out_bound_limit_low</b>	
	<p>Limits the minimum slew used in the analysis to the specified value.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.5</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">delaycal_slew_out_bound_limit_low</a></p>
<b>delaycal_socv_accuracy_mode</b>	
	<p>level-based-accuracy-effort in AAE for delays and slews</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> low medium high ultra</p> <p><b>Default:</b> low</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">delaycal_socv_accuracy_mode</a></p>
<b>delaycal_socv_lvf_mode</b>	
	<p>Controls interpretation of LVF data.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> moments early_late</p> <p><b>Default:</b> early_late</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">delaycal_socv_lvf_mode</a></p>
<b>delaycal_socv_machine_learning_level</b>	
	<p>Enable socv machine learning mode</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
<b>delaycal_socv_use_lvf_tables</b>	

	<p>Controls which type of variations are considered during analysis.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> all</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">delaycal_socv_use_lvf_tables</a></p>
delaycal_support_output_pin_cap	<p>useOutputPinCap</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">delaycal_support_output_pin_cap</a></p>
delaycal_support_wire_load_model	<p>Enables support of Liberty wire-load models and related SDC commands.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">delaycal_support_wire_load_model</a></p>
delaycal_timing_create_clock_use_ideal_slew	<p>When set to true, the software detects created clocks and uses zero input slew. Other slew values, including those set using set_annotation_transition command, will be ignored. When set to false, the software honors set_annotation_transition command settings. By default, this global variable is set to false.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">delaycal_timing_create_clock_use_ideal_slew</a></p>
delaycal_use_default_delay_limit	<p>set threshold to apply the default delay</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1000</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">delaycal_use_default_delay_limit</a></p>
design_bottom_routing_layer	

	<p>specify the lowest lef layer name for global and detail routing</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">design_bottom_routing_layer</a></p>
design_cong_effort	<p>Specify congestion effort level</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> low medium high auto</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">design_cong_effort</a></p>
design_dual_rail_via_pitch	<p>Min stacked-via pitch for dual std-cell power-rails on first and third routing layers. Space separated min stacked-via pitch for dual std-cell power-rails on first and third routing layers.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">design_dual_rail_via_pitch</a></p>
design_early_clock_flow	<p>Enable early clock flow</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">design_early_clock_flow</a></p>
design_express_route	<p>With "-flow_effort express", should routing-stage be forced.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">design_express_route</a></p>
design_flow_effort	

	<p>Specify flow effort level <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> express standard extreme <b>Default:</b> standard <b>Edit:</b> Yes <b>Reference:</b> <a href="#">design_flow_effort</a></p>
	<p>design_ignore_followpin_vias</p>
	<p>if true, ignore followpin vias during detailed placement, optimization and routing. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">design_ignore_followpin_vias</a></p>
	<p>design_pessimistic_mode</p>
	<p>Enable pessimistic mode <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> true false <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">design_pessimistic_mode</a></p>
	<p>design_power_effort</p>
	<p>Specify power effort level <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> none low high <b>Default:</b> none <b>Edit:</b> Yes <b>Reference:</b> <a href="#">design_power_effort</a></p>
	<p>design_process_node</p>
	<p>Process technology <b>Type:</b> <a href="#">int</a> <b>Default:</b> 90 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">design_process_node</a></p>
	<p>design_slack_weighting_method</p>

	<p>Specify slack weighting to be used in implementation flow</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> unity_weighting view_based_weighting</p> <p><b>Default:</b> unity_weighting</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">design_slack_weighting_method</a></p>
design_tech_node	<p>set design tech node</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> N12 N10 N7 N7Plus N6 N5 N3 S11 S10 S8 S7 S5 S4 S3 G7 G5 ICF I7 C12 C7 unspecified</p> <p><b>Default:</b> unspecified</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">design_tech_node</a></p>
design_top_routing_layer	<p>specify the highest lef layer name for global and detail routing</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">design_top_routing_layer</a></p>
design_trim_grid_group	<p>Specifies the GROUP name of which set of trim metal grid to be used for placement and routing. See the LEF documentation on the TRIMMETALTRACK keyword for more details.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">design_trim_grid_group</a></p>
designs	<p>All the designs</p> <p><b>Type:</b> <a href="#">obj(design)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
distributed_mmmc_disable_reports_auto_redirection	

	<p>setting 'true' will preserve path specified in report command. User need to specify unique path for each view to avoid all clients writing to same report file. With default setting (false), distributed mmmc run automatically updates report paths to a view unique directory structure.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">distributed_mmmc_disable_reports_auto_redirection</a></p>
eco_batch_mode	<p>Enter/Exit batch mode</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">eco_batch_mode</a></p>
eco_check_logical_equivalence	<p>Do logical-equivalence checking</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">eco_check_logical_equivalence</a></p>
eco_disable_change_net_name_for_flat_netlist	<p>Specifies whether nets would be renamed in eco report of eco_compare_netlist for flat netlist.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">eco_disable_change_net_name_for_flat_netlist</a></p>
eco_disable_constraints_loading_from_clients	<p>Disable Loading Constraints from Clients</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
eco_disable_derates_loading_from_clients	<p>Disable Loading Derates from Clients</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
eco_disable_parasitic_loading_from_clients	

	<p>Disable Loading Parasitics from Clients</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<p><a href="#">eco_disable_power_format_loading_from_clients</a></p>	
	<p>Disable Loading Power Format from Clients</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<p><a href="#">eco_honor_dont_touch</a></p>	
	<p>Check dont_touch on instances, cells and nets</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">eco_honor_dont_touch</a></p>
<p><a href="#">eco_honor_dont_use</a></p>	
	<p>Skip library cells marked dont_use</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">eco_honor_dont_use</a></p>
<p><a href="#">eco_honor_fixed_status</a></p>	
	<p>Honor fixed (placement) instances</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">eco_honor_fixed_status</a></p>
<p><a href="#">eco_honor_fixed_wires</a></p>	
	<p>Honor fixed wires of nets</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">eco_honor_fixed_wires</a></p>
<p><a href="#">eco_honor_power_intent</a></p>	

	<p>Perform MSV checks during ECO: Do not allow resize of regular cell with always-on cell (and vice-versa), do not change cells belonging to different power domains, do not allow adding buffer to a power domain it doesn't belong to, do not buffer a cross power domain net, do not allow deletion of an always-on buffer, a level-shifter, or a buffer which will cause redundant isolation cell.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">eco_honor_power_intent</a></p>
<b>eco_inherit_net_attribute</b>	
	<p>New net inherits attributes of buffered net</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">eco_inherit_net_attribute</a></p>
<b>eco_prefix</b>	
	<p>Prefix name to be used by ECO commands</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ECO</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">eco_prefix</a></p>
<b>eco_refine_place</b>	
	<p>Refine placement after ECO</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">eco_refine_place</a></p>
<b>eco_spread_inverter</b>	
	<p>Spread inverters on buffered net</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">eco_spread_inverter</a></p>
<b>eco_update_timing</b>	

	Update timing results after ECO <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">eco_update_timing</a>
<b>edit_wire_align</b>	
	Specifies whether to support align objects. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes
<b>edit_wire_allow_45_degree</b>	
	Specifies whether to allow creation of a 45-degree wire. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">edit_wire_allow_45_degree</a>
<b>edit_wire_arrow_incremental</b>	
	Specifies the step increments in microns to move wires with the arrow keys. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 1.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">edit_wire_arrow_incremental</a>
<b>edit_wire_assign_multi_pattern_color</b>	
	Specifies how to assign the mask color on the DPT layer of the wire segment to be created. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> auto mask1 mask2 mask3 <b>Default:</b> auto <b>Edit:</b> Yes <b>Reference:</b> <a href="#">edit_wire_assign_multi_pattern_color</a>
<b>edit_wire_auto_split_bus</b>	
	Splits buses automatically to avoid DRC violations. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">edit_wire_auto_split_bus</a>
<b>edit_wire_bus_honor_start_parameters</b>	

	<p>Specifies that the wire width and spacing of the start points (pins) should be honored when drawing routes for a bus.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_bus_honor_start_parameters</a></p>
	<p><b>edit_wire_bus_honor_width_setting</b></p>
	<p>Specifies whether the tool should adjust the wire width when snapping bus wires to pin.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_bus_honor_width_setting</a></p>
	<p><b>edit_wire_change_order_at_turn</b></p>
	<p>Specifies whether the order of the wires changes or stays the same when the wire makes a 90-degree turn. (Reverse Order   Keep Order)</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> keep_order</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_change_order_at_turn</a></p>
	<p><b>edit_wire_check_design_boundary</b></p>
	<p>Specifies whether stop user to stretch the wire in the forbidden area which defined by edit_wire_pull_back_distance.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_check_design_boundary</a></p>
	<p><b>edit_wire_close_polygons</b></p>
	<p>Specifies whether to close a special route structure toward itself.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_close_polygons</a></p>
	<p><b>edit_wire_color_align_with_track</b></p>

	<p>Specifies whether the wire color is to be changed to match the track color during a move or copy operation.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_color_align_with_track</a></p>
edit_wire_connect_pin	<p>Specifies whether or not generate a via on the pin for specified pin type.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> in out inout nodir</p> <p><b>Default:</b> in out inout nodir</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_connect_pin</a></p>
edit_wire_connect_with_specified_layer	<p>Specifies whether or not the layer of connecting wires should be changed as per the edit_wire_layer_horizontal or edit_wire_layer_vertical setting when moving wires.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_connect_with_specified_layer</a></p>
edit_wire_create_crossover_vias	<p>Specifies whether the software creates a via when you draw a wire that crosses a wire or pin of the same net that is on a different layer.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_create_crossover_vias</a></p>
edit_wire_create_is_edit_flag	<p>Specifies whether to create is_edit flag for wire edit</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_create_is_edit_flag</a></p>
edit_wire_create_via_on_pin	

	<p>Specifies whether the software creates vias at pins.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_create_via_on_pin</a></p>
edit_wire_cut_class	<p>Specifies the cut class name of the generated via when editing wires.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_cut_class</a></p>
edit_wire_cut_wire_overlap	<p>Specifies whether or not overlaps are created while cutting specified type of wires.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> regular special</p> <p><b>Default:</b> regular</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_cut_wire_overlap</a></p>
edit_wire_debug_file	<p>Specifies the report file name.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
edit_wire_delete_pin_with_wire	<p>Delete Pin with Wire</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_delete_pin_with_wire</a></p>
edit_wire_delete_wire_via_through_layers	<p>Delete Wire Via in deep through mode</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_delete_wire_via_through_layers</a></p>
edit_wire_display_wire_length_with_cursor	

	<p>Specifies whether display the total/current wire length with mouse when editing wires.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_display_wire_length_with_cursor</a></p>
edit_wire_draw_shield	<p>Specifies whether draw a shield net only.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_draw_shield</a></p>
edit_wire_drawing_wire	<p>Specifies which of the nets used with the -nets parameter corresponding to the mouse pointer location when adding an array of wires.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_drawing_wire</a></p>
edit_wire_drc_on	<p>Specifies whether to check DRC rules during wire editing.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_drc_on</a></p>
edit_wire_drc_use_non_default_spacing	<p>Specifies whether non-default spacing defined in the Non-Default Rule of the editing net should be used for spacing check during wire editing.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_drc_use_non_default_spacing</a></p>
edit_wire_extend_wires	

	<p>Specifies whether, after completing a signal or power route, the specified boundary of wire segment extends and connects to the first logical target</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> start end start_cell_boundary end_cell_boundary</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_extend_wires</a></p>
<b>edit_wire_final_check_with_verify</b>	
	<p>Specifies whether to do final check with verify</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_final_check_with_verify</a></p>
<b>edit_wire_ignore_drc</b>	
	<p>Specifies which violation type should be ignored during wire editing.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> conn_antenna max_via_stack min_cut min_enclosed_area min_step protrusion</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_ignore_drc</a></p>
<b>edit_wire_jog_connect_layer</b>	
	<p>Specifies the number of layers for connecting wires above the layers for moving wires. If set the parameter of 'set_db edit_wire_jog_connect_layer' to 1, disable this option.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_jog_connect_layer</a></p>
<b>edit_wire_keep_status</b>	
	<p>Specifies whether to keep object status during editing.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_keep_status</a></p>
<b>edit_wire_keep_via</b>	

	<p>Specifies whether keep original via in wire move or change width.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_keep_via</a></p>
<p><b>edit_wire_lateral_movement_range</b></p>	
	<p>Specified the max lateral movement distance to avoid DRC when add a wire.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_lateral_movement_range</a></p>
<p><b>edit_wire_layer</b></p>	
	<p>Specifies the layer for patch wires or polygon wires.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> M1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_layer</a></p>
<p><b>edit_wire_layer_horizontal</b></p>	
	<p>Specifies the layer for horizontal wires.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> M1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_layer_horizontal</a></p>
<p><b>edit_wire_layer_max</b></p>	
	<p>Specifies the maximum layer for routing.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> UNINITIALIZED</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_layer_max</a></p>
<p><b>edit_wire_layer_min</b></p>	
	<p>Specifies the minimum layer for routing.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> UNINITIALIZED</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_layer_min</a></p>
<p><b>edit_wire_layer_vertical</b></p>	

	<p>Specifies the layer for vertical wires.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> M2</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_layer_vertical</a></p>
<p><b>edit_wire_look_down_layers</b></p>	
	<p>Specifies the number of layers below the current layer that added wires will connect to with a via.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 100</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_look_down_layers</a></p>
<p><b>edit_wire_look_up_layers</b></p>	
	<p>Specifies the number of layers above the current layer that added wires will connect to with a via.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 100</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_look_up_layers</a></p>
<p><b>edit_wire_max_pointer_number</b></p>	
	<p>Specifies the maximum number of pointers to be returned by wire edit commands.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 100</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_max_pointer_number</a></p>
<p><b>edit_wire_nets</b></p>	
	<p>Specifies one or more nets for editing.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_nets</a></p>
<p><b>edit_wire_no_merge_special_wire</b></p>	

	<p>Specifies whether automatically merge the added special wires with any existing special wires.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_no_merge_special_wire</a></p>
edit_wire_only_show_edit_layer	<p>Turn on this option, when user editing any wires/vias, only show the layer from edit objects, and dim other objects.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_only_show_edit_layer</a></p>
edit_wire_orthogonal_connection_only	<p>Specifies whether to consider wires and pins that are in the same direction as a target for connection. Only special wire is supported.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_orthogonal_connection_only</a></p>
edit_wire_outer_shield_spacing	<p>Specifies a spacing value in microns to be used by the edit_wire_shield_low and edit_wire_shield_high parameters.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_outer_shield_spacing</a></p>
edit_wire_outer_shield_width	<p>Specifies a width value in microns to be used for outer shield(s) depending on the values of edit_wire_shield_low or edit_wire_shield_high parameters.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_outer_shield_width</a></p>
edit_wire_override	

	<p>Specifies whether to use the override specification.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_override</a></p>
	<p><b>edit_wire_partial_overlap_threshold</b></p>
	<p>Specifies ratio threshold of special via creation on partial overlap wires.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_partial_overlap_threshold</a></p>
	<p><b>edit_wire_pull_back_distance</b></p>
	<p>Specify the value for forbidden distance. Default is Auto, it means use the largest min spacing of the layer.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_pull_back_distance</a></p>
	<p><b>edit_wire_reshape</b></p>
	<p>Specifies that when you add new wires, existing redundant wires within the route are automatically removed.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_reshape</a></p>
	<p><b>edit_wire_return_obj_pointer</b></p>
	<p>Specifies whether return pointers after wire edit operations.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_return_obj_pointer</a></p>
	<p><b>edit_wire_rule</b></p>
	<p>Uses the specified LEF rule for regular wires.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_rule</a></p>

edit_wire_search_route_rule_vias_only	
	<p>Specifies that when the Shift + N/P bindkey is used, the tool should circle through NDR vias only.</p> <p><b>Type:</b> bool  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">edit_wire_search_route_rule_vias_only</a></p>
edit_wire_shape	
	<p>Specifies the shape associated with the wire you draw.</p> <p><b>Type:</b> enum  <b>Enum Values:</b> ring stripe followpin iowire corewire blockwire padring blockring fillwire fillwireopc drcfill none  <b>Default:</b> stripe  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">edit_wire_shape</a></p>
edit_wire_shield	
	<p>Specifies whether to add a minimum width shield wire for specified side.</p> <p><b>Type:</b> enum  <b>Enum Values:</b> high low adjacent  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">edit_wire_shield</a></p>
edit_wire_shield_look_down_layers	
	<p>Specifies the number of layers below the current layer that an added shield wire can connect using a via.</p> <p><b>Type:</b> int  <b>Default:</b> 100  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">edit_wire_shield_look_down_layers</a></p>
edit_wire_shield_look_up_layers	
	<p>Specifies the number of layers above the current layer that an added shield wire can connect using a via.</p> <p><b>Type:</b> int  <b>Default:</b> 100  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">edit_wire_shield_look_up_layers</a></p>
edit_wire_shield_shape	

	<p>Specifies the shape associated with the shield wire you draw.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> ring stripe followpin iowire corewire blockwire padring blockring fillwire drcfill none</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_shield_shape</a></p>
<b>edit_wire_shielding_nets</b>	
	<p>Specifies net names for shield wires, usually power or ground names.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_shielding_nets</a></p>
<b>edit_wire_show_drc_info_for_edit_shape</b>	
	<p>Turn on this option, when user editing any wires/vias and generate a violation, tool can display the detail information nearby marker.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_show_drc_info_for_edit_shape</a></p>
<b>edit_wire_sibling_look_down_layers</b>	
	<p>Specifies the number of layers below the sibling layers that an added shield wire can connect using a via.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_sibling_look_down_layers</a></p>
<b>edit_wire_sibling_look_up_layers</b>	
	<p>Specifies the number of layers above the sibling layers that an added shield wire can connect using a via.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_sibling_look_up_layers</a></p>
<b>edit_wire_snap</b>	

	<p>Specifies whether to enable wire and via snap.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_snap</a></p>
<b>edit_wire_snap_align_to</b>	
	<p>Specifies how to align with a pin when ending a route.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> center low high auto</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_snap_align_to</a></p>
<b>edit_wire_snap_bus_to_pin</b>	
	<p>Specifies whether to change wire width, spacing and order according to the connected pin</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_snap_bus_to_pin</a></p>
<b>edit_wire_snap_end_to</b>	
	<p>Specifies whether to snap the end of wire to specified objects.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> track_regular track_special manufacturing_grid</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_snap_end_to</a></p>
<b>edit_wire_snap_objects_to_track</b>	
	<p>Specifies whether to snap added or moved specified wires to the closest routing track in the preferred direction for the layer automatically.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> special regular patch pin</p> <p><b>Default:</b> regular patch</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_snap_objects_to_track</a></p>
<b>edit_wire_snap_to</b>	

	<p>Specifies whether to snap added or moved wires to specified objects.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> special pg pin row</p> <p><b>Default:</b> special pg pin</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_snap_to</a></p>
edit_wire_snap_to_track_honor_color	<p>Specifies whether to snap wires to a track with the same color automatically.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_snap_to_track_honor_color</a></p>
edit_wire_snap_trim_metal_to_trim_grid	<p>Specify whether snap the trim metal to the closest trim grid during trim metal editing.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_snap_trim_metal_to_trim_grid</a></p>
edit_wire_spacing	<p>Specifies the distance between wires.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_spacing</a></p>
edit_wire_spacing_horizontal	<p>Specifies the distance between horizontal wires.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_spacing_horizontal</a></p>
edit_wire_spacing_vertical	<p>Specifies the distance between vertical wires.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_spacing_vertical</a></p>
edit_wire_status	

	<p>Specifies the status associated with the wire you draw.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> cover fixed noshield routed shield auto</p> <p><b>Default:</b> fixed</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_status</a></p>
edit_wire_stop_at_drc	<p>Specifies whether the software can cause a DRC violation by moving or stretching a wire.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_stop_at_drc</a></p>
edit_wire_stretch_end	<p>Specifies the direction in which to stretch or reduce wires.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> high low</p> <p><b>Default:</b> high</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_stretch_end</a></p>
edit_wire_stretch_with_intersection	<p>Enables wires with intersects to be stretched easily.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_stretch_with_intersection</a></p>
edit_wire_sub_class	<p>Specifies the subclass name of wires and vias.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_sub_class</a></p>
edit_wire_turn_at	

	<p>Specifies the start location of new wire when do turn.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> center_line wire_edge</p> <p><b>Default:</b> center_line</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_turn_at</a></p>
edit_wire_type	<p>Specifies the type of creating wire.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> regular special patch</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_type</a></p>
edit_wire_unrestricted_regular_wire_width	<p>Specifies whether the regular wire width is unrestricted when changing width.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_unrestricted_regular_wire_width</a></p>
edit_wire_update_shield_net	<p>Specifies whether automatically update shield net attribute on the signal net.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_update_shield_net</a></p>
edit_wire_use_fix_via	<p>Specifies whether to use fix_via for special via with minStep DRC violation.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_use_fix_via</a></p>
edit_wire_use_interleaving_wire_group	<p>Alternates the specified wires in the wire group.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_use_interleaving_wire_group</a></p>

edit_wire_use_wire_group	<p>Groups multiple wires from the same net.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_use_wire_group</a></p>
edit_wire_use_wire_group_bits	<p>Specifies the number of times to replicate a wire in the wire group.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_use_wire_group_bits</a></p>
edit_wire_use_wire_group_reinforcement	<p>Creates slots in the wire group by creating wires that connect the wires in the wire group, but are orthogonal to them.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_use_wire_group_reinforcement</a></p>
edit_wire_use_wire_group_reinforcement_group_via	<p>Specifies that the wire group uses group vias.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_use_wire_group_reinforcement_group_via</a></p>
edit_wire_use_wire_group_reinforcement_spacing	<p>Specifies the spacing for the orthogonal wires in the wire groups.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_use_wire_group_reinforcement_spacing</a></p>
edit_wire_use_wire_group_reinforcement_width	<p>Specifies the width of the orthogonal wires in the wire groups.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_use_wire_group_reinforcement_width</a></p>

edit_wire_verbose	<p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
edit_wire_via_allow_geometry_drc	<p>Check Geometry DRC</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_via_allow_geometry_drc</a></p>
edit_wire_via_auto_snap	<p>Controls whether to snap vias to the intersection of wires on the same net or to the manufacturing grid.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_via_auto_snap</a></p>
edit_wire_via_auto_update	<p>Controls whether to replace existing vias.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_via_auto_update</a></p>
edit_wire_via_cell_name	<p>Specifies the name of the via cell from the LEF or DEF file.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_via_cell_name</a></p>
edit_wire_via_columns	<p>Specify the rows of via cut.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_via_columns</a></p>

edit_wire_via_create_by	Controls whether to create vias based on the edit_wire_via_cell_name parameter or to create vias based on the other parameters. <b>Type:</b> enum <b>Enum Values:</b> viacell parameters <b>Default:</b> parameters <b>Edit:</b> Yes <b>Reference:</b> <a href="#">edit_wire_via_create_by</a>
edit_wire_via_cut_layer	Specifies the via layer name for the via to created or modify. <b>Type:</b> string <b>Default:</b> V12 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">edit_wire_via_cut_layer</a>
edit_wire_via_exclude_spec	Specifies the vias to be ignored by wire editor. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">edit_wire_via_exclude_spec</a>
edit_wire_via_override_spec	Specifies the default vias to be used by wire editor. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">edit_wire_via_override_spec</a>
edit_wire_via_rows	Specify the columns of via cut. <b>Type:</b> int <b>Default:</b> 0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">edit_wire_via_rows</a>
edit_wire_via_scale_height	

	<p>Specify the via height scale.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 100</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_via_scale_height</a></p>
edit_wire_via_scale_width	
	<p>Specify the via width scale.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 100</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_via_scale_width</a></p>
edit_wire_via_snap_honor_color	
	<p>Specifies whether to snap the same mask automatically</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_via_snap_honor_color</a></p>
edit_wire_via_snap_to_intersection	
	<p>Specifies whether to snap vias to the intersection of wires</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_via_snap_to_intersection</a></p>
edit_wire_via_type	
	<p>Specifies the type of creating via.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> auto regular special</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_via_type</a></p>
edit_wire_width	
	<p>Specifies the width of patch wires.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_width</a></p>
edit_wire_width_horizontal	

	<p>Specifies the width for horizontal wires.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_width_horizontal</a></p>
<b>edit_wire_width_vertical</b>	
	<p>Specifies the width of vertical wires.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_width_vertical</a></p>
<b>edit_wire_wire_override_spec</b>	
	<p>Contains the details of the override specification.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">edit_wire_wire_override_spec</a></p>
<b>eeq_variant_site_start</b>	
	<p>Site variant_id of the first site on rows in core area. This is specified in library LEF58_CELLVARIANTS property by value of STARTVARIANT in 'CELLVARIANTS totalNum [STARTVARIANT num] YFLIPMAP {flippedVariantNum siteVariantNum} ...'</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p>
<b>enable_distributed_flow</b>	
	<p>Enables the distributed flow, and changes '::Rda_Distributed::useModel' to 0</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
<b>exclusive_group_min_gap</b>	
	<p>This is the minimum gap should be maintained between exclusive_groups (all exclusive groups). The value is measured in microns. It can be set by command create_exclusive_groups -min_gap.</p> <p><b>Type:</b> <a href="#">coord</a></p> <p><b>Default:</b> 5</p> <p><b>Edit:</b> Yes</p>
<b>extract_rc_assume_metal_fill</b>	

	<p>Assume metal fill</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">extract_rc_assume_metal_fill</a></p>
<b>extract_rc_cap_filter_mode</b>	
	<p>Coupling Capacitance Filtering Mode</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> relative_only relative_and_coupling relative_or_coupling</p> <p><b>Default:</b> relative_only</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">extract_rc_cap_filter_mode</a></p>
<b>extract_rc_compress_rcdb</b>	
	<p>Create compressed RCDB</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">extract_rc_compress_rcdb</a></p>
<b>extract_rc_coupled</b>	
	<p>Extract coupling cap</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">extract_rc_coupled</a></p>
<b>extract_rc_coupling_cap_threshold</b>	
	<p>Coupling C threshold value</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 3.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">extract_rc_coupling_cap_threshold</a></p>
<b>extract_rc_def_via_cap</b>	
	<p>Consider via caps for extraction</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">extract_rc_def_via_cap</a></p>
<b>extract_rc_effort_level</b>	

	<p>Specifies the effort level of the post-route extraction engine</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> low medium high signoff</p> <p><b>Default:</b> undefined</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">extract_rc_effort_level</a></p>
<b>extract_rc_engine</b>	
	<p>Extraction engine</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> pre_route post_route</p> <p><b>Default:</b> pre_route</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">extract_rc_engine</a></p>
<b>extract_rc_extra_cmd_file</b>	
	<p>Extra command file for Quantus QRC</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">extract_rc_extra_cmd_file</a></p>
<b>extract_rc_hard_block_obs</b>	
	<p>Makes obstructions and power/ground pin shapes visible to the extractor for hard blocks only</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">extract_rc_hard_block_obs</a></p>
<b>extract_rc_incremental</b>	
	<p>Use incremental signoff mode</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">extract_rc_incremental</a></p>
<b>extract_rc_layer_independent</b>	
	<p>Enable layer independent extraction</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">extract_rc_layer_independent</a></p>

extract\_rc\_lef\_tech\_file\_map

LEF-QRCTechfile layer map file  
**Type:** [string](#)  
**Default:** ""  
**Edit:** Yes  
**Reference:** [extract\\_rc\\_lef\\_tech\\_file\\_map](#)

extract\_rc\_local\_cpu

**Type:** [int](#)  
**Default:** 0  
**Edit:** Yes  
**Reference:** [extract\\_rc\\_local\\_cpu](#)

extract\_rc\_pvs\_fill

Use to send the PVS fill data attached to the Innovus DB (see set\_pvs\_fill) to Quantus  
**Type:** [bool](#)  
**Default:** false  
**Edit:** Yes  
**Reference:** [extract\\_rc\\_pvs\\_fill](#)

extract\_rc\_qrc\_cmd\_file

Quantus QRC user command file name  
**Type:** [string](#)  
**Default:** ""  
**Edit:** Yes  
**Reference:** [extract\\_rc\\_qrc\\_cmd\\_file](#)

extract\_rc\_qrc\_cmd\_type

Quantus QRC command input type  
**Type:** [enum](#)  
**Enum Values:** auto partial custom  
**Default:** auto  
**Edit:** Yes  
**Reference:** [extract\\_rc\\_qrc\\_cmd\\_type](#)

extract\_rc\_qrc\_output\_mode

	Quantus QRC output mode <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> spref rcdb <b>Default:</b> spref <b>Edit:</b> Yes <b>Reference:</b> <a href="#">extract_rc_qrc_output_mode</a>
extract_rc_qrc_run_mode	
	Quantus QRC MMMC run mode <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> concurrent sequential <b>Default:</b> concurrent <b>Edit:</b> Yes <b>Reference:</b> <a href="#">extract_rc_qrc_run_mode</a>
extract_rc_qrc_stream_map_file	
	Quantus stream/oasis file <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">extract_rc_qrc_stream_map_file</a>
extract_rc_relative_cap_threshold	
	Relative C threshold value <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.03 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">extract_rc_relative_cap_threshold</a>
extract_rc_shrink_factor	
	Sets the shrink factor used by the extract_rc command.(Double, default=1) <b>Type:</b> <a href="#">double</a> <b>Default:</b> 1.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">extract_rc_shrink_factor</a>
extract_rc_signoff_stream_layer_map	
	QRC stream map file <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">extract_rc_signoff_stream_layer_map</a>

extract_rc_total_cap_threshold	
	Total C threshold value <b>Type:</b> double <b>Default:</b> 5.0 <b>Edit:</b> Yes <b>Reference:</b> extract_rc_total_cap_threshold
extract_rc_tquantus_model_file	
	TQuantus model file name <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> extract_rc_tquantus_model_file
extract_rc_turbo_reduce	
	Reduce XCap (IQuantus) <b>Type:</b> enum <b>Enum Values:</b> true false auto <b>Default:</b> auto <b>Edit:</b> Yes <b>Reference:</b> extract_rc_turbo_reduce
extract_rc_use_qrc oa_interface	
	Use OA interface for invoking Quantus QRC extraction <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> extract_rc_use_qrc oa_interface
extract_rc_use_shielding_in_detail_mode	
	Considers shielding for a wire segment <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> extract_rc_use_shielding_in_detail_mode
extract_rc_via_cap	
	Consider via caps for extraction <b>Type:</b> bool <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> extract_rc_via_cap

finish_floorplan_active_objs	
	active_object list <b>Type:</b> enum <b>Enum Values:</b> macro macro_halo core io_pad io_cell fence hard_blockage soft_blockage partial_blockage route_blockage row <b>Default:</b> macro macro_halo core <b>Edit:</b> Yes <b>Reference:</b> <a href="#">finish_floorplan_active_objs</a>
finish_floorplan_add_blockage_direction	
	direction <b>Type:</b> enum <b>Enum Values:</b> x y xy <b>Default:</b> xy <b>Edit:</b> Yes <b>Reference:</b> <a href="#">finish_floorplan_add_blockage_direction</a>
finish_floorplan_drc_region_objs	
	drc_region object list <b>Type:</b> enum <b>Enum Values:</b> macro macro_halo hard_blockage min_gap core_spacing non_row_area <b>Default:</b> macro macro_halo hard_blockage min_gap core_spacing <b>Edit:</b> Yes <b>Reference:</b> <a href="#">finish_floorplan_drc_region_objs</a>
finish_floorplan_override	
	override or not <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">finish_floorplan_override</a>
flexible_htrees	
	list of flexible_htree <b>Type:</b> obj(flexible_htree)* <b>Default:</b> "" <b>Edit:</b> No <b>Reference:</b> <a href="#">flexible_htrees</a>
flip_chip_allow_layer_change	

	<p>Specifies if turning on layer change feature</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_allow_layer_change</a></p>
flip_chip_allow_routed_bump_edit	<p>By default bumps are allowed to be edited (moved, deleted, reassigned, swapped). If this variable is set to FALSE, any bump edit command for a bump with routing connected to it will give an error message and fail.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_allow_routed_bump_edit</a></p>
flip_chip_auto_pairing_file	<p>Specifies the output file name to dump out route_flip_chip auto pairing information for bump to I/O connection</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_auto_pairing_file</a></p>
flip_chip_bottom_layer	<p>Specifies the bottom-most metal layer by layer number or layer name that the software can use when routing bumps</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_bottom_layer</a></p>
flip_chip_bump_use_octagon_shape	<p>route_flip_chip use circumferential octagon to replace the complex pin shape</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_bump_use_octagon_shape</a></p>
flip_chip_check_bump_access_directions	

	<p>Specifies whether check the special bump access directions</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_check_bump_access_directions</a></p>
flip_chip_compaction	<p>Specifies if turning on compaction routing</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_compaction</a></p>
flip_chip_connect_power_cell_to_bump	<p>Connects all power bumps to the I/O cell pin. It does not connect to a power or ground stripe or ring</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_connect_power_cell_to_bump</a></p>
flip_chip_constraint_file	<p>Specifies the file that contains constraints for flip chip routing</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_constraint_file</a></p>
flip_chip_drop_via_on_all_shapes	<p>route_flip_chip drop via on all geometries</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_drop_via_on_all_shapes</a></p>
flip_chip_drop_via_on_power_mesh	<p>Specifies the metal layer by layer number or layer name that the software can use to drop via</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_drop_via_on_power_mesh</a></p>
flip_chip_extra_config	

	<p>Specifies the name of an extra configuration file for flip chip routing</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_extra_config</a></p>
<b>flip_chip_finger_direction</b>	
	<p>Specifies main expansion direction for finger routing</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> n e s w</p> <p><b>Default:</b> n</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_finger_direction</a></p>
<b>flip_chip_finger_max_width</b>	
	<p>Specifies the max routing width for one wire segment</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_finger_max_width</a></p>
<b>flip_chip_finger_min_width</b>	
	<p>Specifies the min routing width for one wire segment</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_finger_min_width</a></p>
<b>flip_chip_finger_target_mesh_layer_range</b>	
	<p>Target mesh layer range for finger routing</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_finger_target_mesh_layer_range</a></p>
<b>flip_chip_honor_bump_connect_target_constraint</b>	
	<p>Specifies if enabling port numbering routing</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_honor_bump_connect_target_constraint</a></p>
<b>flip_chip_ignore_pad_type_check</b>	

	<p>Specifies if supporting CLASS PAD cells in flipchip flow</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_ignore_pad_type_check</a></p>
<b>flip_chip_lower_layer_prevent_diagonal_routing</b>	
	<p>Specifies if preventing 45-degree routing for lower layer</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_lower_layer_prevent_diagonal_routing</a></p>
<b>flip_chip_lower_layer_route_width</b>	
	<p>Specifies the different value for lower routing layer</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_lower_layer_route_width</a></p>
<b>flip_chip_multi_pad_routing_style</b>	
	<p>Specifies the routing style for multi-pads routing</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> default serial star</p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_multi_pad_routing_style</a></p>
<b>flip_chip_multiple_connection</b>	
	<p>Specifies routing connections between multiple pads and bumps. Default is no multiple connection</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> multiple_pads_to_bump multiple_bumps_to_pad default</p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flip_chip_multiple_connection</a></p>
<b>flip_chip_pg_mesh_direction</b>	

	<p>Specifies the main routing direction of PG mesh  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> default horizontal vertical  <b>Default:</b> default  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">flip_chip_pg_mesh_direction</a></p>
flip_chip_pg_mesh_main_width	<p>Specifies the main width of PG mesh  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 0.0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">flip_chip_pg_mesh_main_width</a></p>
flip_chip_pg_mesh_max_width	<p>Specifies the max width of PG mesh  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 0.0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">flip_chip_pg_mesh_max_width</a></p>
flip_chip_prevent_via_under_bump	<p>Specifies if generating vias directly under the bump  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">flip_chip_prevent_via_under_bump</a></p>
flip_chip_prevent_via_under_bump_extension	<p>specifies the spacing value around bump to avoid dropping vias  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 0.0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">flip_chip_prevent_via_under_bump_extension</a></p>
flip_chip_route_pg_style	<p>Specifies the routing pattern for route_flip_chip power routing  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> none finger mesh  <b>Default:</b> none  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">flip_chip_route_pg_style</a></p>

flip_chip_route_style	<p>Specifies routing style  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> manhattan diagonal  <b>Default:</b> diagonal  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">flip_chip_route_style</a></p>
flip_chip_route_width	<p>Specifies routing width  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 0.0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">flip_chip_route_width</a></p>
flip_chip_serial_pad_routing	<p>route_flip_chip try to make bump-pad-pad routing  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes</p>
flip_chip_top_layer	<p>Specifies the top-most metal layer by layer number or layer name that the software can use when routing bumps  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">flip_chip_top_layer</a></p>
floorplan_check_types	<p>Specify the check types for check_floorplan. Default is the basic.  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> basic fence odd_even_site_row macro_pin color alignment_following_pin alignment_partition_clone bus_guide_connectivity feed_through partition_in_partition multi_layer_pin power_domain partition place same_length_site narrow_channel block_only all  <b>Default:</b> basic  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">floorplan_check_types</a></p>
floorplan_cut_off_place_blockage_outside_die	

	<p>When creating placement blockages, will cut the part outside of die and snap it by default.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_cut_off_place_blockage_outside_die</a></p>
	<p><b>floorplan_cut_off_route_blockage_outside_die</b></p> <p>When creating routing blockages around inst/Hinst/Partition, will cut the part outside of die and snap it by default. If this option is set to false, don't cut and snap it.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_cut_off_route_blockage_outside_die</a></p>
	<p><b>floorplan_default_blockage_name_prefix</b></p> <p>Name prefix for placement blockage and routing blockage.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_default_blockage_name_prefix</a></p>
	<p><b>floorplan_default_power_domain_site</b></p> <p>Create rows based on default power domain site instead of the design's default site.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_default_power_domain_site</a></p>
	<p><b>floorplan_default_tech_site</b></p> <p>Specify a site as default technical site. After setting a forced one, the auto-calculating default-technical-site functionality will be disabled.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_default_tech_site</a></p>
	<p><b>floorplan_include_io_when_init_area</b></p> <p>Include IO cells when calculating the area of modules.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_include_io_when_init_area</a></p>

<b>floorplan_keep_rows_when_moving_power_domain</b>	<p>specify whether to keep all existing rows in disjoint power domain when moving, resizing or reshaping a power domain on GUI or by command.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_keep_rows_when_moving_power_domain</a></p>
<b>floorplan_max_io_height</b>	<p>Use maximum IO height to calculate a die box with IO placement. By default, minimum IO height is used.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_max_io_height</a></p>
<b>floorplan_minimum_sites</b>	<p>Specify the number of minimal sites (N) that check_floorplan will check for the same length site rule. When same_length_site is specified in floorplan_check_types, this option is required.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_minimum_sites</a></p>
<b>floorplan_narrow_channel_threshold</b>	<p>Reports narrow channels whose width (in microns) is smaller than the specified value. When narrow_channel is specified in floorplan_check_types, this option is required.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_narrow_channel_threshold</a></p>
<b>floorplan_power_rail_layer</b>	<p>Specify the layers for calculating power/ground on bottom attribute of cell or techsite. By default, the lowest metal layer is used.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_power_rail_layer</a></p>
<b>floorplan_row_site_height</b>	

	<p>Specify the odd even row height constraints.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> any odd even</p> <p><b>Default:</b> any</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_row_site_height</a></p>
<a href="#">floorplan_row_site_width</a>	<p>Specify the odd even row width constraints.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> any odd even</p> <p><b>Default:</b> any</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_row_site_width</a></p>
<a href="#">floorplan_snap_block_grid</a>	<p>Specify the block snap rules. It can be set to snap to manufacture grid, instance grid, placement grid, user-define grid, layer_track grid, finfet manufacture grid, finfet instance grid, finfet placement grid. The default is manufacturing_grid. For Finfet design, the default is finfet_manufacturing_grid.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> manufacturing inst placement user_define layer_track finfet_inst finfet_manufacturing finfet_placement</p> <p><b>Default:</b> manufacturing</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_snap_block_grid</a></p>
<a href="#">floorplan_snap_constraint_grid</a>	<p>Specify the constraint snap rules. It can be set to snap to manufacture grid, instance grid, placement grid, user-define grid, layer_track grid, finfet manufacture grid, finfet instance grid, finfet placement grid. The default is inst_grid. For Finfet design, the default is finfet_inst_grid.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> manufacturing inst placement user_define layer_track finfet_inst finfet_manufacturing finfet_placement</p> <p><b>Default:</b> inst</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_snap_constraint_grid</a></p>
<a href="#">floorplan_snap_core_grid</a>	

	<p>Specify the core snap rules. It can be set to snap to manufacture grid, instance grid, placement grid, user-define grid, layer_track grid, finfet manufacture grid, finfet instance grid, finfet placement grid. The default is placement_grid. For Finfet design, the default is finfet_placement_grid.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> manufacturing inst placement user_define layer_track finfet_inst finfet_manufacturing finfet_placement</p> <p><b>Default:</b> placement</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_snap_core_grid</a></p>
floorplan_snap_die_grid	
	<p>Specify the die snap rules. It can be set to snap to manufacture grid, instance grid, placement grid, user-define grid, layer_track grid, finfet manufacture grid, finfet instance grid, finfet placement grid. The default is placement_grid. For Finfet design, the default is finfet_placement_grid.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> manufacturing inst placement user_define layer_track finfet_inst finfet_manufacturing finfet_placement</p> <p><b>Default:</b> placement</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_snap_die_grid</a></p>
floorplan_snap_io_grid	
	<p>Specify the IO snap rules. It can be set to snap to manufacture grid, instance grid, placement grid, user-define grid, layer_track grid, finfet manufacture grid, finfet instance grid, finfet placement grid. The default is manufacturing_grid. For Finfet design, the default is finfet_manufacturing_grid.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> manufacturing inst placement user_define layer_track finfet_inst finfet_manufacturing finfet_placement</p> <p><b>Default:</b> manufacturing</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_snap_io_grid</a></p>
floorplan_snap_place_blockage_grid	
	<p>Specify the placement blockage snap rules. The default is inst_grid.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> manufacturing inst finfet_inst finfet_manufacturing</p> <p><b>Default:</b> inst</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">floorplan_snap_place_blockage_grid</a></p>
floorplan_vertical_row	

	Specifies that the rows in the floorplan are vertical (1) or horizontal (0). <b>Type:</b> int <b>Default:</b> 0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">floorplan_vertical_row</a>
<b>flow_branch</b>	
	Branch being run for a hierarchical flow. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_branch</a>
<b>flow_caller_data</b>	
	Data used by the caller of the tool to identify this flow. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_caller_data</a>
<b>flow_current</b>	
	Flow to execute by default. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_current</a>
<b>flow_db_directory</b>	
	Flow directory where results databases are stored. <b>Type:</b> string <b>Default:</b> dbs <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_db_directory</a>
<b>flow_error_errorinfo</b>	
	Tcl error stack in error database. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_error_errorinfo</a>
<b>flow_error_message</b>	

	Tcl error message in error database. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_error_message</a>
flow_error_write_db	Write a database when a flow step results in an error condition. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_error_write_db</a>
flow_exit_when_done	Exit after running final step. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_exit_when_done</a>
flow_feature_values	Global feature settings. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_feature_values</a>
flow_features	Global feature definitions. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_features</a>
flow_footer_tcl	TCL script to run when a flow ends. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_footer_tcl</a>
flow_header_tcl	

	TCL script to run when a flow starts. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_header_tcl</a>
flow_hier_path	Path of current flow within the flow hierarchy. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_hier_path</a>
flow_history	Complete flow run history. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_history</a>
flow_log_directory	Flow directory where log files are stored. <b>Type:</b> <a href="#">string</a> <b>Default:</b> logs <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_log_directory</a>
flow_log_prefix_generator	TCL script to create log filenames in Flow tool. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_log_prefix_generator</a>
flow_mail_on_error	Email to flow_mail_to if an error is detected. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_mail_on_error</a>
flow_mail_to	

	Email address where results are sent. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_mail_to</a>
<b>flow_metrics_file</b>	
	Flow metrics file for reporting results. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_metrics_file</a>
<b>flow_metrics_snapshot_parent_uuid</b>	
	The snapshot uuid the results from this flow will be appended to. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_metrics_snapshot_parent_uuid</a>
<b>flow_metrics_snapshot_uuid</b>	
	The snapshot uuid of the most recent flow step executed. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_metrics_snapshot_uuid</a>
<b>flow_overwrite_db</b>	
	Enables overwriting databases when saving. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_overwrite_db</a>
<b>flow_plugin_names</b>	
	Names of all internal plug-in points. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_plugin_names</a>
<b>flow_plugin_steps</b>	

	<p>List of plug-in steps that have been added through edit_flow.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_plugin_steps</a></p>
flow_post_db_overwrite	<p>If set within a skip_db flow_step, it allows the user to identify the name and type of database to present to future flows as the flow_starting_db.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_post_db_overwrite</a></p>
flow_remark	<p>Remark from the last flow yaml file loaded.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_remark</a></p>
flow_report_directory	<p>Flow directory where reports are written.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> reports</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_report_directory</a></p>
flow_reset_time_after_flow_init	<p>Reset all time measures after flow init.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_reset_time_after_flow_init</a></p>
flow_run_tag	<p>Tags for this particular flow run.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_run_tag</a></p>
flow_schedule	

	<p>Set of flows to execute after the current flow completes.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_schedule</a></p>
flow_starting_db	<p>Starting database for the flow run.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_starting_db</a></p>
flow_startup_directory	<p>Directory where the tool was started.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> /home/manishk/dbschema/novus/newscript</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_startup_directory</a></p>
flow_status_file	<p>File for flow status.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_status_file</a></p>
flow_step_begin_tcl	<p>Defines the Tcl to run before running the body of each step.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
flow_step_canonical_current	<p>Currently running canonical flow step.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_step_canonical_current</a></p>
flow_step_check_tcl	

	Procedure to check the steps. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_step_check_tcl</a>
<b>flow_step_current</b>	
	Currently running flow step. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_step_current</a>
<b>flow_step_end_tcl</b>	
	Defines the Tcl to run after running the body of each step. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes
<b>flow_step_last</b>	
	Last flow step to have been completed. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_step_last</a>
<b>flow_step_last_msg</b>	
	Message provided for the last step that was run. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_step_last_msg</a>
<b>flow_step_last_status</b>	
	Status for the last flow step run. <b>Type:</b> <a href="#">string</a> <b>Default:</b> not_run <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_step_last_status</a>
<b>flow_step_next</b>	

	Next step to run in the flow. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_step_next</a>
<b>flow_steps</b>	
	List of all created flow_steps <b>Type:</b> <a href="#">obj(flow_step)</a> * <b>Default:</b> "" <b>Edit:</b> No
<b>flow_summary_tcl</b>	
	TCL script to run during run_flow summary. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_summary_tcl</a>
<b>flow_template_feature_definition</b>	
	Features list and status for the current template. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_template_feature_definition</a>
<b>flow_template_tools</b>	
	List of tools included in flow templates being run. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_template_tools</a>
<b>flow_template_type</b>	
	Type of template being run. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flow_template_type</a>
<b>flow_template_version</b>	

	<p>Version of the template being run.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_template_version</a></p>
<b>flow_user_templates</b>	
	<p>Flow user template definitions.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_user_templates</a></p>
<b>flow_verbose</b>	
	<p>Enables printing run information in the logfile.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_verbose</a></p>
<b>flow_working_directory</b>	
	<p>Flow directory where the flow is being run.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> .</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_working_directory</a></p>
<b>flow_yamllint_exec</b>	
	<p>Yamllint executable command and arguments for checking yaml files.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> yamllint</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">flow_yamllint_exec</a></p>
<b>flows</b>	
	<p>List of all created flows</p> <p><b>Type:</b> <a href="#">obj(flow)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>flowtool_exit_timeout</b>	

	Maximum amount of time in seconds Flow tool will wait after a tool exits for a completed status. <b>Type:</b> <a href="#">int</a> <b>Default:</b> 30 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flowtool_exit_timeout</a>
flowtool_extra_arguments	Extra arguments passed to Flowtool when running in tool mode. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flowtool_extra_arguments</a>
flowtool_metrics_qor_excel	Metrics file to write after tools exit. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flowtool_metrics_qor_excel</a>
flowtool_metrics_qor_html	Metrics file to write after tools exit. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flowtool_metrics_qor_html</a>
flowtool_metrics_qor_text	Metrics file to write after tools exit. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flowtool_metrics_qor_text</a>
flowtool_metrics_qor_vivid	Metrics file to write after tools exit. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flowtool_metrics_qor_vivid</a>
flowtool_predict_full_names	

	Show skip_metric flow name in prediction. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flowtool_predict_full_names</a>
<b>flowtool_summary_tcl</b>	
	Tcl script to run at the end of flowtool. <b>Type:</b> <a href="#">string</a> <b>Default:</b> puts [report_metric -format text] <b>Edit:</b> Yes <b>Reference:</b> <a href="#">flowtool_summary_tcl</a>
<b>foreign_cells</b>	
	Short-cut for [get_db base_cells .foreign_cells] <b>Type:</b> <a href="#">obj(foreign_cell)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>gcell_grids</b>	
	Short-cut to all the gcell_grid objects in the design. <b>Type:</b> <a href="#">obj(gcell_grid)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>gcells</b>	
	The gcells for this design. The gcells are only created after global route has occurred. <b>Type:</b> <a href="#">obj(gcell)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>generate_special_via_add_pin_to_pin_vias</b>	
	Inserts vias to connect pins between cover macros <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">generate_special_via_add_pin_to_pin_vias</a>
<b>generate_special_via_align_merged_stack_via_metal</b>	

	<p>Aligns merged stack vias</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_align_merged_stack_via_metal</a></p>
generate_special_via_allow_via_expand	
	<p>Allows via expansion to meet LEF rules</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_allow_via_expand</a></p>
generate_special_via_allow_wire_shape_change	
	<p>Allows via to change the metal shape of existing wire</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_allow_wire_shape_change</a></p>
generate_special_via_area_only	
	<p>adds via only within the specified area</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_area_only</a></p>
generate_special_via_check_signal_routes	
	<p>Honors pre-existing signal routes</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> 0 1 2</p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_check_signal_routes</a></p>
generate_special_via_create_double_row_cut_via	

	<p>Expands vias to have an additional cut than original for one-row or one-column vias if possible</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> no_extra_cut add_extra_cut add_extra_cut_and_metal</p> <p><b>Default:</b> no_extra_cut</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_create_double_row_cut_via</a></p>
generate_special_via_create_max_row_cut_via	
	<p>Creates max rows of via cuts</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_create_max_row_cut_via</a></p>
generate_special_via_cut_class_preference	
	<p>Specifies via cut class preference</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_cut_class_preference</a></p>
generate_special_via_disable_via_merge	
	<p>Disables via merging</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_disable_via_merge</a></p>
generate_special_via_enable_check_drc	
	<p>Invokes check_drc</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_enable_check_drc</a></p>
generate_special_via_extend_out_wire_end	
	<p>Extends via outside of existing wires end</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_extend_out_wire_end</a></p>

generate_special_via_full_cut_via_only	<p>allows to create full cut via only  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">generate_special_via_full_cut_via_only</a></p>
generate_special_via hookup_contact_max	<p>Sets the max distance to create hookup via from contact, and the max distance between two hookup via on a continuous M0 PG pin.  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> 0, 0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">generate_special_via_hookup_contact_max</a></p>
generate_special_via_hookup_contact_pg_track	<p>Sets start point and the pitch of PG track used by hookup contact.  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> 0, 0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">generate_special_via_hookup_contact_pg_track</a></p>
generate_special_via_hookup_fixed_grid	<p>Specifies to add hookup via over the fixed Grid.  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">generate_special_via_hookup_fixed_grid</a></p>
generate_special_via_hookup_min_distance	<p>min distance between two pg vias  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> min  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">generate_special_via_hookup_min_distance</a></p>
generate_special_via_hookup_rail_pair	<p>Create hookup vias over pairing followpins  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">generate_special_via_hookup_rail_pair</a></p>

generate\_special\_via\_hookup\_via\_distance

Sets via hookup distance and boundary spacing

**Type:** [string](#)

**Default:** 4pitch 4pitch 0

**Edit:** Yes

**Reference:** [generate\\_special\\_via\\_hookup\\_via\\_distance](#)

generate\_special\_via\_hookup\_via\_style

Sets via hookup style

**Type:** [enum](#)

**Enum Values:** none loose compact moderate

**Default:** none

**Edit:** Yes

**Reference:** [generate\\_special\\_via\\_hookup\\_via\\_style](#)

generate\_special\_via\_ignore\_drc

Ignores DRC

**Type:** [bool](#)

**Default:** false

**Edit:** Yes

**Reference:** [generate\\_special\\_via\\_ignore\\_drc](#)

generate\_special\_via\_ignore\_rule\_enclosure

Ignores enclosures defined in VIARULE GENERATE

**Type:** [bool](#)

**Default:** true

**Edit:** Yes

**Reference:** [generate\\_special\\_via\\_ignore\\_rule\\_enclosure](#)

generate\_special\_via\_inherit\_wire\_status

Inherits wire status

**Type:** [bool](#)

**Default:** false

**Edit:** Yes

**Reference:** [generate\\_special\\_via\\_inherit\\_wire\\_status](#)

generate\_special\_via\_keep\_existing\_via

	<p>Keeps existing vias</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> remove keep_with_new_via keep_with_no_new_via</p> <p><b>Default:</b> remove</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_keep_existing_via</a></p>
generate_special_via_keep_fixed_via	
	<p>Keeps fixed vias not modifiable</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_keep_fixed_via</a></p>
generate_special_via_opt_cross_via	
	<p>Controls the creation of additional via cuts</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_opt_cross_via</a></p>
generate_special_via_opt_via_on_routing_track	
	<p>Frees up via tracks</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_opt_via_on_routing_track</a></p>
generate_special_via_parameterized_via_only	
	<p>generate parameterized vias only, auto sets true for OA flow, false for non-OA flow.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> auto true false</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_parameterized_via_only</a></p>
generate_special_via_partial_overlap_threshold	
	<p>Specifies ratio threshold of via creation on partial overlap wires</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_partial_overlap_threshold</a></p>

generate\_special\_via\_preferred\_vias\_only

Generate only vias set in -viarule\_preference

**Type:** enum

**Enum Values:** use\_lef open keep

**Default:** use\_lef

**Edit:** Yes

**Reference:** generate\_special\_via\_preferred\_vias\_only

generate\_special\_via\_prefix

Specifies prefix name for all vias

**Type:** string

**Default:** ""

**Edit:** Yes

**Reference:** generate\_special\_via\_prefix

generate\_special\_via\_reference\_boundary

Sets reference boundary

**Type:** enum

**Enum Values:** design core

**Default:** design

**Edit:** Yes

**Reference:** generate\_special\_via\_reference\_boundary

generate\_special\_via\_respect\_stdcell\_geometry

Respects all standard cell patterns

**Type:** bool

**Default:** false

**Edit:** Yes

**Reference:** generate\_special\_via\_respect\_stdcell\_geometry

generate\_special\_via\_rule\_preference

Specifies via rule preference

**Type:** string

**Default:** default

**Edit:** Yes

**Reference:** generate\_special\_via\_rule\_preference

generate\_special\_via\_set\_via\_expand\_dir

	<p>Sets via expansion direction</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> auto horizontal vertical</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_set_via_expand_dir</a></p>
generate_special_via_snap_via_center_to_grid	<p>Specifies the via center alignment style per routing layer</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_snap_via_center_to_grid</a></p>
generate_special_via_split_long_via_global_grid	<p>Controls global grids so vias on them are in line</p> <p><b>Type:</b> string</p> <p><b>Default:</b> 0 0 0 0 0 0 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_split_long_via_global_grid</a></p>
generate_special_via_symmetrical_via_only	<p>adds symmetrical via only, auto sets true for OA flow, false for non-OA flow.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> auto true false</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_symmetrical_via_only</a></p>
generate_special_via_use_track_offset	<p>Uses track offset</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_use_track_offset</a></p>
generate_special_via_use_trim_metal_enclosure	<p>Force tool to use enclosures with trim layer</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">generate_special_via_use_trim_metal_enclosure</a></p>

get_db_display_limit	
	<p>Controls the number of objects that will be displayed when using get_db with an attribute pattern like '*' rather than single attribute name. If the value is 10, 'get_db insts.*' will only display 10 inst objects with all their attributes, and will only display the first 10 objects for any attribute that is an object list (e.g. the first 10 pins for each inst .pins value).</p> <p><b>Type:</b> int  <b>Default:</b> 10  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">get_db_display_limit</a></p>
group_hinst_suffix	
	<p>new hinst name is created from the module name with a suffix added as defined by this tcl global</p> <p><b>Type:</b> string  <b>Default:</b> i  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">group_hinst_suffix</a></p>
groups	
	<p>Short-cut for [get_db current_design .groups]</p> <p><b>Type:</b> obj(group)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
gui_lines	
	<p>Short-cut to all the gui_line objects in the design.</p> <p><b>Type:</b> obj(gui_line)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
gui_polygons	
	<p>Short-cut to all the gui_polygon objects in the design.</p> <p><b>Type:</b> obj(gui_polygon)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
gui_rects	
	<p>Short-cut to all the gui_rect objects in the design.</p> <p><b>Type:</b> obj(gui_rect)*  <b>Default:</b> ""  <b>Edit:</b> No</p>

gui_shapes	
	<p>Short-cut to all the gui_shape objects in the design.</p> <p><b>Type:</b> <a href="#">obj(gui_rect)*</a> <a href="#">obj(gui_line)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
gui_texts	
	<p>Short-cut to all the gui_text objects in the design.</p> <p><b>Type:</b> <a href="#">obj(gui_text)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
gui_verbose	
	<p>Controls which GUI actions are logged. The choices are:</p> <p>all: all GUI actions;</p> <p>db: GUI actions that affect the DB like gui_select, set_layer_preference, but not display-only actions like gui_zoom, gui_pan;</p> <p>none: no gui_* commands are logged, so the .log and .cmd file are incomplete</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> all db none</p> <p><b>Default:</b> db</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">gui_verbose</a></p>
hinsts	
	<p>Short-cut for [get_db current_design .hinsts]</p> <p><b>Type:</b> <a href="#">obj(hinst)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
hnets	
	<p>Short-cut for [get_db current_design .hnets]</p> <p><b>Type:</b> <a href="#">obj(hnet)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
hpins	
	<p>Short-cut for [get_db current_design .hpins]</p> <p><b>Type:</b> <a href="#">obj(hpin)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

hports	
	<p>Short-cut for [get_db hinsts .hports]</p> <p><b>Type:</b> <a href="#">obj(hport)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
ilm_filter_internal_path	
	<p>filterInternalPath</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">ilm_filter_internal_path</a></p>
ilm_keep_async	
	<p>Keep paths from asynchronous input ports</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">ilm_keep_async</a></p>
ilm_keep_flatten	
	<p>Instruct Innovus to keep in flattened state</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">ilm_keep_flatten</a></p>
ilm_keep_high_fanout_ports	
	<p>Keep high fanout input port paths</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">ilm_keep_high_fanout_ports</a></p>
ilm_keep_loopback	
	<p>Keep loop back paths</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">ilm_keep_loopback</a></p>
init_check_netlist	

	<p>After reading in the netlist, will do the same checks as check_design -netlist</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_check_netlist</a></p>
	<p><b>init_check_output_pin_constant</b></p>
	<p>Stops the Verilog reader if any output (or inout) signal pins have any 1'b0 or 1'b1 constants that would cause shorts to power/ground.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_check_output_pin_constant</a></p>
	<p><b>init_delete_floating_hnets</b></p>
	<p>If true, an hnet (Verilog wire statement) that has nothing connected to it, is deleted from the netlist. The default value is false in Innovus to allow for netlist repair, but true in Tempus to delete non-timed nets and reduce memory.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_delete_floating_hnets</a></p>
	<p><b>init_design_netlist_type</b></p>
	<p>Specifies the source of the design netlist. You can specify either "Verilog" or "OA".</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> Verilog</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_design_netlist_type</a></p>
	<p><b>init_design_uniquify</b></p>
	<p>Specifies whether the top is uniquified. When set to 1 (true) the design will be uniquified during the read and flatten process. Optimization is not allowed on a non-unique design. For use in a master/clone partitioning flow, the value should be 0 (false). Default = 0 (false).</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_design_uniquify</a></p>
	<p><b>init_ground_nets</b></p>

	<p>List of global Ground nets.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_ground_nets</a></p>
	<p><b>init_ignore_pg_pin_polarity_check</b></p> <p>List of leaf cell pin names to ignore power/ground pin polarity check. By default connect_global_net and CPF check for matching polarity between the net and pin.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_ignore_pg_pin_polarity_check</a></p>
	<p><b>init_keep_empty_modules</b></p> <p>By default, usage of an empty Verilog module that has no matching library cell name becomes an empty hinst. If this value is false, a dummy library cell is created, and usage of it becomes an inst. You should then use other commands to 'fix' the dummy library cell before proceeding in the flow.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_keep_empty_modules</a></p>
	<p><b>init_lef_files</b></p> <p>List of LEF files to be read. Mutually exclusive with init_oa_ref_lib.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_lef_files</a></p>
	<p><b>init_min_dbu_per_micron</b></p> <p>Minimum DBU per micron</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_min_dbu_per_micron</a></p>
	<p><b>init_mmmc_files</b></p>

	<p>Path to MMMC View Definition file.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_mmmc_files</a></p>
	<p><b>init_no_new_assigns</b></p> <p>Turns on an assign-free flow. By default, applications like optimization can add Verilog assigns to remove unnecessary buffers and reduce power. If you have external tools that do not support Verilog assigns, you can set this value to true to prevent applications from adding any new assign statements to the Verilog netlist. If there are existing assigns in the Verilog netlist you can remove them with the delete_assigns command.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_no_new_assigns</a></p>
	<p><b>init_oa_abstract_views</b></p> <p>List of OpenAccess view names to be processed as abstracts (LEF MACRO equivalent). The read_netlist command uses init_oa_abstract_views list for on-demand loading of missing cells. Used by the read_physical and read_netlist commands.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_oa_abstract_views</a></p>
	<p><b>init_oa_default_rule</b></p> <p>The default rule to be used in OpenAccess. Typically used to specify a metal stack LEFDefaultRouteSpec type constraint group to read from the technology library if the library contains multiple metal stacks. Used by the read_physical command.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_oa_default_rule</a></p>
	<p><b>init_oa_design_cell</b></p> <p>OpenAccess design cell name that was read. Set by the read_netlist -oa_cell_view command.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_oa_design_cell</a></p>

init_oa_design_lib	<p>OpenAccess design lib name that was read. Set by the read_netlist -oa_cell_view command.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_oa_design_lib</a></p>
init_oa_design_view	<p>OpenAccess design view name that was read. Set by the read_netlist -oa_cell_view command.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_oa_design_view</a></p>
init_oa_layout_views	<p>List of OpenAccess view names to be processed for cell layout viewing (GDSII equivalent). Also used in the case where a Verilog netlist is read and views from the init_oa_layout_views list are used in the Quick Abstract Inference flow to derive abstract information from layout views for cells that were not processed from the libraries in the read_physical -oa_ref_libs list. The read_netlist command uses init_oa_layout_view list for on-demand loading of missing cells. Used by the read_physical and read_netlist commands.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_oa_layout_views</a></p>
init_oa_ref_libs	<p>List of OpenAccess reference libraries. The first library in the list indicates the library that was used for technology information unless read_physical -oa_tech_lib is specified. All cells from the specified libraries are read. It is important to include the standard cell library in the list to make sure that cells that are not in the current netlist are read and available for optimization. The init_oa_abstract_views and init_oa_layout_views lists specify which views of the cells are read. Set by the read_physical -oa_ref_libs command.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_oa_ref_libs</a></p>
init_oa_search_libs	

	<p>List of OpenAccess reference libraries to be searched when cells are used in the Verilog netlist that are not found in the list of cells read from the libraries specified by read_physical - oa_ref_libs command, by default all libraries in the cds.lib are searched. The init_oa_abstract_views and init_oa_layout_views lists are used to indicate which view names are looked for during the search. Applies only when read_netlist command is used to process a Verilog netlist specify the connectivity to be read. Set by the read_physical - oa_search_libs command and used by the read_netlist command.</p> <p><b>Type:</b> string <b>Default:</b> * <b>Edit:</b> Yes <b>Reference:</b> <a href="#">init_oa_search_libs</a></p>
init_oa_special_rule	<p>The special rule to be used in OpenAccess to define the via search order for power routing. Typically used to specify a metal stack LEFSpecialRouteRouteSpec type constraint group to read from the technology library if the library contains multiple metal stacks. Used by the read_physical command.</p> <p><b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">init_oa_special_rule</a></p>
init_oa_tech_lib	<p>OpenAccess library to use as source of technology information. If not specified, the first library in the read_physical - oa_ref_libs list will be used. Applies only when read_netlist is used to process a Verilog netlist. Set by the read_physical - oa_tech_lib command.</p> <p><b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">init_oa_tech_lib</a></p>
init_power_intent_files	<p>Power intent files(s) read by last 'read_power_intent' command.</p> <p><b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No <b>Reference:</b> <a href="#">init_power_intent_files</a></p>
init_power_nets	

	<p>List of global Power nets.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_power_nets</a></p>
	<p><b>init_read_netlist_allow_port_mismatch</b></p> <p>If false, a Verilog instance with ports that do not match the Verilog module or library cell definition will cause an error and exit. If true, an error message occurs, but the extra ports are added to the module or library cell definition to allow the inconsistent netlist to be read in and debugged further. The default is true for Innovus to allow repair of 'dirty netlists', but false for Tempus that normally does not tolerate 'dirty netlists'.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_read_netlist_allow_port_mismatch</a></p>
	<p><b>init_read_netlist_allow_undefined_cells</b></p> <p>If false, a Verilog reference to an undefined cell (e.g. a Verilog module name that has no matching library cell and no Verilog module definition) causes an error and an exit after parsing the netlist. If true, an empty Verilog module is created with a warning. The default value is true in Innovus to allow repair of 'dirty netlists' while it is false in Tempus to stop on 'dirty netlists'. An empty module will become an hinst or inst depending on the value of init_keep_empty_modules.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_read_netlist_allow_undefined_cells</a></p>
	<p><b>init_read_netlist_files</b></p> <p>A list of Verilog files read in during initialization. read_netlist will set this root attribute to the list of input files given to it. The original input file names are retained thru the flow for reference, and used by write_do_lec for the default golden netlist comparison file names.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">init_read_netlist_files</a></p>
	<p><b>init_sync_relative_path</b></p>

	<p>Synchronize Relative paths  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">init_sync_relative_path</a></p>
init_timing_enabled	<p>If read_physical is issued before read_mmmc or read_libs in RC and Tempus, an error will be issued. In EDI, doing this will result in init_timing_enabled being set to false by the tool. EDI is now in physical only mode, and any attempt to set timing data will result in an error. By default, init_timing_enabled is set to true.  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> true  <b>Edit:</b> No  <b>Reference:</b> <a href="#">init_timing_enabled</a></p>
insts	<p>insts of current design  <b>Type:</b> <a href="#">obj(inst)*</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
io_constraints	<p>Short-cut for [get_db current_design .io_constraints]  <b>Type:</b> <a href="#">obj(io_constraint)*</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
is_ilm_flattened	<p>Is true if you have ILMs, and the flatten_ilm command has flattened them so the internal ILM insts are visible. unflatten_ilm will set it back to false.  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> No</p>
is_ilm_read	<p>Is true if you have read in any ILMs with read_ilm. It is not affected by flatten_ilm/unflatten_ilm.  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> No</p>
layer_name_no_abbreviation	

	<p>By default this value is true, and most command -layer &lt;layer&gt; options require a LEF/OA layer name, or a routing-layer index value (e.g. 1 for the first routing layer, 2 for the second, etc.) for input. If this global is false, then an older style abbreviation is also allowed (e.g. M1 for the first routing layer, M2 for the second routing layer, etc.). This layer abbreviation style is not recommended, and is only allowed for backward compatibility to migrate older scripts. Eventually this global will be removed, so you should modify your scripts to use LEF/OA layer names, or routing-layer index values for -layer options to avoid problems in the future.</p> <p><b>Type:</b> <code>bool</code>  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">layer_name_no_abbreviation</a></p>
<b>layers</b>	
	<p>All the layers defined in the LEF or OA techfile.</p> <p><b>Type:</b> <code>obj(layer)*</code>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>lib_arcs</b>	
	<p>lib_arcs</p> <p><b>Type:</b> <code>obj(lib_arc)*</code>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>lib_cells</b>	
	<p>lib_cells</p> <p><b>Type:</b> <code>obj(lib_cell)*</code>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>lib_pins</b>	
	<p>lib_pins</p> <p><b>Type:</b> <code>obj(lib_pin)*</code>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>libraries</b>	
	<p>Returns the information about the libraries in the design.</p> <p><b>Type:</b> <code>obj(library)*</code>  <b>Default:</b> ""  <b>Edit:</b> No</p>
<b>library_sets</b>	

	Returns the information about the library sets in the design. <b>Type:</b> <a href="#">obj(library_set)</a> * <b>Default:</b> "" <b>Edit:</b> No
log_file	log file name of the program <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">log_file</a>
log_verbose_type	When verbose logging is enabled (see source_verbose, flow_verbose, or set_proc_verbose), the default logging of each commands is pre-Tcl expansion. In some cases it is helpful to see post-Tcl expansion, or even both pre-Tcl and post-Tcl expansion when doing detailed debugging. You can switch between settings in the middle of a script. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> pre post both <b>Default:</b> pre <b>Edit:</b> Yes <b>Reference:</b> <a href="#">log_verbose_type</a>
logv_file	verbose log file name of the program <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">logv_file</a>
markers	Short-cut to all the marker objects in the design. <b>Type:</b> <a href="#">obj(marker)</a> <b>Default:</b> "" <b>Edit:</b> No
messages	A list of all the message objects. <b>Type:</b> <a href="#">obj(message)</a> * <b>Default:</b> "" <b>Edit:</b> No
metric_advanced_url_endpoint	

	<p>Base URL for the advanced metric server.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">metric_advanced_url_endpoint</a></p>
metric_capture_depth	<p>Depth for capturing hinst design and power metrics.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">metric_capture_depth</a></p>
metric_capture_design_image	<p>Capture design image.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">metric_capture_design_image</a></p>
metric_capture_max_drc_markers	<p>Maximum number of DRC markers to include in metric image.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1000</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">metric_capture_max_drc_markers</a></p>
metric_capture_min_count	<p>Minimum instance count for capturing hinst design and power metrics.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1000</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">metric_capture_min_count</a></p>
metric_capture_overwrite	<p>Overwrite pending metrics during create_snapshot category capture.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">metric_capture_overwrite</a></p>
metric_capture_pba_tns_histogram	

	Capture path based analysis histogram data for TNS. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">metric_capture_pba_tns_histogram</a>
metric_capture_per_view	
	Capture timing metrics per analysis_view. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">metric_capture_per_view</a>
metric_capture_timing_paths	
	Number of paths to capture for detailed display. <b>Type:</b> <a href="#">int</a> <b>Default:</b> 10 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">metric_capture_timing_paths</a>
metric_capture_tns_histogram	
	Capture histogram data for TNS. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">metric_capture_tns_histogram</a>
metric_capture_tns_histogram_buckets	
	Number of buckets for the TNS histogram. <b>Type:</b> <a href="#">int</a> <b>Default:</b> 50 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">metric_capture_tns_histogram_buckets</a>
metric_capture_tns_histogram_max_slack	
	Maximum slack for the TNS histogram. <b>Type:</b> <a href="#">int</a> <b>Default:</b> 0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">metric_capture_tns_histogram_max_slack</a>
metric_capture_tns_histogram_paths	

	<p>Number of paths to capture for the TNS histogram.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 10000</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">metric_capture_tns_histogram_paths</a></p>
metric_category_default	<p>Default metric categories to capture if none are provided.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> design</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">metric_category_default</a></p>
metric_current_run_id	<p>Current unique run ID returned by the advanced metric server.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">metric_current_run_id</a></p>
metric_enable	<p>enable metric snapshot capture with create_snapshot</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">metric_enable</a></p>
metric_summary_metrics	<p>Summary metrics to show when creating snapshots.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> flow.cputime flow.realtime timing.setup.tns timing.setup.wns</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">metric_summary_metrics</a></p>
modules	<p>Short-cut for [get_db current_design .modules]</p> <p><b>Type:</b> <a href="#">obj(module)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
net_groups	

	<p>Short-cut for [get_db current_design .net_groups]</p> <p><b>Type:</b> <a href="#">obj(net_group)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
nets	
	<p>Short-cut for [get_db current_design .nets]. All the nets inside this design, including logical Verilog nets, physical-only nets, Verilog supply0/supply1, and Verilog 1'b0/1'b1 nets.</p> <p><b>Type:</b> <a href="#">obj(net)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
num_eeq_variants	
	<p>Maximum number of EEQ variants of any cell in library, from LIBRARY LEF58_CELLVARIANTS property 'CELLVARIANTS variantTotalNum YFLIPMAP {flippedVariantNum siteVariantNum} ...'</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
oa_allow_analysis_only	
	<p>Allow analysis only flow</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">oa_allow_analysis_only</a></p>
oa_allow_bit_connection	
	<p>Whether to create instance terminal creations bitwise, if bus not found in OA.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">oa_allow_bit_connection</a></p>
oa_allow_tech_update	
	<p>Whether to allow the tech.db to be updated or not.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">oa_allow_tech_update</a></p>
oa_bindkey_file	

	Virtuoso bind key file <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">oa_bindkey_file</a>
oa_cell_view_dir	System defined transient global referring to origin of restored design. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">oa_cell_view_dir</a>
oa_convert_diagonal_path_to	Whether to convert non-conforming pathsegs/paths to polygon or convert the endStyle to truncate on orthogonal and to custom on diagonal pathsegs <b>Type:</b> enum <b>Enum Values:</b> polygon default_style <b>Default:</b> polygon <b>Edit:</b> Yes <b>Reference:</b> <a href="#">oa_convert_diagonal_path_to</a>
oa_cut_rows	Whether to use oa_cut_rows or not <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">oa_cut_rows</a>
oa_display_resource_file	Display resource file <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">oa_display_resource_file</a>
oa_display_resource_file_in_library	Whether to use display resource file in the tech library <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">oa_display_resource_file_in_library</a>

<b>oa_drc_fill_purpose</b>	<p>Whether to save drcFill shapes to gap_fill or drawing purpose. By default DEF routes with + SHAPE DRCFILL are mapped to the OA 'gapFill' purpose. Some OA techfiles do not have this purpose defined, and require these shapes be mapped to 'drawing' purpose. In that case, they get an additional internal attribute so they can round-trip back to DRCFILL shapes properly.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> gap_fill drawing</p> <p><b>Default:</b> gap_fill</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">oa_drc_fill_purpose</a></p>
<b>oa_full_layer_list</b>	<p>Whether to support full list of layer import</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">oa_full_layer_list</a></p>
<b>oa_full_path</b>	<p>Whether to use full path or not</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">oa_full_path</a></p>
<b>oa_inst_placed_if_none</b>	<p>Whether to map OA Placement status oacNonePlacementStatus of an instance to Placed(true)/ Unplaced(false).</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">oa_inst_placed_if_none</a></p>
<b>oa_lib_create_mode</b>	<p>Library creation method during write_db for newly created libraries</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none attach copy reference</p> <p><b>Default:</b> reference</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">oa_lib_create_mode</a></p>

oa_lock	
	<p>Whether to lock the OA database during read_db</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">oa_lock</a></p>
oa_logic_only_import	
	<p>Whether to run read_oa after init_design or not</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">oa_logic_only_import</a></p>
oa_new_lib_compress_level	
	<p>OA Database compression level</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">oa_new_lib_compress_level</a></p>
oa_pin_purpose	
	<p>Whether to set Pin Purpose as Pin or not</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">oa_pin_purpose</a></p>
oa_push_pin_constraint	
	<p>whether write_db to push interoperable pin constraint into its corresponding blackbox abstract cellview.</p> <p>Note: Interoperable pin constraint means pin constraints that are understood by Innovus, Virtuoso and PVS.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">oa_push_pin_constraint</a></p>
oa_silently_ignore_unsupported_vias	

	Whether read_db should issue messages about vias that are not supported in Innovus. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">oa_silently_ignore_unsupported_vias</a>
oa_text_purpose	Specify the purpose name that will be used when text labels (add_text) are written. <b>Type:</b> <a href="#">string</a> <b>Default:</b> drawing <b>Edit:</b> Yes <b>Reference:</b> <a href="#">oa_text_purpose</a>
oa_tie_net	tieHigh tieLow net names <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">oa_tie_net</a>
oa_update_mode	Whether to use (save/restore)OaDesign in update mode or not <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> false true auto <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">oa_update_mode</a>
oa_use_virtuoso_bindkey	Whether to use Virtuoso bind keys <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">oa_use_virtuoso_bindkey</a>
oa_use_virtuoso_color	Whether to use Virtuoso color and stipple <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">oa_use_virtuoso_color</a>
oa_view_sub_type	

	<p>Subtype of view of the OA design  <b>Type:</b> enum  <b>Enum Values:</b> vce vxl none  <b>Default:</b> vxl  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">oa_view_sub_type</a></p>
oa_write_mask_data_locked	<p>Whether to save colored shapes with locked attribute  <b>Type:</b> bool  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">oa_write_mask_data_locked</a></p>
oa_write_net_voltage	<p>Whether to allow write_db to write voltage information to the oaBitNet's voltage attribute  <b>Type:</b> bool  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">oa_write_net_voltage</a></p>
oa_write_relative_path	<p>Whether to save relative path in config file.  <b>Type:</b> bool  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">oa_write_relative_path</a></p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a>  <b>Type:</b> enum (root)  <b>Default:</b> ""  <b>Edit:</b> No</p>
obj_types	<p>object definitions  <b>Type:</b> obj(obj_type)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
opconds	

	Returns the information about the opconds in the design. <b>Type:</b> <a href="#">obj(opcond)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>opt_add_always_on_feed_through_buffers</b>	
	Activates adding Always On Feed Thru buffers <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_add_always_on_feed_through_buffers</a>
<b>opt_add_insts</b>	
	Enables adding of new instances <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_add_insts</a>
<b>opt_add_ports</b>	
	Enables adding ports for optimal buffering <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_add_ports</a>
<b>opt_all_end_points</b>	
	Enables the all end points optimization mode <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_all_end_points</a>
<b>opt_allow_only_cell_swapping</b>	
	Forces the post_route optimization to perform only same-size Vth swapping for timing improvements <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_allow_only_cell_swapping</a>
<b>opt_area_recovery</b>	

	<p>Enables area reclamation step</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> true false default</p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_area_recovery</a></p>
<b>opt_area_recovery_setup_target_slack</b>	
	<p>Specifies target slack value (in nano secs) for area and power reclaim during setup timing optimization</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_area_recovery_setup_target_slack</a></p>
<b>opt_concatenate_default_and_user_prefixes</b>	
	<p>Enables combining default prefix for instances(nets) with the prefix specified by opt_new_inst_prefix(opt_new_net_prefix)</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_concatenate_default_and_user_prefixes</a></p>
<b>opt_consider_routing_congestion</b>	
	<p>Enables routing congestion check at the post_route stage during optimization of setup, hold,drv, &amp; glitch. It also impacts post_cts hold fixing.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> auto false true</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_consider_routing_congestion</a></p>
<b>opt_constant_inputs</b>	
	<p>Force optimization of instances with constant inputs, even if it worsens objective gain</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_constant_inputs</a></p>
<b>opt_constant_nets</b>	

	Enables optimization of constant nets <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_constant_nets</a>
<b>opt_delete_insts</b>	
	Enables instance deletion on all paths <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_delete_insts</a>
<b>opt_detail_drv_failure_reason</b>	
	To enable printing detailed drv failure reason report file <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_detail_drv_failure_reason</a>
<b>opt_detail_drv_failure_reason_max_num_nets</b>	
	Specify how many violating nets printed <b>Type:</b> <a href="#">int</a> <b>Default:</b> 50 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_detail_drv_failure_reason_max_num_nets</a>
<b>opt_down_size_insts</b>	
	Enables instance downsizing <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_down_size_insts</a>
<b>opt_drv_margin</b>	
	Used for scaling max cap/max tran constraints <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_drv_margin</a>
<b>opt_enable_data_to_data_checks</b>	

	<p>enable library data to data checks during optimization for gigaopt</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> true false</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_enable_data_to_data_checks</a></p>
opt_enable_restructure	<p>Enables netlist restructuring</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_enable_restructure</a></p>
opt_fix_drv	<p>Enables fixing max cap/max tran violations on constrained nets</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_fix_drv</a></p>
opt_fix_drv_with_miller_cap	<p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_fix_drv_with_miller_cap</a></p>
opt_fix_fanout_load	<p>Enables fixing fanOut load violations</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_fix_fanout_load</a></p>
opt_fix_hold_allow_overlap	

	<p>Enables hold optimization to insert cells with overlaps when inadequate free space is available. The placement will then be legalized before ECO routing.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> auto false true</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_fix_hold_allow_overlap</a></p>
opt_fix_hold_allow_resize	<p>Enables the resizing capability inside hold optimization.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> false true</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_fix_hold_allow_resize</a></p>
opt_fix_hold_allow_setup_tns_degradation	<p>Allows setup total negative slack to degrade during hold optimization.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_fix_hold_allow_setup_tns_degradation</a></p>
opt_fix_hold_cells	<p>Provide a list of buffer &amp; delay cells to be used for hold buffering. The dont_use constraints for these cells will be ignored.</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_fix_hold_cells</a></p>
opt_fix_hold_ignore_path_groups	<p>Specifies path groups to be excluded in hold timing optimization</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_fix_hold_ignore_path_groups</a></p>
opt_fix_hold_lib_cells	

	<p>Provide a list of buffer &amp; delay cells to be used for hold buffering. The dont_use constraints for these cells will be ignored.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>opt_fix_hold_on_excluded_clock_nets</b>	
	<p>Do hold fixing on the excluded clock nets</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_fix_hold_on_excluded_clock_nets</a></p>
<b>opt_fix_hold_slack_threshold</b>	
	<p>Specifies target slack value (in nano secs) for hold timing optimization</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> -1000.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_fix_hold_slack_threshold</a></p>
<b>opt_fix_hold_verbose</b>	
	<p>Enables verbose information logging</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_fix_hold_verbose</a></p>
<b>opt_hier_add_antenna_cell</b>	
	<p>add antenna diode to interface load</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_hier_add_antenna_cell</a></p>
<b>opt_hier_opt_stage</b>	
	<p>Turn on default settings for hierarchical flows at different optimization stage.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> pre_cts post_cts unset</p> <p><b>Default:</b> unset</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_hier_opt_stage</a></p>
<b>opt_hier_trial_route_honor_read_only</b>	

	<p>trailRoute to honor partition or top read-only settings</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_hier_trial_route_honor_read_only</a></p>
opt_high_effort_cells	<p>Provide a list of cells to be used for high effort optimization. Dont-use and Dont-touch constraints for these cells will be ignored for high effort optimization.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_high_effort_cells</a></p>
opt_high_effort_lib_cells	<p>Provide a list of cells to be used for high effort optimization. Dont-use and Dont-touch constraints for these cells will be ignored for high effort optimization.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
opt_hold_target_slack	<p>Specifies target slack value (in nano secs) for hold timing optimization</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_hold_target_slack</a></p>
opt_honor_density_screen	<p>Control density screen</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_honor_density_screen</a></p>
opt_honor_fences	<p>Specifies that the timing optimization takes fences constraints into account. Placement of cells will be legalized within each fence.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_honor_fences</a></p>

opt_leakage_to_dynamic_ratio	
	<p>relative effort for leakage and dynamic power optimization in the range [0.0 - 1.0]</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 1.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_leakage_to_dynamic_ratio</a></p>
opt_max_density	
	<p>Specifies maximum area utilization</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.95</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_max_density</a></p>
opt_max_length	
	<p>Enables max length constraints in opt_design</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> -1.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_max_length</a></p>
opt_move_insts	
	<p>Enables moving instances while fixing setup violations</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_move_insts</a></p>
opt_multi_bit_flop_ignore_sdc	
	<p>ignore sdc check when do flop merge and split</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_multi_bit_flop_ignore_sdc</a></p>
opt_multi_bit_flop_opt	
	<p>specifies multi bit flop merge/split opt</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> false true mergeOnly splitOnly</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_multi_bit_flop_opt</a></p>

opt_new_inst_prefix	Prefix string for name of new instances <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_new_inst_prefix</a>
opt_new_net_prefix	Prefix string for name of new nets <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_new_net_prefix</a>
opt_pin_swapping	Enables pin swapping <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_pin_swapping</a>
opt_post_route_allow_overlap	Enables post_route optimization to insert cells with overlaps when inadequate free space is available. The placement will then be legalized before ECO routing. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_post_route_allow_overlap</a>
opt_post_route_area_reclaim	To enable area reclaim in post_route optimization <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> none setup_aware hold_and_setup_aware <b>Default:</b> none <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_post_route_area_reclaim</a>
opt_post_route_art_flow	

	<p>Enables optimizing the top-level interface logic for a hierarchical floorplan</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_post_route_art_flow</a></p>
<b>opt_post_route_check_antenna_rules</b>	
	<p>Allows optimization to check/ignore antenna rules in lefsafe swaps</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_post_route_check_antenna_rules</a></p>
<b>opt_post_route_drv_recovery</b>	
	<p>Enables post_route drv recovery in gigaopt.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> auto true false</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_post_route_drv_recovery</a></p>
<b>opt_post_route_fix_clock_drv</b>	
	<p>enables DRV fixing on clock net</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_post_route_fix_clock_drv</a></p>
<b>opt_post_route_fix_glitch</b>	
	<p>Enables glitch fixing in AAE flow</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_post_route_fix_glitch</a></p>
<b>opt_post_route_fix_si_transitions</b>	
	<p>Enables sislew fixing in AAE flow</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_post_route_fix_si_transitions</a></p>
<b>opt_post_route_report_si_transitions</b>	

	report sislew violations <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_post_route_report_si_transitions</a>
<b>opt_post_route_setup_recovery</b>	
	Enables post_route SI setup timing recovery in gigaopt. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> auto true false <b>Default:</b> auto <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_post_route_setup_recovery</a>
<b>opt_power_effort</b>	
	Effort level for power aware mode in optimization <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> none low high <b>Default:</b> none <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_power_effort</a>
<b>opt_pre_route_ndr_aware</b>	
	Provide a list of NDR names that will be used NDR-based optimization <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_pre_route_ndr_aware</a>
<b>opt_preserve_all_sequential</b>	
	Preserve sequential element during the simplify netlist optimization step <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_preserve_all_sequential</a>
<b>opt_preserve_hpin_function</b>	
	Enables preserving logical functions at hierarchical ports <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_preserve_hpin_function</a>

opt_rcp_all_endpoints	
	<p>To control whether to do TNS optimization in RCP  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_rcp_all_endpoints</a></p>
opt_rcp_delay_corner	
	<p>Name of delay corner to use for RCP.  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_rcp_delay_corner</a></p>
opt_rcp_generate_report	
	<p>To control whether to generate timing,DRVs reports in RCP  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_rcp_generate_report</a></p>
opt_rcp_input_dir	
	<p>Path to RCP input data directory.  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_rcp_input_dir</a></p>
opt_rcp_keep_tmp_dir	
	<p>To control whether to delete the RCP internal DB.directory  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_rcp_keep_tmp_dir</a></p>
opt_rcp_local_cpu	
	<p>Number of CPU to use in RCP.  <b>Type:</b> <a href="#">int</a>  <b>Default:</b> 1  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_rcp_local_cpu</a></p>

opt_rcp_log_dir	Path to RCP log file generated. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_rcp_log_dir</a>
opt_rcp_output_dir	Path to RCP output data directory. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_rcp_output_dir</a>
opt_rcp_post_synthesis_tcl	TCL plug-in script to be loaded in RCP after running synthesis inside RCP. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_rcp_post_synthesis_tcl</a>
opt_rcp_pre_read_db_tcl	TCL plug-in script to be loaded in RCP before loading the design. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_rcp_pre_read_db_tcl</a>
opt_rcp_pre_synthesis_tcl	TCL plug-in script to be loaded in RCP before running synthesis inside RCP. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_rcp_pre_synthesis_tcl</a>
opt_rcp_report_dir	Path to RCP reports data directory. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_rcp_report_dir</a>

<b>opt_rcp_synthesis_tcl</b>	
	TCL plug-in script to be loaded in RCP instead of the default RCP synthesis step defined. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_rcp_synthesis_tcl</a>
<b>opt_remove_redundant_insts</b>	
	Enables simplifying the netlist during optimization <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_remove_redundant_insts</a>
<b>opt_resize_flip_flops</b>	
	Enables FF resizing <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_resize_flip_flops</a>
<b>opt_resize_level_shifter_and_iso_insts</b>	
	Enables resizing of shifters and isolation instances <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_resize_level_shifter_and_iso_insts</a>
<b>opt_resize_power_switch_insts</b>	
	Enables resizing of power switch instances during optimization <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_resize_power_switch_insts</a>
<b>opt_setup_target_slack</b>	
	Specifies target slack value (in nano secs) for setup timing optimization <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_setup_target_slack</a>

opt_signoff_add_inst	
	<p>Specifies whether timing optimizer is allowed to add buffer/delay/inverter cell instances.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_add_inst</a></p>
opt_signoff_add_load	
	<p>Specifies whether Hold optimizer is allowed to add dummy cell instances</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_add_load</a></p>
opt_signoff_allow_skewing	
	<p>useful skew based setup opt</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_allow_skewing</a></p>
opt_signoff_along_route_buffering	
	<p>Allow buffer/inverter to be inserted along the route and not only at driver or sink terms.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_along_route_buffering</a></p>
opt_signoff_buffer_cell_list	
	<p>Specifies a list of buffer/delay cells that can be used for DRV and Hold optimizers, regardless of whether those cells have a "dont_use" attribute.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_buffer_cell_list</a></p>
opt_signoff_check_drv_from_hold_views	
	<p>consider DRVs from hold views</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_check_drv_from_hold_views</a></p>

opt_signoff_check_type	
	<p>Check type for path based analysis.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> early late both</p> <p><b>Default:</b> both</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_check_type</a></p>
opt_signoff_clock_cell_list	
	<p>Restricts the list of buffers/inverter/gating cells that are allowed to be used by ECO on the clock tree.</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_clock_cell_list</a></p>
opt_signoff_clock_max_level	
	<p>max level allowed for clock tree</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_clock_max_level</a></p>
opt_signoff_delete_inst	
	<p>delete buffer for optimization</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_delete_inst</a></p>
opt_signoff_disable_geometry_checks	
	<p>Performs Vth swapping without checking pins geometry.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_disable_geometry_checks</a></p>
opt_signoff_drv_margin	

	<p>Specifies a margin value by which ratio the drv check would be relaxed or tightened</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_drv_margin</a></p>
opt_signoff_eco_file_prefix	<p>Specifies the prefix name for the ECO files generated.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_eco_file_prefix</a></p>
opt_signoff_fix_clock_drv	<p>fix max_cap/max_tran violations on clock nets</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_fix_clock_drv</a></p>
opt_signoff_fix_data_drv	<p>fix max_cap/max_tran violations on data nets</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_fix_data_drv</a></p>
opt_signoff_fix_glitch	<p>fix nets with glitch</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_fix_glitch</a></p>
opt_signoff_fix_hold_allow_setup_optimization	<p>simultaneous hold and setup fixing</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_fix_hold_allow_setup_optimization</a></p>
opt_signoff_fix_hold_allow_setup_tns_degrade	

	<p>When active, the Setup Total Negative Slack can be degraded during Hold time violations fixing while still maintaining the Setup Worst Negative Slack in every Setup active views.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_fix_hold_allow_setup_tns_degrade</a></p>
opt_signoff_fix_hold_with_margin	<p>Specifies a slack margin value in nanoseconds for Hold time violations fixing. The purpose is to overfix any Hold violations by the amount of the margin value. This margin is not applied on nets that are already meeting the Hold target slack.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_fix_hold_with_margin</a></p>
opt_signoff_fix_ir_drop	<p>fix ir-drop hotspots</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_fix_ir_drop</a></p>
opt_signoff_fix_max_cap	<p>Enables max_cap violations fixing during DRV optimization.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_fix_max_cap</a></p>
opt_signoff_fix_max_transition	<p>Enables max_tran violations fixing during DRV optimization.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_fix_max_transition</a></p>
opt_signoff_fix_si_slew	

	<p>Performs SI Slew fixing during DRV fixing using resizing and buffering techniques.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_fix_si_slew</a></p>
opt_signoff_fix_xtalk	<p>Reduces the crosstalk on the net that violates the thresholds set by the user.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_fix_xtalk</a></p>
opt_signoff_hold_target_slack	<p>Specifies a target slack value in nanoseconds for hold timing optimize</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_hold_target_slack</a></p>
opt_signoff_hold_xtalk_delta_threshold	<p>Crosstalk delta delay threshold for selecting nets in hold timing views when running Xtalk fixing.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.3</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_hold_xtalk_delta_threshold</a></p>
opt_signoff_hold_xtalk_slack_threshold	<p>Slack threshold for selecting nets in hold timing views when running Xtalk fixing.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 1000.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_hold_xtalk_slack_threshold</a></p>
opt_signoff_ignore_drv_checks	<p>Ignores DRV checks during timing/area/power optimization.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_ignore_drv_checks</a></p>
opt_signoff_keep_tmp_files	

	To keep all the temporary files generated by D-MMMC and Tempus clients for debugging purposes. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_signoff_keep_tmp_files</a>
opt_signoff_legal_only	Enables/disables legal location checks during resizing and buffering <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_signoff_legal_only</a>
opt_signoff_load_cell_list	Specifies the list of load cells <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_signoff_load_cell_list</a>
opt_signoff_max_cap_margin	Specifies the ratio by which the max_cap check would be relaxed or tightened <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_signoff_max_cap_margin</a>
opt_signoff_max_paths	Specifies how many paths are getting retimed for ECO DB generation in PBA mode. <b>Type:</b> <a href="#">int</a> <b>Default:</b> -1 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_signoff_max_paths</a>
opt_signoff_max_runtime	If set to a positive value, would restrict the command runtime by that value, in minutes. <b>Type:</b> <a href="#">int</a> <b>Default:</b> 0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_signoff_max_runtime</a>
opt_signoff_max_slack	

	<p>Specifies the maximum GBA slack value to be used when selecting paths to be retimed for ECO DB generation in PBA mode.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_max_slack</a></p>
opt_signoff_max_transition_margin	<p>Specifies the ratio by which the max_tran check would be relaxed or tightened</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_max_transition_margin</a></p>
opt_signoff_num_report_paths	<p>Number of paths printed after signoff timing analysis per view</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 50</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_num_report_paths</a></p>
opt_signoff_nworst	<p>Specifies the number of paths to be retimed per endpoints for ECO DB generation in PBA mode.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> -1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_nworst</a></p>
opt_signoff_optimize_core_only	<p>Enables the tool to optimize timing or recover area/power only on register to register paths.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_optimize_core_only</a></p>
opt_signoff_optimize_replicated_modules	

	<p>Allows the tool to perform timing optimization inside replicated hierarchies while generating only one ECO file per sets of clones. The cell name of the replicated hierarchies have to be listed in a file pointed by the opt_signoff_partition_list_file option.</p> <p><b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_signoff_optimize_replicated_modules</a></p>
<b>opt_signoff_optimize_sequential_cells</b>	
	<p>Specifies whether the timing/area/power optimizer is allowed to optimize sequential cells.</p> <p><b>Type:</b> <a href="#">bool</a>  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_signoff_optimize_sequential_cells</a></p>
<b>opt_signoff_partition_list_file</b>	
	<p>File containing list of partitions in the design</p> <p><b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_signoff_partition_list_file</a></p>
<b>opt_signoff_pba_effort</b>	
	<p>When enabling "high" effort mode, all the optimization engines will perform more aggressive timing closure or area/power recovery with respect to PBA timing and the expectation is to get better quality of results.</p> <p><b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> medium high  <b>Default:</b> medium  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_signoff_pba_effort</a></p>
<b>opt_signoff_post_sta_tcl</b>	
	<p>File containing the TCL code that will be executed immediately after signoff timing analysis per view</p> <p><b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_signoff_post_sta_tcl</a></p>
<b>opt_signoff_power_aware</b>	

	<p>power awareness in all optimizers and transforms</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_power_aware</a></p>
opt_signoff_power_opt_focus	<p>focus for power optimization</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> total leakage dynamic</p> <p><b>Default:</b> total</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_power_opt_focus</a></p>
opt_signoff_pre_sta_tcl	<p>File containing the TCL code that will be executed immediately prior to signoff timing analysis per view</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_pre_sta_tcl</a></p>
opt_signoff_prefix	<p>Specifies the prefix to be assigned to the new instances inserted.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ESO</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_prefix</a></p>
opt_signoff_preserve_filler	<p>To enable preserve and restore of fillers</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_preserve_filler</a></p>
opt_signoff_read_eco_opt_db	<p>Path of directory where ECO Timing DB files must be loaded from.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_read_eco_opt_db</a></p>

opt_signoff_read_irdrop_db	
	<p>Path of directory where command debug_irdrop generated IR drop DB files are kept</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_read_irdrop_db</a></p>
opt_signoff_resize_inst	
	<p>enable/disable resizing transform</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_resize_inst</a></p>
opt_signoff_retime	
	<p>To enable PBA-based timing report and optimization for all optimizers.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none aocv path_slew_propagation aocv_path_slew_propagation</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_retime</a></p>
opt_signoff_routing_congestion_aware	
	<p>Check routing congestion before adding buffers</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_routing_congestion_aware</a></p>
opt_signoff_select_drv_net_file	
	<p>list of nets to be optimized during DRV fixing</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_select_drv_net_file</a></p>
opt_signoff_select_hold_endpoints	
	<p>select end points for hold fixing</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_select_hold_endpoints</a></p>

opt_signoff_select_setup_endpoints	<p>select end points for setup fixing</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_select_setup_endpoints</a></p>
opt_signoff_set_hold_endpoints_margin	<p>specify end point specific margin for hold fixing</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_set_hold_endpoints_margin</a></p>
opt_signoff_set_setup_endpoints_margin	<p>specify end point specific margin for setup fixing</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_set_setup_endpoints_margin</a></p>
opt_signoff_setup_recovery	<p>Forces Setup fixing to perform Setup timing recovery by using Vth swapping only. Useful feature to recover timing degradation after large ECO change during Power optimization.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_setup_recovery</a></p>
opt_signoff_setup_target_slack	<p>Specifies a target slack value in nanoseconds for setup timing optimize</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">opt_signoff_setup_target_slack</a></p>
opt_signoff_setup_xtalk_delta_threshold	

	Crosstalk delta delay threshold for selecting nets in setup timing views when running Xtalk fixing. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.3 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_signoff_setup_xtalk_delta_threshold</a>
opt_signoff_setup_xtalk_slack_threshold	Slack threshold for selecting nets in setup timing views when running Xtalk fixing. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 1000.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_signoff_setup_xtalk_slack_threshold</a>
opt_signoff_skip_drv_net_file	list of nets to be excluded during DRV fixing <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_signoff_skip_drv_net_file</a>
opt_signoff_swap_inst	Enables/disables VT swap resizing. Setup/leakage optimizers do not honor this option and always perform VT-swapping. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_signoff_swap_inst</a>
opt_signoff_verbose	Specifies whether the command should output log file reporting with verbosity or not. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_signoff_verbose</a>
opt_signoff_write_eco_opt_db	Path of directory where ECO Timing DB files are saved. <b>Type:</b> <a href="#">string</a> <b>Default:</b> ecoTimingDB <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_signoff_write_eco_opt_db</a>

opt_target_based_opt_file	Target based opt input file <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_target_based_opt_file</a>
opt_target_based_opt_file_only	Use data from target based opt file for optimization <b>Type:</b> enum <b>Enum Values:</b> false true <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_target_based_opt_file_only</a>
opt_target_based_opt_hold_file	Target based opt input file for hold <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_target_based_opt_hold_file</a>
opt_tied_inputs	Force optimization of instances with inputs tied together, even if it worsens objective gain <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_tied_inputs</a>
opt_time_design_compress_reports	save reports in compressed format <b>Type:</b> bool <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_time_design_compress_reports</a>
opt_time_design_expanded_view	To report expanded views in time_design <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_time_design_expanded_view</a>

opt_time_design_num_paths	
	<p>Report specified number of paths in time_design  <b>Type:</b> int  <b>Default:</b> 50  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_time_design_num_paths</a></p>
opt_time_design_report_net	
	<p>To report net delays in time_design  <b>Type:</b> bool  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_time_design_report_net</a></p>
opt_unfix_clock_insts	
	<p>Enables unfixing clock instances flow  <b>Type:</b> bool  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_unfix_clock_insts</a></p>
opt_useful_skew	
	<p>Enables triggering the skew_clock command from within opt_design  <b>Type:</b> bool  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_useful_skew</a></p>
opt_useful_skew_ccopt	
	<p>Effort for useful skew optimization within ccopt_design  <b>Type:</b> enum  <b>Enum Values:</b> none standard extreme  <b>Default:</b> standard  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_useful_skew_ccopt</a></p>
opt_useful_skew_delay_pre_cts	
	<p>delaying mode in pre_cts  <b>Type:</b> bool  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">opt_useful_skew_delay_pre_cts</a></p>

opt_useful_skew_macro_only	skew hard blocks <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_useful_skew_macro_only</a>
opt_useful_skew_max_allowed_delay	max allowed skewing delay, unit is 'ns' <b>Type:</b> <a href="#">double</a> <b>Default:</b> 1.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_useful_skew_max_allowed_delay</a>
opt_useful_skew_min_allowed_delay	min allowed skewing delay, unit is 'ns' <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_useful_skew_min_allowed_delay</a>
opt_useful_skew_no_boundary	consider boundary sequential elements <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_useful_skew_no_boundary</a>
opt_useful_skew_post_route	Enables useful skew optimization during post_route timing optimization. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_useful_skew_post_route</a>
opt_useful_skew_pre_cts	Enables useful skew optimization during pre_cts timing optimization. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">opt_useful_skew_pre_cts</a>

package_objects	
	<p>Short-cut for [get_db current_design .package_objects]</p> <p><b>Type:</b> <a href="#">obj(package_object)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
partition_floorplan_export	
	<p>Export setting</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> macro special_route pin_constraint</p> <p><b>Default:</b> special_route</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">partition_floorplan_export</a></p>
partition_floorplan_import	
	<p>Import setting</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> macro special_route pin_constraint</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">partition_floorplan_import</a></p>
partitions	
	<p>Short-cut for [get_db current_design .partitions]</p> <p><b>Type:</b> <a href="#">obj(partition)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
pg_base_pins	
	<p>All the base_pins in all the base_cells.</p> <p><b>Type:</b> <a href="#">obj(pg_base_pin)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
pg_nets	
	<p>Short-cut for [get_db current_design .pg_nets]. List of power/ground nets in the design. This include physical-only PG nets, and Verilog supply0/supply1 nets. Note that Verilog nets assigned to 1'b0/1'b1 are returned by the nets attribute, not the pg_nets attribute.</p> <p><b>Type:</b> <a href="#">obj(net)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

pg_pins	
	<p>Short-cut for [get_db current_design .pg_pins].</p> <p><b>Type:</b> <a href="#">obj(pg_pin)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
phys_insts	
	<p>Short-cut for [get_db current_design .phys_insts]</p> <p><b>Type:</b> <a href="#">obj(inst)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
pin_blockages	
	<p>Short-cut for [get_db current_design .pin_blockages]</p> <p><b>Type:</b> <a href="#">obj(pin_blockage)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
pin_groups	
	<p>Short-cut for [get_db current_design .pin_groups]</p> <p><b>Type:</b> <a href="#">obj(pin_group)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
pin_guides	
	<p>Short-cut for [get_db current_design .pin_guides]</p> <p><b>Type:</b> <a href="#">obj(pin_guide)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
pins	
	<p>Short-cut for [get_db current_design .pins]</p> <p><b>Type:</b> <a href="#">obj(pin)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
place_blockages	
	<p>Short-cut for [get_db current_design .place_blockages]</p> <p><b>Type:</b> <a href="#">obj(place_blockage)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

place_cell_edge_spacing	<p>List of cell edge-type spacing values from LEF CELLEDGESPACINGTABLE or OA techfile that affects the placer. It specifies the min-spacing between different edge-types of std-cells, in a list format: {cell_edge_type1 cell_edge_type2 spacing}. The edge-type names match the base_cell's right_edge_type and left_edge_type attribute values.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p> <p><b>Reference:</b> <a href="#">place_cell_edge_spacing</a></p>
place_design_floorplan_mode	<p>run placement in floorplan mode</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_design_floorplan_mode</a></p>
place_design_refine_place	<p>if set to false, calls to refinePlace from other apps (such as place_opt_design, opt_design) will not run refinePlace</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_design_refine_place</a></p>
place_detail_activity_power_driven	<p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_activity_power_driven</a></p>
place_detail_allow_border_pin_abut	<p>allow instance abut with its neighbors when it has pins near by the cell boundary</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_allow_border_pin_abut</a></p>
place_detail_check_cut_spacing	

	<p>Check via cut spacing during DRC checking</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_check_cut_spacing</a></p>
<b>place_detail_check_inst_space_group</b>	
	<p>check inst space group</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_check_inst_space_group</a></p>
<b>place_detail_check_route</b>	
	<p>do DRV checks against FIXED wires during legalization, along with preroutes</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_check_route</a></p>
<b>place_detail_color_aware_legal</b>	
	<p>enable adjacent cell color conflict check in legalization</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_color_aware_legal</a></p>
<b>place_detail_context_aware_legal</b>	
	<p>specify the types of cell context rules the placer needs to honor. The argument values [optional, required, user ignore_soft] can be used separately or combined, but they are exclusive to all   none (default=all)</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none all optional required user ignore_soft</p> <p><b>Default:</b> all</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_context_aware_legal</a></p>
<b>place_detail_eco_max_distance</b>	

	<p>specify max distance (in micron) for refinePlace ECO mode  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 0.0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_detail_eco_max_distance</a></p>
place_detail_eco_priority_insts	<p>select instance priority for refinePlace ECO mode  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> placed fixed eco  <b>Default:</b> placed  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_detail_eco_priority_insts</a></p>
place_detail_fixed_shifter	<p>mark shifters FIXED once placed  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_detail_fixed_shifter</a></p>
place_detail_honor_inst_pad	<p>honor padding from set_inst_padding in detail placement  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_detail_honor_inst_pad</a></p>
place_detail_io_pin_blockage	<p>ioPins from top-level are treated as pre-routes during DRV checks in legalization  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_detail_io_pin_blockage</a></p>
place_detail_irdrop_aware_effort	<p>selects which IR drop optimization effort level to use during refinePlace  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> none low medium high  <b>Default:</b> none  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_detail_irdrop_aware_effort</a></p>

place_detail_legalization_inst_gap	
	<p>minimum gap between instances (unit sites)</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_legalization_inst_gap</a></p>
place_detail_m3_stripe_push_down	
	<p>Width threshold in site-units for 'virtual' push-down of M3 stripe to M2 for M1 pin-access.</p> <p>Value of 0 means all M3 stripes will be pushed-down.</p> <p><b>Type:</b> int</p> <p><b>Default:</b> -1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_m3_stripe_push_down</a></p>
place_detail_m3_stripe_shrink	
	<p>Shrink the virtual M2 stripe (see spgM3StripePushDown) by given total site units, splitting value to each side, starting on left. e.g. value of 1 shrinks by 1 site on left, 2 shrinks by 1 site on each side, value of 3 shrinks 2 sites on left and 1 on right.</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_m3_stripe_shrink</a></p>
place_detail_max_shifter_column_depth	
	<p>maximum distance from vertical power domain boundary that a shifter can be placed</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 9999.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_max_shifter_column_depth</a></p>
place_detail_max_shifter_depth	
	<p>maximum distance from a horizontal or vertical power domain boundary that a shifter can be placed</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 9999.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_max_shifter_depth</a></p>
place_detail_max_shifter_row_depth	

	maximum distance from a horizontal power domain boundary that a shifter can be placed <b>Type:</b> <a href="#">double</a> <b>Default:</b> 9999.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_detail_max_shifter_row_depth</a>
place_detail_no_filler_without_implant	there is no cell which has no implant obs <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_detail_no_filler_without_implant</a>
place_detail_pad_fixed_insts	honor cell-padding for FIXED instances in refinePlace <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_detail_pad_fixed_insts</a>
place_detail_pad_physical_cells	padding overlap with physical cells would be honored <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_detail_pad_physical_cells</a>
place_detail_preroute_as_obs	specify layers on which preroute are taken as OBS <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_detail_preroute_as_obs</a>
place_detail_preserve_routing	do not delete routed wires during refinePlace <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_detail_preserve_routing</a>
place_detail_remove_affected_routing	

	<p>delete only wires whose nets were touched due to moved cells</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_remove_affected_routing</a></p>
<b>place_detail_sdp_alignment_in_refine</b>	
	<p>call sdp alignment in every refinePlace</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_sdp_alignment_in_refine</a></p>
<b>place_detail_swap_eeq_cells</b>	
	<p>replace master cells by its EEQ cell during legalization, to keep max-dist move low</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_swap_eeq_cells</a></p>
<b>place_detail_use_check_drc</b>	
	<p>Use FGC based DRC engine in legalization</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_use_check_drc</a></p>
<b>place_detail_use_diffusion_transition_fill</b>	
	<p>insert OD transition filler in 1X gap</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_use_diffusion_transition_fill</a></p>
<b>place_detail_use_gate_array_filler_groups</b>	
	<p>filler cell insts will only be replaced by logic insts that belong to same GA groups.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_use_gate_array_filler_groups</a></p>
<b>place_detail_use_no_diffusion_one_site_filler</b>	

	<p>override -fillerGapMinGap to 0 and all source-drain spacing rule to 1 site during legalizing</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_use_no_diffusion_one_site_filler</a></p>
place_detail_wire_length_opt_effort	<p>selects which wire-length optimization effort level to use during refinePlace</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none medium high</p> <p><b>Default:</b> medium</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_detail_wire_length_opt_effort</a></p>
place_global_activity_power_driven	<p>identifies and constrains power-critical nets to reduce switching power</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> false true</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_global_activity_power_driven</a></p>
place_global_activity_power_driven_effort	<p>-place_global_activity_power_driven_effort mode</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> standard high</p> <p><b>Default:</b> standard</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_global_activity_power_driven_effort</a></p>
place_global_auto_blockage_in_channel	<p>Placement will (temporarily) block channels between areas with limited routing capacity</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none soft partial</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_global_auto_blockage_in_channel</a></p>
place_global_clock_gate_aware	

	<p>find better placement for clock gating elements towards the center of gravity for fanout</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_global_clock_gate_aware</a></p>
<p><b>place_global_clock_power_driven</b></p>	
	<p>clock power driven</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_global_clock_power_driven</a></p>
<p><b>place_global_clock_power_driven_effort</b></p>	
	<p>-place_global_clock_power_driven_effort mode</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> low standard high</p> <p><b>Default:</b> low</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_global_clock_power_driven_effort</a></p>
<p><b>place_global_cong_effort</b></p>	
	<p>level of effort for congestion driven global placer</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> low medium high extreme auto</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_global_cong_effort</a></p>
<p><b>place_global_cpg_effort</b></p>	
	<p>level of effort for CPG</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> low medium high</p> <p><b>Default:</b> low</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">place_global_cpg_effort</a></p>
<p><b>place_global_cpg_file</b></p>	

	<b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_global_cpg_file</a>
<b>place_global_enable_distributed_place</b>	
	enable distributed placement platform <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_global_enable_distributed_place</a>
<b>place_global_ignore_scan</b>	
	ignore scan net during placement <b>Type:</b> enum <b>Enum Values:</b> true 1 false 0 auto <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_global_ignore_scan</a>
<b>place_global_ignore_spare</b>	
	discard spare cell connections during global placement <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_global_ignore_spare</a>
<b>place_global_max_density</b>	
	placement strives to not let density exceed given value, in any part of design <b>Type:</b> double <b>Default:</b> -1.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_global_max_density</a>
<b>place_global_module_aware_spare</b>	
	Spare insts are placed randomly along with the containing module's insts <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_global_module_aware_spare</a>
<b>place_global_module_padding</b>	

	define the padding factor for the given module to reduce the local density and congestion <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_global_module_padding</a>
place_global_place_io_pins	place IO Pins concurrently with std.cell placement, and do layer assignment <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_global_place_io_pins</a>
place_global_reorder_scan	turn on reorder scan during placement <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_global_reorder_scan</a>
place_global_sdp_alignment	ensure SDP alignment during placement <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_global_sdp_alignment</a>
place_global_sdp_place	honor SDP groups and places SDP cells closely during placement <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> false true <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_global_sdp_place</a>
place_global_soft_guide_strength	level of effort for user defined softGuide for global placer <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> low medium high <b>Default:</b> low <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_global_soft_guide_strength</a>

place_global_timing_effort	
	<p>level of effort for timing driven global placer  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> medium high  <b>Default:</b> medium  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_global_timing_effort</a></p>
place_global_uniform_density	
	<p>enable even cell distribution for designs with less than 70% utilization  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> false true  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_global_uniform_density</a></p>
place_hard_fence	
	<p>honor fence and region constraints in refinePlace  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_hard_fence</a></p>
place_opt_post_place_tcl	
	<p>a tcl script to be sourced after initial placement and before preCTS optimization in place_opt_design  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_opt_post_place_tcl</a></p>
place_opt_run_global_place	
	<p>place opt run global place  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> none seed full  <b>Default:</b> full  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_opt_run_global_place</a></p>
place_sdp_clock_location	

	<p>ICG cell location  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> center  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_sdp_clock_location</a></p>
place_sdp_disable_extend_core	<p>disable the extended core flag  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_sdp_disable_extend_core</a></p>
place_sdp_fix_overlap_column_cell	<p>-resolve_overlap_column_cell {cell...}. Use empty string to reset the value  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_sdp_fix_overlap_column_cell</a></p>
place_sdp_fix_overlap_row_cell	<p>-resolve_overlap_row_cell {cell...}. Use empty string to reset the value  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_sdp_fix_overlap_row_cell</a></p>
place_sdp_honor_orient	<p>honor user specified orient during legalization  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_sdp_honor_orient</a></p>
place_sdp_legalization	<p>Specify fixed corner of sdp box during legalizing sdp instance  <b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> NONE SW SE NW NE AUTO  <b>Default:</b> NONE  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">place_sdp_legalization</a></p>
place_sdp_max_move_action	

	<pre>-max_move_action {leave_overlap   delete_sdp_group   create_inst_group}</pre> <b>Type:</b> enum <b>Enum Values:</b> leave_overlap delete_sdp_group create_inst_group <b>Default:</b> create_inst_group <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_sdp_max_move_action</a>
place_sdp_max_move_distance	<pre>max sdp group move distance, default is half perimeter of the core box</pre> <b>Type:</b> double <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_sdp_max_move_distance</a>
place_sdp_num_column	<pre>number of column for sdp group</pre> <b>Type:</b> int <b>Default:</b> 2 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_sdp_num_column</a>
place_sdp_place_report	<pre>Output a detailed sdp placement data. Use empty string to reset to no output</pre> <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_sdp_place_report</a>
place_sdp_pre_fixed_cells_blockage_direction	<pre>Specify the direction when covering preplaced std cells using placement blockages</pre> <b>Type:</b> enum <b>Enum Values:</b> NONE X Y <b>Default:</b> NONE <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_sdp_pre_fixed_cells_blockage_direction</a>
place_spare_update_timing_graph	<pre>update timing graph during place_spare_modules</pre> <b>Type:</b> bool <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">place_spare_update_timing_graph</a>

plan_design_boundary_place	
	<p>Places macros along the core boundary for chip and block designs.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">plan_design_boundary_place</a></p>
plan_design_cong_aware	
	<p>Estimates the congestion for the floorplan after macro placement.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">plan_design_cong_aware</a></p>
plan_design_domain	
	<p>Format: -domain {{PD1 &lt;value1&gt; net1} {PD2 &lt;value2&gt; net2}..}</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">plan_design_domain</a></p>
plan_design_effort	
	<p>effort high will perform std cell placement while doing HM placement</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> medium high</p> <p><b>Default:</b> high</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">plan_design_effort</a></p>
plan_design_fence_spacing	
	<p>Specifies the spacing between adjacent fences.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> -1.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">plan_design_fence_spacing</a></p>
plan_design_fix_placed_macros	
	<p>Marks all placed macros as FIXED after running plan_design.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">plan_design_fix_placed_macros</a></p>

plan_design_honor_orientation	Honor original macro orientation <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">plan_design_honor_orientation</a>
plan_design_incremental	Does incremental macro placement <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">plan_design_incremental</a>
plan_design_keep_guide	-plan_design_keep_guide {0 1} <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">plan_design_keep_guide</a>
plan_design_legalize	Legalize macro location, Remove macro overlap <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">plan_design_legalize</a>
plan_design_macro_padding_factor	Specifies the macro padding factor to be used in congestion estimation. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 6.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">plan_design_macro_padding_factor</a>
plan_design_macro_spacing	Specifies the spacing between adjacent hard macros. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">plan_design_macro_spacing</a>

plan_design_minimum_macro_to_core_space	
	<p>Specifies the minimum spacing between macro and core boundary.</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">plan_design_minimum_macro_to_core_space</a></p>
plan_design_rail_model	
	<p>Select rail model: virtual/existing.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> virtual existing</p> <p><b>Default:</b> existing</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">plan_design_rail_model</a></p>
plan_design_total_power	
	<p>total power defined by user.</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">plan_design_total_power</a></p>
plan_design_use_guide_boundary	
	<p>Specifies the macro placement behavior in guide</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> none guide fence</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">plan_design_use_guide_boundary</a></p>
plan_design_utilization	
	<p>Specifies the target utilization for generated floorplan guides</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 0.75</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">plan_design_utilization</a></p>
port_shapes	
	<p>Short-cut for [get_db current_design .port_shapes]</p> <p><b>Type:</b> obj(port_shape)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

ports

Short-cut for [get\_db current\_design .ports]

**Type:** [obj\(port\)\\*](#)

**Default:** ""

**Edit:** No

power\_analysis\_temperature

Sets the temperature for static power calculation. If not set, then uses the current opcond temperature

**Type:** [double](#)

**Default:** no\_value

**Edit:** Yes

**Reference:** [power\\_analysis\\_temperature](#)

power\_average\_rise\_fall\_cap

When set to true, the software uses the average of rise and fall capacitance from the liberty file.

**Type:** [bool](#)

**Default:** false

**Edit:** Yes

**Reference:** [power\\_average\\_rise\\_fall\\_cap](#)

power\_bulk\_pins

Defines power and ground bulk LEF pins for the design.

**Type:** [string](#)

**Default:** ""

**Edit:** Yes

**Reference:** [power\\_bulk\\_pins](#)

power\_clock\_source\_as\_clock

Specifies to use the correct clock frequency for activity calculation.

**Type:** [bool](#)

**Default:** false

**Edit:** Yes

**Reference:** [power\\_clock\\_source\\_as\\_clock](#)

power\_constant\_override

	<p>Specifies to give higher precedence to propagated constants defined using the set_case_analysis command.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_constant_override</a></p>
power_corner	<p>Defines the library corner (for non-MMMC setup).</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_corner</a></p>
power_create_driver_db	<p>Specifies to determine all the drivers/receivers on the ground net.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_create_driver_db</a></p>
power_current_generation_method	<p>choose avg or peak current generation method</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> avg</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_current_generation_method</a></p>
power_db_name	<p>Specifies the name of the binary power database file ( filename.db ).</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_db_name</a></p>
power_decap_cell_list	<p>Specifies the physical only cells, such as decap cells, to include in the power report.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_decap_cell_list</a></p>
power_default_frequency	

	<p>Specifies to set the default frequency in the MHz unit for net not annotated by TWF.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> -1.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_default_frequency</a></p>
power_default_slew	<p>Specifies to set the default slew in the ns unit for net not annotated by TWF.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_default_slew</a></p>
power_default_supply_voltage	<p>Specifies to set a default voltage for power nets in a scenario where the power engine cannot determine the voltage of these nets.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_default_supply_voltage</a></p>
power_disable_clock_gate_clipping	<p>Specifies to enable clock gate output clipping so that the output transition density of an ICG cell does not exceed the input clock pin transition density.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_disable_clock_gate_clipping</a></p>
power_disable_leakage_scaling	<p>Specifies to exclude leakage power during scaling factor computation when target power is specified using the set_power command.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_disable_leakage_scaling</a></p>
power_disable_static	

	<p>When set to true in the dynamic vector-based or dynamic vectorless flows, the command performs only dynamic analysis and turns-off static power calculation.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_disable_static</a></p>
power_distributed_setup	<p>Specifies a file containing the customized setup details for running power analysis in the distributed mode.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_distributed_setup</a></p>
power_domain_based_clipping	<p>Determines the frequency to be used to clip propagated activity that is too high.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_domain_based_clipping</a></p>
power_domains	<p>Short-cut for [get_db current_design .power_domains]</p> <p><b>Type:</b> <a href="#">obj(power_domain)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
power_dynamic_power_view	<p>Specifies a separate dynamic analysis view for power calculation.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_dynamic_power_view</a></p>
power_dynamic_vectorless_ranking_methods	<p>choose ranking options from: load, slack, clock and vector_activity</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_dynamic_vectorless_ranking_methods</a></p>
power_enable_auto_mapping	

	<p>Specifies to automatically perform instance name mapping between the RTL netlist and GATE level netlist.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_enable_auto_mapping</a></p>
power_enable_duty_propagation_with_global_activity	<p>Specifies to propagate duty cycle with the global switching activity setting for all data nets in the dynamic vectorless analysis flow.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_enable_duty_propagation_with_global_activity</a></p>
power_enable_dynamic_scaling	<p>Enables set_power scaling for dynamic power analysis.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_enable_dynamic_scaling</a></p>
power_enable_generated_clock	<p>Specifies to get generated clock frequency during activity propagation for static power analysis.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_enable_generated_clock</a></p>
power_enable_input_net_power	<p>Specifies to calculate the switching power of input nets.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_enable_input_net_power</a></p>
power_enable_pba_for_tempus_pi	

	<p>ensure path based timing analysis in tempus-pi flow.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_enable_pba_for_tempus_pi</a></p>
power_enable rtl dynamic vector based	<p>Specifies to take an RTL or partial VCD/FSDB file as input and use that for dynamic vector-based flow.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_enable rtl dynamic vector based</a></p>
power_enable scan report	<p>enable scan report automatical generation</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_enable_scan_report</a></p>
power_enable state propagation	<p>enable vectorless state propagation dynamic analysis</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_enable_state_propagation</a></p>
power_enable tempus pi	<p>enable timing critical path analysis in state propagation based vectorless flow.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_enable_tempus_pi</a></p>
power_enhanced_blackbox_avg	<p>Specifies to use the average toggle rate of related inputs for enhanced blackbox propagation.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_enhanced_blackbox_avg</a></p>

power_enhanced_blackbox_max	
	<p>Specifies to use the maximum toggle rate of related inputs for enhanced blackbox propagation.</p> <p><b>Type:</b> <code>bool</code>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">power_enhanced_blackbox_max</a></p>
power_fanout_limit	
	<p>Specifies the fanout limit for nets.</p> <p><b>Type:</b> <code>int</code>  <b>Default:</b> -1  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">power_fanout_limit</a></p>
power_from_x_transition_factor	
	<p>activity count for x to 0/1 transition</p> <p><b>Type:</b> <code>double</code>  <b>Default:</b> 0.5  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">power_from_x_transition_factor</a></p>
power_from_z_transition_factor	
	<p>activity count for z to 0/1 transition</p> <p><b>Type:</b> <code>double</code>  <b>Default:</b> 0.25  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">power_from_z_transition_factor</a></p>
power_generate_current_for_rail	
	<p>Generates current files for the specified rail.</p> <p><b>Type:</b> <code>string</code>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">power_generate_current_for_rail</a></p>
power_generate_static_report_from_state_propagation	
	<p>generate static report from state propagation flow</p> <p><b>Type:</b> <code>bool</code>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">power_generate_static_report_from_state_propagation</a></p>

power_grid_libraries	<p>Specifies the name of the Cadence power cell libraries ( .cl ).</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_grid_libraries</a></p>
power_handle_glitch	<p>A transition is defined as a glitch when the time difference between two sequential toggles are less than half of the rise transition time + fall transition time in the vector-based static power calculation.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_handle_glitch</a></p>
power_handle_tristate	<p>When set to true , all tristate device enable pin values will be taken into account when determining the propagation of the activity through tristate gates.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_handle_tristate</a></p>
power_hier_delimiter	<p>Specifies the hierarchical delimiter in the DEF file. The default hierarchical delimiter is a forward slash ( / ) but can be changed by setting the -hierDelimiter parameter.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_hier_delimiter</a></p>
power_honor_combinational_logic_on_clock_net	<p>Specifies the behavior of combination logic on clock net.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_honor_combinational_logic_on_clock_net</a></p>
power_honor_negative_energy	

	A value of true specifies that Voltus will keep negative internal energy numbers from the .lib internal power table. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_honor_negative_energy</a>
power_honor_net_activity	honor net activity from activity file <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_honor_net_activity</a>
power_ignore_control_signals	A value of true specifies that control signals will be ignored when propagating activity. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_ignore_control_signals</a>
power_ignore_data_phase_for_clock	<b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_ignore_data_phase_for_clock</a>
power_ignore_end_toggles_in_profile	ignore toggles on end boundary in profiler analysis <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_ignore_end_toggles_in_profile</a>
power_ignore_glitches_at_same_time_stamp	Specifies to ignore glitches at the same transient time in the vector-based static and dynamic power analysis flow. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_ignore_glitches_at_same_time_stamp</a>

power_ignore_inout_pin_cap	
	<p>When set to true , ignores the bidirectional pin capacitances ( direction : inout ) defined for I/O cells in the .lib file, when calculating switching power and internal power.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_ignore_inout_pin_cap</a></p>
power_include_file	
	<p>Used for adding additional setting for power analysis</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_include_file</a></p>
power_include_initial_x_transitions	
	<p>Controls how the initial X state toggle should be counted.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_include_initial_x_transitions</a></p>
power_include_sequential_clock_pin_power	
	<p>Reports the clock pin power of flip-flops as part of the clock network power.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_include_sequential_clock_pin_power</a></p>
power_intent_allow_back_to_back_isolation	
	<p>Supports back-to-back isolation insertion along cross-domain net based on power intent ISO rule</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_intent_allow_back_to_back_isolation</a></p>
power_intent_allow_nested_default_domain	

	Allows a non-default power domain member to be logically nested in a default power domain <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_intent_allow_nested_default_domain</a>
power_intent_allow_power_domain_min_gap_zero	 <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_intent_allow_power_domain_min_gap_zero</a>
power_intent_assume_iso_enable_pin_is_always_on	To mark all Isolation cell's enable pin as always on <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_intent_assume_iso_enable_pin_is_always_on</a>
power_intent_check_all_nets_for_domain_crossing	Checks all the nets for domain crossings <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_intent_check_all_nets_for_domain_crossing</a>
power_intent_do_not_use_top_domain_for_port_voltage	Controls voltage using top fterm domain for IO pin voltage <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_intent_do_not_use_top_domain_for_port_voltage</a>
power_intent_honor_power_domain_for_domain_crossing_route	to handle nets belong to multiple power domains <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_intent_honor_power_domain_for_domain_crossing_route</a>
power_intent_honor_power_domain_for_intra_domain_route	

	To route intra-power domain nets only within their power domains <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_intent_honor_power_domain_for_intra_domain_route</a>
power_intent_include_dot_lib_related_pg_pin	Honors timing library related PG pins <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_intent_include_dot_lib_related_pg_pin</a>
power_intent_share_well_always_on_buffering_support	<b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_intent_share_well_always_on_buffering_support</a>
power_intent_use_cpf_global_connect_for_always_on_buffer	Honors connection specs for AO buffer based on the power intent rules <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_intent_use_cpf_global_connect_for_always_on_buffer</a>
power_intent_use_cpf_global_connect_for_shifter	Honors connection specs for shifters based on the CPF rules <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_intent_use_cpf_global_connect_for_shifter</a>
power_intent_use_effective_domain_for_iso_shifter_insertion	Honors effective domains for ISO/LS insertions <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_intent_use_effective_domain_for_iso_shifter_insertion</a>
power_ir_derated_timing_view	

	set timing view in tempus-pi flow. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_ir_derated_timing_view</a>
power_leakage_power_view	Specifies a separate leakage analysis view for power calculation. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_leakage_power_view</a>
power_leakage_scale_factor_for_temperature	Performs a linear scaling of the leakage power for temperature in all libraries. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 1.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_leakage_scale_factor_for_temperature</a>
power_lib_files	Specify the lib files to be used for power Analysis. Libs specified through this option are not read in during design loading <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_lib_files</a>
power_library_preference	option to choose instance binding to closest voltage or ecm/ccsp library. <b>Type:</b> <a href="#">string</a> <b>Default:</b> voltage <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_library_preference</a>
power_match_state_for_logic_x	Controls how the logic X will be evaluated in the boolean function of the 'when' state of a power table. <b>Type:</b> <a href="#">string</a> <b>Default:</b> x <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_match_state_for_logic_x</a>

power_merge_switted_net_currents	
	<p>Specifies to merge switched net currents into always-on currents.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_merge_switted_net_currents</a></p>
power_method	
	<p>Specifies the type of analysis to be performed.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> static dynamic dynamic_vectorless dynamic_vectorbased dynamic_mixed_mode vector_profile</p> <p><b>Default:</b> static</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_method</a></p>
power_modes	
	<p>List of the power mode names in the design.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
power_multibit_flop_toggle_behavior	
	<p>select mbff toggle: simultaneous   independent(default)   sbff during vectorless state propagation dynamic analysis</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> simultaneous independent sbff</p> <p><b>Default:</b> independent</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_multibit_flop_toggle_behavior</a></p>
power_off_pg_nets	
	<p>The name of the power rails that will be turned off.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_off_pg_nets</a></p>
power_output_current_data_prefix	

	<p>Specifies a prefix to the static or dynamic current files generated by the software.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_output_current_data_prefix</a></p>
power_output_dir	<p>Used to save power engine output to the defined directory. If not set, will use the current working dir.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_output_dir</a></p>
power_partition_twf	<p>turn on/off twf partitioning in distributed flow</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_partition_twf</a></p>
power_pin_based_twf	<p>turn on/off generation of pin based TWF in dynamic method</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_pin_based_twf</a></p>
power_precision	<p>Specifies precision of decimal range [1-8] to ensure consistent decimal places are displayed for each power component.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 8</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_precision</a></p>
power_quit_on_activity_coverage_threshold	<p>Specifies the activity (VCD/FSDB/TCF) coverage threshold value.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_quit_on_activity_coverage_threshold</a></p>

power_read_rcdb	<p>Specifies to write a SPEF file containing only the total C for signal nets and pass it to the Dynamic Power engine.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_read_rcdb</a></p>
power_report_black_boxes	<p>Specify this parameter to report cells that are used as black boxes.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_report_black_boxes</a></p>
power_report_idle_instances	<p>report non-switching instances in vectorless state propagation dynamic analysis</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_report_idle_instances</a></p>
power_report_instance_switching_info	<p>all or output_logic or none</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> all output_logic none</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_report_instance_switching_info</a></p>
power_report_instance_switching_list	<p>specify file which is having list of instances</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_report_instance_switching_list</a></p>
power_report_library_usage	

	generate report for lib usage <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_report_library_usage</a>
power_report_missing_bulk_connectivity	
	Specifies to report missing bulk pins in the missing input report ( -report_missing_input ). <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_report_missing_bulk_connectivity</a>
power_report_missing_input	
	Specifies to report missing netlist information in input files, such as library, LEF/DEF, PGV, SPEF, TWF, and missing logical connectivity for cell instance (PGNET). <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_report_missing_input</a>
power_report_missing_nets	
	Controls reporting of missing nets in both static and dynamic power analysis. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_report_missing_nets</a>
power_report_scan_chain_statistics	
	report scan chain analysis statistics <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_report_scan_chain_statistics</a>
power_report_statistics	
	Reports a set of statistics on the instance power, instance power density, clock power, or transition density. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">power_report_statistics</a>

power_report_time_display_fraction_digits	
	<p>specify display fraction digits of reporting time  <b>Type:</b> <a href="#">int</a>  <b>Default:</b> -1  <b>Edit:</b> Yes</p>
power_report_twf_attributes	
	<p>TWF attributes report format  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">power_report_twf_attributes</a></p>
power_scale_to_sdc_clock_frequency	
	<p>Specifies to enable the VCD clock frequency to be scaled up to the SDC clock frequency.  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">power_scale_to_sdc_clock_frequency</a></p>
power_scan_chain_name_pattern	
	<p>define scan chain name and pattern  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">power_scan_chain_name_pattern</a></p>
power_scan_control_file	
	<p>Specifies the scan control file name required to run the Scan Mode Analysis flow.  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">power_scan_control_file</a></p>
power_scan_multi_bit_flop_chain_type	
	<p>Specifies the type of multi-bit scan flip-flop.  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> liberty  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">power_scan_multi_bit_flop_chain_type</a></p>
power_settling_buffer	

	<p>Specifies the settling buffer time (in ps unit) between multiple windows of a VCD file.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_settling_buffer</a></p>
power_split_bus_power	<p>A value of false applies the internal power number to each individual bit.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_split_bus_power</a></p>
power_start_time_alignment	<p>Specifies to align all the signals of the activity file at time zero.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_start_time_alignment</a></p>
power_state_dependent_leakage	<p>When set to false , power analysis performs state independent leakage power calculation.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_state_dependent_leakage</a></p>
power_static_netlist	<p>Specifies to perform static power analysis using a Verilog or DEF only netlist.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> verilog</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_static_netlist</a></p>
power_thermal_input_file	<p>Specifies to read a power map file to perform thermal analysis.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_thermal_input_file</a></p>
power_to_x_transition_factor	

	<p>activity count for 0/1 to x transition</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.5</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_to_x_transition_factor</a></p>
<b>power_to_z_transition_factor</b>	
	<p>activity count for 0/1 to z transition</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.25</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_to_z_transition_factor</a></p>
<b>power_transition_time_method</b>	
	<p>Specifies the minimum, maximum, or average transition time method that will be used with the integrated timer or the external TWF.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> max</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_transition_time_method</a></p>
<b>power_twf_delay_annotation</b>	
	<p>Allows you to choose between min, max, or avg arrival times from the timing window file (TWF).</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> avg</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_twf_delay_annotation</a></p>
<b>power_twf_load_cap</b>	
	<p>Allows you to select minimum, maximum, or average value of TWF external load or capacitance for power calculation.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> max</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_twf_load_cap</a></p>
<b>power_use_cell_leakage_power_density</b>	

	<p>Specifies to use library leakage density times area (default_leakage_power_density).</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_use_cell_leakage_power_density</a></p>
<b>power_use_fastest_clock_for_dynamic_scheduling</b>	
	<p>Specifies to use only the respective fastest clock associated with each net or pin to schedule events for a given simulation period.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_use_fastest_clock_for_dynamic_scheduling</a></p>
<b>power_use_lef_for_missing_cells</b>	
	<p>Allows a combination of LEF and PGV in the dynamic analysis flow.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_use_lef_for_missing_cells</a></p>
<b>power_use_zero_delay_vector_file</b>	
	<p>Enables zero delay mode in vector-based dynamic analysis to avoid pessimism in current estimation.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_use_zero_delay_vector_file</a></p>
<b>power_vector_based_multithread</b>	
	<p>Specifies to enable multi-threading for the VCD/FSDB based dynamic vector-based flows.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_vector_based_multithread</a></p>
<b>power_vector_profile_mode</b>	

	<p>activity or density</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> activity event_based power_density transient</p> <p><b>Default:</b> event_based</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_vector_profile_mode</a></p>
power_view	<p>Specifies the power analysis library view (for MMMC setup).</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_view</a></p>
power_worst_case_vector_activity	<p>Specifies to use the worst activity value when multiple vectors are specified in the static power calculation flow.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_worst_case_vector_activity</a></p>
power_worst_step_size	<p>Set worst step size for power analysis</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
power_worst_window_count	<p>Set worst window count for power analysis</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
power_worst_window_size	<p>Set worst window size for power analysis</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
power_worst_window_type	

	<p>Set worst window type for power analysis</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
power_write_db	<p>A value of true creates a binary database of power results.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_write_db</a></p>
power_write_default_pti_files	<p>For instances that are not hooked to any power/ground rail, the current for these instances are reflected in the default static current files.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_write_default_pti_files</a></p>
power_write_profiling_db	<p>turn on/off profiling database writing</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
power_write_static_currents	<p>A value of true tells Voltus to generate the current data files per net.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_write_static_currents</a></p>
power_x_transition_factor	<p>When using VCD/FSDB one can specify how transitions to and from X are counted.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.5</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_x_transition_factor</a></p>
power_z_transition_factor	

	<p>When using VCD/FSDB one can specify how transitions to and from Z are counted.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.25</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_z_transition_factor</a></p>
power_zero_delay_vector_toggle_shift	<p>Specifies to shift the current waveform in the zero-delay VCD flow.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">power_zero_delay_vector_toggle_shift</a></p>
print_full_message_summary	<p>Used to control the format of message summary. If true, print full message, otherwise, print truncated message.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">print_full_message_summary</a></p>
program_major_version	<p>The major version plus one digit. So if program_version = 19.11-e062_1 it would return '19.1'.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p> <p><b>Reference:</b> <a href="#">program_major_version</a></p>
program_name	<p>name of the program</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p> <p><b>Reference:</b> <a href="#">program_name</a></p>
program_short_name	<p>short name of the program</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p> <p><b>Reference:</b> <a href="#">program_short_name</a></p>

program_version	
	<p>version of the program  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> No  <b>Reference:</b> <a href="#">program_version</a></p>
proto_allow_model_with_io	
	<p>Supports model with I/Os.  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_allow_model_with_io</a></p>
proto_characterize_percentage_route_blockage	
	<p>Specifies the percentage of created models that will be used for characterizing default flexFiller routing blockage.  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 0.1  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_characterize_percentage_route_blockage</a></p>
proto_create_dir	
	<p>Specifies the directory to save created models.  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> proto_model  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_create_dir</a></p>
proto_create_high_fanout_ps_per_micron	
	<p>Create high fanout psPM models.  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_create_high_fanout_ps_per_micron</a></p>
proto_create_lib	
	<p>Specifies the OA library to save created models.  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> proto_model_lib  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_create_lib</a></p>

proto_create_metal_fill_ndr	
	<p>Will be used by create_proto_net_delay_model for creating psPM model for nets with non default rules.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">proto_create_metal_fill_ndr</a></p>
proto_create_metal_fill_nominal	
	<p>Will be used by create_proto_net_delay_model for creating psPM model for normal nets.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.5</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">proto_create_metal_fill_nominal</a></p>
proto_create_multi_corner_ps_per_micron	
	<p>Create multi corner psPM models.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">proto_create_multi_corner_ps_per_micron</a></p>
proto_create_ndr_ps_per_micron	
	<p>Control whether create_proto_net_delay_model should generate psPM model for non default rule or not</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> auto on off</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">proto_create_ndr_ps_per_micron</a></p>
proto_create_opt_effort	
	<p>Disabling/enabling optimization with different effort.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none low medium high</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">proto_create_opt_effort</a></p>
proto_create_partition_as_flexmodel	

	Create partition specified as flexmodel automatically. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_create_partition_as_flexmodel</a>
proto_create_pipeline_flop	Specifies a list of pipeline flop instance patterns that are used in the design. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_create_pipeline_flop</a>
proto_create_power_domain_ps_per_micron	Create power domain psPM models. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_create_power_domain_ps_per_micron</a>
proto_create_ps_per_micron_model	Generate psPM.model. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_create_ps_per_micron_model</a>
proto_create_route_blockage	characterize flexFiller routing blockage in model generation. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_create_route_blockage</a>
proto_create_timing_budget	Keep consistent setting of deriveTimingBudget <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_create_timing_budget</a>
proto_create_timing_net_delay_model	

	Generate psPM.model. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_create_timing_net_delay_model</a>
<b>proto_design_congestion_aware</b>	
	aware of congestion when using new plan_design algorithm <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_design_congestion_aware</a>
<b>proto_design_cover_fixed_macros</b>	
	force flexModel cover fixed macros belong to it when using new plan_design algorithm <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_design_cover_fixed_macros</a>
<b>proto_design_flexmodel_constraint_type</b>	
	Convert flexModel to the specified constraint type in proto_design. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> guide region fence <b>Default:</b> region <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_design_flexmodel_constraint_type</a>
<b>proto_design_keep_guide</b>	
	-keep_guide {true false} #default=true <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_design_keep_guide</a>
<b>proto_design_level</b>	
	Set intended floorplan flow type. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> flat top_to_bottom multi_level <b>Default:</b> flat <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_design_level</a>

proto_design_place_macro	control if do macro placement in plan_design <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_design_place_macro</a>
proto_design_remove_overlap	control if do remove overlap in plan_design <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_design_remove_overlap</a>
proto_design_timing_aware	aware of timing when using new plan_design algorithm <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_design_timing_aware</a>
proto_flexfiller_route_blockage	Specifies percentage of route blockage for each routing layer. Layer range is 1 to maxRouteLayer. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_flexfiller_route_blockage</a>
proto_identify_engine	identify_proto algorithm <default=auto> <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> auto module_based instgroup_based <b>Default:</b> auto <b>Edit:</b> Yes <b>Reference:</b> <a href="#">proto_identify_engine</a>
proto_identify_estimated_flexmodel_number	

	<p>Specified the estimated flexModel number to identify for the design when using instance group based identify_proto_model.</p> <p><b>Type:</b> int  <b>Default:</b> 20  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_identify_estimated_flexmodel_number</a></p>
proto_identify_exclude_module	<p>Excludes specified module(s) but not its sub-modules for being marked as models.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_identify_exclude_module</a></p>
proto_identify_exclude_module_and_parent	<p>Excludes specified module(s) and their parents for being marked as models.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_identify_exclude_module_and_parent</a></p>
proto_identify_exclude_module_tree	<p>Excludes specified module(s) and its sub-modules for being marked as models.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_identify_exclude_module_tree</a></p>
proto_identify_honor_objects_hierarchy	<p>Specified the list of objects which instance group based identify_proto_model will honor its hierarchy.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_identify_honor_objects_hierarchy</a></p>
proto_identify_max_inst	

	<p>Specifies the maximum instance count threshold of a module to be marked as model.          (default=8% of total instance count and no lower than 300K instances)</p> <p><b>Type:</b> int  <b>Default:</b> -1  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_identify_max_inst</a></p>
proto_identify_min_inst	<p>Specifies the minimum instance count threshold of a module to be marked as model.</p> <p><b>Type:</b> int  <b>Default:</b> 1000  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_identify_min_inst</a></p>
proto_include_model_route_blockage	<p>Specifies a list of models that will be used for routing blockage characterization.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_include_model_route_blockage</a></p>
proto_keep_inst_file_only	<p>FlexModel only contains inst in keep_inst_file.</p> <p><b>Type:</b> bool  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_keep_inst_file_only</a></p>
proto_keep_instance_defined_in_sdc	<p>FlexModel will keep inst defined in sdc file</p> <p><b>Type:</b> bool  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_keep_instance_defined_in_sdc</a></p>
proto_keep_slack_improve_ndr	<p>Will be used by report_NDR_WNS_gain to keep top critical nets as non default rule nets .</p> <p><b>Type:</b> bool  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">proto_keep_slack_improve_ndr</a></p>
proto_max_report_ndr_net	

	<p>Will be used by create_proto_net_delay_model for creating psPM model for nets with non default rules.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.05</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">proto_max_report_ndr_net</a></p>
proto_partition_level_num	<p>Specifies the current partition level.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">proto_partition_level_num</a></p>
proto_partition_level_ungroup	<p>Specifies what partition level to be ungrouped down to hierarchical instances so they can be visible in floorplan view.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">proto_partition_level_ungroup</a></p>
proto_place_effort	<p>set place effort</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> fp default center</p> <p><b>Default:</b> fp</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">proto_place_effort</a></p>
proto_route_net_ndr	<p>Will be used by create_proto_net_delay_model for creating psPM model for nets with non default rules.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">proto_route_net_ndr</a></p>
proto_timing_net_delay	

	<p>Specifies the estimated delay per micron for each routing layer. Layer range is from 1 to maximum routing layers.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">proto_timing_net_delay</a></p>
proto_use_timing_net_delay_model	<p>set mode of calculating wire delay</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> best_layer_no_detour best_layer_blockage_aware use_actual_wire</p> <p><b>Default:</b> best_layer_no_detour</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">proto_use_timing_net_delay_model</a></p>
proto_verbose	<p>Output detailed information into .log file.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">proto_verbose</a></p>
rc_corners	<p>Returns the information about the rc corners in the design.</p> <p><b>Type:</b> <a href="#">obj(rc_corner)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
read_db_directory	<p>Specifies the directory of current loaded DB.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">read_db_directory</a></p>
read_db_file_check	

	<p>By default, read_db will check all files inside the saved DB directory are unchanged. If any files have been edited, renamed or deleted, then an error will occur unless this value is set to false.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">read_db_file_check</a></p>
<b>read_db_stop_at_design_in_memory</b>	
	<p>By default, tool will error and stop if call read_db more than once in the same Innovus session unless this value is set to false.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">read_db_stop_at_design_in_memory</a></p>
<b>read_db_tool_name</b>	
	<p>Indicates the tool name of the tool that created the restored db on the disk database</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">read_db_tool_name</a></p>
<b>read_db_version</b>	
	<p>Indicates the version of the tool that generates an on disk database</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">read_db_version</a></p>
<b>read_def_check_mask_shifts</b>	
	<p>If on/bypass, will check for conflicts between DEF COMPONENT MASKSHIFT and MACRO MASKSHIFT values with the LEF FIXEDMASK and LAYERMASKSHIFT values in the technology and MACRO sections, error out if on and error without out if bypass</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> off on bypass</p> <p><b>Default:</b> off</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">read_def_check_mask_shifts</a></p>
<b>read_physical_check_mask_shifts</b>	

	<p>If on/bypass, will check for conflicts between LEF FIXEDMASK and LAYERMASKSHIFT values in the technology section and MACRO section when reading in any LEF files, error out if on and error without out if bypass</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> off on bypass</p> <p><b>Default:</b> off</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">read_physical_check_mask_shifts</a></p>
	<p><b>read_physical_extend_polygon_cell_shapes</b></p> <p>A list of {{&lt;layer&gt; &lt;value&gt;} ...} pairs. LEF PIN/OBS shapes on each &lt;layer&gt; that are polygons (not simple rects), will be extended with OBS SPACING 0 rects by &lt;value&gt; (in microns) in the preferred routing direction. This is a workaround for some advanced node libraries to avoid spacing violations during routing.</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">read_physical_extend_polygon_cell_shapes</a></p>
	<p><b>read_physical_must_join_all_ports</b></p> <p>if false, the LEF_MUSTJOINALLPORTS property on a LEF PIN auto-creates MUSTJOIN pins for each PORT. If true, the MUSTJOIN pins are not created, but the router must connect to every port with a signal wire or signal via that physically overlaps all the ports.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">read_physical_must_join_all_ports</a></p>
	<p><b>reorder_scan_allow_swapping</b></p> <p>reorder with new swap mode</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">reorder_scan_allow_swapping</a></p>
	<p><b>reorder_scan_clock_aware</b></p> <p>Clock tree aware reorder</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">reorder_scan_clock_aware</a></p>
	<p><b>reorder_scan_comp_logic</b></p>

	trace considering multiple input logic <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">reorder_scan_comp_logic</a>
<b>reorder_scan_effort</b>	
	Specifies effort level for reorder_scan <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> low medium high auto <b>Default:</b> auto <b>Edit:</b> Yes <b>Reference:</b> <a href="#">reorder_scan_effort</a>
<b>reorder_scan_enable_for_partition</b>	
	enable scanReorder for design with partition <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">reorder_scan_enable_for_partition</a>
<b>reorder_scan_keep_hinst_port_name</b>	
	Specifies filename which contains HInsts <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">reorder_scan_keep_hinst_port_name</a>
<b>reorder_scan_keep_hport</b>	
	Maintains hierarchical ports without adding or deleting shifters <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">reorder_scan_keep_hport</a>
<b>reorder_scan_prefer_horizontal</b>	
	Makes horizontal scan chain connections if possible <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">reorder_scan_prefer_horizontal</a>
<b>reorder_scan_prefer_vertical</b>	

	Makes vertical scan chain connections if possible <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">reorder_scan_prefer_vertical</a>
reorder_scan_skip_mode	Specifies method for handling buffers and inverters <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> skip_none skip_buffer skip_floating_buffer <b>Default:</b> skip_none <b>Edit:</b> Yes <b>Reference:</b> <a href="#">reorder_scan_skip_mode</a>
reorder_scan_swap_effort	Specifies effort level for reorder_scan different chains swapping <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> low medium high <b>Default:</b> high <b>Edit:</b> Yes <b>Reference:</b> <a href="#">reorder_scan_swap_effort</a>
report_pin_density_map_display_step	range step for displaying the pin density map <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.05 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">report_pin_density_map_display_step</a>
report_pin_density_map_grid_size	specify the value (in row-height) of side of square grid for pin density calculations. <b>Type:</b> <a href="#">int</a> <b>Default:</b> 10 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">report_pin_density_map_grid_size</a>
report_pin_density_map_grid_unit	specify the value (in micron) of side of square grid for pin density calculations. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 50.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">report_pin_density_map_grid_unit</a>

report_pin_density_map_threshold	
	<p>threshold value over which the densities must be reported.  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 0.5  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">report_pin_density_map_threshold</a></p>
report_place_density_map_grid_size	
	<p>specify the value (in row-height) of side of square grid for density calculations.  <b>Type:</b> <a href="#">int</a>  <b>Default:</b> 10  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">report_place_density_map_grid_size</a></p>
report_place_density_map_grid_unit	
	<p>specify the value (in micron) of side of square grid for density calculations.  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 50.0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">report_place_density_map_grid_unit</a></p>
report_place_density_map_threshold	
	<p>threshold value over which the densities must be reported.  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 0.75  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">report_place_density_map_threshold</a></p>
resize_blockages	
	<p>Short-cut for [get_db current_design .resize_blockages]  <b>Type:</b> <a href="#">obj(resize_blockage)*</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
resize_floorplan_cong_aware	
	<p>resizes and shifts the floorplan objects by estimating the congestion for the floorplan and automatically deciding where to draw a resize line to avoid the congested area.  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">resize_floorplan_cong_aware</a></p>

#### resize\_floorplan\_honor\_halo

honors placement halo and preserves the space between macros held by halo after the floorplan resize.  
**Type:** [bool](#)  
**Default:** true  
**Edit:** Yes  
**Reference:** [resize\\_floorplan\\_honor\\_halo](#)

#### resize\_floorplan\_io\_fix

fixes I/Os at current location.  
**Type:** [bool](#)  
**Default:** false  
**Edit:** Yes  
**Reference:** [resize\\_floorplan\\_io\\_fix](#)

#### resize\_floorplan\_io\_move\_with\_edge

moves pins on the moved edge orthogonally to edge direction so pins stay on edge after movement.  
**Type:** [bool](#)  
**Default:** false  
**Edit:** Yes  
**Reference:** [resize\\_floorplan\\_io\\_move\\_with\\_edge](#)

#### resize\_floorplan\_io\_relative

resize the space among I/Os proportionally.  
**Type:** [bool](#)  
**Default:** true  
**Edit:** Yes  
**Reference:** [resize\\_floorplan\\_io\\_relative](#)

#### resize\_floorplan\_maintain\_resource\_ratio

Enable to maintain the resource ratio after resize\_floorplan in shift-based mode.  
**Type:** [bool](#)  
**Default:** false  
**Edit:** Yes  
**Reference:** [resize\\_floorplan\\_maintain\\_resource\\_ratio](#)

#### resize\_floorplan\_relative

	<p>resizes the space among floorplan objects proportionally.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">resize_floorplan_relative</a></p>
resize_floorplan_shift_based	<p>shifts floorplan objects at appropriate location(s) without changing the proportional spacing.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">resize_floorplan_shift_based</a></p>
resize_floorplan_shrink_fence	<p>enables resized lines to go through fences and regions in floorplan.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">resize_floorplan_shrink_fence</a></p>
resize_floorplan_snap_to_track	<p>snap values (shrink/expand) of the floorplan to a multiple integer of the metal layer pitch.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">resize_floorplan_snap_to_track</a></p>
route_blockages	<p>Short-cut for [get_db current_design .route_blockages]</p> <p><b>Type:</b> <a href="#">obj(route_blockage)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
route_design_add_antenna_inst_prefix	<p>prefix for the diode insts added to fix antenna</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_add_antenna_inst_prefix</a></p>
route_design_adjust_auto_via_weight	

	adjust auto via weight for via swapping <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_adjust_auto_via_weight</a>
<b>route_design_allow_inst_overlaps</b>	
	don't do instance overlap check <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_allow_inst_overlaps</a>
<b>route_design_allow_pin_as_feedthru</b>	
	allow pin as feedthrough <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> true TRUE false FALSE none NONE output input inout <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_allow_pin_as_feedthru</a>
<b>route_design_antenna_cell_name</b>	
	specify the antenna diode cell names for antenna fixing <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_antenna_cell_name</a>
<b>route_design_antenna_diode_insertion</b>	
	insert antenna diode to fix antenna violation <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_antenna_diode_insertion</a>
<b>route_design_concurrent_minimize_via_count_effort</b>	
	specify the effort of concurrent via minimization <b>Type:</b> <a href="#">string</a> <b>Default:</b> medium <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_concurrent_minimize_via_count_effort</a>
<b>route_design_connect_to_bumps</b>	

	connect to bumps in native NanoRoute in Innovus <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_connect_to_bumps</a>
<b>route_design_detail_add_passive_fill_only_on_layers</b>	
	specify layers where passive fill will be added <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_detail_add_passive_fill_only_on_layers</a>
<b>route_design_detail_antenna_eco_list_file</b>	
	set file name for antenna eco list <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_detail_antenna_eco_list_file</a>
<b>route_design_detail_auto_stop</b>	
	control whether Nanoroute continues routing if there are many violations <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_detail_auto_stop</a>
<b>route_design_detail_check_mar_on_cell_pin</b>	
	Enable mar checking on used cell pins <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_detail_check_mar_on_cell_pin</a>
<b>route_design_detail_end_iteration</b>	
	specify the last iteration pass in a detailed routing step <b>Type:</b> <a href="#">int</a> <b>Default:</b> 0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_detail_end_iteration</a>
<b>route_design_detail_fix_antenna</b>	

	fix antenna violation by jumping metal layers <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_detail_fix_antenna</a>
route_design_detail_min_length_for_spread_wire	
	specify the min. length of a spreaded wire <b>Type:</b> <a href="#">string</a> <b>Default:</b> 0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_detail_min_length_for_spread_wire</a>
route_design_detail_min_length_for_widen_wire	
	specify the min. length of a widened wire <b>Type:</b> <a href="#">double</a> <b>Default:</b> 1.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_detail_min_length_for_widen_wire</a>
route_design_detail_min_slack_for_opt_wire	
	specify the min slack for a net wire optimization <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_detail_min_slack_for_opt_wire</a>
route_design_detail_no_taper_in_layers	
	Specifies the range of the layer where taper is not allowed <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_detail_no_taper_in_layers</a>
route_design_detail_no_taper_on_output_pin	
	forbid wire tapering at output pin <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> false true auto <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_detail_no_taper_on_output_pin</a>
route_design_detail_on_grid_only	

	<p>route on grid only</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_detail_on_grid_only</a></p>
<b>route_design_detail_post_route_litho_repair</b>	
	<p>litho hotspot repair in post route stage</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_detail_post_route_litho_repair</a></p>
<b>route_design_detail_post_route_spread_wire</b>	
	<p>spread wire in post route stage</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_detail_post_route_spread_wire</a></p>
<b>route_design_detail_post_route_swap_via</b>	
	<p>to enforce post route via swapping mode in detail route command.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_detail_post_route_swap_via</a></p>
<b>route_design_detail_post_route_via_pillar_effort</b>	
	<p>Set opt effort/range for opportunistic via pillar</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> low</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_detail_post_route_via_pillar_effort</a></p>
<b>route_design_detail_post_route_wire_widen</b>	
	<p>widen wire in post route stage</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_detail_post_route_wire_widen</a></p>
<b>route_design_detail_post_route_wire_widen_rule</b>	

	<p>specify the rule used to widen wire</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_detail_post_route_wire_widen_rule</a></p>
<b>route_design_detail_postroute_via_priority</b>	
	<p>Set net priority for via swapping based on timing</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_detail_postroute_via_priority</a></p>
<b>route_design_detail_search_and_repair</b>	
	<p>run search-and-repair step after the initial detailed routing</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_detail_search_and_repair</a></p>
<b>route_design_detail_signoff_effort</b>	
	<p>specify when to give up on irresolvable violations</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> high</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_detail_signoff_effort</a></p>
<b>route_design_detail_use_multi_cut_via_effort</b>	
	<p>specify the effort to use multi-cut via during routing</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> low</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_detail_use_multi_cut_via_effort</a></p>
<b>route_design_diode_insertion_for_clock_nets</b>	
	<p>allow diode insertion on clock nets</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_diode_insertion_for_clock_nets</a></p>
<b>route_design_enable_route_rule_si_limit_length</b>	

	use MAR wire length as NDR PRL requirement for metal spacing check <b>Type:</b> <a href="#">string</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_enable_route_rule_si_limit_length</a>
route_design_enforce_route_rule_on_special_net_wire	enforce ndr rule on all special wire segments of specified nets <b>Type:</b> <a href="#">string</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_enforce_route_rule_on_special_net_wire</a>
route_design_extra_via_enclosure	specify an extra via enclosure to use when connecting to block pins and special net wires <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_extra_via_enclosure</a>
route_design_fix_clock_nets	set clock nets routing status to fixed or routed <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_fix_clock_nets</a>
route_design_high_freq_constraint_groups	only route specified constraint groups, legal values are {net match bus pair shield}, add "order" in front to control route order <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_high_freq_constraint_groups</a>
route_design_high_freq_match_report_file	specify match report file name <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_high_freq_match_report_file</a>
route_design_high_freq_num_reserved_layers	

	<p>number of layers reserved for standard cell pin access</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_high_freq_num_reserved_layers</a></p>
<b>route_design_high_freq_remove_floating_shield</b>	
	<p>remove floating shield segments for high frequency nets</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_high_freq_remove_floating_shield</a></p>
<b>route_design_high_freq_search_repair</b>	
	<p>run search and repair to remove violations, legal value is one of {auto false true only}</p> <p><b>Type:</b> string</p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_high_freq_search_repair</a></p>
<b>route_design_high_freq_shield_trim_length</b>	
	<p>specify minimum length of shielding wire to be kept</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_high_freq_shield_trim_length</a></p>
<b>route_design_honor_power_domain</b>	
	<p>honor power domain routing</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_honor_power_domain</a></p>
<b>route_design_ignore_antenna_top_cell_pin</b>	
	<p>ignore antenna check on block I/O pins</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_ignore_antenna_top_cell_pin</a></p>
<b>route_design_ignore_follow_pin_shapes</b>	

	Ignore follow pin via shapes <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_ignore_follow_pin_shapes</a>
<b>route_design_number_fail_limit</b>	
	set limit for number of fails <b>Type:</b> <a href="#">int</a> <b>Default:</b> 0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_number_fail_limit</a>
<b>route_design_number_thread</b>	
	set the number of processors to be used in one workstation for multi-threading <b>Type:</b> <a href="#">int</a> <b>Default:</b> 1 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_number_thread</a>
<b>route_design_number_warning_limit</b>	
	set limit for number of warnings <b>Type:</b> <a href="#">int</a> <b>Default:</b> 0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_number_warning_limit</a>
<b>route_design_process_node</b>	
	Specify the process node <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_process_node</a>
<b>route_design_rc_extraction_corner</b>	
	specific which RC extraction corner to use in routing <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_rc_extraction_corner</a>
<b>route_design_relaxed_route_rule_spacing_to_power_ground_nets</b>	

	<p>relax the spacing requirement from NDR spacing for the layers</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_relaxed_route_rule_spacing_to_power_ground_nets</a></p>
route_design_reserve_space_for_multi_cut	<p>Reserves space to insert multicut vias in postroute stage. This option has to be set before routing. After routing with this parameter specified, you can add double-cut vias or larger overhang vias by using the "route_design -via_opt" command. For examples, see route_design.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_reserve_space_for_multi_cut</a></p>
route_design_reverse_direction	<p>reverse routing direction in area: (lx ly ux uy [bot_lyr : top_lyr]) ... , top_lyr and bot_lyr could be either layer name or layer routing id</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_reverse_direction</a></p>
route_design_route_clock_nets_first	<p>route clock nets first</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_route_clock_nets_first</a></p>
route_design_selected_net_only	<p>route selected net only</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_selected_net_only</a></p>
route_design_shield_crosstie_offset	

	<p>Specifies the offset in terms of number of tracks for adding crossties. The default is 0 for all layers. The syntax is 'layer_name:numTrack1 layer_name2:numTrack2... '.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_shield_crosstie_offset</a></p>
route_design_skip_analog	<p>skip routing nets or pins marked + USE ANALOG in the DEF file</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_skip_analog</a></p>
route_design_strict_honor_route_rule	<p>Strictly enforce non-default rules</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_strict_honor_route_rule</a></p>
route_design_stripe_layer_range	<p>specify the target layer range of stripes for tie net connection</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_stripe_layer_range</a></p>
route_design_third_party_data	<p>Allow third party data as input</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_third_party_data</a></p>
route_design_tieoff_to_shapes	<p>specify the target special wire shapes or target instance pin for tie net connection: [auto stripe ring powergroundpin]</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_tieoff_to_shapes</a></p>

route\_design\_trim\_pull\_back\_distance\_from\_boundary

route\_trim\_pull\_back\_distance\_from\_boundary {<layer>:<value> ...}

**Type:** string

**Default:** ""

**Edit:** Yes

**Reference:** [route\\_design\\_trim\\_pull\\_back\\_distance\\_from\\_boundary](#)

route\_design\_trunk\_with\_cluster\_target\_size

global control of trunk routing pattern for nets with TRUNK pattern attribute. 0: nets with TRUNK pattern will be routed as Steiner tree; 1: default, nets will be routed as traditional trunk pattern, i.e., each pin directly connects to SNET trunk separately; >1: define a proximate max cluster size (in number of pins), and nets will be routed as fishbone style, i.e., several pins in a column are clustered together, and then connects to SNET trunk.

**Type:** int

**Default:** 1

**Edit:** Yes

**Reference:** [route\\_design\\_trunk\\_with\\_cluster\\_target\\_size](#)

route\_design\_unconnected\_ports

Route unconnected ports

**Type:** bool

**Default:** false

**Edit:** Yes

**Reference:** [route\\_design\\_unconnected\\_ports](#)

route\_design\_use\_auto\_via

allow to use internal generated vias

**Type:** string

**Default:** auto

**Edit:** Yes

**Reference:** [route\\_design\\_use\\_auto\\_via](#)

route\_design\_via\_weight

set weight for vias

**Type:** string

**Default:** ""

**Edit:** Yes

**Reference:** [route\\_design\\_via\\_weight](#)

route\_design\_with\_eco

	enable eco routing <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_with_eco</a>
route_design_with_litho_driven	
	enable the litho-driven routing <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_with_litho_driven</a>
route_design_with_si_driven	
	enable si driven routing <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_with_si_driven</a>
route_design_with_timing_driven	
	enable timing driven routing <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_with_timing_driven</a>
route_design_with_trim_metal	
	set cut metal dgrid for short pin extension generated <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_with_trim_metal</a>
route_design_with_via_in_pin	
	enclose via in pin shape <b>Type:</b> <a href="#">string</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_design_with_via_in_pin</a>
route_design_with_via_only_for_block_cell_pin	

	<p>enclose via in pin shape for macro cell pins</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_with_via_only_for_block_cell_pin</a></p>
<b>route_design_with_via_only_for_stdcell_pin</b>	
	<p>disable planar access to standard cell pins</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_design_with_via_only_for_stdcell_pin</a></p>
<b>route_early_global_effort_level</b>	
	<p>Specifies the congestion effort level. Default is "standard", where congestion is more accurate and runtime is larger. If set to "medium", runtime will be much smaller and congestion report will have less accuracy. Setting to "low", it will be faster than "medium" however less accurate.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> low medium standard</p> <p><b>Default:</b> standard</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_early_global_effort_level</a></p>
<b>route_early_global_honor_partition_allow_feedthru</b>	
	<p>Honor partition fences with feedthrough for &lt;list_of_ptn_cell_names&gt;.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_early_global_honor_partition_allow_feedthru</a></p>
<b>route_early_global_honor_partition_fence</b>	
	<p>Honor partition fences for &lt;list_of_ptn_cell_names&gt;.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_early_global_honor_partition_fence</a></p>
<b>route_early_global_honor_partition_pin</b>	

	Honor partition fences and single-entry constraint for <list_of_ptn_cell_names>. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_early_global_honor_partition_pin</a>
<b>route_early_global_honor_partition_pin_guide</b>	
	Honor partition pin guides. Default is true <b>Type:</b> bool <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_early_global_honor_partition_pin_guide</a>
<b>route_early_global_honor_power_domain</b>	
	consider MSV constraints while routing <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_early_global_honor_power_domain</a>
<b>route_early_global_horizontal_supply_scale_factor</b>	
	Horizontal supply scale factor <b>Type:</b> double <b>Default:</b> 1.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_early_global_horizontal_supply_scale_factor</a>
<b>route_early_global_num_tracks_per_clock_wire</b>	
	Specify special number of tracks per clock wires. <b>Type:</b> int <b>Default:</b> 0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_early_global_num_tracks_per_clock_wire</a>
<b>route_early_global_reverse_direction_regions</b>	
	Reverse routing direction in the given region on the specified layer-range. Example: "(x1 y1 x2 y2) M1:M2 (x3 y3 x4 y4) M3:M4 ..." <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_early_global_reverse_direction_regions</a>
<b>route_early_global_route_selected_net_only</b>	

	<p>Only route the nets which are selected in the DB.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_early_global_route_selected_net_only</a></p>
<b>route_early_global_secondary_pg</b>	
	<p>Specifies whether secondary PG pins needs to be routed or not</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_early_global_secondary_pg</a></p>
<b>route_early_global_secondary_pg_max_fanout</b>	
	<p>Specifies the max fanout limit for each secondary PG subnet</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_early_global_secondary_pg_max_fanout</a></p>
<b>route_early_global_stripe_layer_range</b>	
	<p>Route secondary PG pins to access to the PG stripes in the given layer range.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_early_global_stripe_layer_range</a></p>
<b>route_early_global_vertical_supply_scale_factor</b>	
	<p>Vertical supply scale factor</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 1.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_early_global_vertical_supply_scale_factor</a></p>
<b>route_rules</b>	
	<p>All the route_rules. It is initialized from LEF NONDEFAULTRULES section or from OA equivalents. It includes the reserved name "default" for the implicit LEF default rule or the OA LEFDefaultRouteSpec. It also includes design specific route_rules from create_route_rule or read in from DEF or an OA cellview.</p> <p><b>Type:</b> <a href="#">obj(route_rule)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

route_special_allow_non_preferred_direction_route	
	allow wrong way route <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_allow_non_preferred_direction_route</a>
route_special_avoid_over_core_row_layer	
	specify number of layers to avoid routing over core row area <b>Type:</b> <a href="#">string</a> <b>Default:</b> max layer of standard cell pin <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_avoid_over_core_row_layer</a>
route_special_block_pin_connect_ring_pin_corners	
	Extend the ring pins at the corners <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_block_pin_connect_ring_pin_corners</a>
route_special_block_pin_route_with_pin_width	
	Connect using pin width only <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_block_pin_route_with_pin_width</a>
route_special_connect_broken_core_pin	
	Break followpin for standard cell pin or obs <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_connect_broken_core_pin</a>
route_special_core_pin_ignore_obs	
	ignore specified blockage when connecting follow pin <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> none placement_blockage overlap_obs block_halo <b>Default:</b> none <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_core_pin_ignore_obs</a>

route_special_core_pin_length	
	<p>connect core pins of at least specified length  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 0.0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">route_special_core_pin_length</a></p>
route_special_core_pin_length_as_inst	
	<p>connect core pins if their lengths are the same as the instances  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">route_special_core_pin_length_as_inst</a></p>
route_special_core_pin_max_via_scale	
	<p>Maximum via width and height at stripe crossover for standcell pins (%)  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">route_special_core_pin_max_via_scale</a></p>
route_special_core_pin_merge_limit	
	<p>gaps smaller than this variable cause followpin rails to be joined  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> 0.0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">route_special_core_pin_merge_limit</a></p>
route_special_core_pin_refer_to_follow_pin	
	<p>M2 followpin generation uses follow pin wire  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">route_special_core_pin_refer_to_follow_pin</a></p>
route_special_core_pin_reference_macro	
	<p>use specified macro as reference for followpin creation  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">route_special_core_pin_reference_macro</a></p>

route_special_core_pin_snap_to	snap M2 followpin referred to M1 pin to position <b>Type:</b> enum <b>Enum Values:</b> m1_pin opt_routing_track grid half_grid <b>Default:</b> m1_pin <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_core_pin_snap_to</a>
route_special_core_pin_stop_route	<b>Type:</b> enum <b>Enum Values:</b> RowEnd CellPinEnd <b>Default:</b> RowEnd <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_core_pin_stop_route</a>
route_special_endcap_as_core	route_special treat Endcap macro as Core macro <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_endcap_as_core</a>
route_special_extend_nearest_target	extend nearest target so that it can be connected <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_extend_nearest_target</a>
route_special_jog_threshold_ratio	distance ratio between a jogging target and a straight target <b>Type:</b> double <b>Default:</b> 10.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_jog_threshold_ratio</a>
route_special_layer_non_preferred_direction_cost	

	layer cost of non-preferred direction <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_layer_non_preferred_direction_cost</a>
<b>route_special_layer_preferred_direction_cost</b>	
	layer cost of preferred direction <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_layer_preferred_direction_cost</a>
<b>route_special_pad_pin_min_via_size</b>	
	Minimum via width percent between pad and ring. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 20.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_pad_pin_min_via_size</a>
<b>route_special_pad_pin_split</b>	
	Split width and spacing for wide pad pins <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_pad_pin_split</a>
<b>route_special_pad_ring_use_lef</b>	
	Keep user LEF input for pad rings <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_pad_ring_use_lef</a>
<b>route_special_pg_pin_as_signal</b>	
	List of cell/pin information NOT extract from CPF <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_pg_pin_as_signal</a>
<b>route_special_secondary_pin_max_gap</b>	

	<p>gaps bigger than this variable cause level shifter rail to break for them</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_special_secondary_pin_max_gap</a></p>
<b>route_special_secondary_pin_rail_width</b>	
	<p>width of followpin rail</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_special_secondary_pin_rail_width</a></p>
<b>route_special_signal_pin_as_pg</b>	
	<p>signal pins as PG pins</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_special_signal_pin_as_pg</a></p>
<b>route_special_split_long_via</b>	
	<p>Split vias longer than &lt;threshold&gt; into smaller vias with specified &lt;step&gt; and bottom/left end &lt;offset&gt; and vertical/horizontal &lt;height&gt;</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> 0 0 -1 -1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_special_split_long_via</a></p>
<b>route_special_target_number</b>	
	<p>number of target to connect</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_special_target_number</a></p>
<b>route_special_target_search_distance</b>	
	<p>target search distance</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">route_special_target_search_distance</a></p>
<b>route_special_time_limit</b>	

	time limit (in seconds) that the router is allowed in routing each port <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_time_limit</a>
<b>route_special_via_connect_to_shape</b>	
	Make via connection to specified shapes <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> padring ring stripe blockring blockpin coverpin noshape blockwire corewire followpin iowire <b>Default:</b> padring ring stripe blockring blockpin coverpin noshape blockwire corewire followpin iowire <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_via_connect_to_shape</a>
<b>route_special_via_through_to_closest_ring</b>	
	A via should connect only to closest ring layer when multiple rings overlap <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_via_through_to_closest_ring</a>
<b>route_special_welltap_as_endcap</b>	
	route_special treat Welltap macro as Endcap macro <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_special_welltap_as_endcap</a>
<b>route_trial_max_print_ignored_pad_nets</b>	
	Number of nets to be printed connecting a pad term to a fterm without geometry <b>Type:</b> <a href="#">int</a> <b>Default:</b> 0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">route_trial_max_print_ignored_pad_nets</a>
<b>route_types</b>	
	All the route_types from create_route_type command. <b>Type:</b> <a href="#">obj(route_type)*</a> <b>Default:</b> "" <b>Edit:</b> No

rows	
	<p>Short-cut for [get_db current_design .rows]</p> <p><b>Type:</b> <a href="#">obj(row)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
run_abstract_abstract_blockage_cut_around_pin	
	<p>For std cell, we do not want cover obs on pin. So:</p> <p>If -input_cell_type {std}, setting the value to all metal and via layer name list.</p> <p>If -input_cell_type {block} or -input_cell_type {io}, setting the value to all via layer name list.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_abstract_blockage_cut_around_pin</a></p>
run_abstract_antenna_connectivity	
	<p>Specifies the layers for which connectivity is to be extracted. The syntax is {&lt;layer1&gt; &lt;connect_layer&gt; &lt;layer2&gt;}.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_antenna_connectivity</a></p>
run_abstract_antenna_diffusion_geometry	
	<p>Specifies diffusion layer, followed by expression to remove gate channel area from diffusion region.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_antenna_diffusion_geometry</a></p>
run_abstract_antenna_gate_geometry	
	<p>Specifies poly layer that forms a gate, and then the layer expression to derive the gate area. This option also triggers the creation of antenna models.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_antenna_gate_geometry</a></p>
run_abstract_blockage_detailed_layers	

	<p>Specifies the layers for which a detailed blockage model is to be created. The detailed blockage model generates blockages only where there are real shapes in the cell on the layer. This only applies to IO cells and block cells, it does not apply to standard cells.</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_blockage_detailed_layers</a></p>
<p>run_abstract_boundary_layers</p>	
	<p>By default this list is empty, and the prBoundary is used. The prBoundary comes from an explicit GDS layer that is used to compute the LEF SIZE (and OVERLAP OBS shapes for rectilinear boundaries). If there is no explicit GDS prBoundary layer, the boundary can be computed from the bounding box of geometries on this list of layers. Note, this option is almost never correct for core standard cells.</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_boundary_layers</a></p>
<p>run_abstract_cell_symmetry</p>	
	<p>Specifies a property value for cell symmetry. The valid values for the property symmetry include: {R0   X   Y   R90   X Y   X R90   Y R90   X Y R90}. Default {X Y}</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_cell_symmetry</a></p>
<p>run_abstract_export_lef_version</p>	
	<p>Version of LEF to export. The default version is the same as the version of technology LEF file being imported.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> 5.3 5.4 5.5 5.6 5.7 5.8</p> <p><b>Default:</b> 5.7</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_export_lef_version</a></p>
<p>run_abstract_extract_layers_power</p>	

	<p>Specifies the layers through which the extractor extracts each power net. This is used to reduce the search space if abstract is taking too much run time for each cell. Usually not applicable to standard cells. For blocks it is common to only extract the power nets on the top one or two metal layers.</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_extract_layers_power</a></p>
run_abstract_extract_layers_signal	<p>Specifies the layers through which the extractor extracts each net. This is used to reduce the search space if abstract is taking too much run time for each cell. Usually not applicable to standard cells.</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_extract_layers_signal</a></p>
run_abstract_extract_pin_layers_power	<p>Determines which of the shapes found by the extractor should be turned into pins. This argument is valid only if the associated layer, geometry specification and connectivity have been provided in the technology LEF. Usually not applicable to standard cells.</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_extract_pin_layers_power</a></p>
run_abstract_extract_pin_layers_signal	<p>Determines which of the shapes found by the extractor should be turned into pins. This argument is valid only if the associated layer, geometry specification and connectivity have been provided in the technology LEF. Usually not applicable to standard cells.</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_extract_pin_layers_signal</a></p>
run_abstract_input_cell_type	

	<p>Choose the cell type being translated with abstract. The tool adjusts its settings based on this selection. Optional.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> std io block</p> <p><b>Default:</b> std</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_input_cell_type</a></p>
<b>run_abstract_input_lef_tech_file</b>	
	<p>Input technology LEF file. This is used to get all the layer names, their types (routing, cut, etc.) and the layer order for extracting connectivity. Required.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_input_lef_tech_file</a></p>
<b>run_abstract_input_stream_layer_map_file</b>	
	<p>Specify the file that maps GDS layer number / data type to LEF layer names in the Virtuoso format. Required.</p> <p>For example, the gds file is not colorized, you could use the common virtuoso format gds layer map to stream gds file.</p> <pre>#layer name #purpose name #stream layer #stream data type V0 drawing 35 0 V0 drawing 35 235 V0 drawing 35 236 M1 drawing 15 0 M1 drawing 15 235 M1 drawing 15 236 M1 drawing 15 239</pre> <p>For example, the gds file is colorized, you could specify the mask color in gds layer map to stream gds file.</p> <pre>#layer name #purpose name #stream layer #stream data type #photo mask color #color state V0 drawing 35 0 V0 drawing 35 235 mask1Color unlocked V0 drawing 35 236 mask2Color unlocked M1 drawing 15 0 M1 drawing 15 235 mask1Color unlocked M1 drawing 15 236 mask2Color unlocked M1 drawing 15 239 mask3Color unlocked</pre> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_input_stream_layer_map_file</a></p>

run_abstract_keep_output_files	<p>Do not clean up temporary files/libraries that are created in the process after command finishes.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_keep_output_files</a></p>
run_abstract_pins_analog_names	<p>Identifies analog pin names based on label strings in the Abstract to set the LEF "USE ANALOG" property. Enter a list of possible names for the analog pins. This can be a list of regular expressions, each separated by a space.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_pins_analog_names</a></p>
run_abstract_pins_clock_names	<p>Identifies clock pin names based on label strings in the Abstract to set the LEF "USE CLOCK" property. Enter a list of possible names for the clock pins. This can be a list of regular expressions, each separated by a space.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_pins_clock_names</a></p>
run_abstract_pins_ground_names	<p>Identifies ground pins based on label strings in the Abstract to set the LEF "USE GROUND" property. Enter a list of possible names for the ground pins. This can be a list of regular expressions, each separated by a space.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_pins_ground_names</a></p>
run_abstract_pins_output_names	<p>Identifies output pins based on label strings in the GDS to set the LEF direction to OUTPUT. Enter a list of regular expressions separated by spaces.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_pins_output_names</a></p>

run_abstract_pins_power_names	<p>Identifies power pin names based on label strings in the Abstract to set the LEF "USE POWER" property. Enter a list of possible names for the power pins. This can be a list of regular expressions, each separated by a space.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_pins_power_names</a></p>
run_abstract_pins_text_pin_map	<p>Maps text labels to pins on nets. Specify the layer purpose pairs based on which you want the abstract generator to search for geometry of any given layer-purpose pair with a text label.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_pins_text_pin_map</a></p>
run_abstract_pre_abstract_script	<p>a skill file that will be executed in abstract before the auto-generated script is executed. Optional.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_pre_abstract_script</a></p>
run_abstract_selected_cells	<p>Select cells to create abstract for using regex style expressions. Optional.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_selected_cells</a></p>
run_abstract_site_name	<p>Site to be used for macros. This site will be added to all the cells.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_site_name</a></p>
run_abstract_verbose	

	<p>Verbose mode with extra print.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">run_abstract_verbose</a></p>
script_search_path	<p>The variable provides a set of directories for the software to search for files that sourced using the Tcl 'source' command. The software will search in each search path directory for the specified file.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> .</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">script_search_path</a></p>
selected	<p>The list of currently selected objects. It can be set to a list of objects as long as they are selectable.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">selected</a></p>
set_db_verbose	<p>Specifies additional messages are issued describing what attribute is being set on what object.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">set_db_verbose</a></p>
setup_views	<p>Returns the information about the setup analysis views in the design.</p> <p><b>Type:</b> <a href="#">obj(analysis_view)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
si_accumulated_small_aggressor_factor	

	<p>Specifies the multiplication factor that controls the effect of the cap mode accumulated small attacker.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 1.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_accumulated_small_aggressor_factor</a></p>
si_accumulated_small_aggressor_mode	<p>Specifies the multiplication factor that controls the effect of the cap mode accumulated small attacker.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> cap current zero_mean</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_accumulated_small_aggressor_mode</a></p>
si_accumulated_small_aggressor_threshold	<p>Specifies whether to use the current-matching based method for accumulated small attackers.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 10.01</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_accumulated_small_aggressor_threshold</a></p>
si_aggressor_alignment	<p>Specifies the attacker alignment.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> path path_overlap timing_aware_edge</p> <p><b>Default:</b> path</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_aggressor_alignment</a></p>
si_clock_synchronicity	<p>Specifies the value above which the clock delta delay should be calculated.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> asynchronous synchronous</p> <p><b>Default:</b> synchronous</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_clock_synchronicity</a></p>
si_delay_clock_delta_threshold	

	Specifies the value above which the clock delta delay should be calculated. <b>Type:</b> <a href="#">double</a> <b>Default:</b> -1.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_delay_clock_delta_threshold</a>
<b>si_delay_delta_annotation_mode</b>	
	Calculates the delay for each arc (cell arc and net arc) in a path. <b>Type:</b> <a href="#">string</a> <b>Default:</b> arc <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_delay_delta_annotation_mode</a>
<b>si_delay_delta_threshold</b>	
	delta delay analysis threshold <b>Type:</b> <a href="#">double</a> <b>Default:</b> -1.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_delay_delta_threshold</a>
<b>si_delay_enable_double_clocking_check</b>	
	Enables double clocking check in AAE. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> true false <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_delay_enable_double_clocking_check</a>
<b>si_delay_enable_logical_correlation</b>	
	Enables the AAE-SI logical correlation. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> true false <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_delay_enable_logical_correlation</a>
<b>si_delay_enable_report</b>	
	Enables SI delay reports. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_delay_enable_report</a>

si_delay_separate_on_data	Separates the delta delay on data (delta delay is always separated for clock). <b>Type:</b> <a href="#">string</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_delay_separate_on_data</a>
si_enable_bus_attacker_correlation	<b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_enable_bus_attacker_correlation</a>
si_enable_drv_with_delta_slew	Enables SI slews reporting. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_enable_drv_with_delta_slew</a>
si_enable_glitch_overshoot_undershoot	Enables overshoot/undershoot analysis and reporting. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
si_enable_glitch_propagation	Enables glitch propagation and driver weakening through single stage cells. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_enable_glitch_propagation</a>
si_enable_glitch_propagation_spice_deck	Enables glitch propagation in spice deck. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_enable_glitch_propagation_spice_deck</a>
si_enable_two_stage_driver_weakening	

	<p><b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_enable_two_stage_driver_weakening</a></p>
si_enable_virtual_attacker_constituent_report	<p><b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_enable_virtual_attacker_constituent_report</a></p>
si_glitch_constrained_input_threshold_failure_point	<p><b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> input both <b>Default:</b> input <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_glitch_constrained_input_threshold_failure_point</a></p>
si_glitch_enable_dynamic_receiver_peak_limits	<p><b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_glitch_enable_dynamic_receiver_peak_limits</a></p>
si_glitch_enable_report	<p>Enables AAE SI glitch analysis.</p> <p><b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_glitch_enable_report</a></p>
si_glitch_input_threshold	<p>Specifies the input glitch failure threshold value during AAE analysis.</p> <p><b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.4 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_glitch_input_threshold</a></p>
si_glitch_input_voltage_high_threshold	

	<p>Specifies the input glitch vh failure threshold value during AAE analysis.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.4</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_glitch_input_voltage_high_threshold</a></p>
si_glitch_input_voltage_low_threshold	<p>Specifies the input glitch vl failure threshold value during AAE analysis.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.4</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_glitch_input_voltage_low_threshold</a></p>
si_glitch_receiver_clock_peak_limit	<p>Defines the glitch check limit for clock inputs in receiver peak mode. This parameter is specified as a ratio of vdd.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.05</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_glitch_receiver_clock_peak_limit</a></p>
si_glitch_receiver_latch_peak_limit	<p>Defines the glitch check limit for latch inputs in receiver peak mode. This parameter is specified as a ratio of vdd.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_glitch_receiver_latch_peak_limit</a></p>
si_glitch_receiver_peak_limit	<p>Defines the receiver peak/glitch peak limit at all nodes. The value specified for this parameter is a ratio of vdd.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.15</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_glitch_receiver_peak_limit</a></p>
si_individual_aggressor_clock_threshold	

	Sets the glitch tolerance for individual attacker nets on victim clock nets. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.015 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_individual_aggressor_clock_threshold</a>
<b>si_individual_aggressor_simulation_filter</b>	
	Enables electrical filtering based on attackers' simulated glitch peaks. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_individual_aggressor_simulation_filter</a>
<b>si_individual_aggressor_threshold</b>	
	AAE virtual attacker threshold <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.015 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_individual_aggressor_threshold</a>
<b>si_max_virtual_attacker_constituents</b>	
	<b>Type:</b> <a href="#">int</a> <b>Default:</b> 5 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_max_virtual_attacker_constituents</a>
<b>si_net_specific_settings</b>	
	Set a list of globals for nets specified by sgs2net. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes
<b>si_net_type</b>	
	Set the type of nets to apply net specific settings. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> Sim MT <b>Default:</b> Sim <b>Edit:</b> Yes
<b>si_nonlinear_aggressor_slew</b>	

	<p>Uses a non-linear attacker. If set to false , it uses a linear attacker.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> true false</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_nonlinear_aggressor_slew</a></p>
si_num_iteration	<p>Specifies the maximum number of timing window iterations that should be performed during SI delay analysis.</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 2</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_num_iteration</a></p>
si_pessimistic_mode	<p>Pessimistic Mode Settings</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> advanced reduced_optimism reduced_pessimism increased_pessimism</p> <p><b>Default:</b> advanced</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_pessimistic_mode</a></p>
si_reselection	<p>Specifies the SI reselection criteria during timing window iterations.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> delta_delay slack xcap_ratio</p> <p><b>Default:</b> slack</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_reselection</a></p>
si_reselection_delay_threshold	<p>Allows to change the delay reselection criteria.</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 1e-11</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_reselection_delay_threshold</a></p>
si_reselection_hold_slack	

	<p>Specifies the slack reselection threshold for hold.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> -1e-12</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_reselection_hold_slack</a></p>
<b>si_reselection_setup_slack</b>	
	<p>Specifies the slack reselection threshold for setup.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> -1e-12</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_reselection_setup_slack</a></p>
<b>si_secondary_attacker_decoupling_factor</b>	
	<p>Specifies decoupling factor for secondary aggressors.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 1.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_secondary_attacker_decoupling_factor</a></p>
<b>si_sgs2net</b>	
	<p>Specifies a list of nets for which nets specific settings will be applied.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>si_skip_noise_model_check</b>	
	<p>Specifies a list of pins for which noise model check will not take place.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_skip_noise_model_check</a></p>
<b>si_skip_timing_window</b>	
	<p>Specifies the list of nets for which timing window is to be skipped.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">si_skip_timing_window</a></p>
<b>si_switch_probability</b>	

	Sets the attacker switching probability. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.3 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_switch_probability</a>
<b>si_unconstrained_net_use_infinite_timing_window</b>	
	Specifies that unconstrained nets will have an infinite timing window. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> true false <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_unconstrained_net_use_infinite_timing_window</a>
<b>si_use_infinite_timing_window</b>	
	<b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> true false <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">si_use_infinite_timing_window</a>
<b>si_user_specific_settings</b>	
	Specifies a list of globals for persistent settings set <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes
<b>sites</b>	
	All the sites defined in LEF or OA. <b>Type:</b> <a href="#">obj(site)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>skew_groups</b>	
	list of skew_group <b>Type:</b> <a href="#">obj(skew_group)*</a> <b>Default:</b> "" <b>Edit:</b> No <b>Reference:</b> <a href="#">skew_groups</a>
<b>soft_stack_size_limit</b>	

	<p>Soft stacksize limit in mbytes. When the tool is launched, auto-enlarge the soft stacksize limit to 0.2%RAM. If 0.2%RAM is larger than hard limit, set to the hard limit.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> 8</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">soft_stack_size_limit</a></p>
source_continue_on_error	<p>Enable/Disable 'source' to continue the script on TCL_ERROR. If true, the source command will ignore Tcl errors, and continue processing the script files. If false, a Tcl error will halt the script.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">source_continue_on_error</a></p>
source_echo_filename	<p>Display the file name being sourced before the actual sourcing.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">source_echo_filename</a></p>
source_verbose	<p>enable verbose script source</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">source_verbose</a></p>
source_verbose_output_type	<p>Controls 'source -verbose' output style.'echo' will output only the commands. 'debug' will output the file name, line number, and command. 'echo_comments' will output commands, comments and empty lines.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> debug echo echo_comments</p> <p><b>Default:</b> echo_comments</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">source_verbose_output_type</a></p>
stack_via_rules	

	<p>The stack_via_rules available in this design from the LEF or create_stack_via_rules.</p> <p><b>Type:</b> <a href="#">obj(stack_via_rule)*</a></p> <p><b>Default:</b> {}</p> <p><b>Edit:</b> No</p>
	<p><b>tcl_log_post_expansion_length_limit</b></p>
	<p>Limits the length of a single command to this many characters when verbose logging of 'post' Tcl expansion is enabled. See source_verbose, flow_verbose attributes, and the set_proc_verbose command for more details.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 200</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">tcl_log_post_expansion_length_limit</a></p>
	<p><b>tcl_partial_cmd_argument_matching</b></p>
	<p>Use this switch to control command argument partial matching as well as enum value partial matching. When it's turned on, argument '-opt' will match '-option' if no other argument name begins with -opt. Default is 'quiet', which means to silently allow partial-matching when there's no ambiguity. 'warn' means allow partial-matching with a warning message. 'error' means to disable partial-matching, and error out.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> quiet warn error</p> <p><b>Default:</b> quiet</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">tcl_partial_cmd_argument_matching</a></p>
	<p><b>tcl_return_display_length_limit</b></p>
	<p>Limits the number of characters displayed to stdout and the .log file. The Tcl return value itself is not affected--only the display is truncated. A value of -1 indicates that there is no display limit. This is useful to limit the output to the display of any command that can return long lists of objects or values.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 10000</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">tcl_return_display_length_limit</a></p>
	<p><b>tech_db_units</b></p>
	<p>Database units per micron from LEF or OA techfile, unless init_min_dbu_per_micron is larger.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p> <p><b>Reference:</b> <a href="#">tech_db_units</a></p>

tech_finfet_grid_direction	<p>An enum value indicating the direction of the finfet grid from the LEF FINFET statement or OA.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> vertical horizontal</p> <p><b>Default:</b> vertical</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">tech_finfet_grid_direction</a></p>
tech_finfet_grid_offset	<p>The finfet grid offset from 0 in microns from the LEF FINFET statement or OA.</p> <p><b>Type:</b> <a href="#">coord</a></p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">tech_finfet_grid_offset</a></p>
tech_finfet_grid_pitch	<p>Returns a single floating point number indicating the pitch of the FINFET grid as described in LEF.</p> <p><b>Type:</b> <a href="#">coord</a></p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">tech_finfet_grid_pitch</a></p>
tech_inst_mask_shift_layers	<p>Ordered list of layer pointers to layers that allow instance mask shifting. This is the list of layers that will show up in the DEF COMPONENTMASK statement for layers that can have mask values shifted in standard cells.</p> <p><b>Type:</b> <a href="#">obj(layer)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p> <p><b>Reference:</b> <a href="#">tech_inst_mask_shift_layers</a></p>
tech_mfg_grid	<p>Manufacturing grid from LEF or OA techfile. Note, this is the default value for each layer, but it can be overridden for specific layers. In some technologies the mfg_grid for higher metal layers is coarser than for the lower layers.</p> <p><b>Type:</b> <a href="#">coord</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p> <p><b>Reference:</b> <a href="#">tech_mfg_grid</a></p>

### texts

Short-cut to all the text objects in the current\_design.

**Type:** [obj\(text\)](#)

**Default:** ""

**Edit:** No

### timing\_all\_registers\_include\_icg\_cells

Controls whether to include ICG cells as register in all\_registers -edge\_triggered

**Type:** [bool](#)

**Default:** true

**Edit:** Yes

**Reference:** [timing\\_all\\_registers\\_include\\_icg\\_cells](#)

### timing\_allow\_input\_delay\_on\_clock\_source

When set to true allows you to apply input delay constraints on a pin where a clock was previously asserted

**Type:** [bool](#)

**Default:** false

**Edit:** Yes

**Reference:** [timing\\_allow\\_input\\_delay\\_on\\_clock\\_source](#)

### timing\_analysis\_aocv

AOCV Analysis

**Type:** [bool](#)

**Default:** false

**Edit:** Yes

**Reference:** [timing\\_analysis\\_aocv](#)

### timing\_analysis\_async\_checks

Async checks

**Type:** [enum](#)

**Enum Values:** [async](#) [no\\_async](#) [async\\_only](#)

**Default:** [async](#)

**Edit:** Yes

**Reference:** [timing\\_analysis\\_async\\_checks](#)

### timing\_analysis\_case\_analysis

caseAnalysis

**Type:** [bool](#)

**Default:** true

**Edit:** Yes

**Reference:** [timing\\_analysis\\_case\\_analysis](#)

timing_analysis_check_type	Report Violations for hold, setup <b>Type:</b> enum <b>Enum Values:</b> setup hold <b>Default:</b> setup <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_analysis_check_type</a>
timing_analysis_clock_gating	clockGatingCheck <b>Type:</b> bool <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_analysis_clock_gating</a>
timing_analysis_clock_net_marking_mode	clkNetsMarking <b>Type:</b> enum <b>Enum Values:</b> before_constant_propagation after_constant_propagation <b>Default:</b> before_constant_propagation <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_analysis_clock_net_marking_mode</a>
timing_analysis_clock_propagation_mode	Timing arc attributes effect on timing analysis <b>Type:</b> enum <b>Enum Values:</b> sdc_control forced_ideal <b>Default:</b> sdc_control <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_analysis_clock_propagation_mode</a>
timing_analysis_clock_source_paths	clkSrcPath <b>Type:</b> bool <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_analysis_clock_source_paths</a>
timing_analysis_cppr	

	<p>Removes pessimism from clock paths that have a portion of the clock network in common between the clock source and clock destination paths</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> both none setup hold</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_analysis_cppr</a></p>
<b>timing_analysis_engine</b>	
	<p>Statistical or Static</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> statistical static</p> <p><b>Default:</b> static</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_analysis_engine</a></p>
<b>timing_analysis_honor_active_logic_view</b>	
	<p>Honor Active Logic View</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_analysis_honor_active_logic_view</a></p>
<b>timing_analysis_self_loops_paths_no_skew</b>	
	<p>Eliminates clock skew due to clock uncertainty for a path starting and ending at the same register. If the clock skew is not eliminated, the timing for such paths is pessimistic</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_analysis_self_loops_paths_no_skew</a></p>
<b>timing_analysis_socv</b>	
	<p>SOCV Analysis</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_analysis_socv</a></p>
<b>timing_analysis_type</b>	

	<p>Single or BCWC or OCV TimingAnalysis type</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> single best_case_worst_case ocv</p> <p><b>Default:</b> best_case_worst_case</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_analysis_type</a></p>
timing_aocv_analysis_mode	<p>Controls handling of AOCV analysis modes</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> launch_capture clock_only separate_data_clock combine_launch_capture</p> <p><b>Default:</b> launch_capture</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_aocv_analysis_mode</a></p>
timing_aocv_chip_size	<p>Specifies the diagonal length of the chip, in microns</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 1e+30</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_aocv_chip_size</a></p>
timing_aocv_core_size	<p>Specifies the diagonal length of the core area, in microns</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 1e+30</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_aocv_core_size</a></p>
timing_aocv_derate_mode	<p>Controls the AOCV derating mode</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> aocv_multiplicative aocv_additive</p> <p><b>Default:</b> aocv_multiplicative</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_aocv_derate_mode</a></p>
timing_aocv_slack_threshold	<p>Analyze aocv slack based at specified threshold</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p>

timing_aocv_stage_count_update_on_timing_reset	<p>When set to true, the aocv stage counts are recalculated when timing is reset.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_aocv_stage_count_update_on_timing_reset</a></p>
timing_apply_check_derate_to_external_output_delay	<p>Applies check derate to output external delay</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_apply_check_derate_to_external_output_delay</a></p>
timing_apply_default_primary_input_assertion	<p>When set to true, primary input and bidirectional ports that do not have an explicit arrival time specified are provided a default arrival time</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_apply_default_primary_input_assertion</a></p>
timing_apply_exceptions_to_data_check_related_pin	<p>When set to true, any false path assertion which blocks the data path to the related (-from) pin of the data-to-data check also causes the check to be disabled</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_apply_exceptions_to_data_check_related_pin</a></p>
timing_cap_unit	<p>If set, this value is passed to set_library_unit -cap to set the capacitance units used in timing library and .sdc files and timing reports. Legal values are 1pf and 1ff.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_cap_unit</a></p>
timing_case_analysis_for_icg_propagation	

	Determines whether constant propagation continues through integrated clock gating (ICG) cells  <b>Type:</b> enum <b>Enum Values:</b> false require_seq_prop always <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_case_analysis_for_icg_propagation</a>
timing_case_analysis_for_sequential_propagation	
	When set to true, calculates constants on the outputs of sequential elements  <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_case_analysis_for_sequential_propagation</a>
timing_case_analysis_propagation	
	Overrides sequential and ICG propagation behaviors.  <b>Type:</b> bool <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_case_analysis_propagation</a>
timing_check_timing_signal_level_high_to_low_threshold	
	Threshold for warnig about difference in signal level between hight_drv and low_rcv  <b>Type:</b> double <b>Default:</b> 0.0 <b>Edit:</b> Yes
timing_check_timing_signal_level_low_to_high_threshold	
	Threshold for warnig about difference in signal level between low_drv and high_rcv  <b>Type:</b> double <b>Default:</b> 0.0 <b>Edit:</b> Yes
timing_clock_phase_propagation	
	Lets you select appropriate clock phases at register clock pins when both positive and negative phases of the same clock signal are seen in the clock network  <b>Type:</b> enum <b>Enum Values:</b> positive negative both <b>Default:</b> both <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_clock_phase_propagation</a>

<a href="#">timing_clock_source_paths_unconstrained_mark_clock_used_as_data</a>	global is set to true, is_clock_used_as_data returns true for unconstrained clock source network <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_clock_source_paths_unconstrained_mark_clock_used_as_data</a>
<a href="#">timing_clock_source_use_driving_cell</a>	When set to false, the create_clock command for output pins of cells uses default slew instead of the propagated slew from the primary input ports <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_clock_source_use_driving_cell</a>
<a href="#">timing_clock_uncertainty_from_to_precedence</a>	Gives higher precedence to clock-to-clock uncertainty when set to true <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_clock_uncertainty_from_to_precedence</a>
<a href="#">timing_collection_all_fanin_fanout_traversal_mode</a>	Controls the way software processes netlist for all_fanin/all_fanout command processing <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> hierarchical flat <b>Default:</b> flat <b>Edit:</b> Yes
<a href="#">timing_collection_result_display_limit</a>	Limits the number of objects of a collection to be displayed in the output report <b>Type:</b> <a href="#">int</a> <b>Default:</b> 100 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_collection_result_display_limit</a>
<a href="#">timing_collection_variable_assignment_compatibility</a>	

	Enables printing names of output of get objects commands when set to false <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_collection_variable_assignment_compatibility</a>
<b>timing_conditions</b>	
	Returns the information about the timing conditions in the design. <b>Type:</b> <a href="#">obj(timing_condition)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>timing_constraint_disable_min_max_input_delay_worst_casing</b>	
	Used for disabling the override of -max value from -min value in set_input_delay. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_constraint_disable_min_max_input_delay_worst_casing</a>
<b>timing_constraint_enable_detailed_report_invalid_begin_end_points</b>	
	Enables detailed reporting of invalid begin points/end points specified with set_false_path/set_multicycle_path constraints else only checks structural end points <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
<b>timing_constraint_enable_drv_limit_override</b>	
	Enables support of drv override flow <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_constraint_enable_drv_limit_override</a>
<b>timing_constraint_enable_logging</b>	
	Enables dumping of constraint command in log file <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_constraint_enable_logging</a>
<b>timing_constraint_enable_report_invalid_begin_end_points</b>	

	<p>Enables reporting of invalid begin points/end points specified with set_false_path/set_multicycle_path constraints</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_constraint_enable_report_invalid_begin_end_points</a></p>
<b>timing_constraint_enable_search_path</b>	
	<p>Enable searching of constraint files in search_path directory variable</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_constraint_enable_search_path</a></p>
<b>timing_constraint_enable_separate_multicycle_data_checks</b>	
	<p>When set to true, disables multicycle path constraint application on data checks</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_constraint_path_delay_exclude_check_delay_from_ignore_clock_latency</b>	
	<p>Excludes check delays from set_max/min_delay -ignore_clock_latency slack computation</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_constraint_path_delay_exclude_io_delay_from_ignore_clock_latency</b>	
	<p>Excludes input/output delays from set_max/min_delay -ignore_clock_latency slack computation</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_constraint_path_delay_exclude_unconstrained_endpoints</b>	
	<p>When set to true, does not constrain unconstrained path with path delay.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_constraint_path_delay_exclude_unconstrained_endpoints</a></p>
<b>timing_constraint_path_delay_include_clock_pin_endpoints</b>	

	<p>When set to true, considers register clock pins as endpoint's for path delay constraints applied upstream</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_constraint_path_delay_include_clock_pin_endpoints</a></p>
<b>timing_constraint_warn_for_timing_derate_exceeding_max_limit</b>	
	<p>Sets the limit on derate value for giving the warning in case the larger derate is applied</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 100.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_constraint_warn_for_timing_derate_exceeding_max_limit</a></p>
<b>timing_constraints_warning_on_partial_search_match</b>	
	<p>Display Warning in case of partial success/failure while fetching objects in certain constraints</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_continue_on_error</b>	
	<p>When set to true, directs software to skip the error and continue processing when an error occurs during timing analysis</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_continue_on_error</a></p>
<b>timing_cppr_opposite_edge_mean_scale_factor</b>	
	<p>Controls mean delay component for CPPR credit for opposite transition edges at common pin</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 1.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_cppr_opposite_edge_mean_scale_factor</a></p>
<b>timing_cppr_opposite_edge_sigma_scale_factor</b>	

	<p>Controls sigma delay component for CPPR credit for opposite transition edges at common pin</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 1.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_cppr_opposite_edge_sigma_scale_factor</a></p>
<b>timing_cppr_opposite_edge_sigma_scale_factor_cell</b>	
	<p>Controls cell sigma delay component for CPPR credit for opposite transition edges at common pin</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 1.0</p> <p><b>Edit:</b> Yes</p>
<b>timing_cppr_opposite_edge_sigma_scale_factor_net</b>	
	<p>Controls net sigma delay component for CPPR credit for opposite transition edges at common pin</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 1.0</p> <p><b>Edit:</b> Yes</p>
<b>timing_cppr_propagate_thru_latches</b>	
	<p>When set to true, the cppr of a timing path crossing a latch (or latches) is calculated using the common pin of its origin flop and the capture device at the end of the path. Otherwise the usual segment-based cppr calculation is performed. This cppr setting is considered only when the latch thru analysis mode is enabled.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_cppr_propagate_thru_latches</a></p>
<b>timing_cppr_remove_clock_to_data_pessimism</b>	
	<p>When set to true, removes clock reconvergence pessimism (CRP) for clock source paths</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_cppr_remove_clock_to_data_pessimism</a></p>
<b>timing_cppr_self_loop_mode</b>	

	<p>When set to true in case of self-loop paths, computes CPPR adjustment by taking the difference between early and late clock arrival time of the common point</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_cppr_self_loop_mode</a></p>
<b>timing_cppr_skip_clock_reconvergence</b>	
	<p>Specifies the branch point to use for computing clock path pessimism removal (CPPR) adjustment when there is reconvergence in the clock tree</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_cppr_skip_clock_reconvergence</a></p>
<b>timing_cppr_skip_clock_reconvergence_for_unmatched_clocks</b>	
	<p>When set to true, this enables CPPR branch point search in reconverging clock tree only when launching and capturing clocks are different.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_cppr_skip_clock_reconvergence_for_unmatched_clocks</a></p>
<b>timing_cppr_threshold_ps</b>	
	<p>Specifies the maximum amount of pessimism that clock path pessimism removal (CPPR) analysis is allowed to leave in the path</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 20.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_cppr_threshold_ps</a></p>
<b>timing_cppr_transition_sense</b>	
	<p>Specifies the transition sense of the launching and capturing clocks at the common node, to calculate clock path pessimism removal (CPPR)</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> normal same_transition same_transition_expanded</p> <p><b>Default:</b> normal</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_cppr_transition_sense</a></p>
<b>timing_create_clock_default_propagated</b>	

	<p>Enables clocks to be created in propagated mode</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_create_clock_default_propagated</a></p>
<b>timing_default_opcond_per_lib</b>	
	<p>When set to true, use default operating conditions for each lib</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_default_opcond_per_lib</a></p>
<b>timing_defer_mmmc_obj_updates</b>	
	<p>You can set the timing_defer_mmmc_object_updates global to true, so that the software allows a sequence of MMMC updates to be accumulated before new data is loaded and analyzed</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_defer_mmmc_obj_updates</a></p>
<b>timing_derate_aocv_dynamic_delays</b>	
	<p>This global controls whether or not AOCV derating factors are applied to the dynamic, SI-induced delay component or not. With a value of '1', the AOCV derating factor will be applied to both the static and dynamic components of the delay arc. When set to '0', the AOCV derate will only apply to the static component of the delay.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_derate_aocv_dynamic_delays</a></p>
<b>timing_derate_aocv_reference_point</b>	
	<p>Allows specification of reference point for AOCV factors</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_derate_aocv_reference_point</a></p>
<b>timing_derate_dynamic_compatibility</b>	

	<p>This global controls how the set_timing_derate factors that are not specified using either -static or -dynamic options are applied to the delay. When this global is set to '1' the behavior will be compatible with previous releases. In this mode, the static and dynamic components will be summed before applying derating. With a setting of '0', the static and dynamic components will be derated separately and then combined. A setting of '0' is equivalent to using separate derate assertions with the -dynamic and -static options explicitly specified.</p> <p><b>Type:</b> <a href="#">bool</a>  <b>Default:</b> true  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">timing_derate_dynamic_compatibility</a></p>
timing_derate_incremental_adjust_additive_mode	
	<p><b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes</p>
timing_derate_ocv_reference_point	
	<p>Allows specification of reference point for OCV factors</p> <p><b>Type:</b> <a href="#">int</a>  <b>Default:</b> 1  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">timing_derate_ocv_reference_point</a></p>
timing_derate_spatial_distance_unit	
	<p>Set the distance unit.</p> <p><b>Type:</b> <a href="#">enum</a>  <b>Enum Values:</b> default 1um 1nm  <b>Default:</b> default  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">timing_derate_spatial_distance_unit</a></p>
timing_disable_bus_contention_check	
	<p>Checks for setup and hold violations in three-state bus designs</p> <p><b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">timing_disable_bus_contention_check</a></p>
timing_disable_clock_period_checks	

	<p>When set to true, disables timing model clock period checks during timing analysis</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_clock_period_checks</a></p>
<b>timing_disable_constant_propagation_for_sequential_cells</b>	
	<p>When set to true, disables constant prop. across sequential cells if sequential_prop global is false</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_constant_propagation_for_sequential_cells</a></p>
<b>timing_disable_drv_report_on_constant_nets</b>	
	<p>Disables DRV checks for nets having disabled constant propagation:</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_drv_report_on_constant_nets</a></p>
<b>timing_disable_floating_bus_check</b>	
	<p>When set to true, disables propagation of minimum delay through three state disable timing arcs and maximum delay through three state enable arcs. These checks are only valid during floating bus conditions</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_floating_bus_check</a></p>
<b>timing_disable_genclk_combinational_blocking</b>	
	<p>Disables blocking of generated clocks with '-combinational' option which are downstream of another generated clock</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_genclk_combinational_blocking</a></p>
<b>timing_disable_inferred_clock_gating_checks</b>	

	<p>When set to true, disables clock gating checks that are inferred on combinational elements in the clock path. Explicit clock gating checks that are described in the timing library are not affected by this global variable</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_inferred_clock_gating_checks</a></p>
<b>timing_disable inout output side timing checks</b>	
	<p>When set to false, timing checks on both the input and output sides of the bidirectional pin are analyzed</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable inout output side timing checks</a></p>
<b>timing_disable internal inout cell paths</b>	
	<p>When set to false, enables internal bidirectional feedback paths that are completely contained in one instance</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable internal inout cell paths</a></p>
<b>timing_disable internal inout net arcs</b>	
	<p>When set to true, this global disables internal bidirectional feedback paths that span multiple instances</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable internal inout net arcs</a></p>
<b>timing_disable is flop backward compatibility</b>	
	<p>Global to add backward compatibility to is_flop attribute</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p>
<b>timing_disable lib pulse width checks</b>	

	<p>When set to true, disables timing model pulse width checks during timing analysis</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_lib_pulse_width_checks</a></p>
<p><b>timing_disable_library_data_to_data_checks</b></p>	
	<p>When set to true, this global disables data-to-data checks that are coded in the library as non-sequential timing checks</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_library_data_to_data_checks</a></p>
<p><b>timing_disable_library_tieoffs</b></p>	
	<p>Disables constant functions in a library</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_library_tieoffs</a></p>
<p><b>timing_disable_model_parasitics</b></p>	
	<p>Disable write out of parasitics data into model. Load will use the original spefs.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
<p><b>timing_disable_netlist_constants</b></p>	
	<p>When set to true, ignores constants defined in the Verilog netlist</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_netlist_constants</a></p>
<p><b>timing_disable_nochange_checks</b></p>	
	<p>When set to true, disables no change timing model checks during timing analysis</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_nochange_checks</a></p>
<p><b>timing_disable_non_sequential_checks</b></p>	

	<p>When set to true, disables the timing arcs between any data-to-clock or clock-to-clock checks</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_non_sequential_checks</a></p>
<b>timing_disable_output_as_clock_port</b>	
	<p>Controls clock to output port to be treated as data or clock irrespective of constraints set on the port</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_output_as_clock_port</a></p>
<b>timing_disable_parallel_arcs</b>	
	<p>to control enabling/disabling both CTE's parallel arc reduction, and the related task compression on the AAE side. Setting this variable to 'true' should yield AAE task compression mode '2'. Setting it to 'false' will result in task compression mode '0'</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p>
<b>timing_disable_pulse_width_same_edge_si_cppr_mode</b>	
	<p>Enables SI CPPR credit up to the last divergent pin for pulse width checks for zero width pulse clocks</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p>
<b>timing_disable_report_header_info</b>	
	<p>Controls whether timing reports are generated using a common report header.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_report_header_info</a></p>
<b>timing_disable_retime_clock_path_slew_propagation</b>	
	<p>Controls whether analysis is performed on data or clock paths</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_retime_clock_path_slew_propagation</a></p>

timing_disable_sdf_retain_arc_merging	Controls handling of retain arcs in SDF2.1 <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_disable_sdf_retain_arc_merging</a>
timing_disable_skew_checks	When set to true, disables library skew checks for timing analysis <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_disable_skew_checks</a>
timing_disable_test_signal_arc	When set to true, timing analysis will not analyze the signal arcs coming from or going to the test pin <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_disable_test_signal_arc</a>
timing_disable_timing_model_latch_inferencing	Controls whether latch behavior is inferred for cell descriptions tagged with the Liberty timing_model_type attribute, including all values: abstracted, extracted, or qtm <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_disable_timing_model_latch_inferencing</a>
timing_disable_tristate_disable_arcs	When set to true, disables all 0/1->Z transitions of tristate arcs during timing analysis <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_disable_tristate_disable_arcs</a>
timing_disable_user_data_to_data_checks	

	<p>When set to true, disables data-to-data checks that are created by the <code>set_data_check</code> command</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_disable_user_data_to_data_checks</a></p>
<b>timing_driving_cell_override_library</b>	
	<p>Controls the selection of library cells specified using the <code>set_driving_cell</code> command</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_driving_cell_override_library</a></p>
<b>timing_enable_aocv_slack_based</b>	
	<p>Enable aocv analysis using slack based method</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_aocv_slack_based</a></p>
<b>timing_enable_backward_compatible_path_adjust_mode</b>	
	<p>When set to false, enables new <code>set_path_adjust</code> handling mechanism.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_backward_compatible_path_adjust_mode</a></p>
<b>timing_enable_case_analysis_conflict_warning</b>	
	<p>Controls to report case analysis conflict warnings to <code>CTE_constant_mismatch.rpt</code> file.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_case_analysis_conflict_warning</a></p>
<b>timing_enable_clock_phase_based_rise_fall_derating</b>	
	<p>Determines the interpretation of edge-specific derating factors for clock paths, specified using the <code>set_timing_derate -rise/-fall</code> parameters</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_clock_phase_based_rise_fall_derating</a></p>

<code>timing_enable_clock_to_clock_clock_gating_check</code>	When set to true, performs clock to clock gating checks at gating elements <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_enable_clock_to_clock_clock_gating_check</a>
<code>timing_enable_data_through_clock_gating</code>	When set to false, blocks signals arriving on the enable of the clock-gating check <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_enable_data_through_clock_gating</a>
<code>timing_enable_derating_for_pulse_width_checks</code>	Applies check derating for pulse width checks <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_enable_derating_for_pulse_width_checks</a>
<code>timing_enable_early_late_data_slews_for_setuphold_mode_checks</code>	When set to true, the global variable enables propagation of early and late slews on data paths. Delay calculation then uses these early and late slews to calculate timing checks. You can use this global in simultaneous setup and hold mode only. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_enable_early_late_data_slews_for_setuphold_mode_checks</a>
<code>timing_enable_genclk_divide_by_inherit_parent_duty_cycle</code>	Controls inheritance of duty cycle from master clock for generated clocks with divide by option <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_enable_genclk_divide_by_inherit_parent_duty_cycle</a>
<code>timing_enable_genclk_source_path_register_limit</code>	

	<p>Limits generated clock source latency path to traverse across one register only</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_genclk_source_path_register_limit</a></p>
<b>timing_enable_generated_clock_edge_based_source_latency</b>	
	<p>Controls how the software chooses generated clock source latency paths</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_generated_clock_edge_based_source_latency</a></p>
<b>timing_enable_get_obj_escaped_name_backward_compatible</b>	
	<p>Enables printing of escape characters in the get_object_name command output.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_get_obj_escaped_name_backward_compatible</a></p>
<b>timing_enable_hierarchical_get_nets_support</b>	
	<p>Enable the hierarchical segment support for get_nets.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_hierarchical_get_nets_support</a></p>
<b>timing_enable_latch_thru_mode</b>	
	<p>Enable the latch thru analysis mode in which timing paths can propagate across latches, depending on their arrival time with respect to the latch transparency window.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_enable_latency_through_clock_gating</b>	
	<p>Controls propagation of latency phases across a clock gating element.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_latency_through_clock_gating</a></p>
<b>timing_enable_min_max_delay_segmentation</b>	

	<p>Enables path segmentation in the presence of set_min/max_delay -from/-to</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_min_max_delay_segmentation</a></p>
<b>timing_enable_mmmc_loop_breaking</b>	
	<p>When set to true, loop breaking is handled independently per analysis view</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_mmmc_loop_breaking</a></p>
<b>timing_enable_model_constraint_warnings</b>	
	<p>Enable warnings coming from boundary modeled blocks while constraint processing.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
<b>timing_enable_multi_drive_net_reduction_with_assertions</b>	
	<p>Controls whether multi-drive net reduction (if enabled) will attempt to reduce multi-drive nets that also have only either/both set_annotated_delay or set_annotated_transitions assertions present. By default, any assertions present on different drivers of multi-drive nets will prevent reduction of the multi-drive net.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none all delay</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_multi_drive_net_reduction_with_assertions</a></p>
<b>timing_enable_multi_frequency_latch_analysis</b>	
	<p>Enables multi-frequency latch timing analysis of the latch time borrowing for when a data signal coming to a latch is controlled by a clock with a frequency different to a clock of the latch enabling signal</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_multi_frequency_latch_analysis</a></p>
<b>timing_enable_multi_threaded_reporting</b>	

	<p>Enables multi-threaded reporting</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_multi_threaded_reporting</a></p>
<b>timing_enable_multicycle_data_check_compatibility</b>	
	<p>Enables checking for SDC compatible data checks when set_multicycle_path -start parameter is specified</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_multicycle_data_check_compatibility</a></p>
<b>timing_enable_path_delay_to_unconstrained_endpoints_compatibility</b>	
	<p>When set to true, does not constrain path with path delay if path ends at unconnected input pin of combo cell.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_path_delay_to_unconstrained_endpoints_compatibility</a></p>
<b>timing_enable_pessimistic_cppr_for_reconvergent_clock_paths</b>	
	<p>When set to true, enables pessimistic cppr adjustment for re-convergent clock paths</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_pessimistic_cppr_for_reconvergent_clock_paths</a></p>
<b>timing_enable_power_ground_constants</b>	
	<p>Controls whether case analysis is inferred from power and ground rail connections.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_power_ground_constants</a></p>
<b>timing_enable_preset_clear_arcs</b>	

	Determines whether timing arcs are created to model the transition to active state (assertion) of the preset or clear pin, and the subsequent transition of the output to controlled state <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_enable_preset_clear_arcs</a>
<b>timing_enable_pulse_latch</b>	
	Enables pulse-latch analysis <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_enable_pulse_latch</a>
<b>timing_enable_report_cppr_clock_style_check_compatibility</b>	
	setting global to true considers clock pin in clock style checks for common pin <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes
<b>timing_enable_si_cppr</b>	
	Enables more accurate CPPR analysis when incremental delays are present and the <code>timing_remove_clock_reconvergence_pessimism</code> global variable is set to true <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_enable_si_cppr</a>
<b>timing_enable_simultaneous_setup_hold_mode</b>	
	Controls whether setup and hold checks are analyzed separately, or together on the same timing graph <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_enable_simultaneous_setup_hold_mode</a>
<b>timing_enable_spatial_derate_mode</b>	
	When set to true, enables spatial derate feature. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_enable_spatial_derate_mode</a>

timing_enable_timing_window_pessimism_removal	<p>When set to true, removes common clock path pessimism between aggressor and victim pins in the design</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_timing_window_pessimism_removal</a></p>
timing_enable_tristate_clock_gating	<p>When this global is set to true, inferred gated-clock checks are added when clock and data signals converge through the tristate enable and data input of tristate buffers</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_tristate_clock_gating</a></p>
timing_enable_uncertainty_for_clock_checks	<p>Considers clock uncertainty when performing clock checks.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_uncertainty_for_clock_checks</a></p>
timing_enable_uncertainty_for_pulse_width_checks	<p>When set to true, considers clock uncertainty when performing minimum pulse width checks</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_enable_uncertainty_for_pulse_width_checks</a></p>
timing_extract_model_aocv_mode	<p>This global sets the AOCV mode to be used during model extraction</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none graph_based path_based</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_aocv_mode</a></p>
timing_extract_model_case_analysis_in_library	

	<p>When set to false, specifies that port propagated constants are written to the generated constraints file</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_case_analysis_in_library</a></p>
timing_extract_model_check_arcs_as_lvf	<p>With this global turned on, check arcs will be modeled as LVF arcs</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_check_arcs_as_lvf</a></p>
timing_extract_model_compute_latency_paths_with_missing_source_transitions	<p>When set to true, will extract the latency paths having missing source transitions.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
timing_extract_model_consider_design_level_drv	<p>When set to false, specifies that user asserted design level DRVs should not be considered while writing to the extracted timing model</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_consider_design_level_drv</a></p>
timing_extract_model_disable_cycle_adjustment	<p>When set to true, the cycle adjustment for the multicycle-paths that could not be pushed out, is disabled</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_disable_cycle_adjustment</a></p>
timing_extract_model_exhaustive_validation_dir	<p>Specifies the output directory where the validation reports will be written</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_exhaustive_validation_dir</a></p>

timing_extract_model_exhaustive_validation_mode	<p>Enables ETM validation at the minimum and maximum indices of the slew / load indices</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_exhaustive_validation_mode</a></p>
timing_extract_model_gating_as_nochange_arc	<p>When set to false, disables conversion of clock gating checks to nochange arcs in the extracted timing model</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_gating_as_nochange_arc</a></p>
timing_extract_model_ideal_clock_latency_arc	<p>Specifies if latency arc from ideal master clock need to be extracted in timing model</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_ideal_clock_latency_arc</a></p>
timing_extract_model_include_applied_load_in_characterization_range	<p>When set to true, specifies that actual load visible to timer, will be included in the load characterization range for path endpoints</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_include_applied_load_in_characterization_range</a></p>
timing_extract_model_include_applied_slew_in_characterization_range	<p>When set to true, specifies that actual timer slew must be included in the characterization range for timing model.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_include_applied_slew_in_characterization_range</a></p>
timing_extract_model_max_feedthru_characterization_load	

	<p>Load specified will be used by model extractor for feed through path characterization.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p>
	<p><b>timing_extract_model_non_borrowing_latch_path_as_setup</b></p>
	<p>If turned ON, models the non borrowing interface latch paths as setup check.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_non_borrowing_latch_path_as_setup</a></p>
	<p><b>timing_extract_model_slew_propagation_mode</b></p>
	<p>Specifies the type of slew propagation to use for generating extracted timing model</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> worst_slew path_based_slew</p> <p><b>Default:</b> worst_slew</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_slew_propagation_mode</a></p>
	<p><b>timing_extract_model_write_clock_checks_as_arc</b></p>
	<p>Allows timing model to write min pulse width or min period checks as arcs.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_write_clock_checks_as_arc</a></p>
	<p><b>timing_extract_model_write_clock_checks_as_scalar_tables</b></p>
	<p>Allows timing model to write min pulse width or min period checks as scalar arcs.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_write_clock_checks_as_scalar_tables</a></p>
	<p><b>timing_extract_model_write_lvf</b></p>
	<p>When set to true, generated ETM contains LVF model.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_write_lvf</a></p>
	<p><b>timing_extract_model_write_min_max_clock_tree_path</b></p>

	<p>When set to true, writes the min max worst latency for each clock source.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_extract_model_write_min_max_clock_tree_path</a></p>
<b>timing_generate_normalized_driver_waveform</b>	
	<p>To generate ndw if it is not defined in the library.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_generate_normalized_driver_waveform</a></p>
<b>timing_generated_clocks_allow_nested_assertions</b>	
	<p>Enables clock latency handling for nested generated clocks created on the same timing pin as their master clocks</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_generated_clocks_allow_nested_assertions</a></p>
<b>timing_generated_clocks_inherit_ideal_latency</b>	
	<p>When set to true, makes generated clocks to inherit parent's ideal network latency</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_generated_clocks_inherit_ideal_latency</a></p>
<b>timing_get_of_objects_hier_compatibility</b>	
	<p>When set to true, the get_pins -of_objects parameter will return hierarchical leaf pins connected to the specified objects</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_get_of_objects_hier_compatibility</a></p>
<b>timing_hier_obj_name_compatibility</b>	

	<p>Controls how hierarchical delimiters are interpreted in the search pattern, when the -hier parameter is used with the get_* collection command</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_hier_obj_name_compatibility</a></p>
<b>timing_ignore_lumped_rc_assertions</b>	
	<p>When set to false, the set_load and set_resistance values override the actual extracted representation</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_ignore_lumped_rc_assertions</a></p>
<b>timing_inter_power_domain_derate_flow_use_path_segment_delay_difference</b>	
	<p>When set to true, aocv-pba calculation with launch/capture path segment delay difference based computation using interface power domain (ipd) derate offsets is enabled</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_inter_power_domain_derate_flow_use_path_segment_delay_difference</a></p>
<b>timing_io_use_clock_network_latency</b>	
	<p>Controls whether network latency of a reference clock is added or not to the data arrival time on the port</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> always ideal</p> <p><b>Default:</b> ideal</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_io_use_clock_network_latency</a></p>
<b>timing_library_build_async_deassert_arc</b>	
	<p>Controls whether input to output arcs from the preset or clear pins transitioning to inactivestate are included when the timing system is initialized</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_library_build_async_deassert_arc</a></p>
<b>timing_library_ccs_receiver_weight_factor</b>	

	<p>Specifies the weight factor to calculate the rise/fall capacitance range values from ccs receiver capacitance model</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 1.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_library_ccs_receiver_weight_factor</a></p>
<b>timing_library_convert_async_setuphold_to_recrem</b>	
	<p>Controls whether single-edged setup and hold checks on asynchronous pins in the Liberty library are inferred as recovery and removal checks. This is mainly to support older modeling styles in legacy libraries.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_library_convert_async_setuphold_to_recrem</a></p>
<b>timing_library_enable_advanced_capacitance_support</b>	
	<p>Enables support for N-piece CCS receiver capacitance and ecm_capacitance_set groups in libraries</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_library_enable_advanced_capacitance_support</a></p>
<b>timing_library_generated_clock_use_group_name</b>	
	<p>When set to true, the software uses the generated_clock group name when creating a generated clock from a library-generated clock group</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_library_generated_clock_use_group_name</a></p>
<b>timing_library_hold_constraint_corner_sigma_multiplier</b>	
	<p>User control multiplier to generate constraint table applied for hold arc.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_library_hold_constraint_corner_sigma_multiplier</a></p>
<b>timing_library_hold_sigma_multiplier</b>	

	User control multiplier to generate constraint table applied for hold arc. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_library_hold_sigma_multiplier</a>
<b>timing_library_infer_async_pins_from_timing_arcs</b>	
	This global marks the pins as async pins based on the timing arcs associated with the pin. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_library_infer_async_pins_from_timing_arcs</a>
<b>timing_library_infer_cap_range_from_ccs_receiver_model</b>	
	When true infer the rise/fall capacitance range values from ccs receiver capacitance model <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_library_infer_cap_range_from_ccs_receiver_model</a>
<b>timing_library_infer_cap_range_from_ecsm_receiver_model</b>	
	When this global is enabled would infer cap range from ecm capacitance group of library. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_library_infer_cap_range_from_ecsm_receiver_model</a>
<b>timing_library_infer_socv_from_aocv</b>	
	Infer sensitivity data from AOCV libraries <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
<b>timing_library_interpolate_drv_values</b>	
	Allows the software to use a range of trilib DRV values for performing delay calculations <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_library_interpolate_drv_values</a>
<b>timing_library_read_ccs_noise_data</b>	

	can read ccs noise construct from library when enabled. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_library_read_ccs_noise_data</a>
<b>timing_library_read_without_ecsm</b>	
	Switch off loading of ECSM data <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_library_read_without_ecsm</a>
<b>timing_library_read_without_power</b>	
	can read library without power by setting this global to true <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_library_read_without_power</a>
<b>timing_library_read_without_sensitivity</b>	
	Switch off loading of ECSM timing sensitivity data <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_library_read_without_sensitivity</a>
<b>timing_library_scale_aocv_to_socv_to_n_sigma</b>	
	AOCV derates are expected to be derived based on 3-sigma variation <b>Type:</b> <a href="#">double</a> <b>Default:</b> 3.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_library_scale_aocv_to_socv_to_n_sigma</a>
<b>timing_library_setup_constraint_corner_sigma_multiplier</b>	
	User control multiplier to generate constraint table using sigma values applied for setup arc. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_library_setup_constraint_corner_sigma_multiplier</a>
<b>timing_library_setup_sigma_multiplier</b>	

	User control multiplier to generate constraint table using sigma values applied for setup arc. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_library_setup_sigma_multiplier</a>
<b>timing_library_term_voltage_from_lib_pin</b>	
	Use Library pin voltage for reporting the term voltage. <b>Type:</b> <a href="#">int</a> <b>Default:</b> 0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_library_term_voltage_from_lib_pin</a>
<b>timing_library_zero_negative_timing_check_arcs</b>	
	When true check for negative values in timing arcs <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_library_zero_negative_timing_check_arcs</a>
<b>timing_model_netlist_exclude_dummy</b>	
	Whether to exclude dummy modules from model netlist <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
<b>timing_multi_frequency_clock_rounding_factor</b>	
	Rounds off irrational numbers so that they can be read appropriately <b>Type:</b> <a href="#">double</a> <b>Default:</b> 1e-05 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_multi_frequency_clock_rounding_factor</a>
<b>timing_normalized_driver_waveform_clip_linear_part</b>	
	To control the clipping of the generated ndw which is generated by the global timing_generate_normalized_driver_waveform. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_normalized_driver_waveform_clip_linear_part</a>
<b>timing_normalized_driver_waveform_weight_factor</b>	

	Decides the weight factor for the exponential and the linear part in the waveform generated by the global timing_generate_normalized_driver_waveform. <b>Type:</b> double <b>Default:</b> 0.5 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_normalized_driver_waveform_weight_factor</a>
timing_nsigma_multiplier	Controls sigma multiplier to be used in SOCV mode <b>Type:</b> double <b>Default:</b> 3.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_nsigma_multiplier</a>
timing_null_collection_return_compatibility	Allows you to migrate previous release scripts to the new use model <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_null_collection_return_compatibility</a>
timing_path_based_enable_exhaustive_depth_bounded_by_gba	Enable the tool to bound the PBA exhaustive analysis by next worst GBA slack incase the depth is exhausted for any given endpoint <b>Type:</b> bool <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_path_based_enable_exhaustive_depth_bounded_by_gba</a>
timing_path_based_enable_report_launch_clock_path	set it to false to skip reporting launch clock path in pba path_type full report <b>Type:</b> bool <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_path_based_enable_report_launch_clock_path</a>
timing_path_based_enable_verbose_mode	

	<p>controls the verbosity of path based analysis messages printed during and at the end of the analysis</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> 0 1 2 true false</p> <p><b>Default:</b> 1</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_path_based_enable_verbose_mode</a></p>
<b>timing_path_based_exhaustive_enable_design_coverage</b>	
	<p>Enables the exhaustive path based analysis to evaluate all violating endpoints</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_path_based_exhaustive_enable_design_coverage</a></p>
<b>timing_path_based_exhaustive_max_paths_limit</b>	
	<p>Set the maximum number of paths which can be retimed during exhaustive path based analysis</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 2000000</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_path_based_exhaustive_max_paths_limit</a></p>
<b>timing_path_based_low_memory_mode</b>	
	<p>A lower value for this variable will reduce the peak memory footprint of path based analysis (PBA) at the cost of some addition runtime.</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 10.0</p> <p><b>Edit:</b> Yes</p>
<b>timing_pba_exhaustive_path_nworst_limit</b>	
	<p>Specify the nworst exhaustive limit to be honored by tool during PBA exhaustive limit</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 10000</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_pba_exhaustive_path_nworst_limit</a></p>
<b>timing_prefix_module_name_with_library_generated_clock</b>	

	<p>When set to true, the software appends the instance name to the clock pin name when creating a generated clock</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_prefix_module_name_with_library_generated_clock</a></p>
timing_propagate_latch_data_uncertainty	<p>When set to true, uses the clock phase associated with a flush latch's data pin as the from clock phase for downstream uncertainty timing calculations</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_propagate_latch_data_uncertainty</a></p>
timing_property_arrival_window_enable_tcl_dict_format	<p>When set to TRUE, new format for the arrival_windows property will be used to print.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
timing_property_return_null_collection_with_quiet	<p>Enables returning properties values for all objects when -quiet option is used in get_property</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
timing_rail_swing_checks_high_voltage_threshold	<p>user to specify voltage thresholds for high rail swing checks</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.95</p> <p><b>Edit:</b> Yes</p>
timing_rail_swing_checks_low_voltage_threshold	<p>user to specify voltage thresholds for low rail swing checks</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> 0.05</p> <p><b>Edit:</b> Yes</p>
timing_recompute_sdf_in_setuphold_mode	

	<p>Controls the recomputing of SDF delays when the software is in simultaneous setup and hold analysis mode</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_recompute_sdf_in_setuphold_mode</a></p>
<b>timing_reduce_multi_drive_net_arcs</b>	
	<p>Controls the reduction of the number of net arcs created for timing analysis for nets driven by parallel buffers</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_reduce_multi_drive_net_arcs</a></p>
<b>timing_reduce_multi_drive_net_arcs_threshold</b>	
	<p>Sets a threshold number used by the tool to trigger the reduction of timing arcs of nets driven by parallel buffers</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 10000</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_reduce_multi_drive_net_arcs_threshold</a></p>
<b>timing_report_backward_compatible_max_paths_reporting</b>	
	<p>When set to false, worst max_paths across all the groups are reported (with each endpoint paths limited to nworst)</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_backward_compatible_max_paths_reporting</a></p>
<b>timing_report_clock_pin_as_begin_point</b>	
	<p>Enable whether to show CLK as start point</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_clock_pin_as_begin_point</a></p>
<b>timing_report_constraint_enable_extended_drv_format</b>	

	<p>Enables reporting of report_constraint as per clock/data phases and rise/fall</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_constraint_enable_extended_drv_format</a></p>
<b>timing_report_disable_backward_compatible_required_borrow_mode</b>	
	<p>Setting this to true would turn on slack based worst causinfo instead of worst casing required times</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_report_disable_backward_compatible_socv_cppr_in_time_given</b>	
	<p>turning global on will handle sigma in cppr in time borrow and time given value</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_report_drv_enable_clock_source_as_clock</b>	
	<p>Enables clock drv for pure clock source path in place of data drv</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_report_drv_enable_frequency_per_view</b>	
	<p>Enables view based frequency drv flow</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_drv_enable_frequency_per_view</a></p>
<b>timing_report_drv_enable_slew_threshold_scaling</b>	
	<p>Enables transition constraints scaling as per slew threshold</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_report_enable_cppr_point</b>	

	<p>Enable Cppr Point reporting in report timing command</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_enable_cppr_point</a></p>
<b>timing_report_enable_flag_field_symbols</b>	
	<p>Enables reporting of Instance/Net related bits in report_timing Flags column</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_enable_flag_field_symbols</a></p>
<b>timing_report_enable_markers</b>	
	<p>Enables marker for report_timing for Pin/timing points columns</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_enable_markers</a></p>
<b>timing_report_enable_max_capacitance_drv_for_constant_nets</b>	
	<p>Enables max capacitance DRV checks for nets having disabled constant propagation</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_enable_max_capacitance_drv_for_constant_nets</a></p>
<b>timing_report_enable_max_path_limit_warning</b>	
	<p>warning message if max_paths option specified is not enough for coverage</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_enable_max_path_limit_warning</a></p>
<b>timing_report_enable_max_paths_per_group</b>	
	<p>This global controls whether or not group-based mode semantics are used when -group and -max_paths are used with report_timing.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_report_enable_merged_path_count</b>	

	<p>Enable slack-sorted path number printing in merged timing reports</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_report_enable_si_debug</b>	
	<p>For decision regarding SI attribute debugging through path collection objects</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_enable_si_debug</a></p>
<b>timing_report_enable_unique_pins_multiple_capture_clock_paths</b>	
	<p>enables reporting different paths w.r.t ref clocks in unique_pins</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_report_enable_verbose_ssta_mode</b>	
	<p>Enables new format for header in report_timing SOCV mode</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_enable_verbose_ssta_mode</a></p>
<b>timing_report_fields</b>	
	<p>Specifies a report_timing format</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> instance arc cell delay arrival required</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_fields</a></p>
<b>timing_report_generated_clock_info</b>	
	<p>When set to true (the default), generated clock information is automatically added to the report if generated clocks are encountered in either the launching or latching clock paths</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_generated_clock_info</a></p>
<b>timing_report_group_based_mode</b>	

	<p>Groups paths by clock domain</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_group_based_mode</a></p>
<b>timing_report_max_transition_check_using_nsigma_slew</b>	
	<p>Enables report_constraintdrv checking to use mean+nsigma slew values in socv flow</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_max_transition_check_using_nsigma_slew</a></p>
<b>timing_report_property_fastest_clock_consider_data_phase</b>	
	<p>When on, it will consider data phase also while finding the fastest clock.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_report_pulse_width_matching_launch_capture_paths</b>	
	<p>Reports only those pulse_width paths that have same pins on launch and capture path</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_report_redirect_message_types</b>	
	<p>Redirect reporting messages to report file</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> info warning error all none</p> <p><b>Default:</b> none</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_redirect_message_types</a></p>
<b>timing_report_reset_persistent_group_based_cache</b>	
	<p>Allow resetting of persistent cache during group based reporting</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p>
<b>timing_report_retime_formatting_mode</b>	

	<p>This variable can be used to manage the retiming fields in reporting format. Based upon given setting it would automatically replaces (or add) the default columns with respective retiming columns. For example in case of delay column it will add(or replace) the 'Retime Delay' automatically.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> manual retime_compare retime_replace</p> <p><b>Default:</b> manual</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_retime_formatting_mode</a></p>
timing_report_skip_constraint_loop_check	<p>skip reporting of loop in case timing graph inside loop is broken due to create_clock, set_input_delay, set_output_delay defined inside the loop</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_skip_constraint_loop_check</a></p>
timing_report_split_other_end_arrival	<p>This global splits the printing of other end arrival time in timing reports into other end path delay and clock edge time.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
timing_report_timing_header_detail_info	<p>Controls whether the report_timing reports are generated using the default or extended report header</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> default extended</p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_timing_header_detail_info</a></p>
timing_report_unconstrained_path_early_late_header	<p>When set to true, prints late and early type for unconstrained path</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_unconstrained_path_early_late_header</a></p>
timing_report_unconstrained_paths	

	<p>When set to true, the report_timing command reports unconstrained paths if it cannot find a constrained path to report</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_unconstrained_paths</a></p>
<b>timing_report_use_receiver_model_capacitance</b>	
	<p>Uses ECSM pin capacitance values for load or DRV calculation</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_report_use_worst_parallel_cell_arc</b>	
	<p>When set to false, setting the -nworst parameter reports several paths by selecting parallel arcs in the library cell between two pins</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_report_use_worst_parallel_cell_arc</a></p>
<b>timing_report_write_detailed_sigma_split</b>	
	<p>Setting this to true would turn on reporting of correlated and other components in required fields</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
<b>timing_resolve_driver_conflicts</b>	
	<p>Resolves values of nets having multiple drivers</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> conservative aggressive</p> <p><b>Default:</b> aggressive</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_resolve_driver_conflicts</a></p>
<b>timing_scaling_for_negative_checks</b>	

	<p>Modifies the scaling of the negative timing analysis check value</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> default divider multiplier</p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_scaling_for_negative_checks</a></p>
timing_scaling_for_negative_delays	<p>Modifies the scaling of the negative delay value to be used during timing analysis</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> default divider multiplier</p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_scaling_for_negative_delays</a></p>
timing_sdf_adjust_negative_setuphold	<p>Controls how Setup and Hold check values are adjusted when both are initially negative.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_sdf_adjust_negative_setuphold</a></p>
timing_sdf_enable_setuphold_scond_ccond	<p>To enable proper generation of SDF (Standard Delay Format) with scond and ccond qualifiers on SETUPHOLD and RECREM timing checks</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_sdf_enable_setuphold_scond_ccond</a></p>
timing_self_loop_paths_no_skew_max_depth	<p>Identifies self-loop paths at the specified depth.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 10</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_self_loop_paths_no_skew_max_depth</a></p>
timing_self_loop_paths_no_skew_max_slack	

	<p>Identifies self-loop paths at the specified threshold</p> <p><b>Type:</b> double</p> <p><b>Default:</b> 0.0</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_self_loop_paths_no_skew_max_slack</a></p>
<b>timing_set_clock_source_to_output_as_data</b>	
	<p>When set to true, causes a clock source path leading to an output or bidi port to be treated as a data path if there is a set_output_delay or set_data_check assertion on the port</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_set_clock_source_to_output_as_data</a></p>
<b>timing_socv_rc_variation_mode</b>	
	<p>Enable interconnect variation mode in SOCV mode</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_socv_rc_variation_mode</a></p>
<b>timing_socv_statistical_min_max_mode</b>	
	<p>Controls worstcasing mode to be used for SOCV</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> statistical three_sigma_bounded mean_and_sigma_bounded mean_and_three_sigma_bounded max_mean_and_sigma</p> <p><b>Default:</b> mean_and_three_sigma_bounded</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_socv_statistical_min_max_mode</a></p>
<b>timing_socv_view_based_nsigma_multiplier_mode</b>	
	<p>Enables setting of view-based separate setup and hold sigma multipliers</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_socv_view_based_nsigma_multiplier_mode</a></p>
<b>timing_spatial_derate_chip_size</b>	

	<p><b>Type:</b> double <b>Default:</b> 1e+30 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_spatial_derate_chip_size</a></p>
timing_spatial_derate_distance_mode	
	<p><b>Type:</b> enum <b>Enum Values:</b> bounding_box chip_size <b>Default:</b> bounding_box <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_spatial_derate_distance_mode</a></p>
timing_suppress_escape_characters	
	<p>Suppresses the reporting of escape characters in timing object names <b>Type:</b> bool <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_suppress_escape_characters</a></p>
timing_suppress_ilm_constraint_mismatches	
	<p>When set to true, the software suppresses all error and warning messages related to objects not found when loading SDC constraint files for the ILM flow <b>Type:</b> bool <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_suppress_ilm_constraint_mismatches</a></p>
timing_time_unit	
	<p>This value is passed to set_library_unit -time to set the time units used in timing library and .sdc files and timing reports. Legal values are none, 1ns, 1ps, 10ps, 100ps. <b>Type:</b> string <b>Default:</b> none <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_time_unit</a></p>
timing_use_clock_pin_attribute_for_clock_net_marking	

	To allow the propagation of clocks to pins with clock attributes regardless of the presence of check arcs or trigger arcs at the pins <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_use_clock_pin_attribute_for_clock_net_marking</a>
timing_use_incremental_si_transition	When set to true, enables usage of incremental slew during DRV violation reporting <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes
timing_use_latch_early_launch_edge	Enables the latch use early launch edge feature. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_use_latch_early_launch_edge</a>
timing_use_latch_time_borrow	When set to false, does not consider time borrowing during timing analysis. Time borrowing is the amount of time borrowed by a previous logic <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">timing_use_latch_time_borrow</a>
timing_waveform_aware_pulse_width_checks_high_voltage_level	User to specify high voltage level to be used for waveform aware pulse-width checks <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.95 <b>Edit:</b> Yes
timing_waveform_aware_pulse_width_checks_low_voltage_level	User to specify low voltage level to be used for waveform aware pulse-width checks <b>Type:</b> <a href="#">double</a> <b>Default:</b> 0.05 <b>Edit:</b> Yes
timing_write_sdf_no_escape_backslash	

	<p>Supports various patterns of the escape character.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">timing_write_sdf_no_escape_backslash</a></p>
top_sdps	<p>Short-cut to all top level structured data path (sdp) objects.</p> <p><b>Type:</b> <a href="#">obj(sdp)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
trace_obj_macro_pins	<p>specify macro pin name patterns in regular expression</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">trace_obj_macro_pins</a></p>
trace_obj_max_fanin_fanout	<p>Specify the maximum number of a pin's fanin/fanout,a pin will be ignored in tracing connectivity if its fanin/fanout larger than the specified number</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 1000</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">trace_obj_max_fanin_fanout</a></p>
trace_obj_register_inputs	<p>Specify register input pin names</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">trace_obj_register_inputs</a></p>
trace_obj_register_outputs	<p>Specify register output pin names</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">trace_obj_register_outputs</a></p>
track_patterns	

	<p>Short-cut to all the track_pattern objects in the design.</p> <p><b>Type:</b> <a href="#">obj(track_pattern)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>trim_grids</b>	
	<p>Short-cut to all the trim_grid objects in the design from the LEF TRIMMETALTRACK statement.</p> <p><b>Type:</b> <a href="#">obj(trim_grid)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>ui_precision</b>	
	<p>Specifies the number of significant digits to be displayed in timing reports for data with no specific type.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 3</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">ui_precision</a></p>
<b>ui_precision_capacitance</b>	
	<p>Specifies the number of significant digits to be displayed in timing reports for data of type capacitance.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 3</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">ui_precision_capacitance</a></p>
<b>ui_precision_derating</b>	
	<p>Specifies the number of significant digits to be displayed in timing reports for derating factors such as those specified via set_timing_derate constraints or AOCV derating libraries.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 3</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">ui_precision_derating</a></p>
<b>ui_precision_power</b>	

	<p>Specifies the number of significant digits to be displayed in timing reports for data of type power.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 3</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">ui_precision_power</a></p>
ui_precision_sensitivities	<p>Specifies the number of significant digits to be displayed in timing reports for statistical sensitivity values and SOCV sigma values.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 3</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">ui_precision_sensitivities</a></p>
ui_precision_timing	<p>Specifies the number of significant digits to be displayed for timing reports for delay type values including cell and net delays, transitions, arrival and required times, and slacks.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 3</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">ui_precision_timing</a></p>
via_def_rules	<p>All the via_def_rules defined in the LEF or OpenAccess techfile.</p> <p><b>Type:</b> <a href="#">obj(via_def_rule)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
via_defs	<p>All the via_defs (via master definitions).</p> <p><b>Type:</b> <a href="#">obj(via_def)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
write_db_auto_save_user_globals	

	<p>If true, write_db automatically saves user created Tcl global variables. User globals are defined as any "info globals" names that do not exist at startup (e.g. created by user executed code). See the define_variables command to add or delete specific Tcl variables from the automatic save list.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_db_auto_save_user_globals</a></p>
	<p><b>write_db_binary_timing_constraints</b></p>
	<p>If true, write_db will save timing constraints in binary format. The value of the global should be persistent in subsequent write_db and read_db operations.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_db_binary_timing_constraints</a></p>
	<p><b>write_db_cmd_file_limit</b></p>
	<p>write_db saves the complete .cmd history across multiple sessions in the inn.cmd.gz file inside the save directory up to this file length limit in units of Mb. If it is set to 0, no history is saved at all</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 10</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_db_cmd_file_limit</a></p>
	<p><b>write_db_copy_timing_constraints_always</b></p>
	<p>Specifies whether SDC files are always copied to the DB directory rather than links to external SDC files. By default they are only copied if the constraints were modified.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_db_copy_timing_constraints_always</a></p>
	<p><b>write_db_create_read_file</b></p>
	<p>If true, 'write_db my_db' will also create a 'my_db.read' file with a 'read_db my_db' command inside it. This is a Tcl file that can be passed to the Linux executable to make it easy to load the DB at startup like this: 'innovus -files my_db.read'. For OA usage, it would have the appropriate 'read_db -oa_lib_cell_view {&lt;lib&gt; &lt;cell&gt; &lt;view&gt;}' command inside it.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_db_create_read_file</a></p>

write_db_include_metal_fill_rules	
	<p>specify whether to save metalfill settings  <b>Type:</b> <a href="#">int</a>  <b>Default:</b> 0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">write_db_include_metal_fill_rules</a></p>
write_db_save_unused_lef_block_names	
	<p>Specifies whether to remember a list of unused macros during saving  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">write_db_save_unused_lef_block_names</a></p>
write_def_compress_vias	
	<p>Compress the via statement in SPECIALNETS section. This variable controls write_def to sort vias with two dimension array, so it can use 'DO numX BY numY STEP stepX stepY' statement.  <b>Type:</b> <a href="#">int</a>  <b>Default:</b> 0  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">write_def_compress_vias</a></p>
write_def_hierarchy_delimiter	
	<p>Specify the write_def hierarchy delimiter.  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">write_def_hierarchy_delimiter</a></p>
write_def_include_lef_ndr	
	<p>Output LEF NONDEFAULTRULES in DEF. This variable controls write_def to output LEF nondefault rule information. By default, write_def does not write out nondefaultrules defined in LEF. Set this variable to true to output nondefault rules defined in LEF .  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> false  <b>Edit:</b> Yes  <b>Reference:</b> <a href="#">write_def_include_lef_ndr</a></p>
write_def_include_lef_vias	

	<p>Output LEF vias in DEF. This variable controls write_def to output LEF via information. By default, write_def does not write out via defined in LEF. Set this variable to true to output LEF via.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_def_include_lef_vias</a></p>
<b>write_def_lef_out_version</b>	
	<p>Specify LEF/DEF output version. Possible string value are 5.5, 5.6, 5.7 and 5.8. The default is 5.8.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> 5.5 5.6 5.7 5.8</p> <p><b>Default:</b> 5.8</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_def_lef_out_version</a></p>
<b>write_def_polygon_die_area</b>	
	<p>By default write_def writes out polygon DIEAREA if the design is rectilinear. To write out rectangular DIEAREA along with blockages in cut-out area for a rectilinear design, set this variable to false.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_def_polygon_die_area</a></p>
<b>write_def_stream_check_uncolored</b>	
	<p>Specify whether or not to check and ignore uncolored shapes on DPT layers during DEF out or stream out. It's automatically set to true for TSMC N5 or N3 tech node.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_def_stream_check_uncolored</a></p>
<b>write_lec_dft_constraints</b>	
	<p>This attribute is a TCL dict and holds the LEC dft pin constraints from the last LEC run by Genus. It is passed forward through write_design. The write_do_lec command will automatically include this constraints in the do file.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_lec_dft_constraints</a></p>

#### write\_lec\_directory\_naming\_style

The directory name where 'write\_do\_lec' will write verification files when the 'write\_lec\_files' attribute is 'true'. The directory will be created if it does not already exist, and will overwrite an existing directory of the same name. A %s in the string is replaced with the design name (e.g. it will overwrite the directory for the same design but not for a different design). A %d in the string is replaced with a unique integer to avoid overwriting any existing directory.

**Type:** [string](#)

**Default:** fv/invs/%s

**Edit:** Yes

**Reference:** [write\\_lec\\_directory\\_naming\\_style](#)

#### write\_lec\_files

Specifies whether 'write\_do\_lec' should write intermediate files to the verification directory specified by the 'write\_lec\_directory\_naming\_style' attribute. If false, no files are written.

**Type:** [bool](#)

**Default:** true

**Edit:** Yes

**Reference:** [write\\_lec\\_files](#)

#### write\_lef\_abstract\_customer\_header

Write lef abstract files with customer specified header information.

**Type:** [string](#)

**Default:** ""

**Edit:** Yes

**Reference:** [write\\_lef\\_abstract\\_customer\\_header](#)

#### write\_netlist\_full\_pin\_out

Output all pins.

**Type:** [bool](#)

**Default:** false

**Edit:** Yes

**Reference:** [write\\_netlist\\_full\\_pin\\_out](#)

#### write\_netlist\_port\_association\_style

Do implicit port mapping.

**Type:** [bool](#)

**Default:** false

**Edit:** Yes

**Reference:** [write\\_netlist\\_port\\_association\\_style](#)

#### write\_stream\_allow\_path\_type4

	If false, converts PATHTYPE4 to PATHTYPE0. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">write_stream_allow_path_type4</a>
<b>write_stream_cell_instance_color</b>	
	stream out the instance based color. The instance mask shift is honored in write_stream. When the option is on and -merge option is used, the merged gds files with mask shift suffix must be provided through option -merge. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">write_stream_cell_instance_color</a>
<b>write_stream_cell_master_color</b>	
	stream out the cell based color from innovus color engine. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">write_stream_cell_master_color</a>
<b>write_stream_cell_name_prefix</b>	
	Add a prefix to ALL cell names being written out, use user specified prefix can avoid potential conflict when integrating different macros, which potentially 2 different cells (in 2 different libraries) with the same name. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">write_stream_cell_name_prefix</a>
<b>write_stream_cell_name_suffix</b>	
	Instead of appending color pattern to normal cell names, use user specified suffix. This applies to fixed color shift (flip) pattern only. i.e., only single shift (flip) pattern applied to the design. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes <b>Reference:</b> <a href="#">write_stream_cell_name_suffix</a>
<b>write_stream_check_map_file</b>	

	<p>Check the specified map file. If the objects existed in innovus, but the objects have no objects mapping in map file, print the missed objects mapping and missed objects in log file, only the main objects mapping are checked by the option.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_stream_check_map_file</a></p>
<p><b>write_stream_compatible</b></p>	
	<p>Output instance only is FOREIGN is specified.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_stream_compatible</a></p>
<p><b>write_stream_define_via_name</b></p>	
	<p>Specifies the naming convention that the write_stream command uses for via cells declared in the DEF file.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_stream_define_via_name</a></p>
<p><b>write_stream_ignore_fixed_mask</b></p>	
	<p>Ignore macro FIXEDMASK keywords, enable color flip function.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_stream_ignore_fixed_mask</a></p>
<p><b>write_stream_label_all_pin_shape</b></p>	
	<p>If true, label pin name to its all shapes.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_stream_label_all_pin_shape</a></p>
<p><b>write_stream_merge_append</b></p>	

	<p>Append cell color information in current design to cell geometries that are from merging files. This option is for TSMC 10nm fixed-mask design. It is exclusive with write_stream_ignore_inst_color attribute and write_stream_ignore_inst_cce_color attribute, it will set those two attributes to false automatically when it is set to true.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_stream_merge_append</a></p>
<b>write_stream_oasis_compression</b>	
	<p>CBLOCK compression is partial-selective encryption technology uses OASIS CBLOCK records to encrypt arbitrarily encapsulated sets of data records within an OASIS layout file. REPETITION compression supports an 'array' of cell placements, geometries, or text elements, instead of write each the element separate only different in position, this can save duplicate information for an OASIS layout file size.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> true</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_stream_oasis_compression</a></p>
<b>write_stream_oasis_layer_name</b>	
	<p>Support LAYERNAME in OASIS file.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_stream_oasis_layer_name</a></p>
<b>write_stream_pin_text_orientation</b>	
	<p>Output pin name on the boundary of design to improve readability.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_stream_pin_text_orientation</a></p>
<b>write_stream_remove_nets</b>	
	<p>Don't output nets in the list.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p> <p><b>Reference:</b> <a href="#">write_stream_remove_nets</a></p>
<b>write_stream_snap_to_mfg</b>	

	Snap net's wire to manufacture grid if it is not. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">write_stream_snap_to_mfg</a>
<b>write_stream_stream_convert_rect_to_path</b>	
	When enabled, DEF SPECIALNETS path/rect and FILLS shapes are converted to GDSII/stream PATH data instead of BOUNDARY data. Conversion to path data can result in significantly smaller output database when there are many rectangle shapes (example: after metal fill is included). <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">write_stream_stream_convert_rect_to_path</a>
<b>write_stream_stream_version</b>	
	Specify GDSII version to output. <b>Type:</b> <a href="#">int</a> <b>Default:</b> 3 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">write_stream_stream_version</a>
<b>write_stream_text_size</b>	
	Changes the size of the text used in the text labels. <b>Type:</b> <a href="#">double</a> <b>Default:</b> 1.0 <b>Edit:</b> Yes <b>Reference:</b> <a href="#">write_stream_text_size</a>
<b>write_stream_uniquify_cell_names_prefix</b>	
	Adds a prefix, instead of a suffix, to uniquified cell names. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">write_stream_uniquify_cell_names_prefix</a>
<b>write_stream_via_names</b>	

	Determines the naming convention used for vias declared in the LEF file. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> false <b>Edit:</b> Yes <b>Reference:</b> <a href="#">write_stream_via_names</a>
<b>write_stream_virtual_connection</b>	
	Specifies whether a colon (:) label is appended to pin names for DEF pins with the .extraN syntax and to LEF pins with multiple ports (if -output_macros is specified for LEF pin ports that have disjoint shapes). <b>Type:</b> <a href="#">bool</a> <b>Default:</b> true <b>Edit:</b> Yes <b>Reference:</b> <a href="#">write_stream_virtual_connection</a>

## route\_blockage

### Parent Objects

[design](#), [root](#)

### Definition

Routing blockage

Attribute	Description
density	The density percentage allowed for a partial routing blockage. It causes the global router to only use up to this percent of the routing resource on the layer in the blockage area, so the global router will see higher congestion and put fewer routes on that layer in the area. <b>Type:</b> <a href="#">int</a> <b>Default:</b> "" <b>Edit:</b> Yes
design_rule_width	

**Stylus Common UI Database Object Information**  
**Database Objects--route\_blockage**

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	<p>Specifies that the blockage has an effective width for the purposes of spacing calculations to other shapes on the same layer. A value of 0 indicates that there is no specified design_rule_width value. The design_rule_width and spacing attributes are not allowed to have non-default values at the same time, so the design_rule_width value cannot be changed when the spacing attribute's value is not the default.</p> <p><b>Type:</b> coord</p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p>
inst	<p>The instance that the routing blockage is associated with (equivalent to DEF BLOCKAGES + COMPONENT)</p> <p><b>Type:</b> obj(inst)</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_except_pg_net	<p>Indicates that Power/Ground routing is ignored when checking for DRC violations (including shorts) involving the current shape (equivalent to DEF BLOCKAGES + EXCEPTPGNET)</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
is_pushdown	<p>Indicates that routing blockage has been pushed down from a higher level in the design hierarchy. The idea is that the routing blockage is owned by a higher level(equivalent to DEF BLOCKAGES + PUSHDOWN)</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
layer	<p>layer of blockage</p> <p><b>Type:</b> obj(layer)</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
name	<p>name of blockage</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>

**Stylus Common UI Database Object Information**  
Database Objects--route\_blockage

obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum</a> ( <code>route_blockage</code> ) <b>Default:</b> "" <b>Edit:</b> No
rects	List of non-overlapping rectangles that defines the shape of the route_blockage. If the blockage was defined with a polygon, it is broken up into non-overlapping rectangles <b>Type:</b> <a href="#">rect</a> * <b>Default:</b> "" <b>Edit:</b> No
shapes	List of shapes that define the blockage area <b>Type:</b> <a href="#">obj(shape)</a> * <b>Default:</b> "" <b>Edit:</b> No
spacing	Specifies the minimum spacing allowed between the blockage and any other shape on the same layer (e.g. DEF BLOCKAGES with +SPACING). If there is no spacing value defined, the default is -1 in DB units, which will appear like a small value < 0 (e.g.-0.0005 if the get_db db_units is 2000). The design_rule_width and spacing attributes are not allowed to have non-default values at the same time, so the spacing value cannot be changed when the design_rule_width attribute's value is also set. To reset the spacing value use [set_db -dbu route_blockages.spacing -1]. <b>Type:</b> <a href="#">coord</a> <b>Default:</b> no_value <b>Edit:</b> Yes
type	

	<p>The routing blockage type. default: means the blockage is completely blocked and check_drc will treat it like min-width routing for spacing checks. partial: means a percentage of the routing resource is available on the layer (see density attribute). fills: means do not add any metal fill in the area. slots: means don't add slots to the area. slots is not used in Innovus but is allowed to match DEF. The type corresponds to the DEF BLOCKAGES + FILLS or + SLOTS value. There is no DEF syntax for 'partial', so partial blockages are currently lost when written to DEF.</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> default slots fills partial</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
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## route\_rule

### Parent Objects

[patch\\_wire](#), [track\\_pattern](#), [wire](#), [pg\\_base\\_pin](#), [net](#), [via](#), [route\\_type](#), [root](#), [base\\_pin](#)

### Definition

Rule information

Attribute	Description
is_from_lib	<p>Indicates whether the rule came from the library technology (true: from LEF or OA tech) or from the design (false: from DEF, OA database, or create_route_rule).</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
is_hard_spacing	<p>Indicates that any spacing values that exceed the LEF LAYER spacing requirements are 'hard' rules instead of 'soft' rules.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
layer_rules	

	List of layers rules <b>Type:</b> <a href="#">obj(layer_rule)*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>min_cuts</b>	
	List of cut layer and minimum number of cuts allowed for any via using the specified cut layer <b>Type:</b> <a href="#">string*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>name</b>	
	Name of non-default rule. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
<b>obj_type</b>	
	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (route_rule)</a> <b>Default:</b> "" <b>Edit:</b> No
<b>via_defs</b>	
	List of via, default or USEVIA or derived from mincut. <b>Type:</b> <a href="#">obj(via_def)*</a> <b>Default:</b> "" <b>Edit:</b> No

## route\_type

### Parent Objects

[root](#)

### Definition

route type

Attribute	Description
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bottom_mask_layer_num	
	<p>Specify the bottom layer number that the mask constraint should be applied.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
bottom_one_side_layer_num	
	<p>Specify the bottom layer number that one side spacing constrain should be applied on. By default, NDR spacing is applied to both sides of an NDR net or wire. Use this to specify the layer range for wires that have only one neighboring wire with minimum spacing, which means only one side needs to follow larger NDR spacing.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
bottom_preferred_layer	
	<p>The preferred lowest routing layer. This attribute is a soft limit; that is, NanoRoute might use a layer below the specified layer if necessary to complete routing.</p> <p><b>Type:</b> <a href="#">obj(layer)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
driver_use_multi_cut_via	
	<p>If true, then driver pins will use multi-cut vias.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
em_route_rule	
	<p>Specifies the EM route_rule to associate with this route type. When routing within the distance specified in em_route_rule_distance from the output pin, the router will use this route_rule to route. By default no em_route_rule is used.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
em_route_rule_distance	

**Stylus Common UI Database Object Information**  
Database Objects--route\_type

	<p>Specifies the distance from the output pin, when the em_route_rule is applied to the net. This allows a larger width route_rule for a short distance to avoid EM violations near the output pin. When routing outside this distance from the output pin, the router uses the normal net route_rule.</p> <p><b>Type:</b> double <b>Default:</b> no_value <b>Edit:</b> Yes</p>
is_table	
	<p>Indicates that whether the route type is table based.</p> <p><b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No</p>
mask	
	<p>Indicates mask number for multiple mask layer usage. Refer to layers .numMask attribute for valid range, 0 indicates unconstrained. Layers that do not support the specified value will be treated as unconstrained. (Legal range: 0-3).</p> <p><b>Type:</b> int <b>Default:</b> 0 <b>Edit:</b> Yes</p>
min_stack_layer	
	<p>The net should use a stacked via from output pins up to the given layer before starting normal routing. This is normally used to force the routing to higher layers with wider widths to reduce wiring resistance or avoid EM current limits for high-drive outputs. If output_stack_via_rule or input_stack_via_rule is also specified, the specified stack via rule is used for the input or output pins accordingly. If both output_stack_via_rule/input_stack_via_rule are not specified, a single-cut stacked-via will be used for the output pins only.</p> <p><b>Type:</b> obj(layer) <b>Default:</b> "" <b>Edit:</b> Yes</p>
name	
	<p>Name of route_type object.</p> <p><b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No</p>
obj_type	

	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (route_type)</a> <b>Default:</b> "" <b>Edit:</b> No
route_effort	route effort <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> low medium high <b>Default:</b> "" <b>Edit:</b> Yes
route_rule	The non-default rule corresponding to the net, nets with the default routing rule will return NULL (0x0). <b>Type:</b> <a href="#">obj(route_rule)</a> <b>Default:</b> "" <b>Edit:</b> No
shield_net	shield net <b>Type:</b> <a href="#">obj(net)</a> <b>Default:</b> "" <b>Edit:</b> No
shield_side	Specifies whether to perform one sided or two sided shielding for the route type specified. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> one_side both_side <b>Default:</b> "" <b>Edit:</b> Yes
stack_distance	Specifies that the cut distance of cuts on adjacent layers in the stacked vias are defined in min_stack_layer. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> double <b>Default:</b> no_value <b>Edit:</b> Yes
top_mask_layer_num	

	<p>Specify the top layer number that the mask constraint should be applied.</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
<b>top_one_side_layer_num</b>	
	<p>Specify the top layer number that one side spacing constrain should be applied on. By default, NDR spacing is applied to both sides of an NDR net or wire. Use this to specify the layer range for wires that have only one neighboring wire with minimum spacing, which means only one side needs to follow larger NDR spacing.</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
<b>top_preferred_layer</b>	
	<p>The preferred highest routing layer. This attribute is a soft limit; that is, NanoRoute might use a layer above the specified layer if necessary to complete routing.</p> <p><b>Type:</b> obj(layer)</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## row

### Parent Objects

[design](#), [root](#)

### Definition

Row (core), constructed from sites (equivalent to DEF ROWS)

Attribute	Description
name	
	<p>Name of row (generated name)</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
num_x	

	<p>Number of sites in X direction (refer to DEF ROW syntax)</p> <p><b>Type:</b> int</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
num_y	<p>Number of sites in Y direction (refer to DEF ROW syntax)</p> <p><b>Type:</b> int</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> enum (row)</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
orient	<p>Orientation of the sites in the row</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> r0 r90 r180 r270 mx mx90 my my90</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
rect	<p>Rectangle that defines the row shape</p> <p><b>Type:</b> rect</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
site	<p>The site used in the row</p> <p><b>Type:</b> obj(site)</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
step_x	<p>Step in the X direction (refer to DEF ROW syntax)</p> <p><b>Type:</b> coord</p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p>

## step\_y

Step in the Y direction (refer to DEF ROW syntax)  
**Type:** [coord](#)  
**Default:** no\_value  
**Edit:** Yes

# sdp

## Parent Objects

[inst](#), [design](#), [root](#)

## Definition

A structured datapath object. Each sdp is formed hierarchically from a list of sdps below it. Each sdp can be a row, column, space or inst (see .type). At the leaf-level, an sdp can only be a space or inst. See the `create_sdp_group` command for more help.

Attribute	Description
bbox	Bounding box of the data path. <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No
flip	Specifies if an sdp group or an sdp element is flipped in vertical, horizontal, or both directions. If an sdp group is flipped, its members will also be flipped. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> none flip_x flip_y flip_xy <b>Default:</b> "" <b>Edit:</b> Yes
hier_name	

	<p>Specifies the hierarchical path name prepended to inst names inside the sdp file. This attribute is only available when .is_top = 1.</p> <p><b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
insts	<p>All the insts from a hierarchical descent below this sdp to the bottom of the tree.</p> <p><b>Type:</b> obj(inst)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
is_placed	<p>Specifies if the data path is placed. This attribute is only available when .is_top = 1.</p> <p><b>Type:</b> bool  <b>Default:</b> ""  <b>Edit:</b> No</p>
is_top	<p>Indicates that the data path is a top data path group.</p> <p><b>Type:</b> bool  <b>Default:</b> ""  <b>Edit:</b> No</p>
justify_by	<p>Specifies the anchor point that will be used for aligning an sdp group or an sdp element. If the justify_by constraint is not specified at current level, it will be inherited from its parent level.</p> <p><b>Type:</b> enum  <b>Enum Values:</b> sw se nw ne mid  <b>Default:</b> ""  <b>Edit:</b> Yes</p>
local_list	<p>An ordered list of sdp objects and inst objects contained by this sdp (e.g. just one-level of the sdp hierarchy).</p> <p><b>Type:</b> obj(sdp)* obj(inst)*  <b>Default:</b> ""  <b>Edit:</b> No</p>
location	

	<p>Lower left location of the data path.</p> <p><b>Type:</b> <a href="#">point</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
name	
	<p>Name of Data Path.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (sdp)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
orient	<p>The orientation of an sdp group or an sdp element. If the orientation is specified at sdp group level, it will be applied to instances that belong to this sdp group.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> r0 r180 mx my none</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
parent	<p>Return parent sdp group that the sdp belongs to.</p> <p><b>Type:</b> <a href="#">obj(sdp)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
pin_alignment	<p>The sdp edge to use for pin alignment. The w, e, mid values are only available for sdp objects in a column sdp group (.type = column), that have .pin_names set. All others will have a value of unknown.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> unknown w e mid</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
pin_names	

	The pin names by which sdps are aligned using the .pin_alignment setting. <b>Type:</b> <a href="#">string</a> * <b>Default:</b> "" <b>Edit:</b> Yes
sdps	
	List of all the sdps from a hierarchical descent inside and below this sdp. <b>Type:</b> <a href="#">obj(sdp)</a> * <b>Default:</b> "" <b>Edit:</b> No
space	
	Specifies a space value to be skipped. If the space value is defined in a column, then this value is for row skipping and represents the number of skipped rows. If the space value is defined in a row, then this value is for column skipping and represents the number of M2 tracks (pitch of first vertical routing layer). This attribute is only valid when .type = space. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes
type	
	Type of data path object. A row or column sdp has a .local_list with an ordered list of sdp and inst objects, while a space type only has a .space value. <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> row column space <b>Default:</b> "" <b>Edit:</b> No

## shape

### Parent Objects

[route\\_blockage](#), [place\\_blockage](#), [layer\\_shape](#)

### Definition

shape

Attribute	Description
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**Stylus Common UI Database Object Information**  
Database Objects--shape

mask	
	Indicates mask number for multiple mask layer usage. Refer to layer's .numMask attribute for legal range, 0 indicates uncolored. <b>Type:</b> int <b>Default:</b> 0 <b>Edit:</b> Yes
obj_type	
	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (shape) <b>Default:</b> "" <b>Edit:</b> No
path	
	Points of the path (if type = path) <b>Type:</b> point* <b>Default:</b> "" <b>Edit:</b> No
polygon	
	Points of the polygon (if type = polygon) <b>Type:</b> point* <b>Default:</b> "" <b>Edit:</b> No
rect	
	Bounding box of shape <b>Type:</b> rect <b>Default:</b> "" <b>Edit:</b> No
type	
	Type of shape (path, rect, polygon) <b>Type:</b> enum <b>Enum Values:</b> rect polygon <b>Default:</b> "" <b>Edit:</b> Yes

# shape\_via

## Parent Objects

[base\\_cell](#), [physical\\_pin](#)

## Definition

layer shape via

Attribute	Description
bottom_mask	<p>Indicates mask number for bottom layer for multiple mask layer usage. Refer to layer's .numMask attribute for legal range, 0 indicates uncolored</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
bottom_rects	<p>List of rectangles (typically only one) on bottom routing layer in terms of design coordinates (equivalent attribute on the via master is in coordinates local to the via master)</p> <p><b>Type:</b> <a href="#">rect</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
cut_mask	<p>Indicates mask number for cut layer for multiple mask layer usage. Applies to lower left cut of the via, other cuts are rotated from the reference cut in the lower left corner. Refer to layer's .numMask attribute for legal range, 0 indicates uncolored},cutMask,,</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
cut_rects	<p>List of rectangles on cut layer in terms of design coordinates (equivalent attribute on the via master is in coordinates local to the via master).</p> <p><b>Type:</b> <a href="#">rect*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

location	
	<p>Via location  <b>Type:</b> <a href="#">point</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
obj_type	
	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a>  <b>Type:</b> <a href="#">enum (shape_via)</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
top_mask	
	<p>Indicates mask number for top layer for multiple mask layer usage. Refer to layer's .numMask attribute for legal range, 0 indicates uncolored  <b>Type:</b> <a href="#">int</a>  <b>Default:</b> 0  <b>Edit:</b> Yes</p>
top_rects	
	<p>List of rectangles (typically only one) on top routing layer in terms of design coordinates (equivalent attribute on the via master is in coordinates local to the via master)  <b>Type:</b> <a href="#">rect</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
via_def	
	<p>The via master of this via  <b>Type:</b> <a href="#">obj(via_def)</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>

## site

### Parent Objects

[base\\_cell](#), [design](#), [row](#), [root](#)

## Definition

LEF SITE

Attribute	Description
class	<p>Site class (equivalent to LEF SITE CLASS)</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> pad core</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
name	<p>Name of site (equivalent to LEF SITE NAME)</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (site)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
size	<p>Size of the site (equivalent to LEF SITE SIZE)</p> <p><b>Type:</b> <a href="#">point</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
symmetry	<p>site symmetry.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> none x y xy any</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>

# skew\_group

## Parent Objects

[pin](#), [root](#), [port](#)

## Definition

skew group

Attribute	Description
cts_skew_group_constraints	<p>A list of CCOpt components which should be constrained by this skew group. If this list includes "icts" or "ccopt_initial", this skew group will constrain sinks during "ccopt_design -cts" and during the initial global balancing step of a regular "ccopt_design" run. "icts" and "ccopt_initial" are synonymous. If this list includes ccopt or all, this skew group will constrain both "ccopt_design -cts" and the whole of "ccopt_design" - not just the initial solution. "ccopt" and "all" are synonymous. The special value "none" is a synonym for an empty list, and specifies that the skew group will only be used for reporting purposes. Valid values: icts ccopt_initial ccopt all none</p> <p><b>Type:</b> <a href="#">string</a> <b>Default:</b> ccopt_initial icts <b>Edit:</b> Yes</p>
cts_skew_group_created_from_clock	<p>This contains the name of the SDC clock that this skew group has been created to represent the balancing constraints in CCOpt. Valid values: string</p> <p><b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes</p>
cts_skew_group_created_from_constraint_mode	

**Stylus Common UI Database Object Information**  
Database Objects--skew\_group

	<p>This contains the name of the constraint mode that this skew_group has been created to represent the balancing constraints in CCOpt.</p> <p>Valid values: string</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
cts_skew_group_created_from_delay_corners	
	<p>This contains the delay corners associated with this skew_group that has been created to represent the balancing constraints in CTS.</p> <p>Valid values: string</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
cts_skew_group_include_source_latency	
	<p>Specifies whether clock tree source latency should be included when timing the skew group.</p> <p>Valid values: true false</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> Yes</p>
cts_skew_group_target_insertion_delay	
	<p>The target insertion delay used for clock tree synthesis. This may be set to the following values:</p> <p>auto - Allow the minimum clustered insertion delay to be pushed up a little (around 5%) to facilitate clock tree power reduction.</p> <p>A numeric value - Attempt to balance the clock tree to the specified insertion delay (specified in library units). CTS will attempt to have a longest clock path delay of no more than this value plus half of the skew target, and a shortest path delay of no less than this value minus half the skew target.</p> <p>The value must be positive and real valued.</p> <p>Valid values: auto   double</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> auto</p> <p><b>Edit:</b> Yes</p>
cts_target_skew	

	<p>This specifies the target skew for clock tree balancing. This may be set to a numeric value, or one of 'auto', 'ignore' or 'default'.          If set to 'auto' this indicates that an appropriate skew target should be computed.          If set to 'ignore' this indicates that skew should not be balanced for this corner/path combination.          If unspecified then the value of this attribute is 'default'.          If the value of the attribute is 'default' the target skew for late delays in the primary delay corner is interpreted as 'auto' and as 'ignore' otherwise.          Valid values: default   auto   ignore   double</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Allowed -index values:</b> delay_corner</p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p>
<b>ignore_pins</b>	
	<p>ignored pins within the skew group</p> <p><b>Type:</b> <a href="#">obj(pin)* obj(port)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>name</b>	
	<p>name of skew_group</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>obj_type</b>	
	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (skew_group)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>sinks</b>	
	<p>sinks (pins or ports) of the skew group</p> <p><b>Type:</b> <a href="#">obj(pin)* obj(port)*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>sinks_active</b>	

	active sinks (pins or ports) of the skew group <b>Type:</b> <a href="#">obj(pin)*</a> <a href="#">obj(port)*</a> <b>Default:</b> "" <b>Edit:</b> No
sources	
	source(s) (pins or ports) of the skew group <b>Type:</b> <a href="#">obj(pin)*</a> <a href="#">obj(port)*</a> <b>Default:</b> "" <b>Edit:</b> No

## special\_via

### Parent Objects

[net](#)

### Definition

A special\_via is normally used for power-vias, flip-chip routing, and sometimes pre-routed nets. special\_vias (along with special\_wires) are not changed during signal routing. They appear in the DEF SPECIALNETS section.

Attribute	Description
bottom_mask	Is the mask number for the lower, left shape on the bottom layer of the via. Normally there is only one shape on the bottom layer of a via, but if there are two or more bottom layer shapes, then the mask for the other shapes on the bottom layer are derived from the corresponding via_def mask values by "shifting" the via_def's mask values to match. See the DEF manual section on 'Multi-Mask Layers with Special Wiring' for figures and examples. A value of 0 indicates the bottom layer is uncolored, or the layer is not a multi-mask layer. <b>Type:</b> <a href="#">int</a> <b>Default:</b> 0 <b>Edit:</b> Yes
bottom_rects	

	<p>List of rectangles (typically only one) on bottom routing layer in terms of design coordinates (equivalent attribute on the via master is in coordinates local to the via master)</p> <p><b>Type:</b> <a href="#">rect*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
bottom_rects	<p>bottom_rects</p> <p>List of mask values for each rect in bottom_rects in the same order as bottom_rects. A value of 0 means it is uncolored, or this layer is not a multi-mask layer.</p> <p><b>Type:</b> <a href="#">int*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
cut_mask	<p>cut_mask</p> <p>Is the mask number for the lower, left cut of the via. The mask for the other cuts of the special_via are derived from the via_def by "shifting" the via_def's cut masks to match. So, if the via_def lower, left cut is mask 1, and the special_via cut_mask is set to 3, then all the via_def cuts on mask 1 become mask 3 for this special_via, and similarly cuts on 2 shift to 1, and cuts on 3 shift to 2. See the layer .num_masks attribute for the max mask value allowed. See the DEF manual section on 'Multi-Mask Layers with Special Wiring' for figures and examples. A value of 0 indicates the cut layer is uncolored, or the layer is not a multi-mask layer.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
cut_rects	<p>cut_rects</p> <p>List of rectangles on cut layer in terms of design coordinates (equivalent attribute on the via master is in coordinates local to the via master)</p> <p><b>Type:</b> <a href="#">rect*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
cut_rects_mask	<p>cut_rects</p> <p>List of mask values for each rect in cut_rects in the same order as cut_rects. A value of 0 means it is uncolored, or this layer is not a multi-mask layer.</p> <p><b>Type:</b> <a href="#">int*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
net	

	The net that the special_via belongs to <b>Type:</b> obj(net) <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (special_via) <b>Default:</b> "" <b>Edit:</b> No
point	Location of Via <b>Type:</b> point <b>Default:</b> "" <b>Edit:</b> No
shape	DEF SPECIALNETS + SHAPE equivalents (ring, stripe, etc.) <b>Type:</b> enum <b>Enum Values:</b> notype ring stripe followpin iowire corewire blockwire fillwire blockagewire padring blockring drcfill fillwireopc <b>Default:</b> "" <b>Edit:</b> Yes
shield_net	The net that is shielded if status is shield <b>Type:</b> obj(net) <b>Default:</b> "" <b>Edit:</b> No
status	Wiring status (equivalent to DEF SPECIALNETS special wiring status) <b>Type:</b> enum <b>Enum Values:</b> routed fixed cover shield unknown <b>Default:</b> "" <b>Edit:</b> Yes
top_mask	

	<p>Is the mask number for the lower, left shape on the top layer of the via. Normally there is only one shape on the top layer of a via, but if there are two or more top layer shapes, then the mask for the other shapes on the top layer are derived from the corresponding via_def mask values by "shifting" the via_def's mask values to match. See the DEF manual section on 'Multi-Mask Layers with Special Wiring' for figures and examples. A value of 0 indicates the top layer is uncolored, or the layer is not a multi-mask layer.</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
<b>top_rects</b>	
	<p>List of rectangles (typically only one) on top routing layer in terms of design coordinates (equivalent attribute on the via master is in coordinates local to the via master)</p> <p><b>Type:</b> rect*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>top_rects_mask</b>	
	<p>List of mask values for each rect in top_rects in the same order as top_rects. A value of 0 means it is uncolored, or this layer is not a multi-mask layer.</p> <p><b>Type:</b> int*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>user_class</b>	
	<p>User_class value (empty string is returned if no user_class is specified)</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
<b>via_def</b>	
	<p>The via master</p> <p><b>Type:</b> obj(via_def)</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## special\_wire

### Parent Objects

[net](#)

## Definition

Special wire (equivalent to DEF SPECIALNETS wiring)

Attribute	Description
area	<p>Area of the special wire as defined by the LEF MACRO SIZE or OVERLAP information</p> <p><b>Type:</b> area</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
begin_extension	<p>Extension of path at the first point (only on path type)</p> <p><b>Type:</b> coord</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
end_extension	<p>Extension of path at the last point (only on path type)</p> <p><b>Type:</b> coord</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
has_trim_metal	<p>Indicate the special wire has trimmetal or not</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
layer	<p>The layer of special_wire</p> <p><b>Type:</b> obj(layer)</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
mask	<p>Indicates mask number for multiple mask layer usage. Refer to layer's .numMask attribute for legal range, 0 indicates uncolored.</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>

**Stylus Common UI Database Object Information**  
Database Objects--special\_wire

net	
	<p>The net that the special_wire belongs to <b>Type:</b> <a href="#">obj(net)</a> <b>Default:</b> "" <b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (special_wire)</a> <b>Default:</b> "" <b>Edit:</b> No</p>
path	<p>2 points for pathSeg center-line, n points for path center-line, n points for polygon, null for rect <b>Type:</b> <a href="#">point*</a> <b>Default:</b> "" <b>Edit:</b> No</p>
polygon	<p>Polygon boundary for the object, the first point is not repeated as the last point in the list <b>Type:</b> <a href="#">polygon</a> <b>Default:</b> "" <b>Edit:</b> No</p>
rect	<p>Rectangle that defines the special_wire shape if type = rect, or if type = path_seg and it is orthogonal. If type = polygon, or 45-degree path_seg, this is the bounding box of the shape <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> Yes</p>
shape	<p>DEF SPECIALNETS + SHAPE equivalents (ring, stripe, etc.) <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> notype ring stripe followpin iowire corewire blockwire fillwire blockagewire padring blockring drcfill fillwireopc <b>Default:</b> "" <b>Edit:</b> Yes</p>
shield_net	

**Stylus Common UI Database Object Information**  
**Database Objects--special\_wire**

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	The net that is shielded if status is shieldNet <b>Type:</b> <a href="#">obj(net)</a> <b>Default:</b> "" <b>Edit:</b> No
status	Wiring status (equivalent to DEF SPECIALNETS special wiring status) <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> routed fixed cover shield unknown <b>Default:</b> "" <b>Edit:</b> Yes
trim_metal_color	Color of this special wire trim metal <b>Type:</b> <a href="#">int</a> <b>Default:</b> "" <b>Edit:</b> No
trim_metal_rect	The trim_metal rect if the special_wire has a trim_metal shape attached. This only occurs for some advanced node layers that use self-aligned patterning. {0 0 0} is returned if there is no trim_metal attached. <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No
type	Type of shape (rect, polygon, etc.) <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> rect polygon path_seg path <b>Default:</b> "" <b>Edit:</b> No
user_class	User_class value (empty string is returned if no user_class is specified) <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes
width	

	Width of path/pathSeg type <b>Type:</b> coord <b>Default:</b> no_value <b>Edit:</b> Yes
--	--

## stack\_via\_rule

### Parent Objects

[pin](#), [root](#), [base\\_pin](#)

### Definition

Stack via rule information

Attribute	Description
name	Stack Via Rule name. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (stack_via_rule) <b>Default:</b> "" <b>Edit:</b> No

## text

### Parent Objects

[design](#), [root](#)

### Definition

Interoperable text labels

**Stylus Common UI Database Object Information**  
**Database Objects--stack\_via\_rule**

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Attribute	Description
alignment	<p>Horizontal and vertical alignment of the text string</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> upper_left center_left lower_left upper_center center_center lower_center upper_right center_right lower_right</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
drafting	<p>Indicates if the text is always displayed left-to-right or top-to-bottom. Text will remain readable even if rotated and mirrored if this value is true.</p> <p><b>Type:</b> bool</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
font_name	<p>Font name</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> euro_style gothic math roman script stick fixed swedish mil_spec</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
font_number	<p>Font Number</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> 0 1 2 3 4 5 6 7 8</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
height	<p>Text height</p> <p><b>Type:</b> coord</p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p>
label	<p>Text string value</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>

layer	The layer of text <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> Yes
oa_purpose	User specified purpose name for OA text layer purpose pair support. Only values available that exist in the library's tech graph are allowed. The default value is 'drawing'. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> Yes
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (text)</a> <b>Default:</b> "" <b>Edit:</b> No
orient	Text Orientation <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> r0 r90 r180 r270 mx mx90 my my90 <b>Default:</b> "" <b>Edit:</b> No
point	Text location <b>Type:</b> <a href="#">point</a> <b>Default:</b> "" <b>Edit:</b> No

## timing\_condition

### Parent Objects

[delay\\_corner, root](#)

## Definition

A timing\_condition represents a set of libraries at a specific operating condition - effectively defining a device corner. When assigned to a power domain - the domain uses the library and PVT bindings defined by the timing\_condition. Timing conditions may be assigned to one or several power domains in the design via the delay\_corner object's timing condition attributes. Use the create\_timing\_condition and update\_timing\_condition commands to create and modify timing\_conditions.

Attribute	Description
library_sets	<p>Specifies the associated library_set object(s). A list of library_sets (a bundle) can be used for voltage interpolation.</p> <p><b>Type:</b> <a href="#">obj(library_set)</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
name	<p>Provides the name of this timing_condition object as specified by create_timing_condition.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (timing_condition)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
opcond	<p>Specifies the associated opcond object. If this is not set, the opcond is derived from timing library itself. The root attribute timing_default_opcond_per_lib can also affect which opcond is used if it is not set here.</p> <p><b>Type:</b> <a href="#">obj(opcond)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
opcond_library	<p>The library of the opcond for this timing condition. Can be empty if this is a virtual opcond.</p> <p><b>Type:</b> <a href="#">obj(library)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

# timing\_path

## Parent Objects

### Definition

cte timing path

Attribute	Description
arrival	
	arrival <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
arrival_mean	Returns the arrival_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
arrival_sigma	Returns the arrival_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
borrowing_path_q_pin_and_transition	Returns the borrowing_path_q_pin_and_transition property for a timing_path <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
borrowing_path_q_pin_transition	Returns the borrowing_path_q_pin_transition property for a timing_path <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No

capture_clock_path	
	<p>Returns the capture_clock_path property for a timing_path  <b>Type:</b> <a href="#">obj(timing_path)*</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
capturing_clock	
	<p>Returns the capturing_clock property for a timing_path  <b>Type:</b> <a href="#">obj(clock)*</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
capturing_clock_close_edge_time	
	<p>Returns the capturing_clock_close_edge_time property for a timing_path  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
capturing_clock_close_edge_type	
	<p>Returns the capturing_clock_close_edge_type property for a timing_path  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
capturing_clock_is_inverted	
	<p>Returns the capturing_clock_is_inverted property for a timing_path  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
capturing_clock_is_propagated	
	<p>Returns the capturing_clock_is_propagated property for a timing_path  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
capturing_clock_latency	
	<p>Returns the capturing_clock_latency property for a timing_path  <b>Type:</b> <a href="#">double</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>

capturing_clock_open_edge_type	Returns the capturing_clock_open_edge_type property for a timing_path <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
capturing_clock_pin	Returns the capturing_clock_pin property for a timing_path <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
capturing_clock_source_arrival_time	Returns the capturing_clock_source_arrival_time property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
capturing_clock_source_arrival_time_mean	Returns the capturing_clock_source_arrival_time_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
capturing_clock_source_arrival_time_sigma	Returns the capturing_clock_source_arrival_time_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
capturing_point	Returns a pointer to the end point of the timing path. <b>Type:</b> obj(port)* obj(pin)* <b>Default:</b> "" <b>Edit:</b> No
capturing_point_is_level_sensitive	Returns a value of true if the end point of the data path is level sensitive. <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No

check_delay	Returns the check_delay property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
check_delay_mean	Returns the check_delay_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
check_delay_sigma	Returns the check_delay_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
check_type	Returns the check_type property for a timing_path <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
clock_path_end_point	clock_path_end_point <b>Type:</b> obj(timing_point)* <b>Default:</b> "" <b>Edit:</b> No
clock_source_jitter	clock_source_jitter <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
clock_uncertainty	clock_uncertainty <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No

cppr_adjustment	Returns the CPPR adjustment of the timing path. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
cppr_adjustment_mean	Returns the cppr_adjustment_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
cppr_adjustment_sigma	Returns the cppr_adjustment_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
cppr_branch_point	Returns the CPPR branch point of the given timing path. <b>Type:</b> obj(port)* obj(pin)* <b>Default:</b> "" <b>Edit:</b> No
cumulative_manhattan_length	Returns the cumulative_manhattan_length property for a timing_path. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
cumulative_manhattan_length_x	Returns the cumulative_manhattan_length_x property for a timing_path. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
cumulative_manhattan_length_y	Returns the cumulative_manhattan_length_y property for a timing_path. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No

cycle_adjustment	
	Returns the cycle_adjustment property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
drive_adjustment	
	Returns the drive_adjustment property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
drive_adjustment_mean	
	Returns the drive_adjustment_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
drive_adjustment_sigma	
	Returns the drive_adjustment_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
external_delay	
	external_delay <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
gba_slack	
	Returns the gba_slack property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
gba_slack_mean	
	Returns the gba_slack_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No

gba_slack_sigma	Returns the gba_slack_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
hold	hold <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
is_clock_gating_hold	Returns a value of true if the path is a clock gating hold check. <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_clock_gating_setup	Returns a value of true if the path is a clock gating setup check. <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_invalid	Returns the is_invalid property for a timing_path <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_path_borrowing	Returns the is_path_borrowing property for a timing_path <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
is_retimed	Returns the is_retimed property for a timing_path <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No

is_time_given	Returns the is_time_given property for a timing_path <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_transparent_latch	Returns a value of true if the path is a transparent latch path. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
launch_clock_path	launch_clock_path <b>Type:</b> <a href="#">obj(timing_path)</a> * <b>Default:</b> "" <b>Edit:</b> No
launching_clock	launching_clock <b>Type:</b> <a href="#">obj(clock)</a> * <b>Default:</b> "" <b>Edit:</b> No
launching_clock_is_inverted	launching_clock_is_inverted <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
launching_clock_is_propagated	launching_clock_is_propagated <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
launching_clock_latency	launching_clock_latency <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No

launching_clock_open_edge_time	launching_clock_open_edge_time <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
launching_clock_open_edge_type	launching_clock_open_edge_type <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
launching_clock_source_arrival_time	launching_clock_source_arrival_time <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
launching_clock_source_arrival_time_mean	Returns the launching_clock_source_arrival_time_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
launching_clock_source_arrival_time_sigma	Returns the launching_clock_source_arrival_time_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
launching_input_delay	launching_input_delay <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
launching_point	Returns a pointer to the start point of the timing path. <b>Type:</b> obj(port)* obj(pin)* <b>Default:</b> "" <b>Edit:</b> No

launching_point_is_level_sensitive	Returns a value of true if the begin point of the data path is level sensitive. <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
lending_path_d_pin	Returns the lending_path_d_pin property for a timing_path <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
lending_path_d_pin_transition	Returns the lending_path_d_pin_transition property for a timing_path <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
num_cell_arcs	Returns the num_cell_arcs property for a timing_path <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No
num_net_arcs	Returns the num_net_arcs property for a timing_path <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (timing_path)</a> <b>Default:</b> "" <b>Edit:</b> No
path_cell_delay	Returns the path_cell_delay property for a timing_path <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No

path_cell_delay_mean	
	<p>Returns the path_cell_delay_mean property for a timing_path  <b>Type:</b> double  <b>Default:</b> ""  <b>Edit:</b> No</p>
path_cell_delay_sigma	
	<p>Returns the path_cell_delay_sigma property for a timing_path  <b>Type:</b> double  <b>Default:</b> ""  <b>Edit:</b> No</p>
path_delay	
	<p>Returns the path_delay property for a timing_path  <b>Type:</b> double  <b>Default:</b> ""  <b>Edit:</b> No</p>
path_delay_adjustment	
	<p>Returns the path_delay_adjustment property for a timing_path  <b>Type:</b> double  <b>Default:</b> ""  <b>Edit:</b> No</p>
path_delay_mean	
	<p>Returns the path_delay_mean property for a timing_path  <b>Type:</b> double  <b>Default:</b> ""  <b>Edit:</b> No</p>
path_delay_sigma	
	<p>Returns the path_delay_sigma property for a timing_path  <b>Type:</b> double  <b>Default:</b> ""  <b>Edit:</b> No</p>
path_group	
	<p>path_group  <b>Type:</b> obj(path_group)*  <b>Default:</b> ""  <b>Edit:</b> No</p>

**Stylus Common UI Database Object Information**  
Database Objects--timing\_path

path_group_name	Returns the name of the path group for the timing path. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
path_net_delay	Returns the path_net_delay property for a timing_path <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No
path_net_delay_mean	Returns the path_net_delay_mean property for a timing_path <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No
path_net_delay_sigma	Returns the path_net_delay_sigma property for a timing_path <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No
path_type	Reports max type for late path and min type for early path <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
period	Returns the period property for a timing_path <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No
phase_shift	Returns the phase_shift property for a timing_path <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No

**Stylus Common UI Database Object Information**  
Database Objects--timing\_path

recovery	
	Returns the recovery time at the end point of the path. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
removal	
	removal <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
required_time	
	Returns the required time for the timing path. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
required_time_mean	
	Returns the required_time_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
required_time_sigma	
	Returns the required_time_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
setup	
	The setup time at the end point of the path. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
skew	
	Returns the skew property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No

slack	
	<p>Returns the slack of the timing path.</p> <p><b>Type:</b> double</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_mean	
	<p>Returns the slack_mean property for a timing_path</p> <p><b>Type:</b> double</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
slack_sigma	
	<p>Returns the slack_sigma property for a timing_path</p> <p><b>Type:</b> double</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
spatial_distance	
	<p>Returns the spatial_distance property for a timing_path</p> <p><b>Type:</b> double</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
time_borrowed	
	<p>Returns the amount of time borrowed from the timing end point.</p> <p><b>Type:</b> double</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
time_lent	
	<p>Returns the amount of time lent to the timing start point.</p> <p><b>Type:</b> double</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
timing_points	
	<p>timing_points</p> <p><b>Type:</b> obj(timing_point)*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

**Stylus Common UI Database Object Information**  
Database Objects--timing\_path

total_cell_delta_delay	Returns the total_cell_delta_delay property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
total_cell_delta_delay_mean	Returns the total_cell_delta_delay_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
total_cell_delta_delay_sigma	Returns the total_cell_delta_delay_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
total_delta_delay	Returns the total_delta_delay property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
total_delta_delay_mean	Returns the total_delta_delay_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
total_delta_delay_sigma	Returns the total_delta_delay_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
total_net_delta_delay	Returns the total_net_delta_delay property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No

**Stylus Common UI Database Object Information**  
Database Objects--timing\_path

total_net_delta_delay_mean	Returns the total_net_delta_delay_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
total_net_delta_delay_sigma	Returns the total_net_delta_delay_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
underated_slack	Returns the underated slack time for the timing path. The underated slack value is available with timing path object only if it is generated using the -derate parameter. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
view_name	The name of the analysis view for the timing_path <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
worst_cell_delay	Returns the worst_cell_delay property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
worst_cell_delay_mean	Returns the worst_cell_delay_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
worst_cell_delay_sigma	

	Returns the worst_cell_delay_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
worst_cell_delta_delay	Returns the worst_cell_delta_delay property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
worst_cell_delta_delay_mean	Returns the worst_cell_delta_delay_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
worst_cell_delta_delay_sigma	Returns the worst_cell_delta_delay_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
worst_delay	Returns the worst_delay property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
worst_delay_mean	Returns the worst_delay_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
worst_delay_sigma	Returns the worst_delay_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
worst_delta_delay	

**Stylus Common UI Database Object Information**  
Database Objects--timing\_path

	Returns the worst_delta_delay property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
worst_delta_delay_mean	Returns the worst_delta_delay_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
worst_delta_delay_sigma	Returns the worst_delta_delay_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
worst_manhattan_length	Returns the worst_manhattan_length property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
worst_manhattan_length_net_name	Returns the worst_manhattan_length_net_name property for a timing_path. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
worst_net_delay	Returns the worst_net_delay property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
worst_net_delay_mean	Returns the worst_net_delay_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
worst_net_delay_sigma	

	Returns the worst_net_delay_sigma property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>worst_net_delta_delay</b>	
	Returns the worst_net_delta_delay property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>worst_net_delta_delay_mean</b>	
	Returns the worst_net_delta_delay_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>worst_net_delta_delay_sigma</b>	
	Returns the worst_net_delta_delay_mean property for a timing_path <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No

## timing\_point

### Parent Objects

[timing\\_path](#)

### Definition

cte timing point

Attribute	Description
arrival	
	Returns the arrival time at the timing point. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No

**Stylus Common UI Database Object Information**  
Database Objects--timing\_point

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arrival_mean	Returns the arrival_mean property for a timing_point <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
arrival_sigma	Returns the arrival_sigma property for a timing_point <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
delay	Returns the delay property for a timing_point. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
delay_mean	Returns the delay_mean property of a timing_point <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
delay_sigma	Returns the delay_sigma property for a timing_point. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
delta_delay	Returns the delta_delay property for a timing_point <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
direction	Returns the direction property for a timing_point <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No

hierarchical_name	Returns the hierarchical_name property for a timing_point <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
is_fanin_arc_cell_arc	Returns cell arc in the fanin of the timing point <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
is_hierarchical	Returns the is_hierarchical property for a timing_point <b>Type:</b> <a href="#">bool</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (timing_point)</a> <b>Default:</b> "" <b>Edit:</b> No
pin	Returns the pin property for a timing_point <b>Type:</b> <a href="#">obj(port)* obj(pin)*</a> <b>Default:</b> "" <b>Edit:</b> No
slack	Returns the slack property for a timing_point <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No
slack_mean	Returns the slack_mean property for a timing_point <b>Type:</b> <a href="#">double</a> <b>Default:</b> "" <b>Edit:</b> No

slack_sigma	Returns the slack_sigma property for a timing_point <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
slew	Returns the path-specific slew of the timing point. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
slew_mean	Returns the slew_mean property for a timing_point. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
slew_sigma	Returns the slew_sigma property for a timing_point <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
spatial_derate	Returns the spatial_derate property for a timing_point <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
spatial_derate_sigma	Returns the spatial_derate_sigma property for a timing_point <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
ssi_derate	Returns the path-specific ssi_derate of the timing point. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No

**Stylus Common UI Database Object Information**  
Database Objects--timing\_point

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total_derate	Returns the total_derate property for a timing_point <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
total_derate_sigma	Returns the total_derate_sigma property for a timing_point <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
transition_type	Returns the transition type of the timing point: rise or fall . <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
user_derate	Returns the user_derate property for a timing_point <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
user_derate_sigma	Returns the user_derate_sigma property for a timing_point <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
voltage	Returns the voltage property for a timing_point <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No

# track\_pattern

## Parent Objects

design, root

## Definition

Floorplan track information (DEF TRACKS equivalent)

Attribute	Description
direction	<p>Specifies the location and direction of the first track defined. x indicates vertical lines; y indicates horizontal lines.</p> <p><b>Type:</b> enum <b>Enum Values:</b> y x <b>Default:</b> "" <b>Edit:</b> No</p>
layers	<p>List of layers</p> <p><b>Type:</b> obj(layer)* <b>Default:</b> "" <b>Edit:</b> No</p>
mask	<p>Specifies the mask number for the first track.</p> <p><b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No</p>
num_tracks	<p>Specifies the number of tracks to create for the grid</p> <p><b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> Yes</p>
obj_type	

	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (track_pattern)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
route_rule	<p>Pointer to route_rule object (DEF NONDEFAULTRULE) to be used as a constraint for wiring that can be created on the track. An empty value indicates that there is no constraint on the rules of the wires on the track. This value can be set with add_tracks and is intended for advanced nodes that do not allow different route_rules on the same track for lower routing layers.</p> <p><b>Type:</b> <a href="#">obj(route_rule)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
start	<p>Specifies the coordinate of the first line</p> <p><b>Type:</b> <a href="#">coord</a></p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p>
step	<p>Specifies the spacing between the tracks</p> <p><b>Type:</b> <a href="#">coord</a></p> <p><b>Default:</b> no_value</p> <p><b>Edit:</b> Yes</p>
width	<p>Width constraint for wiring that can be created on the track. A value of 0 indicates that there is no constraint on the width of wires on the track. This value can be set with add_tracks and is intended for advanced nodes that do not allow different widths on the same track for lower routing layers.</p> <p><b>Type:</b> <a href="#">coord</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## via

### Parent Objects

[net](#)

## Definition

DEF NETS via instance

Attribute	Description
bottom_mask	<p>Is the mask number for the lower, left shape on the bottom layer of the via. Normally there is only one shape on the bottom layer of a via, but if there are two or more bottom layer shapes, then the mask for the other shapes on the bottom layer are derived from the corresponding via_def mask values by "shifting" the via_def's mask values to match. See the DEF manual section on 'Multi-Mask Patterns for Routing Points' for figures and examples. A value of 0 indicates the bottom layer is uncolored, or the layer is not a multi-mask layer.</p> <p><b>Type:</b> int  <b>Default:</b> 0  <b>Edit:</b> Yes</p>
bottom_rects	<p>List of rectangles (typically only one) on bottom routing layer in terms of design coordinates (equivalent attribute on the via master is in coordinates local to the via master)</p> <p><b>Type:</b> rect*  <b>Default:</b> ""  <b>Edit:</b> No</p>
bottom_rects_mask	<p>List of mask values for each rect in bottom_rects in the same order as bottom_rects. A value of 0 means it is uncolored, or this layer is not a multi-mask layer.</p> <p><b>Type:</b> int*  <b>Default:</b> ""  <b>Edit:</b> No</p>
cut_mask	<p>Is the mask number for the lower, left cut of the via. The mask for the other cuts of the via are derived from the via_def by "shifting" the via_def's cut masks to match. So, if the via_def lower, left cut is mask 1, and the via cut_mask is set to 3, then all the via_def cuts on mask 1 become mask 3 for this via, and similarly cuts on 2 shift to 1, and cuts on 3 shift to 2. See the layer .num_masks attribute for the max mask value allowed. See the DEF manual section on 'Multi-Mask Patterns for Routing Points' for figures and examples. A value of 0 indicates the cut layer is uncolored, or the layer is not a multi-mask layer.</p> <p><b>Type:</b> int  <b>Default:</b> no_value  <b>Edit:</b> Yes</p>
cut_rects	

	<p>List of rectangles on cut layer in terms of design coordinates (equivalent attribute on the via master is in coordinates local to the via master)</p> <p><b>Type:</b> <a href="#">rect</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>cut_rects_mask</b>	
	<p>List of mask values for each rect in cut_rects in the same order as cut_rects. A value of 0 means it is uncolored, or this layer is not a multi-mask layer.</p> <p><b>Type:</b> <a href="#">int*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>location</b>	
	<p>Location of Via</p> <p><b>Type:</b> <a href="#">point</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>net</b>	
	<p>The net that the via belongs to</p> <p><b>Type:</b> <a href="#">obj(net)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>obj_type</b>	
	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (via)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>route_rule</b>	
	<p>The non-default rule corresponding to the via, vias with the default routing rule will return an empty string.</p> <p><b>Type:</b> <a href="#">obj(route_rule)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
<b>status</b>	

	<p>Wiring status (equivalent to DEF NETS regular wiring status)</p> <p><b>Type:</b> enum</p> <p><b>Enum Values:</b> unknown routed fixed cover noshield</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> Yes</p>
top_mask	<p>Indicates mask number for top layer for multiple mask layer usage. Refer to layer's .numMask attribute for legal range, 0 indicates uncolored</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> Yes</p>
top_rects	<p>List of rectangles (typically only one) on top routing layer in terms of design coordinates (equivalent attribute on the via master is in coordinates local to the via master)</p> <p><b>Type:</b> rect</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
top_rects_mask	<p>List of mask values for each rect in top_rects in the same order as top_rects. A value of 0 means it is uncolored, or this layer is not a multi-mask layer.</p> <p><b>Type:</b> int*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
via_def	<p>The via cell</p> <p><b>Type:</b> obj(via_def)</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## **via\_def**

### **Parent Objects**

[route\\_rule](#), [shape\\_via](#), [via](#), [special\\_via](#), [root](#)

## Definition

A via definition. This is equivalent to the LEF/DEF VIA section statements. A via\_def can be either a parameterized via (VIA with VIARULE parameters), or a fixed via (VIA with just RECT statements). See the LEF/DEF manual VIA section for more details.

Attribute	Description
bottom_layer	<p>The bottom routing layer  <b>Type:</b> obj(layer)  <b>Default:</b> ""  <b>Edit:</b> No</p>
bottom_rects	<p>List of rectangles (typically only one) on bottom routing layer.  <b>Type:</b> rect*  <b>Default:</b> ""  <b>Edit:</b> No</p>
bottom_rects_mask	<p>List of mask values for each rect in bottom_rects in the same order as bottom_rects. A value of 0 means it is uncolored, or this layer is not a multi-mask layer.  <b>Type:</b> int*  <b>Default:</b> no_value  <b>Edit:</b> Yes</p>
cut_class	<p>Returns the name of the CUTCLASS definition (from LEF or OA tech) for the cut_rects in this via_def. It returns an empty string if no CUTCLASS exists for the cut layer, or no CUTCLASS matches the size of the cut_rects.  <b>Type:</b> string  <b>Default:</b> ""  <b>Edit:</b> No</p>
cut_columns	<p>The number of cut columns. It is only set for generated vias created from a via_def_rule. See the LEF/DEF manual VIA definition with VIARULE and ROWCOL values for more details. It is 0 for fixed vias (e.g. a LEF/DEF VIA definition with only RECT values).  <b>Type:</b> int  <b>Default:</b> 0  <b>Edit:</b> No</p>

cut_layer	
	<p>The cut layer of via  <b>Type:</b> <a href="#">obj(layer)</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
cut_rects	
	<p>List of rectangles on cut layer  <b>Type:</b> <a href="#">rect*</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
cut_rects_mask	
	<p>List of mask values for each rect in cut_rects in the same order as cut_rects. A value of 0 means it is uncolored, or this layer is not a multi-mask layer.  <b>Type:</b> <a href="#">int*</a>  <b>Default:</b> no_value  <b>Edit:</b> Yes</p>
cut_rows	
	<p>The number of cut rows. It is only set for generated vias created from a via_def_rule. See the LEF/DEF manual VIA definition with VIARULE and ROWCOL values for more details. It is 0 for fixed vias (e.g. a LEF/DEF VIA definition with only RECT values).  <b>Type:</b> <a href="#">int</a>  <b>Default:</b> 0  <b>Edit:</b> No</p>
cut_size	
	<p>The {width height} of the first rect in cut_rects in microns.  <b>Type:</b> <a href="#">string</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
from_design	
	<p>Indicates that the via is from design  <b>Type:</b> <a href="#">bool</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
from_lib	

	Indicates that the via is from library <b>Type:</b> <code>bool</code> <b>Default:</b> "" <b>Edit:</b> No
<b>is_default</b>	
	Indicates that the via is a default via (LEF VIA DEFAULT) <b>Type:</b> <code>bool</code> <b>Default:</b> "" <b>Edit:</b> No
<b>is_non_default</b>	
	Indicates that the via is declared in a LEF NONDEFAULTRULE <b>Type:</b> <code>bool</code> <b>Default:</b> "" <b>Edit:</b> No
<b>name</b>	
	Via name <b>Type:</b> <code>string</code> <b>Default:</b> "" <b>Edit:</b> No
<b>obj_type</b>	
	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <code>enum (via_def)</code> <b>Default:</b> "" <b>Edit:</b> No
<b>resistance</b>	
	Via resistance in ohms that is derived from LEF or OA data. This may not match the resistance of RC extraction results derived from extraction coefficient data. If the via is a fixed via with a resistance value defined in the LEF VIA definition statement or OA via_def, that value is returned. For vias without a resistance value, the resistance is computed from the cut-layer resistance_per_cut value and the number of cuts in the via (or equivalent cuts for a LEF CUTCLASS or OA cut_class via with different cut sizes). If both the via definition, and the cut-layer has no resistance value, then 0.0 is returned <b>Type:</b> <code>double</code> <b>Default:</b> "" <b>Edit:</b> No
<b>top_layer</b>	

	The top routing layer of via <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> No
<b>top_rects</b>	
	List of rectangles (typically only one) on top routing layer. <b>Type:</b> <a href="#">rect*</a> <b>Default:</b> "" <b>Edit:</b> No
<b>top_rects_mask</b>	
	List of mask values for each rect in top_rects in the same order as top_rects. A value of 0 means it is uncolored, or this layer is not a multi-mask layer. <b>Type:</b> <a href="#">int*</a> <b>Default:</b> no_value <b>Edit:</b> Yes
<b>via_def_rule</b>	
	The via_def_rule for this via_def. It is only set for generated vias created from via_def_rule parameters. See the LEF/DEF manual VIA statement with VIARULE for more details. It returns {} for fixed vias (e.g. a LEF/DEF VIA with only RECT values). <b>Type:</b> <a href="#">obj(via_def_rule)</a> <b>Default:</b> "" <b>Edit:</b> No

## **via\_def\_rule**

### **Parent Objects**

[via\\_def](#), [root](#)

### **Definition**

Equivalent of one LEF VIARULE GENERATE statement that has the rules to create new generated vias (e.g. LEF/DEF VIA statements with VIARULE parameters). See the LEF manual for more details.

<b>Attribute</b>	<b>Description</b>
bottom_enclosure	

**Stylus Common UI Database Object Information**  
Database Objects--via\_def\_rule

	<p>Two minimum enclosure values for the cuts in the via. The order of the two values does not matter. The bottom layer shape must enclose all the cuts by one of the enclosure values in one direction (e.g. either X or Y), and by the other enclosure value in the other direction. If it is {0 0}, which is recommended for newer technologies, then only the DRC rules are used to compute the minimum enclosure..</p> <p><b>Type:</b> point <b>Default:</b> "" <b>Edit:</b> No</p>
<p>bottom_layer</p>	
	<p>The bottom routing layer for the via.</p> <p><b>Type:</b> obj(layer) <b>Default:</b> "" <b>Edit:</b> No</p>
<p>bottom_width</p>	
	<p>Optional min and max width. If given, this rule should only be used if the bottom wire width is greater than or equal to the first value (min-width), and less than or equal to the second value (max-width). For example, {1 2} means min-width is &gt;= 1.0, and max_width is &lt;= 2.0). If not given, the default is {0 0}, which means this rule can be used for any width.</p> <p><b>Type:</b> point <b>Default:</b> "" <b>Edit:</b> No</p>
<p>cut_layer</p>	
	<p>The cut layer for the via.</p> <p><b>Type:</b> obj(layer) <b>Default:</b> "" <b>Edit:</b> No</p>
<p>cut_rect</p>	
	<p>The size of one cut rectangle.</p> <p><b>Type:</b> rect <b>Default:</b> "" <b>Edit:</b> No</p>
<p>cut_spacing</p>	
	<p>Minimum center-to-center spacing in the X and Y directions..</p> <p><b>Type:</b> point <b>Default:</b> "" <b>Edit:</b> No</p>
<p>name</p>	

**Stylus Common UI Database Object Information**  
Database Objects--via\_def\_rule

	Via rule name. <b>Type:</b> string <b>Default:</b> "" <b>Edit:</b> No
<b>obj_type</b>	
	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (via_def_rule) <b>Default:</b> "" <b>Edit:</b> No
<b>resistance_per_cut</b>	
	Optional via resistance per cut in ohms that is defined in LEF or OA data. This value is useful for estimation, but will not match the resistance extracted by RC extraction commands that use more accurate coefficient files. It is 0.0 if not given in the library data. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
<b>top_enclosure</b>	
	Two minimum enclosure values for the cuts in the via. The order of the two values does not matter. The top layer shape must enclose all the cuts by one of the enclosure value in one direction (e.g. either X or Y), and by the other enclosure value in the other direction. If it is {0 0}, which is recommended, then only the DRC rules are used to compute the minimum enclosure. <b>Type:</b> point <b>Default:</b> "" <b>Edit:</b> No
<b>top_layer</b>	
	The top routing layer for the via. <b>Type:</b> obj(layer) <b>Default:</b> "" <b>Edit:</b> No
<b>top_width</b>	

Optional min and max width. If given, this rule should only be used if the top wire width is greater than or equal to the first value (min-width), and less than or equal to the second value (max-width). For example, {1 2} means min-width is  $\geq 1.0$ , and max\_width is  $\leq 2.0$ . If not given, the default is {0 0}, which means this rule can be used for any width.

**Type:** [point](#)

**Default:** ""

**Edit:** No

## virtual\_wire

### Parent Objects

[net](#)

### Definition

DEF NETS VIRTUAL wire

Attribute	Description
begin_layer	The begin layer for the virtual connection <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> No
begin_point	Reference point to the begin symbolic location <b>Type:</b> <a href="#">point</a> <b>Default:</b> "" <b>Edit:</b> No
end_layer	The end layer for the virtual connection <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> No
end_point	

	Reference point to the end symbolic location <b>Type:</b> <a href="#">point</a> <b>Default:</b> "" <b>Edit:</b> No
net	
	The net that the virtual connection belongs to <b>Type:</b> <a href="#">obj(net)</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	
	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (virtual_wire)</a> <b>Default:</b> "" <b>Edit:</b> No
status	
	Wiring status ( equivalent to DEF NET regular wiring status) <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> unknown routed fixed cover noshield <b>Default:</b> "" <b>Edit:</b> No

## wire

### Parent Objects

[net](#)

### Definition

A 2-point wire segment intended for symbolic routing where the end-points normally align with other wire or via end-points, or end on a pin shape or special\_wire. The wire, via, and patch\_wire objects correspond to the DEF NETS symbolic routing data.

Attribute	Description
begin_extension	

	Extension of wire at the first point <b>Type:</b> <a href="#">coord</a> <b>Default:</b> no_value <b>Edit:</b> Yes
direction	Direction of wire, consistent with layer direction from LEF/OpenAccess <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> vertical other horizontal <b>Default:</b> "" <b>Edit:</b> No
end_extension	Extension of wire at the second point <b>Type:</b> <a href="#">coord</a> <b>Default:</b> no_value <b>Edit:</b> Yes
layer	The layer of wire <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> No
length	The center-line length of the wire between the two end points. It does not include the extension values <b>Type:</b> <a href="#">coord</a> <b>Default:</b> "" <b>Edit:</b> No
mask	Indicates mask number for multiple mask layer usage. Refer to layer's .numMask attribute for legal range, 0 indicates uncolored. <b>Type:</b> <a href="#">int</a> <b>Default:</b> 0 <b>Edit:</b> Yes
net	

	The net that the wire belongs to <b>Type:</b> <a href="#">obj(net)</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (wire)</a> <b>Default:</b> "" <b>Edit:</b> No
points	2 points (center-line) for the wire <b>Type:</b> <a href="#">point*</a> <b>Default:</b> "" <b>Edit:</b> No
rect	Rectangle that defines the wire shape, including any begin extension or end extension. <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No
route_rule	The non-default rule corresponding to the wire, wires with the default routing rule will return empty string. <b>Type:</b> <a href="#">obj(route_rule)</a> <b>Default:</b> "" <b>Edit:</b> No
status	Wiring status (equivalent to DEF NETS regular wiring status) <b>Type:</b> <a href="#">enum</a> <b>Enum Values:</b> unknown routed fixed cover noshield <b>Default:</b> "" <b>Edit:</b> Yes
width	Width of wire <b>Type:</b> <a href="#">coord</a> <b>Default:</b> "" <b>Edit:</b> No

# resistor

## Parent Objects

### Definition

After loading a Voltus IR-drop analysis result, you can select a resistor in the GUI. The pointer of the object is the same as its name, like resistor

Attribute	Description
capacitance	<p>The capacitance for the two nodes before any effects of set_rail_what_if_capacitance in units of farads.</p> <p><b>Type:</b> <a href="#">double</a>*</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
current	<p>The current of the resistor in units of A. For static rail_analysis it is the average value, for dynamic power analysis it is the rms value.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
current_direction	<p>The direction of current. no_value is returned for non-orthogonal resistors or if it is not available.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> no_value left right up down</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
em_jmax_dc_avg_ratio	

	<p>The ratio of the current / em_jmax_dc_avg limit in the Quantus ICT file. This is computed during static rail analysis. The jmax name is used for legacy reasons, but the value is a current value ratio, not a current density ratio.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
em_jmax_dc_rms_ratio	<p>The ratio of the current / em_jmax_dc_rms limit in the Quantus ICT file. This is computed during dynamic rail analysis. The jmax name is used for legacy reasons, but the value is a current value ratio, not a current density ratio.</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
failure_in_time	<p>The failure in time value of the resistor in units of 1e9 hours (e.g. 1.0 means one failure in 1e9 hours of operation).</p> <p><b>Type:</b> <a href="#">double</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
layer	<p>The layer of the resistor. A via resistor will have a via-layer, and a routing layer resistor will have a routing layer.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
length	<p>The length of the resistor in unit of um.</p> <p><b>Type:</b> <a href="#">coord</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
location	<p>The x, y location of the two nodes at each end of the resistor.</p> <p><b>Type:</b> <a href="#">point*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
name	

	This is an R followed by an integer to identify the resistor. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
net	
	The net of the resistor. <b>Type:</b> <a href="#">obj(net)</a> <b>Default:</b> "" <b>Edit:</b> No
node_names	
	This is an N followed by an integer to identify the two nodes at each end of the resistor. <b>Type:</b> <a href="#">string</a> <b>Default:</b> "" <b>Edit:</b> No
node_reff	
	The values are in units of ohms and are valid whenever the node reff db is available in the loaded state directory. <b>Type:</b> <a href="#">double*</a> <b>Default:</b> "" <b>Edit:</b> No
node_voltage_drop	
	The IR voltage drop of the two nodes in units of mV. <b>Type:</b> <a href="#">double*</a> <b>Default:</b> "" <b>Edit:</b> No
node_voltages	
	The IR voltage drop of the two nodes in units of mV. <b>Type:</b> <a href="#">double*</a> <b>Default:</b> "" <b>Edit:</b> No
obj_type	
	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (resistor)</a> <b>Default:</b> "" <b>Edit:</b> No

resistance	The resistance before any effects from set_rail_what_if_resistance in units of ohms. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
switch_net	The switched net of the resistor. <b>Type:</b> obj(net) <b>Default:</b> "" <b>Edit:</b> No
what_if_capacitance	The capacitance after any effects of set_rail_what_if_capacitance. This is the capacitance actually used in the rail analysis in units of farads. <b>Type:</b> double* <b>Default:</b> "" <b>Edit:</b> No
what_if_resistance	The resistance after any effects of set_rail_what_if_resistance. This is the resistance actually used in the rail analysis in units of ohms. <b>Type:</b> double <b>Default:</b> "" <b>Edit:</b> No
width	The width of the resistor in unit of um. <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No

## message

### Parent Objects

root

## Definition

Formatted error, warning and info messages (e.g. ERROR)

Attribute	Description
count	<p>The number of times message has been issued in current session.</p> <p><b>Type:</b> int</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
long_help	<p>Some messages have additional help information. It is also available with 'man ABCDEF-123' in the DESCRIPTION section.</p> <p>This is also the "DESCRIPTION" part of get_message -long. If the "DESCRIPTION" of a message is "There are no further details for this message", get_db doesn't need to return it, but return an empty string instead.</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
max_print	<p>Specifies the maximum number of times the message will be printed to the log file and screen. -1 is unlimited. 0 is suppressed.</p> <p><b>Type:</b> int</p> <p><b>Default:</b> 20</p> <p><b>Edit:</b> Yes</p>
message	<p>A brief explanation of the message. It is also available with 'help ABCDEF-123'. It uses printf syntax with %s, %d, etc. for message specific arguments.</p> <p>This is the get_message -short string.</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
name	<p>The message name (e.g. ABCDEF-123 for the message "ERROR: (ABCDEF-123):..."). The DPO name would be "message:ABCDEF-123".</p> <p><b>Type:</b> string</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (message)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
on_error	<p>The error action for the specified message. This only applies if the message has severity = error, and is ignored for messages with severity of warning or info. Valid values are:</p> <ul style="list-style-type: none"><li>msg_only: Write out message, with normal command behavior.</li><li>exit: Fatal error. Exit and return to Linux.</li><li>stop_script: If message occurs inside 'source &lt;file&gt;', then the source command stops and returns.</li></ul> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> exit stop_script msg_only</p> <p><b>Default:</b> msg_only</p> <p><b>Edit:</b> Yes</p>
severity	<p>The severity of the message. The severity is "default" until some application writes it out and sets the severity, or the user sets it. Setting it to "default" will undo any previous setting, and then applications will set it if again the next time they write it out. Valid values are:</p> <ul style="list-style-type: none"><li>default: A default severity is set to all messages until it is issued at least once.</li><li>info: An information message. No user action needed.</li><li>warning: A possible problem, but the command can continue.</li><li>error: A problem causing wrong behavior. In some cases, the command cannot continue and stops, and sometimes it can continue to enable debugging or prototyping with errors.</li></ul> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> default error warning info</p> <p><b>Default:</b> default</p> <p><b>Edit:</b> Yes</p>

## what\_if\_wire

### Parent Objects

[net](#)

## Definition

After loading a Voltus IR-drop analysis result, you can use add\_what\_if\_shapes to add 'what if' power wires to see how they would improve the IR-drop results without modifying the real power-mesh.

Attribute	Description
layer	<p>The layer for the wire. <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> No</p>
net	<p>The net of the wire. <b>Type:</b> <a href="#">obj(net)</a> <b>Default:</b> "" <b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> <a href="#">enum (what_if_wire)</a> <b>Default:</b> "" <b>Edit:</b> No</p>
rect	<p>The rect for the wire. <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No</p>
width	<p>The width of the wire. <b>Type:</b> <a href="#">coord</a> <b>Default:</b> "" <b>Edit:</b> No</p>

# what\_if\_via

## Parent Objects

[net](#)

## Definition

After loading a Voltus IR-drop analysis result, you can use add\_what\_if\_shapes to add 'what if' power vias to see how they would improve the IR-drop results without modifying the real power-mesh.

Attribute	Description
bottom_layer	<p>The bottom routing layer for this what_if_via. <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> No</p>
cut_layer	<p>The cut_layer for this what_if_via. <b>Type:</b> <a href="#">obj(layer)</a> <b>Default:</b> "" <b>Edit:</b> No</p>
cut_rect	<p>The rect on the cut_layer for this what_if_via. <b>Type:</b> <a href="#">rect</a> <b>Default:</b> "" <b>Edit:</b> No</p>
net	<p>The net for this what_if_via. <b>Type:</b> <a href="#">obj(net)</a> <b>Default:</b> "" <b>Edit:</b> No</p>
obj_type	

	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (what_if_via)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
top_layer	<p>The top routing layer for this what_if_via.</p> <p><b>Type:</b> <a href="#">obj(layer)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## inst\_obs

### Parent Objects

### Definition

obstruction shape on an instance

Attribute	Description
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (inst_obs)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>

## trim\_grid

### Parent Objects

[design](#), [root](#)

## Definition

Trim grid pattern. Equivalent to LEF TRIMMETALTRACK statement that defines the grids that trim shapes must align to. See the LEF manual for more descriptions, figures and examples of how these attributes are defined.

Attribute	Description
group	<p>Specifies the group names of the trim_grid from the LEF TRIMMETALSTACK GROUP value.</p> <p><b>Type:</b> <a href="#">string</a>  <b>Default:</b> {}  <b>Edit:</b> No</p>
layer	<p>The trim layer of this trim_grid from the LEF TRIMMETALSTACK trimLayer value</p> <p><b>Type:</b> <a href="#">obj(layer)</a>  <b>Default:</b> {}  <b>Edit:</b> No</p>
mask	<p>Specifies the mask number for the trim_grid, from the LEF TRIMMETALSTACK MASK value.</p> <p><b>Type:</b> <a href="#">int</a>  <b>Default:</b> {}  <b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (trim_grid)</a>  <b>Default:</b> ""  <b>Edit:</b> No</p>
offset	<p>Specifies the offset from the lower left point of the core box to the first trim_grid from the LEF TRIMMETALSTACK COREOFFSET value.</p> <p><b>Type:</b> <a href="#">coord</a>  <b>Default:</b> {}  <b>Edit:</b> No</p>
on_track	

	<p>True if the LEF TRIMMETALSTACK ONTRACK keyword is given for this trim_grid.</p> <p><b>Type:</b> <a href="#">bool</a></p> <p><b>Default:</b> false</p> <p><b>Edit:</b> No</p>
<b>pitch</b>	<p>Specifies the spacing between each trim_grid from the LEF TRIMMETALSTACK PITCH value.</p> <p><b>Type:</b> <a href="#">coord</a></p> <p><b>Default:</b> {}</p> <p><b>Edit:</b> No</p>
<b>track_count</b>	<p>The number of times to repeat the pitch for this track_index from the LEF TRIMMETALSTACK METALTRACKPITCH value. See the LEF manual for figures and examples of how this is used.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> No</p>
<b>track_index</b>	<p>Specifies the index value of the trim_grid from the LEF TRIMMETALSTACK METALTRACKOFFSET value. The offset and pitch values apply to this track_index for track_count times. See the LEF manual for figures and examples of how this is used to overlay different track_index settings on one layer on top of each other to create non-uniform grid patterns.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> No</p>

## gcell

### Parent Objects

[design](#), [root](#)

### Definition

A global-routing cell. It only exists after global routing has been run, and includes the number of routing tracks available (supply), and the tracks used (demand) for each gcell.

Attribute	Description
demand	<p>Number of routing tracks used in the preferred routing direction for the layer. If no layer index is given, the value is not useful, so -1 is returned.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Allowed -index values:</b> layer</p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> No</p>
horizontal_demand	<p>Number of routing tracks used in horizontal direction for all routing layers.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> No</p>
horizontal_remaining	<p>Number of routing tracks remaining in horizontal direction for all routing layers.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> No</p>
horizontal_supply	<p>Number of routing tracks available in horizontal direction for all routing layers.</p> <p><b>Type:</b> <a href="#">int</a></p> <p><b>Default:</b> 0</p> <p><b>Edit:</b> No</p>
index	<p>The X and Y index values into the gcell array. The bottom, left gcell has index = {0 0}</p> <p><b>Type:</b> <a href="#">int*</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
name	<p>Object name derived from index value</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obj_type	

	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (gcell) <b>Default:</b> "" <b>Edit:</b> No
rect	
	Physical dimensions {{llx lly} {urx ury}} <b>Type:</b> rect <b>Default:</b> "" <b>Edit:</b> No
remaining	
	Number of routing tracks remaining in the preferred routing direction for the layer. A negative value indicates overflow. If no layer index is given, the value is not useful, so -1 is returned. <b>Type:</b> int <b>Allowed -index values:</b> layer <b>Default:</b> 0 <b>Edit:</b> No
supply	
	Number of routing tracks available in the preferred routing direction for the layer. If no layer index is given, the value is not useful, so -1 is returned. <b>Type:</b> int <b>Allowed -index values:</b> layer <b>Default:</b> 0 <b>Edit:</b> No
vertical_demand	
	Number of routing tracks used in vertical direction for all routing layers. <b>Type:</b> int <b>Default:</b> 0 <b>Edit:</b> No
vertical_remaining	
	Number of routing tracks remaining in vertical direction for all routing layers. <b>Type:</b> int <b>Default:</b> 0 <b>Edit:</b> No
vertical_supply	

	Number of routing tracks available in vertical direction for all routing layers. <b>Type:</b> int <b>Default:</b> 0 <b>Edit:</b> No
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## inst\_obs\_shape

### Parent Objects

### Definition

This corresponds to one of the .base\_cell.obs\_layer\_shapes.shapes (LEF OBS shapes) for a given inst. It carries a link to the 'inst' object, that a 'shape' object does not have. This allows GUI operations that need both the shape and the inst object together to select, highlight or query the shape. It can only be accessed by selecting the object with the GUI.

Attribute	Description
inst	The inst of this OBS shape <b>Type:</b> obj(inst) <b>Default:</b> "" <b>Edit:</b> No
is_ignore_pg_net	Indicates that Power/Ground routing is ignored when checking for DRC violations (including shorts) involving the current shape (equivalent to LEF MACRO OBS LAYER EXCEPTPGNET). <b>Type:</b> bool <b>Default:</b> "" <b>Edit:</b> No
layer	The layer of the obstruction <b>Type:</b> obj(layer) <b>Default:</b> "" <b>Edit:</b> No
mask	

**Stylus Common UI Database Object Information**  
Database Objects--inst\_obs\_shape

	Indicates mask number for multiple mask layer usage. Refer to layer's .num_mask attribute for legal range, 0 indicates uncolored. <b>Type:</b> int <b>Default:</b> "" <b>Edit:</b> No
obj_type	The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a> <b>Type:</b> enum (inst_obs_shape) <b>Default:</b> "" <b>Edit:</b> No
polygon	Points of the polygon (if type = polygon) in design coordinates (e.g. base_cell values are transformed for this inst). <b>Type:</b> point* <b>Default:</b> "" <b>Edit:</b> No
rect	Box of the shape (if type = rect) in design coordinates (e.g. base_cell values are transformed for this inst). <b>Type:</b> rect <b>Default:</b> "" <b>Edit:</b> No
spacing	LEF OBS SPACING value, no_value if not specified in LEF. <b>Type:</b> coord <b>Default:</b> "" <b>Edit:</b> No
type	Type of shape (rect, polygon) <b>Type:</b> enum <b>Enum Values:</b> rect polygon <b>Default:</b> "" <b>Edit:</b> No

# bus\_sink\_group

## Parent Objects

[design](#), [root](#)

## Definition

A group of sinks (loads) that some floorplan and routing commands use to control adding buffers and routing for a bus. See 'help \*bus\_sink\*' for a list of commands related to this object.

Attribute	Description
name	<p>The name of the bus_sink_group.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> {}</p> <p><b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (bus_sink_group)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
sinks	<p>A list of sinks (pins of insts, or ports of the design) for this bus.</p> <p><b>Type:</b> <a href="#">obj(pin)* obj(port)*</a></p> <p><b>Default:</b> {}</p> <p><b>Edit:</b> No</p>

# bump\_pin

## Parent Objects

[bump](#)

## Definition

PIN in bump LEF

Attribute	Description
base_name	<p>The bump_pin name without bump path.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
base_pin	<p>The equivalent base_pin.</p> <p><b>Type:</b> <a href="#">obj(base_pin)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
bump	<p>The bump that the bump_pin belongs to.</p> <p><b>Type:</b> <a href="#">obj(bump)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
direction	<p>bump_pin's direction from the corresponding base_pin.</p> <p><b>Type:</b> <a href="#">enum</a></p> <p><b>Enum Values:</b> in out inout</p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
escaped_name	<p>The bump_pin name including bump path.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
layer	

	<p>The layer of the bump_pin. For bump_pin with more than one shape, it is the layer of the first shape (which is the same shape used for the .location value).</p> <p><b>Type:</b> <a href="#">obj(layer)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
location	<p>The location of the bump_pin. For bump_pin with more than one shape, it is the location of the first shape (which is the same shape used for the .layer value).</p> <p><b>Type:</b> <a href="#">point</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
name	<p>The bump_pin name including bump path.</p> <p><b>Type:</b> <a href="#">string</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
obj_type	<p>The obj_type name for this object. To see all obj_type names, go to <a href="#">Contents</a></p> <p><b>Type:</b> <a href="#">enum (bump_pin)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>
port	<p>The port that the bump_pin connects to.</p> <p><b>Type:</b> <a href="#">obj(port)</a></p> <p><b>Default:</b> ""</p> <p><b>Edit:</b> No</p>