cadence®

Innovus Error Message Reference

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1

Error and Warning Messages

CHKCTS-1

NAME

CHKCTS-1

SUMMARY

CTS maximum transition target must be set to a numeric value for delay_corner %s, delay_type %s, and %s for clock_tree %s and net_type %s.

DESCRIPTION

Make sure there is a numeric value set for the target_max_trans property for all delay corners and power domains. Run 'get_ccopt_property -help target_max_trans' for more details on how to set the maximum transition time.

CHKCTS-2

NAME

CHKCTS-2

SUMMARY

CTS maximum transition target must be set to a numeric value for the primary corner %s and %s for clock_tree %s and net_type %s.

DESCRIPTION

Make sure there is a numeric value set for the target_max_trans property for the primary half corner in all power domains. Run 'get_ccopt_property -help target_max_trans' for more details on how to set the maximum transition time.

CHKCTS-3

NAME

CHKCTS-3

SUMMARY

CTS maximum transition target %s is too low (minimum %s) for delay_corner %s and delay_type %s for clock_tree %s and net_type %s.

DESCRIPTION

Increase the value set for the target_max_trans property to avoid excessive buffering for this clock_tree. Run 'get_ccopt_property -help target_max_trans' for more details on how to set the maximum transition time.

CHKCTS-4

NAME

CHKCTS-4

SUMMARY

An auto generated scaled skew target of %s will be used for delay_corner %s and delay_type %s for skew_group %s.

DESCRIPTION

When using multi-corner skew targets it is recommended to set explicit numeric targets for each delay_corner you want to balance in. Run 'get_ccopt_property -help target_skew' for more details on how to set skew targets.

CHKCTS-5

NAME

CHKCTS-5

SUMMARY

CTS skew target must be set to a numeric value for the primary corner %s for skew_group %s.

DESCRIPTION

Set a skew target using the target_skew property for the primary half corner. Run 'get_ccopt_property -help target_skew' for more details on how to set skew targets.

CHKCTS-6

NAME

CHKCTS-6

SUMMARY

The value for the target_skew property %s is too low (minimum %s) for skew_group %s, delay_corner %s and delay_type %s.

DESCRIPTION

Increase the value set for the target_skew property to avoid excessive buffering for this skew_group. Run 'get_ccopt_property -help target_skew' for more details on how to set skew targets.

CHKCTS-9

NAME

CHKCTS-9

SUMMARY

No route_type has been specified for clock_tree %s and net_type %s.

DESCRIPTION

Route types must be created and then specified for use by CTS by setting the route_type property. Run 'help create_route_type' for more details on how to create route_types. Run 'get_ccopt_property -help route_type' for more details on how to specify which route_types CTS should use.

CHKCTS-10

NAME

CHKCTS-10

SUMMARY

Route type(s) %s used for trunk or top clock nets do not have a non-default rule (NDR) set.

DESCRIPTION

Make sure there is a NDR specifed for each route_type for top and trunk nets. Check the route_type property to see which route_types are in use for clock nets. Run 'dbGet [dbGet -p head.routeTypes.name <name>].rule.name' to see NDR for a route_type called <name>. Run 'get_ccopt_property -help route_type' for more details on how to specify which route_types CTS should use. Run 'help create_route_type' for more details on how to create route_types.

CHKCTS-12

NAME

CHKCTS-12

SUMMARY

No preferred routing layers are set for route_type(s) %s for clock nets.

DESCRIPTION

All route_types for clock nets should have preferred routing layers set. Check the route_type property to see which route_types are in use for clock nets. Run 'dbGet [dbGet -p head.routeTypes.name <name>].bottomPreferredLayer.name' and 'dbGet [dbGet -p head.routeTypes.name <name>].topPreferredLayer.name' to see preferred layers for a route_type called <name>. Run 'help create_route_type' for more details on how to create route_types.

CHKCTS-13

NAME

CHKCTS-13

SUMMARY

More than two preferred routing layers are set for route_type(s) %s for clock nets, and automatic route_type trimming is disabled. This can cause poor routing correlation.

DESCRIPTION

Either enable automatic route_type trimming (by running 'set_ccopt_property route_type_autotrim true'), or manually reduce the number of preferred layers in the route_type. Run 'dbGet [dbGet -p head.routeTypes.name <name>].bottomPreferredLayer.name' and 'dbGet [dbGet -p head.routeTypes.name <name>].topPreferredLayer.name' to see preferred layers for a route_type

called <name>. Run 'help create_route_type' for more details on how to create route_types.

CHKCTS-14

NAME

CHKCTS-14

SUMMARY

Route type(s) %s used for leaf clock nets will use routing layers above those for trunk clock nets.

DESCRIPTION

Leaf nets should be configured to use lower layers than trunk nets. Check the route_type property to see which route_types are in use for clock nets. Run 'dbGet [dbGet -p head.routeTypes.name <name>].bottomPreferredLayer.name' and 'dbGet [dbGet -p head.routeTypes.name <name>].topPreferredLayer.name' to see preferred layers for a route_type called <name>. Run 'help create_route_type' for more details on how to create route_types.

CHKCTS-15

NAME

CHKCTS-15

SUMMARY

Preferred routing layers use Double Pattern Technology (DPT) for route_type(s) %s for clock nets.

DESCRIPTION

It is recommended to use non-DPT layers for clock nets. Check the route_type property to see which route_types are in use for clock nets. Run 'dbGet [dbGet -p head.routeTypes.name <name>].bottomPreferredLayer.name' and 'dbGet [dbGet -p head.routeTypes.name

<name>].topPreferredLayer.name' to see preferred layers for a route_type called <name>. To check the number of masks for a layer called <name> run 'dbGet [dbGetLayerByName <name>].numMasks'.

CHKCTS-16

NAME

CHKCTS-16

SUMMARY

Preferred routing layers for route_type %s do not have similar RC characteristics. Mismatch found on layers: %s.

DESCRIPTION

Preferred layer ranges for clock nets should have similar RC characteristics for both horizontal and vertical layers. Check the route_type property to see which route_types are in use for clock nets. Run 'help report_unit_parasitics' for details on how to check the layer RC values for the preferred layers specified in the route_type.

CHKCTS-17

NAME

CHKCTS-17

SUMMARY

CTS has found the clock tree is inconsistent with the power management setup: %s has %s but drives %s which has %s%s

DESCRIPTION

A clock node cannot drive its fanout since they are in different power domains. Check power management setup.

CHKCTS-18

NAME

CHKCTS-18

SUMMARY

Buffer cells are not specified for these clock_tree(s): %s.

DESCRIPTION

Clock buffer cells must be specified for CTS. Set the buffer_cells property to a list of buffers, or a list of patterns to match buffers. Run 'get_ccopt_property -help buffer_cells' for more details on how to specify which buffers CTS should use.

CHKCTS-19

NAME

CHKCTS-19

SUMMARY

Inverter cells are not specified for these clock_tree(s): %s.

DESCRIPTION

Clock inverter cells must be specified for CTS. Set the inverter_cells property to a list of inverters, or a list of patterns to match inverters. Run 'get_ccopt_property -help inverter_cells' for more details on how to specify which inverters CTS should use.

CHKCTS-20

NAME

CHKCTS-20

SUMMARY

Clock gating cells are not specified for these clock_tree(s): %s.

DESCRIPTION

Clock gating cells must be specified for CTS. Set the clock_gating_cells property to a list of clock gates, or a list of patterns to match clock gates. Run 'get_ccopt_property -help clock_gating_cells' for more details on how to specify which clock gates CTS should use.

CHKCTS-21

NAME

CHKCTS-21

SUMMARY

Clock logic cells are not specified for these clock_tree(s): %s.

DESCRIPTION

It is recommended to specify clock logic cells for CTS. Set the logic_cells property to a list of clock logics, or a list of patterns to match clock logics. Run 'get_ccopt_property -help clock_logic_cells' for more details on how to specify which clock logics CTS should use.

CHKCTS-22

NAME

CHKCTS-22

SUMMARY

Insufficient number of buffer cells for clock_tree %s and power_domain %s. Have cells: %s.

DESCRIPTION

Provide at least three cells to allow CTS to choose from a range of different buffer sizes. Run 'get_ccopt_property -help buffer_cells' for more details on how to specify which buffers CTS should use.

CHKCTS-23

NAME

CHKCTS-23

SUMMARY

Insufficient number of inverter cells for clock_tree %s and power_domain %s. Have cells: %s.

DESCRIPTION

Provide at least three cells to allow CTS to choose from a range of different inverter sizes. Run 'get_ccopt_property -help inverter_cells' for more details on how to specify which inverters CTS should use.

CHKCTS-24

NAME

CHKCTS-24

SUMMARY

Insufficient number of clock gating cells for clock_tree %s and power_domain %s. Have cells: %s.

DESCRIPTION

Provide at least three cells to allow CTS to choose from a range of different clock gate sizes. Run 'get_ccopt_property -help clock_gating_cells' for more details on how to specify which clock gates CTS should use.

CHKCTS-25

NAME

CHKCTS-25

SUMMARY

The pin %s is a sink in skew_group %s but is not part of any defined clock_tree.

DESCRIPTION

This may indicate that this pin was expected to be in a clock_tree.

CHKCTS-29

NAME

CHKCTS-29

SUMMARY

Cannot determine a primary timing corner for %s.

DESCRIPTION

Make sure there is at least one setup delay corner and check the primary_delay_corner property. Run 'report_analysis_views -setup' to check the current multi-mode multi-corner configuration.

CHKCTS-30

NAME

CHKCTS-30

SUMMARY

The clock instances %s with base_cell %s are cant_use for the following reason: %s.

DESCRIPTION

Check that timing and lef libraries are loaded for all the base_cells used in the clock_trees, or specify the capacitance_override property for all instances of the pins without library data.

CHKCTS-31

NAME

CHKCTS-31

SUMMARY

The clock_tree %s traces through an hterm on hinst %s. This hinst is an instance of module %s which has no definition in the netlist.

DESCRIPTION

Check that there is a definition in the Verilog for the module, and check the log for Verilog parse errors.

CHKCTS-32

NAME

CHKCTS-32

SUMMARY

Power domain %s contains clock instances but has no placeable area.

DESCRIPTION

Check the power_domain definitions are correct and that the specified drivers are compatible with the power_domain. CTS quality will be impacted since it will be unable to add drivers to this power_domain.

CHKCTS-37

NAME

CHKCTS-37

SUMMARY

CTS cannot use the preferred layers from route type %s: top %s(%s) and bottom %s(%s) for clock_tree %s and net_type %s. CTS will instead use preferred layers: top %s(%s) and bottom %s(%s).

DESCRIPTION

All route_types for CTS should have at least one horizontal layer and at least one vertical layer. Check the route_type property to see which route_types are in use for clock nets. Modify the route_type preferred layers or change which route_types will be used for CTS by changing the route_type property.

CHKCTS-38

NAME

CHKCTS-38

SUMMARY

Found %d clock instances which have been set to fixed placement status by the user. Refer to the CHKCTS-59 messages to identify details of each such fixed node.

DESCRIPTION

Fixed clock tree instances (clock gates, clock drivers and clock logic) cannot be moved or sized by CTS. This can adversely affect clock QoR.

CHKCTS-39

NAME

CHKCTS-39

SUMMARY

More than %.1f%% (%d of %d) of clock instances have been set to fixed placement status by the user.

DESCRIPTION

Fixed clock tree instances (clock gates, clock drivers and clock logic) cannot be moved or sized by CTS. This can adversely affect clock QoR.

CHKCTS-40

NAME

CHKCTS-40

SUMMARY

More than half of the clock gates in clock_tree %s are instances of cells that are not in the clock gating cell lists for the clock_tree. These cells are not specified for the clock_tree: %s.

DESCRIPTION

Check the clock_gating_cells property setting for this clock_tree. Run 'get_ccopt_property -help clock_gating_cells' for more details on how to specify which clock gates CTS should use.

CHKCTS-41

NAME

CHKCTS-41

SUMMARY

The setting of %s for the max_source_to_sink_net_length property for %s may be too low. Increase it to more than %s to avoid this warning.

DESCRIPTION

Check the value of the max_source_to_sink_net_length property. Run 'get_ccopt_property -help max_source_to_sink_net_length' for more details on how to control the max net length in CTS.

CHKCTS-42

NAME

CHKCTS-42

SUMMARY

The setting of %s for the max_source_to_sink_net_length property for %s is too low (less than %s). Increase the value (preferably to at least %s).

DESCRIPTION

Check the value of the max_source_to_sink_net_length property or increase the limit. Run 'get_ccopt_property -help max_source_to_sink_net_length' for more details on how to control the max net length in CTS.

CHKCTS-43

NAME

CHKCTS-43

SUMMARY

Buffer cells are not specified for clock_tree %s and power_domain %s.

DESCRIPTION

Set the buffer_cells property to a list of buffers, or a list of patterns to match buffers. Run 'get_ccopt_property -help buffer_cells' for more details on how to specify which buffers CTS should use.

CHKCTS-44

NAME

CHKCTS-44

SUMMARY

Inverter cells are not specified for clock_tree %s and power_domain %s.

DESCRIPTION

Set the inverter_cells property to a list of inverters, or a list of patterns to match inverters. Run 'get_ccopt_property -help inverter_cells' for more details on how to specify which inverters CTS should use.

CHKCTS-45

NAME

CHKCTS-45

SUMMARY

Clock gating cells are not specified for clock_tree %s and power_domain %s.

DESCRIPTION

Set the clock_gating_cells property to a list of clock gates, or a list of patterns to match clock gates. Run 'get_ccopt_property -help clock_gating_cells' for more details on how to specify which clock gates CTS should use.

CHKCTS-46

NAME

CHKCTS-46

SUMMARY

Clock logic cells are not specified for clock_tree %s and power_domain %s.

DESCRIPTION

Set the logic_cells property to a list of clock logics, or a list of patterns to match clock logics. Run 'get_ccopt_property -help clock_logic_cells' for more details on how to specify which clock logics CTS should use.

CHKCTS-48

NAME

CHKCTS-48

SUMMARY

The route_type %s used for net_type (%s) has a non-default rule (NDR) set but the NDR does not change the width or spacing of the following preferred routing layers: %s.

DESCRIPTION

Check the NDR definition has the intended width and spacing for the preferred routing layers. Run 'dbGet [dbGet -p head.routeTypes.name <name>].rule.name' to see NDR for a route_type called <name>.

CHKCTS-50

NAME

CHKCTS-50

SUMMARY

Found one or more Verilog module ports with the wrong direction. This may cause CTS to crash.

DESCRIPTION

Run 'fix_multi_drivers [-report_only]' to identify and repair incorrect port directions.

CHKCTS-51

NAME

CHKCTS-51

SUMMARY

The timing analysis type is not set to OCV (on chip variation).

DESCRIPTION

The analysis type should be set to onChipVariation. Run 'setAnalysisMode -analysisType onChipVariation' to change to OCV analysis. Without OCV analysis post-CTS timing is inaccurate. Furthermore, OCV analysis is required by the clock source latency update ('IO latency update') that is performed by default during CTS. It is recommended to set the analysis type to OCV before placement, and to ensure the SDC timing constraints are compatible: the analysis type changes the interpretation of any SDC timing constraints using -min and -max qualifiers.

CHKCTS-53

NAME

CHKCTS-53

SUMMARY

Over %s (%d of %d) of clock insts have been set by the user to be don't touch.

DESCRIPTION

Too many dont_touch insts can impact clock QoR. Check the dont_touch status for clock insts and correct if necessary. Run 'dbSet [dbGetInstByName <name>].dontTouch none' to clear the flag on an inst called <name>'.

CHKCTS-54

NAME

CHKCTS-54

SUMMARY

More than %d of the sinks in clock tree source group %s are in the transitive fanout of uncloneable inst %s.

DESCRIPTION

Multi-tap allocation can be severely impacted by uncloneable insts especially those in the path to many sinks. Refer to the CHKCTS-55 messages to identify details of each such uncloneable inst.

CHKCTS-55

NAME

CHKCTS-55

SUMMARY

Inst %s in clock tree source group %s can not be cloned for the following reason(s): %s. There are %d sinks in the transitive fanout of this inst.

DESCRIPTION

Multi-tap allocation can be severely impacted by uncloneable insts especially those in the path to many sinks. Run 'get_ccopt_property -help cannot_clone_reason' for more details on the possible reasons why a clock inst may be uncloneable.

CHKCTS-56

NAME

CHKCTS-56

SUMMARY

Net %s cannot be buffered for reason(s): %s. (HPL: %s, Num fanout: %u, Transitive fanout: %u)

DESCRIPTION

Unbufferable nets can severely impact QoR. Check the reason(s) why this net cannot be buffered, and correct the configuration if needed. This check is sorted by importance, based on fanout count and half perimeter length of the net bounding box (HPL).

CHKCTS-58

NAME

CHKCTS-58

SUMMARY

Found a user don't touch instance %s (source is %s).

DESCRIPTION

If this is not desired then remove the user don't touch setting. Run 'dbSet [dbGetInstByName <name>].dontTouch none' to clear the flag on an inst called <name>'.

CHKPTNFEED-90

NAME

CHKPTNFEED-90

SUMMARY

Pin %s of abutted partition %s could not be assigned. Could not find a feasible slot for the pin. Create more feasible location before for pin assignment by inserting feedthrough buffers using insertPtnFeedthrough command or allowing more layers for assigning pins or using setPinAssignMode -strict_abutment false or using setPinAssignMode -allow_unconnected_in_abutted_edge true for relaxing this check.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1 In abutted designs, pins of following type can not be placed on common edges between two adjoining partitions.

.in +2

A. Pins of net not connected to adjacent partition (fences of the two partitions being connected are not touching each other in floorplan).

B. Pins of nets having connections to two or more partitions any pin belonging to net of above type will have to route over an unconnected partition and result in illegal routing.

Feedthrough step is required to get rid of pins which connect non-adjacent partitions or multiple partitions, by changing netlist and making all pins connect to only one pin on adjacent partition to make the routing of net feasible/legal

C. Floating pins

.in

#2. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

#3. Use setPinAssignMode -strict_abutment false to relax abutment violations checks for placing multi partition pin of a net, non neighbor pins of a net and floating pins on abutted edges.

#4. Use setPinAssignMode -allow_unconnected_in_abutted_edge true to relax abutment violations checks for placing floating pins on abutted edges.

Example:

---

eg. if pins are not assigned for a net which has more than two partition pins to connect use insertPtnFeedthrough command to change netlist to have new nets added and older net modified in way that, now nets only connect two pins of adjacent partitions only.

CHKPTNFEED-100

NAME

CHKPTNFEED-100

SUMMARY

The net %s is not connected to any terminal. This net will not be considered for feedthrough buffer insertion. Correct the netlist to get this net considered for feedthrough buffer insertion.

DESCRIPTION

An unconnected net will not be considered for feedthrough insertion. The net should be connected

to an output port and an input port to be considered for feedthrough insertion.

CHKPTNFEED-233

NAME

CHKPTNFEED-233

SUMMARY

No legal free slots available for %s of partition %s. Create additional slots using definePartition command or by removing blockage before pin assignment.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

CHKPTNFEED-426

NAME

CHKPTNFEED-426

SUMMARY

Adjusting partition %s core to left from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

This is happening because the core spacing values specified (I/O to core distance of partition block) are not multiple of placement grid. Same issue for IMPPTN-427, IMPPTN-428 and IMPPTN-429 based or the side.

Example:

<CMD> definePartition -hinst uCORE/uPKTSS/uPKTSS_PPCS_PMA_SYS -coreSpacing {2.7 2.7 1.9 1.9} -reservedLayer {1 2 3 4 5 6 7 8} -routingHalo 1.9 -routingHaloTopLayer 7 -routingHaloBottomLayer 1 -placementHalo {2.7 2.7 1.9 1.9} -railwidth 0.1 -minPitchLeft 3 -minPitchRight 3 -minPitchTop 3 -minPitchBottom 3 -pinLayerTop {3 5} -pinLayerBottom {3 5} -pinLayerLeft {4 6} -pinLayerRight {4 6}

Creating partition PKTSS_PPCS_PMA_SYS.

**WARN: (IMPPTN-426): Adjusting partition PKTSS_PPCS_PMA_SYS core to left from 1.900000 to 2.025000.

**WARN: (IMPPTN-427): Adjusting partition PKTSS_PPCS_PMA_SYS core to right from 1.900000 to 2.025000.

**WARN: (IMPPTN-428): Adjusting partition PKTSS_PPCS_PMA_SYS core to top from 2.700000 to 2.850000.

**WARN: (IMPPTN-429): Adjusting partition PKTSS_PPCS_PMA_SYS core to bottom from 2.700000 to 2.850000.

Placement grid is at 0.135 x-direction, 0.095 y-direction.

CHKPTNFEED-427

NAME

CHKPTNFEED-427

SUMMARY

Adjusting partition %s core to right from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

During partitioning, the warnings above are issued. How does Innovus determine these adjustments?

\t Innovus snaps the partition coreBox (area where rows are created and placement can be done) boundary to the placement grid. The remaining difference between coreBox and partition box is adjusted in core to right, core to top values.

Example:

**WARN: (IMPPTN-427): Adjusting partition lbrx_top_0 core to right from 0.000000 to 0.100000.

CHKPTNFEED-428

NAME

CHKPTNFEED-428

SUMMARY

Adjusting partition %s core to top from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

During partitioning, the warnings above are issued. How does Innovus determine these adjustments?

\t Innovus snaps the partition coreBox (area where rows are created and placement can be done) boundary to the placement grid. The remaining difference between coreBox and partition box is adjusted in core to right, core to top values.

Example:

**WARN: (IMPPTN-428): Adjusting partition lbrx_top_0 core to top from 0.000000 to 3.680000.

CHKPTNFEED-429

NAME

CHKPTNFEED-429

SUMMARY

Adjusting partition %s core to bottom from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

This is happening because the core spacing values specified (I/O to core distance of partition block) are not multiple of placement grid. Same issue for IMPPTN-427, IMPPTN-428 and IMPPTN-429 based or the side.

Example:

**WARN: (IMPPTN-429): Adjusting partition PKTSS_PPCS_PMA_SYS core to bottom from 2.700000 to 2.850000.

CHKPTNFEED-555

NAME

CHKPTNFEED-555

SUMMARY

A feasible legal location was not found for %d (out of %d) pins. Consequently, the following pins could not be assigned:

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

2. Insert feedthrough buffers using the insertPtnFeedthrough command.

CHKPTNFEED-624

NAME

CHKPTNFEED-624

SUMMARY

insertPtnFeedthrough could not find a path for net '%s' to reach '%s'. If the -topoFile option is being used, the topology specified for this net is incomplete.

DESCRIPTION

In case automatic feedthrough insertion is being done, it means that a path to some of the terminals could not be found. If the routeBased option is used, the routing may be incomplete. For the case the topology file is used an explanation follows.

Tool issues above warning during insertPtnFeedthrough command step, when topology file provided with -topoFile is used to guide the tool for creating the feedthrough in a specified partition for multi-fanout nets. You will get above warning if the topology file did not define for all the terminals for a multi-fanout net. Always follow the convention from_pin to to_pin for writing the topology file.

Example:

If the net goes to three partition A, B and C and you want to make a part of the net from A to D then to C, then you can use the following approach to write the topology file.

net n123

hinst-hinst A D;

hinst-hinst D C;

hinst-hinst A B;

end net

So, here all the combinations are covered where the net goes, instead of defining the A-D-C.

CHKPTNFEED-646

NAME

CHKPTNFEED-646

SUMMARY

insertPtnFeedthrough is trying to find a feedthrough path for net %s. It could not find a path to partition or terminal [%s]. Partitions connected to this net may not be adjacent to each other.

DESCRIPTION

Automatic feedthrough insertion derives the feedthrough topology using the placement. It assumes a channel-less design. The possibility of routing through channels is considered minimal. In this design a path to a partition or terminal connected to the above mentioned net could not be found without avoiding the channels.

CHKPTNFEED-647

NAME

CHKPTNFEED-647

SUMMARY

insertPtnFeedthrough skipping net [%s] because a path to some of the partitions or terminals could not be found. It might not be necessary to insert feedthrough buffers for this net. If you wish to insert feedthrough buffers for this net, then use the topology file for guided feedthrough buffer insertion or use the -routeBased option after routing the net.

DESCRIPTION

insertPtnFeedthrough assumes the design to be channel-less and partitions to be in the line of sight for feedthrough path to pass from one partition to another. In case of channel based designs where

this is not true, the named net is ignored. In case feedthrough insertion is required for the net, either route the design and used insertPtnFeedthrough -routeBased or define the path for the net in a topology file and use insertPtnFeedthrough -topoFile <filename>

Example:

---

earlyGlobalRoute

insertPtnFeedthrough -routeBased

Or

insertPtnFeedthrough -topoFile <filename>

CHKPTNFEED-652

NAME

CHKPTNFEED-652

SUMMARY

The pushdownBuffer command cannot create an instance with name [%s%s]. An instance with this name already exists in the design. Using default prefix and name [%s] for this instance.

DESCRIPTION

This message is issued if the pushdownBuffer uses the prefix provided with the -prefix option and the resulting name has a conflict with an existing instance name. No action needs to be taken as it will make another name with the default prefix.

CHKPTNFEED-716

NAME

CHKPTNFEED-716

SUMMARY

Partition %s constraint missing. Specify a Guide, Region, Fence constraint on the partition or place the blackbox instance.

DESCRIPTION

While committing partitions 1. Blackboxes should be placed inside core 2. Partitions fences must be core

CHKPTNFEED-780

NAME

CHKPTNFEED-780

SUMMARY

Selected pin assignment: could not assign %d (out of %d) pins because feasible legal location was not found for following pins, need legal locations for pin to be assigned.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

2. Insert feedthrough buffers using the insertPtnFeedthrough command.

CHKPTNFEED-882

NAME

CHKPTNFEED-882

SUMMARY

The insertPtnFeedthrough command was invoked with the -routeBased option, but the design has not yet been routed. The insertPtnFeedthrough command will skip the nets that are not routed. Route the design using earlyGlobalRoute for these nets to be considered for feedthrough insertion.

DESCRIPTION

The insertPtnFeedthrough command invoked with the -routeBased option requires routing for the net to find a path based on which it will insert the feedthrough ports.

The net reported is not routed so it gets ignored. Route the design prior to running this command. The earlyGlobalRoute command can be used to route the design.

Otherwise insertPtnFeedthrough should be invoked without using the -routeBased option in which case the command will try to find a path for the net based on the floorplan and placement (placement based feedthrough insertion).

Example:

---

earlyGlobalRoute

insertPtnFeedthrough -routeBased.

CHKPTNFEED-946

NAME

CHKPTNFEED-946

SUMMARY

Pin named [%s] does not exist in cell [%s]. Ignoring the pin. Check and correct the pin name.

DESCRIPTION

Pin name specified for the specified partition does not exist. Check the pin name and partition name and correct accordingly. Problem could be case sensitivity. Command requires exact name which is case sensitive or incorrect manipulation of "alphabet l or numeric 1" "likewise "alphabet o and numeric 0"

Example:

Pin name could be "isCaseSensitive" but pin name supplied could be "iscasesensitive

CHKPTNFEED-1211

NAME

CHKPTNFEED-1211

SUMMARY

Specified layer [%s] is not within the allowed pin layer range [%s] and [%s] of the partition %s. Re-specify a valid pin layer value or change the partition definition to allow this pin layer and rerun the command again.

DESCRIPTION

Specified layer is not within the allowed pin layer range of the specified partition. Use the Partition->Specify Partition GUI to view the current specified allowed layers. Edit the current allowed pin layers of the partition to include this specified pin layer or re-specify pin layer and rerun the

command again.

CHKPTNFEED-1250

NAME

CHKPTNFEED-1250

SUMMARY

Pin placement has been enabled on metal layer 1.

DESCRIPTION

You have this message because you have enabled metal layer 1 for pin placement. However, metal layer 1 is generally reserved for follow pins. Make sure follow pins are already routed, to ensure that the pins do not block follow pins creation.

Example:

---

setDesignMode -bottomRoutingLayer 1 enables pins in M1

CHKPTNFEED-1520

NAME

CHKPTNFEED-1520

SUMMARY

Pin '%s' of %s '%s' cannot be placed at the constrained location [%0.2f %0.2f] due to a blocked pin slot close to the location. Placing the pin at location [%0.2f %0.2f].

DESCRIPTION

Pin slot can be blocked because of the following reasons

\t 1. pin blockages

\t 2. routing blockages

\t 3. Power ground routing

\t 4. availability of layers to put pins

CHKPTNFEED-1521

NAME

CHKPTNFEED-1521

SUMMARY

Unable to get any valid location for the constrained pin [%s] at location [%0.2f %0.2f].

DESCRIPTION

Pin slot can be blocked because of the following reasons

\t 1. pin blockages

\t 2. routing blockages

\t 3. Power ground routing

\t 4. availability of layers to put pins

CHKPTNFEED-1550

NAME

CHKPTNFEED-1550

SUMMARY

Cell [%s] cannot be specified as a black box because the design does not have any instance associated with this cell or instance may create nested blackBox. Ensure the design has an instance referenced to this cell or specify correct name of cell and rerun %s again.

DESCRIPTION

Specified cell cannot be defined as a black box because the design does not have any instance that is referenced to this cell or instance may create nested blackBox. Ensure there is at least one instance that is associated with this cell and rerun the command again.

CHKPTNFEED-1669

NAME

CHKPTNFEED-1669

SUMMARY

Ptn %s does not have any reserved slots for assigning ptn pins. Check the allowed layers for the partition and make sure that layers based on preferred routing tracks are reserved.

DESCRIPTION

This warning message is issued while assigning pins on a partition using the Innovus GUI with Partition => Assign Pin... or when using the assignPtnPin Tcl command.

The floorplan likely contains a problem with routing tracks and/or pin layer definitions. The problem can be debugged graphically using: Partition => Specify Partition

Select the offending partition and review the Partition Pin Layer Used section. Make sure the layers defined for pins are included in the Layers Reserved For Partition. Corrections may be made and applied with this form. Check the min max layer allowed though getDesignMode another reason could be presence of route blockage or PG on partition edge blocking the routing tracks.

Next, confirm there are preferred routing tracks defined for the pin layers using the Layer Control =>

Track => Pref Track and the Wire&Via layer defined for the pins. If the tracks are incorrect, they may be regenerated using the "generateTracks" Tcl command.

Example:

getPinConstraint -cell c -side all -layer

Constraint on partition c :

Allowed layer on side [top] : 2 4 6

Allowed layer on side [left] : 3 5

Allowed layer on side [bottom] : 2 4 6

Allowed layer on side [right] : 3 5

getDesignMode -bottomRoutingLayer -topRoutingLayer

-bottomRoutingLayer 2 # string, default=""

-topRoutingLayer 15 # string, default=""

{bottomRoutingLayer 2} {topRoutingLayer 15}

Look for the Tracks in a section with: Track:

While corrections can be made to the tmp.fp file and reloaded with the "loadFPlan tmp.fp" Tcl command, it is generally easier to do make changes with the Innovus GUI.

CHKPTNFEED-1671

NAME

CHKPTNFEED-1671

SUMMARY

The option %s cannot be used for updating pin attribute. Correct the command options and run the command again.

DESCRIPTION

Specified option cannot be used for just updating pin attribute. This option is used with other options for assigning pin location. Check the reference manual for the legal specified options. Then

correct the command options and rerun the editPin command again.

CHKPTNFEED-1699

NAME

CHKPTNFEED-1699

SUMMARY

Selective-pin-assignment by specifying just partition name(s) to command assignPtnPin is obsolete and will be removed in future releases. The old usage still works in this release, but to avoid this warning and to ensure compatibility with future releases, replace the obsolete usage with "assignPtnPin -ptn -pin ".

DESCRIPTION

To avoid this warning and to ensure compatibility with future releases, replace the obsolete usage with 'assignPtnPin -ptn <ptnName> -pin <pinName>'

Example:

---

* The following command assign pins name starting with "in" of partition "A" and pins name starting with "out" of partition "B"

assignPtnPin -ptn {A} -pin {in*} -ptn {B} -pin {out*}

* The following command accept a file pinLst.txt that contains the list of pins to be placed for partition A and partition B.

assignPtnPin -ptn A -ptn B -pin_file pinLst.txt

CHKPTNFEED-1704

NAME

CHKPTNFEED-1704

SUMMARY

The options [-row] and [-bringBackRow] are obsolete. Rows are brought back automatically, without using any of these options. To avoid this warning and ensure compatibility with future releases, update your script to not use any of these options.

DESCRIPTION

This messages is issued when obsolete options are used.Using these options will have no impact in this case.

Example:

---

eg. use flattenPartition

CHKPTNFEED-1717

NAME

CHKPTNFEED-1717

SUMMARY

The specifyPartition command will be obsolete in the next release. Use the definePartition command to define the partitions.

DESCRIPTION

The message occurs because you are using 'specifyPartition' which is obsoletelease use the 'definePartition' command to define the partitions.

Example:

The following example defines a partition:

definePartition \

-hinst ctr_inst \

-coreSpacing 0.56 0.56 0.0 0.0 \

-railwidth 0.0 \

-minPitchLeft 2 \

-minPitchRight 2 \

-minPitchTop 2 \

-minPitchBottom 2 \

-reservedLayer {1 2 3 4} \

-pinLayerTop {2 4} \

-pinLayerLeft {3} \

-pinLayerBottom {2 4} \

-pinLayerRight {3} \

-placementHalo 1.0 1.0 1.0 1.0 \

-routingHalo 1.0 \

-routingHaloTopLayer 7 \

-routingHaloBottomLayer 1

CHKPTNFEED-1755

NAME

CHKPTNFEED-1755

SUMMARY

Pin [%s] of %s [%s] connected to net [%s] is [%s] at location (%8.3f, %8.3f) on layer %1d %s.

DESCRIPTION

Message reports specific error/violation on a partition pin.

Example of ABUTMENT violation on a pin:

Pin [pin_1] of partition [ptn_1] connected to net [net_1] is [PLACED] at location (210.452, 540.160) on layer 8 has ABUTMENT violation WITH partition chip.

In above example error/violation is being reported for partition “ptn_1” pin's “pin_1” which is connected to net “net_1” and is placed at location “210.452, 540.160” on layer “8” having assignment status as “placed”. Pin has abutment (is placed on adjoining boundary of “ptn_1” and “chip”) violation with partition named “chip”. Ideally the pin pair of two adjoining (abutting) partitions should be placed on same track on edge of partition boundaries, touching each other (abutting).

Abutment violation could be because of following two reasons:

1. Net has multi-partition-pins. Since all other pins of different partitions cannot be placed at same location (no electrical connection through any overlap of physical shape), so it is reported as abutment violation.

2. “pin_1” pin of net “net_1” is not connected to any pin of adjoining (abutted) partition “chip”.

List other violations on pin:

- pin min-width violation
- pin min-depth violation
- pin missing metal shape violation
- pin min-area violation
- pin-color violation
- pin not on routing track (or ndr-rule-routing-track) violation
- pin not on fence violation
- pin spacing (drc and spacing constraints) violation
- pin not on allowed layer violation
- For nested partition it checks for child fence area violation
- pin outside pin-guide or bus-guide violation
- Pin associated pin-group or net-group violation

CHKPTNFEED-1802

NAME

CHKPTNFEED-1802

SUMMARY

Route layer setting through routing modes [setRouteMode %s <value>] or [setNanoRouteMode %s <value>] setting will not be honored. Set the value using setDesignMode command [setDesignMode %s <value>] and run the command again.

DESCRIPTION

This message is reported related to IO pin routing if there are any IO pins falls above maxRouteLayer. Message ENCPTN-1802 is generated to correct the user expectation, when user had set either setRouteMode or setNanoRouteMode for minLayer but has missed to set setDesignMode for minLayer, and user would like to set min/max layer of pin that is different from earlyGlobalRoute. Innovus checks for this issue and generate the message as user may forget to set min/max layer of pin when it differs from earlyGlobalRoute.

Example:

Because of the following reason the ENCPTN-1802 is reported.

Message ENCPTN-1802 is generated to correct the user expectation, when user had set either setRouteMode or setNanoRouteMode for minLayer but has missed to set setDesignMode for minLayer.

Use "setDesignMode -topRoutingLayer <layer>" to placing IO pins, to avoid this problem.

CHKPTNFEED-3207

NAME

CHKPTNFEED-3207

SUMMARY

The hierarchical-PG net %s is connected to an instance term %s inside the partition hinst %s. However, it is not connected to any PG port of the partition hinst. This is erroneous data. As a consequence, instance term %s will become unconnected. To correct this error, ensure that the above net is connected to a partition PG port when connecting to an instance PG term inside the partition, and run the command again.

DESCRIPTION

Reason of such incorrect PG net connection is generally introduced by either incorrect UPF or incorrect GNC rule. To correct this error, ensure that the above net is connected to a partition PG port when connecting to an instance PG term inside partition. Or, if this connection is not needed inside the partition hinst, then ensure that the net does not connect to any of the PG terms inside the partition hinst.

CHKPTNPIN-90

NAME

CHKPTNPIN-90

SUMMARY

Pin %s of abutted partition %s could not be assigned. Could not find a feasible slot for the pin. Create more feasible location before for pin assignment by inserting feedthrough buffers using insertPtnFeedthrough command or allowing more layers for assigning pins or using setPinAssignMode -strict_abutment false or using setPinAssignMode -allow_unconnected_in_abutted_edge true for relaxing this check.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1 In abutted designs, pins of following type can not be placed on common edges between two adjoining partitions.

.in +2

A. Pins of net not connected to adjacent partition (fences of the two partitions being connected are not touching each other in floorplan).

B. Pins of nets having connections to two or more partitions any pin belonging to net of above type will have to route over an unconnected partition and result in illegal routing.

Feedthrough step is required to get rid of pins which connect non-adjacent partitions or multiple partitions, by changing netlist and making all pins connect to only one pin on adjacent partition to make the routing of net feasible/legal

C. Floating pins

.in

#2. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

#3. Use setPinAssignMode -strict_abutment false to relax abutment violations checks for placing multi partition pin of a net, non neighbor pins of a net and floating pins on abutted edges.

#4. Use setPinAssignMode -allow_unconnected_in_abutted_edge true to relax abutment violations checks for placing floating pins on abutted edges.

Example:

---

eg. if pins are not assigned for a net which has more than two partition pins to connect use insertPtnFeedthrough command to change netlist to have new nets added and older net modified in way that, now nets only connect two pins of adjacent partitions only.

CHKPTNPIN-100

NAME

CHKPTNPIN-100

SUMMARY

The net %s is not connected to any terminal. This net will not be considered for feedthrough buffer insertion. Correct the netlist to get this net considered for feedthrough buffer insertion.

DESCRIPTION

An unconnected net will not be considered for feedthrough insertion. The net should be connected to an output port and an input port to be considered for feedthrough insertion.

CHKPTNPIN-233

NAME

CHKPTNPIN-233

SUMMARY

No legal free slots available for %s of partition %s. Create additional slots using definePartition command or by removing blockage before pin assignment.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

CHKPTNPIN-426

NAME

CHKPTNPIN-426

SUMMARY

Adjusting partition %s core to left from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

This is happening because the core spacing values specified (I/O to core distance of partition block) are not multiple of placement grid. Same issue for IMPPTN-427, IMPPTN-428 and IMPPTN-429 based or the side.

Example:

<CMD> definePartition -hinst uCORE/uPKTSS/uPKTSS_PPCS_PMA_SYS -coreSpacing {2.7 2.7 1.9 1.9} -reservedLayer {1 2 3 4 5 6 7 8} -routingHalo 1.9 -routingHaloTopLayer 7 -routingHaloBottomLayer 1 -placementHalo {2.7 2.7 1.9 1.9} -railwidth 0.1 -minPitchLeft 3 -minPitchRight 3 -minPitchTop 3 -minPitchBottom 3 -pinLayerTop {3 5} -pinLayerBottom {3 5} -pinLayerLeft {4 6} -pinLayerRight {4 6}

Creating partition PKTSS_PPCS_PMA_SYS.

**WARN: (IMPPTN-426): Adjusting partition PKTSS_PPCS_PMA_SYS core to left from 1.900000 to 2.025000.

**WARN: (IMPPTN-427): Adjusting partition PKTSS_PPCS_PMA_SYS core to right from 1.900000 to 2.025000.

**WARN: (IMPPTN-428): Adjusting partition PKTSS_PPCS_PMA_SYS core to top from 2.700000 to 2.850000.

**WARN: (IMPPTN-429): Adjusting partition PKTSS_PPCS_PMA_SYS core to bottom from 2.700000 to 2.850000.

Placement grid is at 0.135 x-direction, 0.095 y-direction.

CHKPTNPIN-427

NAME

CHKPTNPIN-427

SUMMARY

Adjusting partition %s core to right from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

During partitioning, the warnings above are issued. How does Innovus determine these adjustments?

\t Innovus snaps the partition coreBox (area where rows are created and placement can be done) boundary to the placement grid. The remaining difference between coreBox and partition box is adjusted in core to right, core to top values.

Example:

**WARN: (IMPPTN-427): Adjusting partition lbrx_top_0 core to right from 0.000000 to 0.100000.

CHKPTNPIN-428

NAME

CHKPTNPIN-428

SUMMARY

Adjusting partition %s core to top from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

During partitioning, the warnings above are issued. How does Innovus determine these adjustments?

\t Innovus snaps the partition coreBox (area where rows are created and placement can be done) boundary to the placement grid. The remaining difference between coreBox and partition box is adjusted in core to right, core to top values.

Example:

**WARN: (IMPPTN-428): Adjusting partition lbrx_top_0 core to top from 0.000000 to 3.680000.

CHKPTNPIN-429

NAME

CHKPTNPIN-429

SUMMARY

Adjusting partition %s core to bottom from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

This is happening because the core spacing values specified (I/O to core distance of partition block) are not multiple of placement grid. Same issue for IMPPTN-427, IMPPTN-428 and IMPPTN-429 based or the side.

Example:

**WARN: (IMPPTN-429): Adjusting partition PKTSS_PPCS_PMA_SYS core to bottom from 2.700000 to 2.850000.

CHKPTNPIN-555

NAME

CHKPTNPIN-555

SUMMARY

A feasible legal location was not found for %d (out of %d) pins. Consequently, the following pins could not be assigned:

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

2. Insert feedthrough buffers using the insertPtnFeedthrough command.

CHKPTNPIN-624

NAME

CHKPTNPIN-624

SUMMARY

insertPtnFeedthrough could not find a path for net '%s' to reach '%s'. If the -topoFile option is being used, the topology specified for this net is incomplete.

DESCRIPTION

In case automatic feedthrough insertion is being done, it means that a path to some of the terminals could not be found. If the routeBased option is used, the routing may be incomplete. For the case the topology file is used an explanation follows.

Tool issues above warning during insertPtnFeedthrough command step, when topology file provided with -topoFile is used to guide the tool for creating the feedthrough in a specified partition for multi-fanout nets. You will get above warning if the topology file did not define for all the terminals for a multi-fanout net. Always follow the convention from_pin to to_pin for writing the topology file.

Example:

If the net goes to three partition A, B and C and you want to make a part of the net from A to D then to C, then you can use the following approach to write the topology file.

net n123

hinst-hinst A D;

hinst-hinst D C;

hinst-hinst A B;

end net

So, here all the combinations are covered where the net goes, instead of defining the A-D-C.

CHKPTNPIN-646

NAME

CHKPTNPIN-646

SUMMARY

insertPtnFeedthrough is trying to find a feedthrough path for net %s. It could not find a path to partition or terminal [%s]. Partitions connected to this net may not be adjacent to each other.

DESCRIPTION

Automatic feedthrough insertion derives the feedthrough topology using the placement. It assumes a channel-less design. The possibility of routing through channels is considered minimal. In this design a path to a partition or terminal connected to the above mentioned net could not be found without avoiding the channels.

CHKPTNPIN-647

NAME

CHKPTNPIN-647

SUMMARY

insertPtnFeedthrough skipping net [%s] because a path to some of the partitions or terminals could not be found. It might not be necessary to insert feedthrough buffers for this net. If you wish to insert feedthrough buffers for this net, then use the topology file for guided feedthrough buffer insertion or use the -routeBased option after routing the net.

DESCRIPTION

insertPtnFeedthrough assumes the design to be channel-less and partitions to be in the line of sight for feedthrough path to pass from one partition to another. In case of channel based designs where this is not true, the named net is ignored. In case feedthrough insertion is required for the net, either route the design and used insertPtnFeedthrough -routeBased or define the path for the net in a topology file and use insertPtnFeedthrough -topoFile <filename>

Example:

---

earlyGlobalRoute

insertPtnFeedthrough -routeBased

Or

insertPtnFeedthrough -topoFile <filename>

CHKPTNPIN-652

NAME

CHKPTNPIN-652

SUMMARY

The pushdownBuffer command cannot create an instance with name [%s%s]. An instance with this name already exists in the design. Using default prefix and name [%s] for this instance.

DESCRIPTION

This message is issued if the pushdownBuffer uses the prefix provided with the -prefix option and the resulting name has a conflict with an existing instance name. No action needs to be taken as it will make another name with the default prefix.

CHKPTNPIN-716

NAME

CHKPTNPIN-716

SUMMARY

Partition %s constraint missing. Specify a Guide, Region, Fence constraint on the partition or place the blackbox instance.

DESCRIPTION

While committing partitions 1. Blackboxes should be placed inside core 2. Partitions fences must be core

CHKPTNPIN-780

NAME

CHKPTNPIN-780

SUMMARY

Selected pin assignment: could not assign %d (out of %d) pins because feasible legal location was not found for following pins, need legal locations for pin to be assigned.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

2. Insert feedthrough buffers using the insertPtnFeedthrough command.

CHKPTNPIN-882

NAME

CHKPTNPIN-882

SUMMARY

The insertPtnFeedthrough command was invoked with the -routeBased option, but the design has not yet been routed. The insertPtnFeedthrough command will skip the nets that are not routed. Route the design using earlyGlobalRoute for these nets to be considered for feedthrough insertion.

DESCRIPTION

The insertPtnFeedthrough command invoked with the -routeBased option requires routing for the net to find a path based on which it will insert the feedthrough ports.

The net reported is not routed so it gets ignored. Route the design prior to running this command. The earlyGlobalRoute command can be used to route the design.

Otherwise insertPtnFeedthrough should be invoked without using the -routeBased option in which case the command will try to find a path for the net based on the floorplan and placement (placement based feedthrough insertion).

Example:

---

earlyGlobalRoute

insertPtnFeedthrough -routeBased.

CHKPTNPIN-946

NAME

CHKPTNPIN-946

SUMMARY

Pin named [%s] does not exist in cell [%s]. Ignoring the pin. Check and correct the pin name.

DESCRIPTION

Pin name specified for the specified partition does not exist. Check the pin name and partition name and correct accordingly. Problem could be case sensitivity. Command requires exact name which is case sensitive or incorrect manipulation of "alphabet l or numeric 1" "likewise "alphabet o and numeric 0"

Example:

Pin name could be "isCaseSensitive" but pin name supplied could be "iscasesensitive

CHKPTNPIN-1211

NAME

CHKPTNPIN-1211

SUMMARY

Specified layer [%s] is not within the allowed pin layer range [%s] and [%s] of the partition %s. Re-specify a valid pin layer value or change the partition definition to allow this pin layer and rerun the command again.

DESCRIPTION

Specified layer is not within the allowed pin layer range of the specified partition. Use the Partition->Specify Partition GUI to view the current specified allowed layers. Edit the current allowed pin layers of the partition to include this specified pin layer or re-specify pin layer and rerun the

command again.

CHKPTNPIN-1250

NAME

CHKPTNPIN-1250

SUMMARY

Pin placement has been enabled on metal layer 1.

DESCRIPTION

You have this message because you have enabled metal layer 1 for pin placement. However, metal layer 1 is generally reserved for follow pins. Make sure follow pins are already routed, to ensure that the pins do not block follow pins creation.

Example:

---

setDesignMode -bottomRoutingLayer 1 enables pins in M1

CHKPTNPIN-1520

NAME

CHKPTNPIN-1520

SUMMARY

Pin '%s' of %s '%s' cannot be placed at the constrained location [%0.2f %0.2f] due to a blocked pin slot close to the location. Placing the pin at location [%0.2f %0.2f].

DESCRIPTION

Pin slot can be blocked because of the following reasons

\t 1. pin blockages

\t 2. routing blockages

\t 3. Power ground routing

\t 4. availability of layers to put pins

CHKPTNPIN-1521

NAME

CHKPTNPIN-1521

SUMMARY

Unable to get any valid location for the constrained pin [%s] at location [%0.2f %0.2f].

DESCRIPTION

Pin slot can be blocked because of the following reasons

\t 1. pin blockages

\t 2. routing blockages

\t 3. Power ground routing

\t 4. availability of layers to put pins

CHKPTNPIN-1550

NAME

CHKPTNPIN-1550

SUMMARY

Cell [%s] cannot be specified as a black box because the design does not have any instance associated with this cell or instance may create nested blackBox. Ensure the design has an instance referenced to this cell or specify correct name of cell and rerun %s again.

DESCRIPTION

Specified cell cannot be defined as a black box because the design does not have any instance that is referenced to this cell or instance may create nested blackBox. Ensure there is at least one instance that is associated with this cell and rerun the command again.

CHKPTNPIN-1669

NAME

CHKPTNPIN-1669

SUMMARY

Ptn %s does not have any reserved slots for assigning ptn pins. Check the allowed layers for the partition and make sure that layers based on preferred routing tracks are reserved.

DESCRIPTION

This warning message is issued while assigning pins on a partition using the Innovus GUI with Partition => Assign Pin... or when using the assignPtnPin Tcl command.

The floorplan likely contains a problem with routing tracks and/or pin layer definitions. The problem can be debugged graphically using: Partition => Specify Partition

Select the offending partition and review the Partition Pin Layer Used section. Make sure the layers defined for pins are included in the Layers Reserved For Partition. Corrections may be made and applied with this form. Check the min max layer allowed though getDesignMode another reason could be presence of route blockage or PG on partition edge blocking the routing tracks.

Next, confirm there are preferred routing tracks defined for the pin layers using the Layer Control => Track => Pref Track and the Wire&Via layer defined for the pins. If the tracks are incorrect, they may be regenerated using the "generateTracks" Tcl command.

Example:

getPinConstraint -cell c -side all -layer

Constraint on partition c :

Allowed layer on side [top] : 2 4 6

Allowed layer on side [left] : 3 5

Allowed layer on side [bottom] : 2 4 6

Allowed layer on side [right] : 3 5

getDesignMode -bottomRoutingLayer -topRoutingLayer

-bottomRoutingLayer 2 # string, default=""

-topRoutingLayer 15 # string, default=""

{bottomRoutingLayer 2} {topRoutingLayer 15}

Look for the Tracks in a section with: Track:

While corrections can be made to the tmp.fp file and reloaded with the "loadFPlan tmp.fp" Tcl command, it is generally easier to do make changes with the Innovus GUI.

CHKPTNPIN-1671

NAME

CHKPTNPIN-1671

SUMMARY

The option %s cannot be used for updating pin attribute. Correct the command options and run the command again.

DESCRIPTION

Specified option cannot be used for just updating pin attribute. This option is used with other options for assigning pin location. Check the reference manual for the legal specified options. Then correct the command options and rerun the editPin command again.

CHKPTNPIN-1699

NAME

CHKPTNPIN-1699

SUMMARY

Selective-pin-assignment by specifying just partition name(s) to command assignPtnPin is obsolete and will be removed in future releases. The old usage still works in this release, but to avoid this warning and to ensure compatibility with future releases, replace the obsolete usage with "assignPtnPin -ptn -pin ".

DESCRIPTION

To avoid this warning and to ensure compatibility with future releases, replace the obsolete usage with 'assignPtnPin -ptn <ptnName> -pin <pinName>'

Example:

---

* The following command assign pins name starting with "in" of partition "A" and pins name starting with "out" of partition "B"

assignPtnPin -ptn {A} -pin {in*} -ptn {B} -pin {out*}

* The following command accept a file pinLst.txt that contains the list of pins to be placed for partition A and partition B.

assignPtnPin -ptn A -ptn B -pin_file pinLst.txt

CHKPTNPIN-1704

NAME

CHKPTNPIN-1704

SUMMARY

The options [-row] and [-bringBackRow] are obsolete. Rows are brought back automatically, without using any of these options. To avoid this warning and ensure compatibility with future releases, update your script to not use any of these options.

DESCRIPTION

This messages is issued when obsolete options are used.Using these options will have no impact in this case.

Example:

---

eg. use flattenPartition

CHKPTNPIN-1717

NAME

CHKPTNPIN-1717

SUMMARY

The specifyPartition command will be obsolete in the next release. Use the definePartition command to define the partitions.

DESCRIPTION

The message occurs because you are using 'specifyPartition' which is obsoletelease use the 'definePartition' command to define the partitions.

Example:

The following example defines a partition:

definePartition \

-hinst ctr_inst \

-coreSpacing 0.56 0.56 0.0 0.0 \

-railwidth 0.0 \

-minPitchLeft 2 \

-minPitchRight 2 \

-minPitchTop 2 \

-minPitchBottom 2 \

-reservedLayer {1 2 3 4} \

-pinLayerTop {2 4} \

-pinLayerLeft {3} \

-pinLayerBottom {2 4} \

-pinLayerRight {3} \

-placementHalo 1.0 1.0 1.0 1.0 \

-routingHalo 1.0 \

-routingHaloTopLayer 7 \

-routingHaloBottomLayer 1

CHKPTNPIN-1755

NAME

CHKPTNPIN-1755

SUMMARY

Pin [%s] of %s [%s] connected to net [%s] is [%s] at location (%8.3f, %8.3f) on layer %1d %s.

DESCRIPTION

Message reports specific error/violation on a partition pin.

Example of ABUTMENT violation on a pin:

Pin [pin_1] of partition [ptn_1] connected to net [net_1] is [PLACED] at location (210.452, 540.160) on layer 8 has ABUTMENT violation WITH partition chip.

In above example error/violation is being reported for partition “ptn_1” pin's “pin_1” which is connected to net “net_1” and is placed at location “210.452, 540.160” on layer “8” having assignment status as “placed”. Pin has abutment (is placed on adjoining boundary of “ptn_1” and “chip”) violation with partition named “chip”. Ideally the pin pair of two adjoining (abutting) partitions should be placed on same track on edge of partition boundaries, touching each other (abutting).

Abutment violation could be because of following two reasons:

1. Net has multi-partition-pins. Since all other pins of different partitions cannot be placed at same location (no electrical connection through any overlap of physical shape), so it is reported as abutment violation.

2. “pin_1” pin of net “net_1” is not connected to any pin of adjoining (abutted) partition “chip”.

List other violations on pin:

- pin min-width violation

- pin min-depth violation

- pin missing metal shape violation

- pin min-area violation
- pin-color violation
- pin not on routing track (or ndr-rule-routing-track) violation
- pin not on fence violation
- pin spacing (drc and spacing constraints) violation
- pin not on allowed layer violation
- For nested partition it checks for child fence area violation
- pin outside pin-guide or bus-guide violation
- Pin associated pin-group or net-group violation

CHKPTNPIN-1802

NAME

CHKPTNPIN-1802

SUMMARY

Route layer setting through routing modes [setRouteMode %s <value>] or [setNanoRouteMode %s <value>] setting will not be honored. Set the value using setDesignMode command [setDesignMode %s <value>] and run the command again.

DESCRIPTION

This message is reported related to IO pin routing if there are any IO pins falls above maxRouteLayer. Message ENCPTN-1802 is generated to correct the user expectation, when user had set either setRouteMode or setNanoRouteMode for minLayer but has missed to set setDesignMode for minLayer, and user would like to set min/max layer of pin that is different from earlyGlobalRoute. Innovus checks for this issue and generate the message as user may forget to set min/max layer of pin when it differs from earlyGlobalRoute.

Example:

Because of the following reason the ENCPTN-1802 is reported.

Message ENCPTN-1802 is generated to correct the user expectation, when user had set either setRouteMode or setNanoRouteMode for minLayer but has missed to set setDesignMode for minLayer.

Use "setDesignMode -topRoutingLayer <layer>" to placing IO pins, to avoid this problem.

CHKPTNPIN-3207

NAME

CHKPTNPIN-3207

SUMMARY

The hierarchical-PG net %s is connected to an instance term %s inside the partition hinst %s. However, it is not connected to any PG port of the partition hinst. This is erroneous data. As a consequence, instance term %s will become unconnected. To correct this error, ensure that the above net is connected to a partition PG port when connecting to an instance PG term inside the partition, and run the command again.

DESCRIPTION

Reason of such incorrect PG net connection is generally introduced by either incorrect UPF or incorrect GNC rule. To correct this error, ensure that the above net is connected to a partition PG port when connecting to an instance PG term inside partition. Or, if this connection is not needed inside the partition hinst, then ensure that the net does not connect to any of the PG terms inside the partition hinst.

CHKTB-2

NAME

CHKTB-2

SUMMARY

Cannot complete command %s, not able to open %s for write, provide a file path which can be opened for write to complete execution.

DESCRIPTION

The possible reasons you have this message might be:

1. You may not have necessary file operation permissions to create a file on current working directory.

2. There is a same-name file which you do not have write permission on it.

3. You may have run out of disk space.

Example:

Check whether you have permission to create a file on current working directory:

innovus 7> file writable [pwd]

1

Check whether you have a same-name file which you do not have write permission on it on current working directory:

set fileName innovus.log1

if {[file exists $fileName]} {

puts [file writable $fileName]

} else {

puts 0

}

Check if you have run out of disk space:

innovus 16> df -kH [pwd]

Filesystem Size Used Avail Use% Mounted on

/dir/subdirectory1/case/case11189 2.2T 2.0T 271G 88% /dir/subdirectory1/case/case11189

CHKTB-36

NAME

CHKTB-36

SUMMARY

Partition name %s does not match a hierarchical instance or a black box and will be ignored.

DESCRIPTION

The specified name does not match an uncommitted partition (hierarchical instance with a fence) or a black box (floorplan block object).

Example:

deriveTimingBudget -ptn ptnA

Warning: Partition name ptnA does not match a hierarchical instance or a black box and will be ignored.

CHKTB-178

NAME

CHKTB-178

SUMMARY

Command setFixedBudget cannot accept option "-fromFlopsOf" and "-toFlopsOf" together.

DESCRIPTION

setFixedBudget command can only be applied on a path segment. Please use it with pins at either "-from" or "-to" option.

CHKTB-521

NAME

CHKTB-521

SUMMARY

No SDC file found for analysis view %s. Make sure analysis views are properly constrained prior to running deriveTimingBudget.

DESCRIPTION

Check if viewDefinition file has correct SDC files (not a physical only flow or absent timing constraints).

CHKTB-522

NAME

CHKTB-522

SUMMARY

Partition %s's ports %s and %s are connected through verilog assign. Budgeting requires a physical pin inside partition in order to budget timing path inside partition.

DESCRIPTION

Verilog assign statements can be removed using 'remove_assigns -buffering' command before running deriveTimingBudget.

IMPAFP-1873

NAME

IMPAFP-1873

SUMMARY

Old constraint file format for planDesign.

DESCRIPTION

This message occurs because the constraint file format you have specified for planDesign is not up-to-date. Please use 'planDesign -genTemplateOnly <file>'to get a template file or use 'mp::dumpConstraint <outFile>' to convert your constraint to new format.

Example:

For more detail, please run 'man planDesign'.

IMPAFP-1909

NAME

IMPAFP-1909

SUMMARY

Same seed name %s specified twice in constraint file.

DESCRIPTION

If constraint file has same seed name defined under BEGIN SEED statement then the commands "planDesign -constraint <file_name>" and "multiPlanDesign-constraint <file_name> on " will output this warning.

Example:

Say a constraint file 'seed.txt' has the below content :-

BEGIN SEED

name= DTMF_INST/SPI_INST util=0.6 createFence=true

name= DTMF_INST/SPI_INST util=0.75 createFence=true minFenceToFenceSpace=60

END SEED

Then, 'planDesign -constraint seed.txt' or 'multiPlanDesign -constraint

seed.txt on' will give the warning. " **WARN: (IMPAFP-1909): Same seed name

DTMF_INST/SPI_INST specified twice in constraint file.

IMPAFP-2031

NAME

IMPAFP-2031

SUMMARY

Module %s has a createFence=true constraint on it, but it already has a fence in the database. Check constraint file and remove this constraint to avoid this message.

DESCRIPTION

When parsing the constraints file planDesign verifies modules with createFence=true are not already defined as fences in the floorplan. If they are, this error message is issued. To avoid this error remove this constraint from the planDesign constraint file or edit the attributes of the module and change its Constraint Type to None.

Example:

BEGIN SEED

name=%s createFence=true

IMPAFP-3353

NAME

IMPAFP-3353

SUMMARY

Failed to honor at least one MPGroup Fence|Hard or Power Domain constraint.

DESCRIPTION

Check planDesign constraint file whether the seed names are provided correctly."name" in the constraint file should be a hierarchy or inst group.

Example:

Example:

BEGIN SEED

name=A1/B2 util=0.75

name=C1/D3/M5 createFence=true minFenceToFenceSpace=60

name=E1 minWHRatio=0.25 maxWHRatio=4.0

name=F2 master=E1 cloneOrient={R0|MX}

name=PDGp1 util=0.6 createFence=true minFenceToInsideMacroSpace=10

H1 and H2 can be existing fences.

name=H1 minFenceToInsideMacroSpace=10 minFenceToOutsideMacroSpace=10

name=H2 minInsideFenceMacroToMacroSpace=15

END SEED

IMPAFP-3928

NAME

IMPAFP-3928

SUMMARY

Something wrong in parsing your seed file %s.

DESCRIPTION

The message is issued due to syntax error that is parsed as constraint file for planDesign. User to look and correct the syntax.

Example:

Follow below example for correct syntax

For example:

BEGIN SEED

name=A1/B2 util=0.75

name=C1/D3/M5 createFence=true minFenceToFenceSpace=60

name=E1 minWHRatio=0.25 maxWHRatio=4.0

name=F2 master=E1 cloneOrient={R0|MX}

name=PDGp1 util=0.6 createFence=true minFenceToInsideMacroSpace=10

H1 and H2 can be existing fences.

name=H1 minFenceToInsideMacroSpace=10 minFenceToOutsideMacroSpace=10

name=H2 minInsideFenceMacroToMacroSpace=15

END SEED

IMPAFP-3952

NAME

IMPAFP-3952

SUMMARY

It is not recommended to run planDesign with too many instances (%d) already pre-placed.

DESCRIPTION

Too many preplaced std. cells can affect planDesign quality as well as slow down run. So we will issue this ERROR message when pre-placed instances is over 5000 for non-IO & non-Hardmacro.

Example:

[DEV]innovus 4> placeJtag -nrRowLeft 8 -nrRowRight 8 -nrRowTop 8 -nrRowBottom

[DEV]innovus 4> planDesign

Design Statistics :

Fixed StdCells: 9113, Fixed HMs: 0, IO Cells: 982

**ERROR: (SOCAFP-3952): It is not recommended to run planDesign with too many

instances (9113) already pre-placed.

The limit is 5000 non-IO non-Hardmacro pre-placed standard cells.

Please use setPlanDesignMode -freePreplaced or setPlanDesignMode

-ignorePreplaced to continue

IMPAFP-5000

NAME

IMPAFP-5000

SUMMARY

Seed constraint %s at line %d is not a fence in db. Ignore this constraint.

DESCRIPTION

checkFPlanSpace will check fences inside Masterplan constraint file. If it is not fence, it will issue this message to tell user checkFPlanSpace will not check it.

Example:

(1) Seed file

VERSION 1.0

BEGIN SEED

name=U_IOP/U_IOP_MPI

name=U_IOP/U_IOP_MPI

END SEED

(2)

<CMD> checkFPlanSpace -reportWarning -constraint tn_seed

**WARN: (IMPAFP-5000): Seed constraint U_IOP/U_IOP_MPI at line 3 is not a

fence in db. Ignore this constraint.

IMPAFP-5002

NAME

IMPAFP-5002

SUMMARY

Macro constraint %s at line %d is not placed in db (macro %s). Ignore this macro.

DESCRIPTION

This warning comes during planDesign -constraint <> or multiPlanDesign-constraint <> when there is Macro defined in Macro Section BEGIN MACRO ... END MACRO in constraint file without isCell=true/false defined for the macro.

IMPAFP-5029

NAME

IMPAFP-5029

SUMMARY

Found Fence to fence violation on area %.3f %.3f %.3f %.3f for fence %s and %s.

DESCRIPTION

We could add this line along with the existing WARN message.There is not enough area for fence to adjust its location inside core area hence there is overlap between fences.

Example:

(1) Seed file

VERSION 1.0

BEGIN SEED

name=U_IOP/INSTANCE_IOP_CHANNEL_AND_CLK_GATING[9].U_IOP_CHANNEL

createfence=true util=0.75 minFenceToFenceSpace=50

name=U_IOP/INSTANCE_IOP_CHANNEL_AND_CLK_GATING[10].U_IOP_CHANNEL

createfence=true util=0.75 minFenceToFenceSpace=50

name=U_IOP/INSTANCE_IOP_CHANNEL_AND_CLK_GATING[11].U_IOP_CHANNEL

createfence=true util=0.75 minFenceToFenceSpace=50

END SEED

(2)

<CMD> planDesign -constraints tn_seed.11

**WARN: There is not enough area for fence to adjust its location inside core

area hence there is overlap between fences.

**WARN: (IMPAFP-5029): Found Fence to fence violation on area 995.150 335.650

1203.670 335.750 for fence

U_IOP/INSTANCE_IOP_CHANNEL_AND_CLK_GATING[9].U_IOP_CHANNEL and

U_IOP/INSTANCE_IOP_CHANNEL_AND_CLK_GATING[11].U_IOP_CHANNEL.

IMPAFP-9003

NAME

IMPAFP-9003

SUMMARY

No license for %s In Innovus 11.1 and prior .

DESCRIPTION

The error is reported because Innovus does not have the proper license available to run these features.%s requires one of the following licenses. The command in parenthesis shows what options to use when invoking the tool to check out the proper license:For more information on Innovus Digital Implementation (Innovus) System licensing and packaging please see the chapter titled "Product and Licensing Information"in the Innovus User Guide.

Example:

First Innovus XL or GXL (innovus -fexl or -fegxl)

SOC Innovus XL or GXL (innovus -socexl or -socegxl)

Innovus Digital Implementation System L or XL (velocity -edsl or -edsxl)

IMPAFP-9021

NAME

IMPAFP-9021

SUMMARY

Failed to read in timing data, check timing constraint or library, set timingDriven false.

DESCRIPTION

planDesign command in Innovus generates a quick, initial floorplan that can be used as a starting point for making the final floorplan. Use the planDesign command to create multiple alternative floorplans. User can then test the floorplans to find the one that gives the best placement and routing results. PlanDesign can be run in timingDrivenMode. By default, Automatic Floorplan Synthesis takes timing constraints into account during floorplan generation, if timing libraries (.lib) and SDC constraint files are loaded in the design. It will not perform timing aware floorplanning if either the timing library or constraint file is not loaded, and if either liberty or constraint file is missing planDesign would issue the warning message : "Failed to read in timing data, check timing constraint or library, set timingDriven false." This warning message is added to tell user the reason is that the timing data is lacking or not colmplete.

IMPAFP-9117

NAME

IMPAFP-9117

SUMMARY

Set option %s to on, it is invalid to use -autoTrial -%s on_off.

DESCRIPTION

If you specify the -autoTrials parameter, you can specify only the on value for boolean parameters. You cannot specify on_off. For example, you can specify -boundaryPlace on, but you cannot specify -boundaryPlace on_off.

Example:

<CMD> multiPlanDesign -autoTrials 2 -congAware on_off

-effort medium # string, default=medium

**WARN: (IMPAFP-9117): Set option congAware to on, it is invalid to use

-autoTrial -congAware on_off.

IMPAFP-9641

NAME

IMPAFP-9641

SUMMARY

Constraint file %s does not exist. Check input.

DESCRIPTION

The message is issued due to syntax error that is parsed as constraint file for planDesign. User to look and correct the syntax.

Example:

Follow below example for correct syntax

For example:

BEGIN SEED

name=A1/B2 util=0.75

name=C1/D3/M5 createFence=true minFenceToFenceSpace=60

name=E1 minWHRatio=0.25 maxWHRatio=4.0

name=F2 master=E1 cloneOrient={R0|MX}

name=PDGp1 util=0.6 createFence=true minFenceToInsideMacroSpace=10

H1 and H2 can be existing fences.

name=H1 minFenceToInsideMacroSpace=10 minFenceToOutsideMacroSpace=10

name=H2 minInsideFenceMacroToMacroSpace=15

END SEED

IMPAFP-9642

NAME

IMPAFP-9642

SUMMARY

The utilization of seed %s is greater than %100.

DESCRIPTION

Density over 100% is likely caused by PlanDesign shrinking its constraint to avoid an overlap. One solution for this case is to setPlanDesign -refineSeed{-rectilinearGuides}. This will enable the refineSeed to create the rectilinear guides to avoid overlaps. In default, planDesign only create rectangle guides.

Example:

setPlanDesign -refineSeed {-rectilinearGuides}

IMPAFP-9643

NAME

IMPAFP-9643

SUMMARY

The needed area is greater than the available place area in fence %s with current utilization %f, adjust the fence utilization to %f.

DESCRIPTION

This Warning message is generated when total cell area of the module/modules assigned to this fence is greater than available placable area in the fence

Example:

In order to fix this issue the user needs to change the fence utilization,

thereby increasing placement area in the Fence. This can be done using

Move/Resize/Reshape button in the floorplan GUI or by re-running "createFence"

command with the increased box size

IMPAFP-9644

NAME

IMPAFP-9644

SUMMARY

Adjust the seed %s utilization from %f to %f.

DESCRIPTION

When defining utilization for fence is too small in Masterplan constraint file,total fence area is possible too large and over core area. In this condition,tool will issue this message.We could add this line along with the existing WARN message being specified.

Example:

(1) Seed file:

VERSION 1.0

BEGIN SEED

name=U_IOP/U_IOP_MPI createfence=true util=0.3

name=U_IOP/INSTANCE_IOP_CHANNEL_AND_CLK_GATING[0].U_IOP_CHANNEL

createfence=true util=0.3

name=U_IOP/INSTANCE_IOP_CHANNEL_AND_CLK_GATING[1].U_IOP_CHANNEL

createfence=true util=0.3

END SEED

(2) planDesign -constraints tn_seed.11

**WARN: (IMPAFP-9644): Adjust the seed U_IOP/U_IOP_MPI utilization from

0.300000 to 0.727028.

**WARN: (IMPAFP-9644): Adjust the seed

U_IOP/INSTANCE_IOP_CHANNEL_AND_CLK_GATING[0].U_IOP_CHANNEL utilization from

0.300000 to 0.727028.

**WARN: (IMPAFP-9644): Adjust the seed

U_IOP/INSTANCE_IOP_CHANNEL_AND_CLK_GATING[1].U_IOP_CHANNEL utilization from

0.300000 to 0.727028.

IMPAFP-9645

NAME

IMPAFP-9645

SUMMARY

The needed area is greater than the available place area in top level, adjust the fence utilization to %f.

DESCRIPTION

When fence utilization in the Masterplan constraint file is too small, the fence area is possible

greater than the available place area in top level. In this scenario, it will issue this message.

Example:

(1) Seed file of tn_seed.11

VERSION 1.0

BEGIN SEED

name=U_IOP/U_IOP_MPI createfence=true util=0.3

name=U_IOP/INSTANCE_IOP_CHANNEL_AND_CLK_GATING[0].U_IOP_CHANNEL createfence=true util=0.3

name=U_IOP/INSTANCE_IOP_CHANNEL_AND_CLK_GATING[1].U_IOP_CHANNEL createfence=true util=0.3

END SEED

(2) planDesign -constraints tn_seed.11

**WARN: (IMPAFP-9645): The needed area is greater than the available place area in top level, adjust the fence utilization to 0.727028.

**WARN: (IMPAFP-9644): Adjust the seed U_IOP/U_IOP_MPI utilization from 0.300000 to 0.727028.

**WARN: (IMPAFP-9644): Adjust the seed U_IOP/INSTANCE_IOP_CHANNEL_AND_CLK_GATING[0].U_IOP_CHANNEL utilization from 0.300000 to 0.727028.

**WARN: (IMPAFP-9644): Adjust the seed U_IOP/INSTANCE_IOP_CHANNEL_AND_CLK_GATING[1].U_IOP_CHANNEL utilization from 0.300000 to 0.727028.

IMPAFP-9649

NAME

IMPAFP-9649

SUMMARY

The option %s is not supported in high effort; it is a medium effort option .

DESCRIPTION

setPlanDesignMode -keepGuide is only supported when Automatic FloorPlan Synthesis is run in medium effort.Module guides created as part of Automatic FloorPlan Synthesis can be either retained or discarded. This can be controlled by option:

Example:

The following script will result in this error when using Innovus version 13.1 and

older

setPlanDesignMode -effort high

setPlanDesignMode -keepGuide false

planDesign

To avoid this error, change effort from -high to -medium

setPlanDesignMode -effort medium

setPlanDesignMode -keepGuide false

planDesign

IMPAFP-9801

NAME

IMPAFP-9801

SUMMARY

Cannot find any instance pins or hierarchical instance pins from specified %s points '%s'.

DESCRIPTION

The specified start points or end points should be hinst or hinst pins or instance pins.

Example:

<CMD> create_dataflow_bus -name dataflow1 {{hinst1/inst1*/out* hinst2/inst2*/in*}}

<CMD> create_dataflow_bus -name dataflow2 {{hinst1 hinst2} {hinst1 hinst3}}

IMPAFP-9805

NAME

IMPAFP-9805

SUMMARY

The format of data flow bus definition is not correct.

DESCRIPTION

The format is {{<startPoint> <endPoint>}*}

Example:

<CMD> create_dataflow_bus -name dataflow1 {{hinst1/inst1*/out* hinst2/inst2*/in*}}

<CMD> create_dataflow_bus -name dataflow2 {{hinst1 hinst2} {hinst1 hinst3}}

IMPAFP-9811

NAME

IMPAFP-9811

SUMMARY

Not flatten '%s' since no hierarchical instances under '%s' will be placed.

DESCRIPTION

If the area of a hierarchical instance is less than one fiftieth of parent's, it will not be placed. Please check if there are hierarchical instances under the specified module and the area of hierarchical instances.

IMPAFPU-3817

NAME

IMPAFPU-3817

SUMMARY

-timing is ignored because .lib or sdc is not available.

DESCRIPTION

The option -timing is ignored because timing information is not available. Check to make sure both timing libraries and SDC constraints have been loaded properly. Timing libraries are defined using create_library_set and SDC constraints are defined using create_constraint_mode. These commands are either part of a user initialization (TCL) script or in the viewDefinition.tcl file that is part of the design database. Verify that this information is being defined properly and that the relevant files exist and are readable.

IMPAFPU-3819

NAME

IMPAFPU-3819

SUMMARY

-timing is ignored in low effort.

DESCRIPTION

Command analyzeFloorplan with low effort provides cluster mode placement (non-timing driven). This results in low analysis accuracy, but a fast run time. Option '-timing' is ignored in low effort because placement is in cluster mode and without timing driven. Option '-timing' can be specified in medium or high effort analyzeFloorplan.

IMPAFPU-9005

NAME

IMPAFPU-9005

SUMMARY

In Flex-model flow, 'analyzeFloorplan -cong' should be run before 'analyzeFloorplan -timing' to ensure the design is routable before checking timing.

DESCRIPTION

In Flex-model flow, analyzeFloorplan -timing is running by 4 iterations of timing-driven trialroute by default. During the flex model flow the first call to analyzeFloorplan is recommended to use analyzeFloorplan -cong (instead of -timing) to run trialroute only once and make sure quickly that your design is routable.

IMPAFPU-9201

NAME

IMPAFPU-9201

SUMMARY

The created fence of %s overlaps with HInst %s.

DESCRIPTION

Fence has a boundary shape that overlaps with the bounding box for another hierarchical instance. Remove the overlap by resizing one of the objects. To do this, select the object in the GUI and use the resize button or use setObjFPlanBox and setObjFPlanBoxList commands to redefine the boundary.

IMPAFPU-9202

NAME

IMPAFPU-9202

SUMMARY

The created fence of %s overlaps with Inst %s.

DESCRIPTION

Fence has a bounding box that overlaps with the placement of instance. If the instance should be placed inside the fence, then add it to the instance group using 'addInstToInstGroup <group> <instance>'. If not, then remove the overlap by resizing the fence or by moving the instance.

IMPCCD-3001

NAME

IMPCCD-3001

SUMMARY

To avoid passing multi-view timing information to CCD when only one view's constraints are read in by CCD, please use: %s -view <view_name>

DESCRIPTION

In MMMC Mode, constraints may be specified using the -view or
-constraints options. By default, a timing report file is
generated for all MMMC views but given that CCD only supports
reading a single mode SDC there may be a mismatch between the
multi-view timing information and single-view constraints passed to CCD
To ensure CCD is passed the same view timing and SDCs, use:
deriveFalsePathCCD -view <view_name>
Example:
deriveFalsePathCCD -view mission+worst-rcTyp

IMPCCOPT-1007

NAME

IMPCCOPT-1007

SUMMARY

Did not meet the max transition constraint. %s

DESCRIPTION

Failure to meet a maximum transition time constraint in the clock tree network usually occurs because:

- Specified transition time is too low. Use 'get_ccopt_property target_max_trans' to check the global setting, and 'get_ccopt_property -clock_tree clk target_max_trans' to check the setting on each clock tree. Use 'report_ccopt_clock_trees' to get a list of violating pins, then check the isDontTouch property on the attached net.

- A net cannot be buffered because it has been marked dont_touch. Use 'report_ccopt_clock_trees' to get a list of violating pins, then check the isDontTouch property on the attached net.

- A net cannot be buffered because some aspect of the floorplan (power domains, blockages,

regions, macros or other fixed instances), prevent placement of buffers.

- Detailed routing of the clock tree has produced routing detours, or excessive numbers of small jogs with vias.

For floorplan and/or routing issues, find the offending net(s) with 'report_ccopt_clock_trees' as above, and observe the floorplan where the net has been routed.

IMPCCOPT-1013

NAME

IMPCCOPT-1013

SUMMARY

The target_max_trans is too low for at least one clock tree, net type and timing corner. Search the log for the string 'Too low;' to find the minimum acceptable targets for each combination. CTS will now terminate.

DESCRIPTION

This usually occurs because:

- The transition time specified has no units specified. For example a user may specify a transition time target of 0.1, not realizing that the library units are ps. In this case, specify the units explicitly (0.1ns instead of 0.1).

- The specified list of clock tree cells (buffers, inverters, clock gates) is very weak. Use 'ccopt_check_prerequisites' to obtain a list of clock tree cells used, and check their drive strength.

If you have reason to believe this is not a problem in your design (eg. it only applies to one power domain which does not need buffering), then the test can be overridden with the property override_minimum_max_trans_target. Forcing CTS to proceed with a value that is too low here may cause long runtimes.

IMPCCOPT-1014

NAME

IMPCCOPT-1014

SUMMARY

In power domain %s, CTS has found that %s can drive %lfcm of wire. This will effectively result in CTS ignoring placement. %s

DESCRIPTION

CTS timing code has found that a single buffer can drive a huge amount of wire in a given power domain. This could be caused by one or more of the following:

1) The layer technology information in the LEF file(s) might be missing or incorrect.

2) An operating condition might be incorrectly configured or using incorrect library data.

3) A capacitance or resistance multiplier may be set incorrectly.

4) The QRC technology file (or captables if no QRC technology file is present) is incorrect.

5) A buffer cell may be poorly characterized.

6) The SDC file and .lib files may be in different time or capacitance units.

IMPCCOPT-1020

NAME

IMPCCOPT-1020

SUMMARY

None of the library cells specified in CCOpt property %s are usable. Clock tree synthesis for clock tree %s will not be possible.

DESCRIPTION

Clock tree synthesis requires at least one buffer cell and one inverter cell to start. When these cannot be found, there are several possible causes:

-There is no explicit cell list set, and all of the clock tree buffers and inverters in the library are marked dont_Use. Either set an explicit list of cells, or mark the clock tree cells needed as 'dont_Use false' (see examples below).

If you have set an explicit list of cells, this message could occur because:

1.the cells listed are missing descriptions in one more analysis views.

2.the cells listed are not usable in a power domain where the named clock tree must be buffered.

3.none of the cells listed have balanced rise/fall characteristics.

For Example:

To designate an explicit lists of cells as buffer cells, inverter cells (NOTE:Both should be set in all cases):

set_ccopt_property buffer_cells <cell list> [-clock_tree <name>]

set_ccopt_property inverter_cells <cell list> [-clock_tree <name>]

To set cells with name pattern CK* as usable cell:

innovus> setDontUse CK* false

IMPCCOPT-1021

NAME

IMPCCOPT-1021

SUMMARY

The lib cell '%s' specified in %s property is not a valid %s. Either remove this cell from the list, or check the .lib model description.

DESCRIPTION

The user has specified a lib cell in a list of cells to be used by CTS (buffers, inverters, clock gates,

delay cells), but the cell specified does not have the requisite function. Either remove the cell from the list defined by CCOpt properties (buffer_cells, inverter_cells, clock_gating_cells, logic_cells, delay_cells), or look closely at the .lib model description.

IMPCCOPT-1023

NAME

IMPCCOPT-1023

SUMMARY

Did not meet the skew target of %s

DESCRIPTION

The user can specify the skew limit on specific skew groups (explore set_ccopt_property target_skew). Failure to meet this constraint could occur because the skew limit target (set by the CCOpt property target_skew) is too tight for CTS to achieve. If that target is reasonable, then check the result of 'report_ccopt_skew_groups' for the following items:

1. One or more nets in the clock tree are unbufferable.

2. Poor availability of clock tree buffer/inverter cells.

3. A skew target had to be slackened off due to conflicts with other skew groups. Check the log file for messages containing the phrase 'slackened off'.

IMPCCOPT-1026

NAME

IMPCCOPT-1026

SUMMARY

Did not meet the insertion delay target of %s

DESCRIPTION

The user can specify the insertion delay limit on specific skew groups (explore set_ccopt_property target_insertion_delay). Failure to meet this constraint could occur because the insertion delay limit target (set by the CCOpt property target_insertion_delay) is too tight for CTS to achieve. If that target is reasonable, then check the result of 'report_ccopt_skew_groups' for the following items:

1. One or more nets in the clock tree are unbufferable.

2. Poor availability of clock tree buffer/inverter cells.

3. An insertion delay target had to be slackened off due to conflicts with other skew groups. Check the log file for messages containing the phrase\0'slackened off'.

IMPCCOPT-1033

NAME

IMPCCOPT-1033

SUMMARY

Did not meet the max_capacitance constraint of %s

DESCRIPTION

This warning at the end of the CCOpt run indicates that the max_capacitance constraint is not met on certain clock tree cell in a given clock tree.

This could happen for the following reasons:

1. Inappropriate max_capacitance constraint on clock tree cells (too tight to be achieved).

2. One or more of the nets in the clock tree are unbufferable, due to power_domain, blockages, region constraints or dont_touch settings.

3. Congestion has yielded detoured nets during detailed routing of the clock nets.

4. The clock tree has a very large load (such as memory, hard blocks) that exceeds the max_capacitance limit on its own.

IMPCCOPT-1038

NAME

IMPCCOPT-1038

SUMMARY

CTS cannot be performed on this design currently because no area is available in which to place clock tree cells in the entire floorplan. Check that you have some rows defined which are not covered by blockages.

DESCRIPTION

CTS cannot be performed on this design currently because no area is available in which to place clock tree cells in the entire floorplan. Check that you have some rows defined which are not covered by blockages. You can avoid this error check by setting the property cts_override_zero_placeable_area, which tells CTS to run despite having zero placeable area.

IMPCCOPT-1041

NAME

IMPCCOPT-1041

SUMMARY

The source_output_max_trans is set for %s, but source_max_capacitance is not. %s will assume a maximum driven capacitance of %s.

DESCRIPTION

At the root pin of the clock tree, the user has set a target for the transition time at the output pin, but has not a max capacitance constraint at the pin. CTS will compute and use a reasonable value for the maximum capacitance. If you are satisfied with this setting, you need not do anything. If not, then

set source_max_capacitance explicitly.

IMPCCOPT-1051

NAME

IMPCCOPT-1051

SUMMARY

No sources are specified for skew group %s. At least one pin must be specified as the source of a skew group.

DESCRIPTION

This skew group is missing its source pin(s), i.e. the reference pin(s) relative to which all of the sinks will be balanced. Correcting this requires deleting and redefining this skew group, making sure the '-sources' argument is included when you redefine it.

IMPCCOPT-1052

NAME

IMPCCOPT-1052

SUMMARY

Skew group %s has source %s which is in the transitive fanout of source %s. Skew group sources must be unrelated to balance the skew group. This can probably be fixed by removing the redundant/conflicting sources.

DESCRIPTION

A skew group in CCOpt may have multiple sources, but among the sources of a skew group no source may be in the fanout cone of any other. This must be resolved by removing the source that is

in the fanout cone. Also, check the SDC file to see if the sources of the corresponding SDC clock are correct.

IMPCCOPT-1053

NAME

IMPCCOPT-1053

SUMMARY

CTS has set the opt_ignore property on clock tree %s. This clock tree cannot be synthesized. It is most likely that there are no buffers or inverters available for this clock tree, or this clock tree is in a dont_touch module or all nets in this clock tree are dont_touch or this clock tree is in an unbufferable or fully blocked power-domain.

DESCRIPTION

CTS has set the opt_ignore property on the clock_tree. This clock tree cannot be synthesized.

This may have occurred for any/all of the following reasons:

1) All nets in the clock tree are dont_touch.

2) The clock tree is in a dont_touch module.

3) The clock tree is in an unbufferable or fully-blocked power-domain.

4) There are no buffers or inverters available to use for the clock tree. You may be able to fix this issue by specifying lib_cells for CTS to use, with the buffer_cells and inverter_cells properties on this clock tree.

IMPCCOPT-1062

NAME

IMPCCOPT-1062

SUMMARY

The following skew groups have invalid sink and/or ignore_pin assignments: %s

DESCRIPTION

This occurs when one or more has been specified as either active sink pins or ignore pins of a skew group, but the pin does not reside in the clock tree network. All pins on skew groups must reside in the clock tree network. This usually occurs because of incorrect user edits made to the skew groups and/or clock trees after automatic creation of the clock tree specification with create_ccopt_clock_tree_spec.

IMPCCOPT-1070

NAME

IMPCCOPT-1070

SUMMARY

Found no matching paths from %s.

DESCRIPTION

The source indicated was specified as an argument to -from in the report_skew_groups command, however no paths matched begin at this pin.

IMPCCOPT-1071

NAME

IMPCCOPT-1071

SUMMARY

Found no matching paths through %s.

DESCRIPTION

The pin indicated was specified as an argument to -through in the report_skew_groups command, however no paths matched run through this pin.

IMPCCOPT-1072

NAME

IMPCCOPT-1072

SUMMARY

Found no matching paths to %s.

DESCRIPTION

The sink indicated was specified as an argument to -to in the report_skew_groups command, however no paths matched terminate at this pin.

IMPCCOPT-1073

NAME

IMPCCOPT-1073

SUMMARY

Found no matching paths in any skew groups.

DESCRIPTION

The arguments supplied define no paths through any skew group.

IMPCCOPT-1074

NAME

IMPCCOPT-1074

SUMMARY

Created clock sink for %s, which was an enable pin of a clock gate.

DESCRIPTION

A clock gate enable pin was found in the clock tree and a clock sink was created. This means the clock gate will not be subject to some optimizations, and will be treated as if it were a piece of combinational logic. It will appear in the clock tree visualizations with a question-mark symbol.

IMPCCOPT-1075

NAME

IMPCCOPT-1075

SUMMARY

In %s, CTS timing code has found that %s is unable to drive any amount of wire when buffering another instance of itself. %s

DESCRIPTION

CTS timing code has found that a single buffer is unable to drive any amount of wire when buffering another instance of itself. This could be caused by one or more of the following:

1) The wire data in the loaded LEF file(s) might be missing or broken.

2) An operating condition might be incorrectly configured or using incorrect library data.

3) A capacitance multiplier may be set incorrectly.

4) A resistance multiplier may be set incorrectly.

5) A buffer cell may be poorly characterized.

6) The SDC file and .lib files may be in different time or capacitance units.

IMPCCOPT-1080

NAME

IMPCCOPT-1080

SUMMARY

Unable to find a %d signal from %s to %s.

DESCRIPTION

Either a rise or fall (or both) output signal from one cell to the pin of another could not be determined.

IMPCCOPT-1081

NAME

IMPCCOPT-1081

SUMMARY

Could not determine if the library cell %s has at least one valid %s.

DESCRIPTION

During balancing, a library cell can be rejected if at least one input and one output could not be found.

IMPCCOPT-1088

NAME

IMPCCOPT-1088

SUMMARY

The clustering attempt breaks insertion delay targets. Trying again.

DESCRIPTION

A clustering attempt breaks insertion delay constraints. After CCOpt issues this message, an additional clustering will be attempted to try and meet the constraints.

IMPCCOPT-1089

NAME

IMPCCOPT-1089

SUMMARY

Did not meet the max_source_to_sink_net_length constraint of %s

DESCRIPTION

This warning at the end of the CCOpt run indicates that the max_source_to_sink_net_length constraint is not met below certain clock tree cell in a given clock tree.

This could happen for the following reasons:

1. Inappropriate max_source_to_sink_net_length constraint (too tight to be achieved).

2. One or more of the nets in the clock tree are unbufferable, due to power_domain, blockages, region constraints or dont_touch settings.

3. Congestion has yielded detoured nets during detailed routing of the clock nets.

IMPCCOPT-1090

NAME

IMPCCOPT-1090

SUMMARY

Did not meet the max_source_to_sink_net_resistance constraint of %s

DESCRIPTION

This warning at the end of the CCOpt run indicates that the max_source_to_sink_net_resistance constraint is not met below certain clock tree cell in a given clock tree.

This could happen for the following reasons:

1. Inappropriate max_source_to_sink_net_resistance constraint (too tight to be achieved).

2. One or more of the nets in the clock tree are unbufferable, due to power_domain, blockages, region constraints or dont_touch settings.

3. Congestion has yielded detoured nets during detailed routing of the clock nets.

IMPCCOPT-1092

NAME

IMPCCOPT-1092

SUMMARY

A target has been set on skew group %s where the constrains property is set to none. The target will not be optimized for.

DESCRIPTION

A skew or insertion delay target has been set on an unconstrained skew group. The target will not be optimized for unless the constrains property for the skew group is changed.

IMPCCOPT-1093

NAME

IMPCCOPT-1093

SUMMARY

The constrains property has been set to none for skew group %s which also has skew or insertion delay targets set. The targets will not be optimized for.

DESCRIPTION

A skew group with insertion delay or skew target has the constrains property set to none. The target will not be optimized for.

IMPCCOPT-1107

NAME

IMPCCOPT-1107

SUMMARY

An over latency of %s is present at the start of skew fixing.

DESCRIPTION

Skew fixing expects no over latency to be present when it is run. This indicates a potential mismatch in window constraints between modes.

IMPCCOPT-1154

NAME

IMPCCOPT-1154

SUMMARY

The original placement group of %s is %s and that is not the same as the parent group of the group on the spine, which is: %s.

DESCRIPTION

When setting property legalized_on_clock_spine the pin was in a different power domain to the pins already legalized on the clock spine. The property legalized_on_clock_spine for a pin can only refer to a clock spine which is in the same power domain as the pin.

IMPCCOPT-1157

NAME

IMPCCOPT-1157

SUMMARY

Did not meet the max_fanout constraint. %s

DESCRIPTION

This warning at the end of the CCOpt run indicates that the max_fanout constraint is not met below certain clock tree cell in a given clock tree.

This could happen due to the following reasons:

1. Inappropriate max_fanout constraint (too small to be achieved).

2. One or more of the nets in the clock tree are unbufferable, due to power_domain, blockages, region constraints or dont_touch settings.

IMPCCOPT-1173

NAME

IMPCCOPT-1173

SUMMARY

The library cell %s has an invalid rising arc.

DESCRIPTION

The rising arc of the library cell is invalid. This is most likely as a result of invalid or incomplete library cell data.

IMPCCOPT-1174

NAME

IMPCCOPT-1174

SUMMARY

The library cell %s has an invalid falling arc.

DESCRIPTION

The falling arc of the library cell is invalid. This is most likely as a result of invalid or incomplete library cell data.

IMPCCOPT-1195

NAME

IMPCCOPT-1195

SUMMARY

Path optimization has given up on node %s for this round because it has been optimized too many times. This could mean path optimization would otherwise hang on this node.

DESCRIPTION

Path optimization has given up on a node because it has been optimized too many times.

IMPCCOPT-1209

NAME

IMPCCOPT-1209

SUMMARY

Non-leaf slew time target of %s%s is too low on %s. The largest %sclock gate is unable to drive the largest %s in %s. To adhere to the given slope target, you will need to select a stronger clock gate, increase the slew target to at least %s or remove these driver cells from the CTS cell lists: %s %s.

DESCRIPTION

Slope/slew/transition target for the clock tree is too small.

CCOpt calculates the slew that arises when you drive a buffer/inverter with a single other buffer/inverter with no wire present between them. If the supplied slew target is smaller than this computed transition time then CTS has no chance of driving multiple buffers so this error is produced and the run stopped.

Increase the slew target to something bigger.

IMPCCOPT-1239

NAME

IMPCCOPT-1239

SUMMARY

CCOpt has updated an 'ignore' skew target for late timing in the CTS primary delay corner for the skew group %s because it has non ignored targets in another corner.

DESCRIPTION

CCOpt has updated an 'ignore' skew target for late timing in the CTS primary delay corner for a skew group because it has non ignored targets in another corner. If you are trying to do CTS for a design where a skew group should explicitly not be balanced in the primary delay corner, such as for a design which uses dynamic voltage and frequency scaling (DVFS), then you can turn off this behavior by setting the cts_allow_ignore_skew_in_primary_corner_for_mmmc property to true.

IMPCCOPT-1241

NAME

IMPCCOPT-1241

SUMMARY

ResizeGates hit its iteration limit and gave up.

DESCRIPTION

ResizeGates hit its iteration limit and gave up. The iteration limit can be controlled by setting the property cts_fine_balance_resize_gates_iteration_limit.

IMPCCOPT-1247

NAME

IMPCCOPT-1247

SUMMARY

More than %.1f%% of clock instances have been set to fixed placement status by the user (%d instances).

DESCRIPTION

A significant proportion of the clock tree instances (clock gates, clock drivers and clock logic) are fixed; either in DEF or fixed by the user. This may adversely affect the clock tree QoR that can be achieved by CCOpt.

If this is a configuration error, the instances can be unlocked using the following command.

foreach inst [get_ccopt_clock_tree_cells *] { dbSet [dbGet -p top.insts.name $inst].pStatus placed }

IMPCCOPT-1260

NAME

IMPCCOPT-1260

SUMMARY

The skew target of %s for %s is too small. For best results, it is recommended that the skew target be set no lower than %s. Using this skew target anyway, because override_minimum_skew_target is set.

DESCRIPTION

Skew target is too small.

CCOpt calculates a minimum skew target which should not lead to excessive buffering. You have set a skew target to a value lower than this minimum.

Either increase the offending skew target, or set the cts_override_minimum_skew_target property to true to disable this check.

IMPCCOPT-1261

NAME

IMPCCOPT-1261

SUMMARY

The skew target of %s for %s is too small. For best results, it is recommended that the skew target be set no lower than %s. The skew target has been relaxed to %s. You may force the use of the tighter skew target by setting override_minimum_skew_target to true.

DESCRIPTION

Skew target is too small.

CCOpt calculates a minimum skew target which should not lead to excessive buffering. You have set a skew target to a value lower than this minimum.

Either increase the offending skew target, or set the cts_override_minimum_skew_target property to true to disable this check.

IMPCCOPT-1262

NAME

IMPCCOPT-1262

SUMMARY

Slew violating nets have been found in the design, but CCOpt is unlikely to resolve these violations due to the design configuration. Review your configuration for the nets shown, or do {set_ccopt_property cts_error_on_problematic_slew_violating_nets 0} to continue with your current configuration. %s

DESCRIPTION

Slew violating nets have been found in the design, but CCOpt is unlikely to resolve these violations due to the design configuration. Review your configuration for the nets shown, or do 'set_ccopt_property cts_error_on_problematic_slew_violating_nets 0' to continue with your current configuration.

IMPCCOPT-1263

NAME

IMPCCOPT-1263

SUMMARY

%s Terminating the run, as it is unlikely to produce good results. Do {set_ccopt_property cts_error_on_problematic_slew_violating_nets 0} to continue with your current configuration.

DESCRIPTION

Slew violating nets have been found in the design, but CCOpt is unlikely to resolve these violations due to the design configuration. Review your configuration for the nets shown, or do 'set_ccopt_property cts_error_on_problematic_slew_violating_nets 0' to continue with your current configuration.

IMPCCOPT-1274

NAME

IMPCCOPT-1274

SUMMARY

Rejecting rectangle: %s.

DESCRIPTION

The property value for cts_cell_density_regions was badly formed and could not be decoded.

IMPCCOPT-1275

NAME

IMPCCOPT-1275

SUMMARY

Property value %s is badly formed: %s %s.

DESCRIPTION

The property cts_cell_density_regions was badly formed and could not be decoded.

IMPCCOPT-1278

NAME

IMPCCOPT-1278

SUMMARY

Special case dont_touch logic cell selections:

DESCRIPTION

When specified, CTS will provide additional log information on the lists of cells that it will consider using when determining if a cell can be resized. This information is only provided for the more specialized cases. Specialized cases include logic cells and any cells marked (either by the user or by an internal constraint) as dont_touch.

IMPCCOPT-1279

NAME

IMPCCOPT-1279

SUMMARY

Special case logic cell selections:

DESCRIPTION

When specified, CTS will provide additional log information on the lists of cells that it will consider using when determining if a cell can be resized. This information is only provided for the more specialized cases. Specialized cases include logic cells and any cells marked (either by the user or by an internal constraint) as dont_touch.

IMPCCOPT-1280

NAME

IMPCCOPT-1280

SUMMARY

Suitable cells available to use for %s are: %s

DESCRIPTION

When specified, CTS will provide additional log information on the lists of cells that it will consider using when determining if a cell can be resized. This information is only provided for the more specialized cases. Specialized cases include logic cells and any cells marked (either by the user or by an internal constraint) as dont_touch.

IMPCCOPT-1281

NAME

IMPCCOPT-1281

SUMMARY

No suitable cells available to use for %s.

DESCRIPTION

When specified, CTS will provide additional log information on the lists of cells that it will consider using when determining if a cell can be resized. This information is only provided for the more specialized cases. Specialized cases include logic cells and any cells marked (either by the user or by an internal constraint) as dont_touch.

IMPCCOPT-1282

NAME

IMPCCOPT-1282

SUMMARY

Special case dont_touch cell selections:

DESCRIPTION

When specified, CTS will provide additional log information on the lists of cells that it will consider using when determining if a cell can be resized. This information is only provided for the more specialized cases. Specialized cases include logic cells and any cells marked (either by the user or by an internal constraint) as dont_touch.

IMPCCOPT-1287

NAME

IMPCCOPT-1287

SUMMARY

CCOpt clustering wanted to clone for insertion delay but the node, %s, cannot be cloned for these reasons: %s.

DESCRIPTION

For more information do:

get_ccopt_property -help cannot_clone_reason

IMPCCOPT-1288

NAME

IMPCCOPT-1288

SUMMARY

CCOpt wanted to clone for balancing (clustering_clone_cells_to_reduce_balancing_conflicts is true) but the node, %s, cannot be cloned for these reasons: %s.

DESCRIPTION

For more information do:

get_ccopt_property -help cannot_clone_reason

IMPCCOPT-1289

NAME

IMPCCOPT-1289

SUMMARY

CCOpt wanted to clone the node, %s, into %d clones for multi-tap off but the node cannot be cloned for these reasons: %s.

DESCRIPTION

For more information do:

get_ccopt_property -help cannot_clone_reason

IMPCCOPT-1299

NAME

IMPCCOPT-1299

SUMMARY

Found property target_max_trans set to ignore for clock tree %s in the primary half corner %s and %s, %s will not be possible.

DESCRIPTION

Consider setting the target_max_trans property.

IMPCCOPT-1314

NAME

IMPCCOPT-1314

SUMMARY

The setting of %s for the max_source_to_sink_net_length property may be too low. Increase it to more than %s to avoid this warning.

DESCRIPTION

The lower limit for the property is calculated as max_source_to_sink_net_length_warn_multiple times the row height.

Check the value of the property or reduce max_source_to_sink_net_length_warn_multiple.

IMPCCOPT-1315

NAME

IMPCCOPT-1315

SUMMARY

The setting of %s for the max_source_to_sink_net_length property is too low. Increase it to more than %s to avoid this error.

DESCRIPTION

The lower limit for the property is calculated as max_source_to_sink_net_length_error_multiple times the row height.

Check the value of the property or reduce max_source_to_sink_net_length_error_multiple.

IMPCCOPT-1316

NAME

IMPCCOPT-1316

SUMMARY

Reason(s) why cloning is prevented for %s: %s

DESCRIPTION

For more information do:

get_ccopt_property -help cannot_clone_reason

IMPCCOPT-1317

NAME

IMPCCOPT-1317

SUMMARY

CCOpt clustering wanted to clone to meet DRV constraints, because the allow_buffering property is false, but the node, %s, cannot be cloned for these reasons: %s.

DESCRIPTION

For more information do:

get_ccopt_property -help cannot_clone_reason

IMPCCOPT-1322

NAME

IMPCCOPT-1322

SUMMARY

CCOpt clustering wanted to clone to meet a maximum_stage_depth constraint but the node, %s, cannot be cloned for these reasons: %s.

DESCRIPTION

For more information do:

get_ccopt_property -help cannot_clone_reason

IMPCCOPT-1348

NAME

IMPCCOPT-1348

SUMMARY

CCOpt wanted to clone %s, but it cannot be cloned for these reasons: %s.

DESCRIPTION

For more information do:

get_ccopt_property -help cannot_clone_reason

IMPCCOPT-1368

NAME

IMPCCOPT-1368

SUMMARY

CTS cannot use the preferred layers from route type %s: top %s(%s) and bottom %s(%s). CTS will instead use preferred layers: top %s(%s) and bottom %s(%s).

DESCRIPTION

To be suitable for CTS a route_type must have at least one horizontal layer and one vertical layer. Check the preferred layers for the route_type.

IMPCCOPT-1372

NAME

IMPCCOPT-1372

SUMMARY

Found multiple values of cts_max_fanout for cells within the same family (%s). CTS may take the most constraining value for the family (%u). Consider setting cts_max_fanout for all family members to the same value.

DESCRIPTION

CTS will try to satisfy cts_max_fanout constraints and will report violations. The property cts_max_fanout can be set per library output pin, however, the same value should be used for all cells in a cell family. Violations of this rule may produce spurious violation reporting or unexpected optimization results.

IMPCCOPT-1373

NAME

IMPCCOPT-1373

SUMMARY

Found libary-pin specific values of cts_max_fanout (%s) that are set higher than the global value (%u). Consider increasing the global value to be larger than the libary-pin specific values.

DESCRIPTION

CTS will try to satisfy cts_max_fanout constraints and will report violations. The property cts_max_fanout can be set per library output pin or globally (without a library pin). Optimization expects that the global value is set >= than the per library cell value. Violations of this rule may produce spurious violation reporting or unexpected optimization results.

IMPCCOPT-1405

NAME

IMPCCOPT-1405

SUMMARY

The estimated amount of delay that will be added in Balancing is very high: %s. Delay will be added at many locations in the tree, and continuing will result in high runtimes and poor area.

DESCRIPTION

Most likely an ideal or dont_touch net is preventing CTS to add delay high in the clock tree, such that delay is added at many locations lower in the tree.

We suggest doing a trial balancing and investigating with the clock tree debugger.

To force CCOpt to exit please enable the CCOpt property "exit_if_trial_balance_delay_estimation_high".

IMPCCOPT-1470

NAME

IMPCCOPT-1470

SUMMARY

%s is in the skew group %s but is not a sink of the skew group. Try 'report_ccopt_skew_groups -skew_group %s -through %s' instead.

DESCRIPTION

Given pin is in the given skew group but is not a sink of the skew group. When command 'report_ccopt_skew_groups' is used with the argument '-to' expected argument after '-to' is a sink.

Try using the argument '-through' instead of '-to'.'

IMPCCOPT-1471

NAME

IMPCCOPT-1471

SUMMARY

%s is a source of the skew group %s.

DESCRIPTION

Given pin is a source of the skew group. When command 'report_ccopt_skew_groups' is used with the argument '-to' expected argument after '-to' is a sink.

IMPCCOPT-2001

NAME

IMPCCOPT-2001

SUMMARY

Clock domain skew group creation did not visit %s.

DESCRIPTION

Clock domain skew group creation did not visit every node in the clock DAG. The clock domain skew groups may be incomplete which may create problems clustering the clock tree or implementing the clock schedule.

IMPCCOPT-2006

NAME

IMPCCOPT-2006

SUMMARY

Output hInstTerm %s is not connected to any driver inside the hInst. Ignoring %s.

DESCRIPTION

An output hInstTerm is not connected to any driver inside the hInst. You should check the Verilog; one possibility is that the output port should be an input port.

IMPCCOPT-2023

NAME

IMPCCOPT-2023

SUMMARY

All CCOpt commands require that the ILM type is set to '%s', however, this is currently not the case. The ILM type '%s' will now be set.

DESCRIPTION

CCOpt requires that all ILMs are flat and configured to use the correct model for the current routing status of the design. Unrouted or partially routed designs should use 'timing' ILMs, while fully routed designs should use 'SI' ILMs. The current routing status can be controlled with the CCOpt property 'force_design_routing_status'.

IMPCCOPT-2024

NAME

IMPCCOPT-2024

SUMMARY

The command 'setIlmType -model timing' was run, but did not exit cleanly.

DESCRIPTION

The command 'setIlmType -model timing' was run, but did not exit cleanly. This may lead to problems in the CCOpt flow. Consider setting this manually in your design.

IMPCCOPT-2025

NAME

IMPCCOPT-2025

SUMMARY

CCOpt properties set with 'set_ccopt_property' will have no effect when the scripted integration of CCOpt is run.

DESCRIPTION

CCOpt properties set with 'set_ccopt_property' will have no effect when the scripted integration of CCOpt is run. If you are setting CCOpt properties, you should switch to the native integration before running optimization by using: 'set_ccopt_mode -integration native'.

IMPCCOPT-2026

NAME

IMPCCOPT-2026

SUMMARY

Always on cell %s will not be used as buffer or inverter in CCOpt because power management checks are turned off.

DESCRIPTION

An always on cell will not be used as buffer or inverter in CCOpt because power management checks are turned off. Set CCOpt property 'consider_power_management' to true to turn on power management checking.

IMPCCOPT-2027

NAME

IMPCCOPT-2027

SUMMARY

Computing a standard slew value for view '%s' and power domain '%s'. This view/power domain combination did not exist when CCOpt was initialized.

DESCRIPTION

CCOpt had to compute a standard slew value for a view and power domain combination which did not exist when CCOpt was initialized. One possibility is that the active views have changed, which is currently not supported by CCOpt.

IMPCCOPT-2267

NAME

IMPCCOPT-2267

SUMMARY

Cell %s will not be used as it is unable to drive %d instances of itself (input cap is %s) because its max cap at clock period %s is %s. The number of instances used in this check can be adjusted with the frequency_dependent_max_cap_usability_check_max_cap_fanout_factor property.

DESCRIPTION

This message appears when a cell has been found to be unable to drive enough capacitance at a particular frequency. This is determined from the frequency dependent max cap defined in the lib file (the max_cap property on the cell's output pin). In order to build a tree, a cell must be able to drive at least two other cells, and some wire, so CCOpt checks that the cell can drive at least four instances of itself at each frequency used in the clock tree. The number of instances used in this calculation can be set using the property frequency_dependent_max_cap_usability_check_max_cap_fanout_factor. Reducing it may prevent CCOpt from being able to build valid trees, and may introduce runtime issues.

IMPCCOPT-2319

NAME

IMPCCOPT-2319

SUMMARY

ILM pin %s has %u fanout, which is more than the configured limit of %d. CCOpt will consider the fanout as ignore pins.

DESCRIPTION

An ILM pin had a large number of fanout, probably caused by unsynthesized clock trees in the ILM. This check can be controlled with the property extract_ilm_fanout_limit, but raising it may lead to slow runtimes.

IMPCCOPT-2327

NAME

IMPCCOPT-2327

SUMMARY

Internal Error: %s power context changed in SetCellDecl on %s.

DESCRIPTION

CCOpt has replaced a cell and now the power context is different. This is an internal error, and should not happen. Please report it to your local Cadence support representative. There are likely to be power management violations in the clock tree.

IMPCCOPT-2347

NAME

IMPCCOPT-2347

SUMMARY

Could not build any timing models for the generated clock tree %s (output pin %s, library cell pin %s). Clock tree timing may be inaccurate.

DESCRIPTION

This message appears when CCOpt is unable to set up a timing model for the specified output pin and may be caused by e.g. missing timing arcs for that pin in the Liberty data for one or more

analysis views. This will prevent the tool from correctly determining the transition time and delay at the specified output pin and may lead to inaccurate optimization and reporting of delays and DRVs.

To avoid this situation, the Liberty timing data (.lib data) must be checked and corrected to ensure arcs are present for the library pin in question for all analysis views. Alternatively, consider setting the property source_output_max_trans.

More detailed reporting of which timing arcs are missing is avialable in the 'Missing Timing Arcs' table produced by report_ccopt_clock_trees.

IMPCCOPT-2393

NAME

IMPCCOPT-2393

SUMMARY

Useful skew engine failed to restore: encountered %u errors.

DESCRIPTION

This message typically indicates that the clock network has been modified such that it is no longer consistent with the saved state of the useful skew engine. Searching earlier in the flow for IMPCCOPT-2231 messages will normally help identify the problem. The number of reported errors gives a sense of the scale of the problem.

IMPCCOPT-2396

NAME

IMPCCOPT-2396

SUMMARY

Reached the maximum number of arc chains defined by the attribute nma_finder_max_arc_chains (%d) when adding chain for cell (%s), input (%s), output (%s).

DESCRIPTION

The number of arc chains reached %d, the maximum defined by attribute nma_finder_max_arc_chains. Further arcs we be pruned.

IMPCCOPT-2400

NAME

IMPCCOPT-2400

SUMMARY

Property useful_skew_ideal_mode_set_clock_latency is set to false. Early clock flow pre-CTS useful skew has been disabled.

DESCRIPTION

If ECF is not able to generate set_clock_latency assertions it is unable to implement useful skews. Therefore the useful skew transform is disabled in this case. This situation is probably unintended. To resolve this error, either disable pre-CTS useful skew entirely, or else set the specified property back to its default value.

IMPCCOPT-3084

NAME

IMPCCOPT-3084

SUMMARY

%d arguments were supplied to the ccopt_log command. This is too few. The minimum is a log identifier.

DESCRIPTION

Too few argument were supplied to the ccopt_log command. The minimum is a log identifier.

IMPCCOPT-3085

NAME

IMPCCOPT-3085

SUMMARY

The log identifier %d was not found. It should appear in a .logid file.

DESCRIPTION

A log identifier was not found. It should appear in a .logid file.

IMPCCOPT-4144

NAME

IMPCCOPT-4144

SUMMARY

The SDC clock %s has source pin %s, which is an input pin. Clock trees for this clock will be defined under the corresponding output pins instead.

DESCRIPTION

An SDC clock has a source pin which is an input pin. There is no obvious output pin on the same cell which propagates the clock signal. No clock tree definition will be extracted for this clock.

IMPCCOPT-4156

NAME

IMPCCOPT-4156

SUMMARY

The SDC clock %s has source pin %s, which drives a net that has other drivers. Clock trees for this clock will be defined on the fanout pins of the net instead.

DESCRIPTION

The pin (or port) referenced in an SDC create_clock or create_generated_clock is an output pin driving a net that has multiple drivers. CTS cannot build a clock tree rooted at that pin because it is not possible to control the delay since the other drivers of the net are not in the clock tree. CTS will move the clock tree and skew group definitions to the fanout pins, creating a skew group with multiple sources if needed to ensure that the entire transitive fanout of the original pin is included.

To eliminate this message, change the SDC to avoid defining clocks on pins whose driven nets have multiple drivers.

IMPCCOPT-4196

NAME

IMPCCOPT-4196

SUMMARY

Found a cycle containing the following generated clock trees:%s%s

DESCRIPTION

Found a cycle caused by generated clock trees. Where possible, this is resolved by removing some parents of generated clock trees.

IMPCCOPT-4205

NAME

IMPCCOPT-4205

SUMMARY

Differing SDC set_clock_transition constraints exist for the clocks present at %s across the timing configs specified. The tightest found constraint of %f will be used.

DESCRIPTION

An SDC derived clock tree constraint differs between timing configs. The tightest applicable constraint has been applied.

IMPCCOPT-4232

NAME

IMPCCOPT-4232

SUMMARY

No usable inverter has been found. It could be that there are no inverters defined in the libraries or all inverters are set as dont_use. Ensure that all required libraries have been loaded and check the dont_use settings for inverter cells within your libraries.

DESCRIPTION

For example:

To get a list of all cells marked dont_use: reportDontUseCells

To disable a dont_use on a library cell: setDontUse <cell-name> false

IMPCCOPT-4245

NAME

IMPCCOPT-4245

SUMMARY

The width of the vertical clock spine %s will implicitly be increased so its boundary is aligned on a multiple of the placement site grid. It is now from %s

DESCRIPTION

Spine flow for CCOpt is currently not supported. Please consult support AE.

IMPCCOPT-4246

NAME

IMPCCOPT-4246

SUMMARY

Found a cell which overlaps a cleared hard clock spine region: %s at %s.

DESCRIPTION

Spine flow for CCOpt is currently not supported. Please consult support AE.

IMPCCOPT-4251

NAME

IMPCCOPT-4251

SUMMARY

The design database has been modified by one or more Tcl commands and '%s' was unable to resynchronize the CCOpt data structures. The reason is: %s%s

DESCRIPTION

The design database has been modified by one or more Tcl commands. The CCOpt data structures could not be resynchronized. The command 'delete_ccopt_clock_tree_spec' may run internally to reset the CCOpt state.

IMPCCOPT-4318

NAME

IMPCCOPT-4318

SUMMARY

No default buffer cell family identified.

DESCRIPTION

This message occurs because there is no buffer cell available for clock tree synthesis. Please make sure the buffers you have specified with '-cts_buffer_cells' for '' are available in the current Innovus session.

For example, the follow example returns the library cells with prefix 'CKBUF':

innovus> get_lib_cells CKBUF*#@innovus> get_db lib_cells CKBUF*

slowlib/CKBUFD1 slowlib/CKBUFD2 fastlib/CKBUFD1 fastlib/CKBUFD2

IMPCCOPT-4319

NAME

IMPCCOPT-4319

SUMMARY

Default buffer cell family exemplar %s has all members marked dont_use.

DESCRIPTION

All the buffer cells specified by the buffer_cells property are marked as dont_use.

Please check the dont_use state of the given buffer cells.

For example, resetting dont_use attribute on cells with prefix 'CK*':

innovus> setDontUse CK* false

IMPCCOPT-4320

NAME

IMPCCOPT-4320

SUMMARY

No default Inverter cell family identified.

DESCRIPTION

This message occurs because there is no inverter cell available for clock tree synthesis. Please make sure the inverters you have specified with the inverter_cells property are available in the

current Innovus session.

For example, The follow example returns the library cells with prefix 'CKINV':

innovus> get_lib_cells CKINV*

slowlib/CKINVD1 slowlib/CKINVD2 fastlib/CKINVD1 fastlib/CKINVD2

IMPCCOPT-4321

NAME

IMPCCOPT-4321

SUMMARY

Default inverter cell family exemplar %s has all members marked dont use. It could be that all inverters defined by the inverter_cells property cannot be used due to dont_use setting. Check the dont_use settings for inverter cells within your libraries.

DESCRIPTION

For example:

To get a list of all cells marked dont_use: reportDontUseCells

To disable a dont_use on a library cell: setDontUse <cell-name> false

IMPCCOPT-4322

NAME

IMPCCOPT-4322

SUMMARY

No default Or cell family identified.

DESCRIPTION

This message occurs because there is no OR cell available for clock tree synthesis. Please make sure the OR cells you have specified by the logic_cells property are available in the current Innovus session.

For example, the follow example returns the library cells with prefix 'CKOR':

innovus> get_lib_cells CKOR*

slowlib/CKORD1 slowlib/CKORD2 fastlib/CKORD1 fastlib/CKORD2

IMPCCOPT-4323

NAME

IMPCCOPT-4323

SUMMARY

Default OR2 family exemplar %s has all members marked dont_use. It could be that all the OR2 cells defined in the logic_cells property are set dont_use. Check the dont_use settings for OR gates within your libraries.

DESCRIPTION

For example:

To get a list of all cells marked dont_use: reportDontUseCells

To disable a dont_use on a library cell: setDontUse <cell-name> false

IMPCCOPT-4324

NAME

IMPCCOPT-4324

SUMMARY

No default Nor cell family identified.

DESCRIPTION

This message occurs because there is no NOR cell available for clock tree synthesis. Please make sure the NOR cells you have specified in the logic_cells property are available in the current Innovus session.

For example, the follow example returns the library cells with prefix 'CKNOR':

innovus> get_lib_cells CKNOR*

slowlib/CKNORD1 slowlib/CKNORD2 fastlib/CKNORD1 fastlib/CKNORD2

IMPCCOPT-4325

NAME

IMPCCOPT-4325

SUMMARY

Default NOR2 family exemplar %s has all members marked dont_use. It could be that all the NOR2 cells defined in the logic_cells property are set dont_use. Check the dont_use settings for NOR gates within your libraries.

DESCRIPTION

For example:

To get a list of all cells marked dont_use: reportDontUseCells

To disable a dont_use on a library cell: setDontUse <cell-name> false

IMPCCOPT-4327

NAME

IMPCCOPT-4327

SUMMARY

Cannot find a smallest inverter. It could be that there are no inverters defined in the libraries or all inverters are set as dont_use. Ensure that all required libraries have been loaded and check the dont_use settings for inverter cells.

DESCRIPTION

For example:

To get a list of all cells marked dont_use: reportDontUseCells

To disable a dont_use on a library cell: setDontUse <cell-name> false

IMPCCOPT-4338

NAME

IMPCCOPT-4338

SUMMARY

There are %u clock paths leading to %s. This may cause long CCOpt runtimes.

DESCRIPTION

The design contains a lot of converging clock paths leading to some sinks. This may cause long CCOpt runtimes. The sinks with the most paths leading to them can be found with report_ccopt_clock_tree_convergence. See CCOpt Clock Tree Specification under Clock Concurrent Optimization in the User Guide for more information.

IMPCCOPT-4339

NAME

IMPCCOPT-4339

SUMMARY

CCOpt is unable to time a clock gating check on term %s. In most cases, this will not prevent optimization but it could result in an incorrect worst chain report.

DESCRIPTION

If you see this message during optimization, in most cases, optimization will proceed correctly. If you find the specified gate has not been pushed low enough in the clock tree, you need to add a negative pin insertion delay to the pin in order to push it lower.

If you see this message just before a worst chain report, be aware that the chain reported may not be the worst chain in the design. The reported chain will be wrong when the gate with the clock gating check is the most critical next or previous path in the chain. In this case, the worst chain will report a different next or previous path.

IMPCCOPT-4346

NAME

IMPCCOPT-4346

SUMMARY

Failed to restore clock tree %s which had source %s.

DESCRIPTION

If any clock tree is modified by ECO commands then CCOpt will save its internal state. Any subsequent CCOpt command will prompt a restore from this saved internal state. In some cases CCOpt cannot restore a clock tree. For example, this can occur if the source pin for the clock tree has been deleted by an ECO command.

IMPCCOPT-4347

NAME

IMPCCOPT-4347

SUMMARY

Failed to restore clock spine %s.

DESCRIPTION

If any clock tree is modified by ECO commands then CCOpt will save its internal state. Any subsequent CCOpt command will prompt a restore from this saved internal state. In some cases CCOpt cannot restore a clock spine. For example, this can occur if CCOpt could not restore any of the clock trees in the design after running ECO commands.

IMPCCOPT-4348

NAME

IMPCCOPT-4348

SUMMARY

Failed to restore flexible H-tree %s.

DESCRIPTION

If any clock tree is modified by ECO commands then CCOpt will save its internal state. Any

subsequent CCOpt command will prompt a restore from this saved internal state. In some cases CCOpt cannot restore a flexible H-tree. For example, this can occur if the pin where the H-tree was created has been deleted by an ECO command.

IMPCCOPT-4349

NAME

IMPCCOPT-4349

SUMMARY

Failed to restore clock tree source group %s.

DESCRIPTION

If any clock tree is modified by ECO commands then CCOpt will save its internal state. Any subsequent CCOpt command will prompt a restore from this saved internal state. In some cases CCOpt cannot restore a clock tree source group. For example, this can occur if CCOpt could not restore some of the clock trees in the source group.

IMPCCOPT-4350

NAME

IMPCCOPT-4350

SUMMARY

Failed to restore skew group %s which had source(s) %s.

DESCRIPTION

If any clock tree is modified by ECO commands then CCOpt will save its internal state. Any subsequent CCOpt command will prompt a restore from this saved internal state. In some cases

CCOpt cannot restore a skew group. For example, this can occur if a source pin for the skew group has been deleted by an ECO command.

IMPCCOPT-4352

NAME

IMPCCOPT-4352

SUMMARY

Cannot resolve any source(s) '%s' for auto_sinks skew group '%s'.

DESCRIPTION

CCOpt cannot automatically add sinks to a skew group when it has no resolved source pin(s). Check that the defined source(s) for this skew group are output pins.

IMPCCOPT-4353

NAME

IMPCCOPT-4353

SUMMARY

Created a new clock tree %s with source %s after failing to restore a generated clock tree with this source.

DESCRIPTION

In some cases CCOpt cannot recreate a generated clock tree when restoring from state saved before a change to the clock trees. For example, this can occur if the generator input pins are not sinks in a parent clock tree. CCOpt has created a new non-generated clock tree with the same source and name as the old generated clock tree. Any skew groups which have this source pin as a

source will become constraining skew groups (i.e. the constrains property for these skew groups will no longer be 'none').

IMPCCOPT-4355

NAME

IMPCCOPT-4355

SUMMARY

Restoring from CCOpt config file '%s' produced %zu error(s). The following command(s) failed: %s

DESCRIPTION

Restoring from a CCOpt config file produced one or more errors. This can happen if the file contains references to insts or pins which no longer exist in the DB, or if the config was saved using a different version of the software. To avoid this warning save the design again: the new CCOpt config will be up-to-date and should load without errors.

IMPCCOPT-4356

NAME

IMPCCOPT-4356

SUMMARY

Found unexpected period value %f for clock %s in analysis view %s.

DESCRIPTION

CCOpt will automatically set the clock_period property when creating clock trees. The clock period values are extracted from the loaded constraint files. Period values that are not greater than zero are not supported by CCOpt, and will be ignored. To avoid this warning update the -period setting

for this clock in your SDC file.

IMPCCOPT-4360

NAME

IMPCCOPT-4360

SUMMARY

Found preserved output port(s) on hierarchical net %s which has Verilog assign(s).

DESCRIPTION

Preserved output hterms which are assigned to input hterms may prevent CCOpt from buffering the hierarchical net connecting the hterms. CCOpt will attempt to add a new hterm to allow for buffering fanout which was connected via a hierarchical net with Verilog assigns. To disable this behavior set the CCOpt property add_new_ports_to_avoid_buffering_nets_with_assigns to be false, and restart your run.

IMPCCOPT-4362

NAME

IMPCCOPT-4362

SUMMARY

Failed to restore preferred cell stripes %s.

DESCRIPTION

If any clock tree is modified by ECO commands then CCOpt will save its internal state. Any subsequent CCOpt command will prompt a restore from this saved internal state. In this case a preferred cell stripes instance has failed to be restored; this may have happened because it is

referencing one or more cell declarations which are no longer available.

IMPCCOPT-4375

NAME

IMPCCOPT-4375

SUMMARY

Term %s (connected to net %s) %s so cannot be used by CCOpt

DESCRIPTION

A term cannot be used by CCOpt because it is either an internal term, a power term, a ground term or it has no direction.

CCOpt cannot understand terms without a direction.

CCOpt cannot query or optimize power or ground terms.

Verify the design data for the term is correct.

IMPCCOPT-4379

NAME

IMPCCOPT-4379

SUMMARY

Ignoring command which refers to deleted power domain %s (command was '%s').

DESCRIPTION

If any clock tree is modified by ECO commands or if a new power intent is committed then CCOpt

will save its internal state. Any subsequent CCOpt command will prompt a restore from this saved internal state. In this case a property setting cannot be restored because it refers to a power domain that no longer exists. Check your CCOpt configuration for this property.

IMPCCOPT-4383

NAME

IMPCCOPT-4383

SUMMARY

Treating %s port %s as having effective direction %s.

DESCRIPTION

CCOpt is treating a port as having a different direction than is specified in the netlist. CCOpt has calculated this effective direction based on how the port is connected in the netlist. This warning can occur if the Verilog port direction is not correct for the way the signal is being used (e.g. an input port driven by an output inst term which is inside the hinst). Update the Verilog definition for this port, or change the port connections to avoid this warning.

IMPCCOPT-4386

NAME

IMPCCOPT-4386

SUMMARY

Encountered clock node input pin %s that is in clock tree %s but is shared with generated clock tree %s. The clock tree below pin %s will be excluded.

DESCRIPTION

CCOpt is creating a generated clock tree on the output pin of a multi-output instance, where there also exists a clock node associated with a different output pin of the instance. The latter will have been specified via property trace_through_to. CCOpt is unable to satisfy both of these configurations, so will respect the generated clock tree creation by excluding the clock tree below the existing extract_through_to output pin. If the excluded portion of the tree is to be retained, an additional generated clock tree will need to be created with a source of that output pin.

IMPCCOPT-4388

NAME

IMPCCOPT-4388

SUMMARY

The pin %s is a non-sink pin in a clock tree. You will need to delete the clock tree before setting this property will have any effect.

DESCRIPTION

Properties sink_type and insertion_delay affect how the clock trees are traced through the nelist. For this reason, attempting to set such a property on a non-sink pin in a clock tree is an error.

It is generally recommended to apply sink_type and insertion_delay settings to non-sink pins before creating the clock spec.

However, to make such a setting on a given pin after a spec has been created: first delete the affected clock trees; next apply the setting; and lastly re-create the deleted clock trees. Note that as a consequence of the setting, the re-created clock trees will treat the given pin a clock sink, and will no longer trace past it.

IMPCCOPT-5026

NAME

IMPCCOPT-5026

SUMMARY

The obstruction grid has %ld cells. This is too large to consider blockages and LEF obstructions. Current limit is %d.

DESCRIPTION

The obstruction is too large. Blockages and LEF obstructions are ignored for routing. You can consider blockages and LEF obstructions by increasing the value of the property routing_max_num_obstruction_grid_cells.

IMPCCOPT-5037

NAME

IMPCCOPT-5037

SUMMARY

Found %d pre-routed clock net(s). Pre-routed clock nets are treated as dont_touch and their routing geometry will be preserved.

DESCRIPTION

Found pre-routed clock net(s). Pre-routed clock nets are treated as dont_touch and their routing geometry will be preserved.

IMPCCOPT-5046

NAME

IMPCCOPT-5046

SUMMARY

Net '%s' in clock tree '%s' has existing routing that will be removed by CCOpt.

DESCRIPTION

By default, CCOpt will remove any pre-routing on clock tree nets. To preserve this routing (and treat the net as dont_touch) change its routing status to FIXED and set the 'skip_routing' attribute on the net.

IMPCCOPT-5047

NAME

IMPCCOPT-5047

SUMMARY

Found %d clock net(s) with existing routing that will be removed by CCOpt.

DESCRIPTION

Found clock net(s) with existing routing that will be removed by CCOpt. To preserve this routing (and treat the net as dont_touch) consider changing its routing status to FIXED or setting the 'skip_routing' attribute.

IMPCK-29

NAME

IMPCK-29

SUMMARY

The -routeNonDefaultRule parameter in the setCTSMode command contains an invalid rule name %s.

DESCRIPTION

Please specify a valid rule name. A valid rule name is either the name of a NONDEFAULTRULE statement specified in a previouly-loaded LEF/DEF file, or the name of a non-default rule created by command "add_ndr".

IMPCK-157

NAME

IMPCK-157

SUMMARY

Cell %s is set as dont_touch in the timing libraries. May have to use 'set_dont_touch [get_lib_cells %s] false' in order to delete the buffers in clock tree.

DESCRIPTION

deleteClockTree does not delete the buffer whose dont_touch attribute is set.

But clockDesign will ignore the dont_touch attribute of buffers and inverters.

For details of deleteClockTree and clockDesign usage, see documents.

IMPCK-209

NAME

IMPCK-209

SUMMARY

Clock %s has been synthesized. Type 'man ENCCK-209' to see extended message about this warning.

DESCRIPTION

This message indicates Clock Tree Synthesis (CTS) thinks this clock tree has already been built and, therefore, will not run. The reason it thinks clock has been synthesized is explained in one of the messages that precede it. For example, if a clock buffer or excluded cell is found on the clock net while tracing it, it will issue an ENCCK-766 or ENCCK-767 message and stop. In order to run CTS you must delete the existing clock tree first.
When running clockDesign it will automatically call deleteClockTree at beginning to remove buffers on the clock. However deleteClockTree cannot remove fixed instances. You should run following command to unfix existing buffers on the clock so deleteClockTree can remove them:
changeClockStatus -clk clockName -noFixedNetWires -noFixedBuffers
This will set status to Placed for all buffers and wires in the specified clock tree. You can use the -all option in place of -clk <clockName> to perform this operation on all clocks defined in the CTS specification file. Once you change the status to Placed, deleteClockTree will be able to remove all existing buffers in the clock tree.

IMPCK-361

NAME

IMPCK-361

SUMMARY

The parameter '-localSkew' is not supported in Multi-Corner CTS. To run ckECO -localSkew on a single corner, specify the same analysis view for both setup and hold. For example, if the desired analysis view is func_worst, then do "set_analysis_view -setup func_worst -hold func_worst" and reload the clock spec file.

DESCRIPTION

The above error is generated in Innovus when trying to run command "ckECO -localSkew" in MMMC mode.

What is the recommended way to run "ckECO -localSkew" in MMMC mode?

By default, CTS attempts to optimize across all active setup and hold views.

The -localSkew parameter of ckECO does not support this, and hence the above error is generated.

The workaround is to run "ckECO -localSkew" for a single setup view. Select the setup view which you want to target and specify this view for both setup and hold.

Example:

set_analysis_view -setup setup_func -hold setup_func

IMPCK-657

NAME

IMPCK-657

SUMMARY

No cell is specified for clock %s in the clock tree specification file. What CTS is complaining about is the lack of a line specifying which buffers and/or inverters may be used for building the clock tree. THAT'S the cell that is 'not specified'. If you add a line specifying which buffers from your technology library CTS is allowed to use, CTS will run correctly.

DESCRIPTION

Why does tool report above error message on running clock tree synthesis?

User has defined a root pin as follows in his clock tree specification file:

AutoCTSRootPin ck

Period \10ns

MaxDelay 0.01ns #sdc driven default

MinDelay 0ns #sdc driven default

MaxSkew \400ps #sdc driven default

SinkMaxTran \200ps #sdc driven default

BufMaxTran \200ps #sdc driven default

END

What CTS is complaining about is the lack of a line specifying which buffers and/or inverters may be used for building the clock tree. THAT'S the cell that is 'not specified'. If you add a line specifying which buffers from your technology library CTS is allowed to use, CTS will run correctly:

Current example:

AutoCTSRootPin ck

Period \10ns

MaxDelay 0.01ns # sdc driven default

MinDelay 0ns # sdc driven default

MaxSkew \400ps # sdc driven default

SinkMaxTran \200ps # sdc driven default

BufMaxTran \200ps # sdc driven default

Following line was added

Buffer CLKBUFX1 CLKBUFX12 CLKINVX1 CLKINVX12

END

IMPCK-661

NAME

IMPCK-661

SUMMARY

Clock %s has multiple definitions in the clock tree specification file.

DESCRIPTION

This warning is issued when there are multiple definitions of the clock in the database. This typically occurs when you run specifyClockTree multiple times without running cleanupSpecifyClockTree first. Before running specifyClockTree run cleanupSpecifyClockTree to clear any CTS specification currently in the database. Then run specifyClockTree. Note, if you are running "clockDesign -spefFile specFileName", it automatically runs cleanupSpecifyClockTree before specifyClockTree.
The other cause of this message is if you have multiple autoCTSRootPin definitions for the same clock inside your CTS constraints file. If this is the case, remove the multiple definitions.

IMPCK-766

NAME

IMPCK-766

SUMMARY

Find excluded cell %s in the clock tree.

DESCRIPTION

This message indicates an excluded cell was found downstream of from the clock root you are trying to synthesize. Therefore, Clock Tree Synthesis (CTS) will not run. Avoid this warning by deleting the clock tree prior to CTS using the deleteClockTree command. clockDesign automatically runs deleteClockTree before tracing the clock but deleteClockTree cannot remove fixed instances. Therefore, you should run the following to unfix the clock tree so deleteClockTree can remove the existing buffers in the tree:
changeClockStatus -clk clockName -noFixedNetWires -noFixedBuffers
This will set the placement status to Placed for all buffers and wires in the specified clock tree. You can use the -all option in place of -clk clockName to perform this on all clocks defined in the CTS specification file. Once you set the status to Placed, deleteBufferTree will be able to remove these existing buffers in the tree.

IMPCK-767

NAME

IMPCK-767

SUMMARY

Find clock buffer %s in the clock tree.

DESCRIPTION

This message indicates a clock tree buffer was found downstream from the clock

root you are trying to synthesize. Therefore, Clock Tree Synthesis (CTS) will not run. Avoid this warning by deleting the clock tree prior to CTS using the deleteClockTree command. clockDesign automatically runs deleteClockTree before tracing the clock but deleteClockTree cannot remove fixed instances. Therefore, you should run the following to unfix the clock tree so deleteClockTree can remove the existing buffers in the tree:
changeClockStatus -clk clockName -noFixedNetWires -noFixedBuffers
This will set the placement status to Placed for all buffers and wires in the specified clock tree. You can use the -all option in place of -clk clockName to perform this on all clocks defined in the CTS specification file. Once you set the status to Placed, deleteBufferTree will be able to remove these existing buffers in the tree.
Alternatively, if you prefer to preserve portions of the clock tree and synthesize the rest you can use PreservePin. PreservePin preserves the netlist for the pin and pins below the pin in the clock tree. However, CTS considers any synchronized pins after the pin when computing skew. For example:
PreservePin
+ CLK__L1_I0/A

IMPCK-6001

NAME

IMPCK-6001

SUMMARY

Clock %s has a maximum of %d levels of logic before synthesis. Sample path: %s

DESCRIPTION

This will make ckSynthesis difficult to balance all sinks and achieve reasonable skew.

Please check those deeply gated clock paths to see if any tracing directive (for example, LeafPin, ExcludedPin, SetDPinAsSync NO) is necessary, but missed from clock spec file.

IMPCK-6336

NAME

IMPCK-6336

SUMMARY

Clock %s contains equivalent gates that have bounding boxes of their downstream leaf pins overlapped. This is most probably caused by cloning without adequate placement information. Use one clock gate to drive all leaf pins, or, division of leaf pins based on physical locations between clock gates may help improve this situation.

DESCRIPTION

This warning is part of the new CTS diagnostic feature which is designed to highlight potential issues or inefficiencies in the clock setup.

It is issued by clock gating instance location check at pre-synthesis stage.

The message means that two (or more) cloned gates are driving registers in a common area where the bounding boxes of downstream sinks overlap each other physically. This can lead to poor QoR.

A possible reason for that is previous clock gate cloning was not done properly, therefore they could be good candidates for decloning/cloning by performing ckDecloneGate followed by ckCloneGate on suggested gating instances.

Either one gate could drive all the registers here or the division of the registers between the clock gates could be done better.

IMPCPF-190

NAME

IMPCPF-190

SUMMARY

INFO: CPF file %s is hierarchical; Flattening hierarchical CPF file, the logfile is %s/flattencpf.log ...

DESCRIPTION

The CPF file is hierarchical CPF format, will be flattened via CLP integrator by read_power_intent when 'setMsvMode -supportHierCPF false'

Example:

Before hierarchical CPF native support, Innovus needs to flatten it via CLP

integrator and load the flattened CPF file.

With beta-quality hierarchical CPF native support feature 'setMsvMode

-supportHierCPF true', Innovus can load this CPF without flattening

IMPCPF-201

NAME

IMPCPF-201

SUMMARY

error parsing CPF file %s.

DESCRIPTION

This error is a general message issued when the parsing of CPF fails.

This is typically due to syntax errors in the CPF. When you receive this message, review the log file for warning and error messages which precede the IMPCPF-201 message. You should see messages which report the specific lines in CPF which Innovus System is complaining about.
Correct the CPF and then try loading it in again. See the Common Power Format Language Reference for CPF syntax and examples.

IMPCPF-209

NAME

IMPCPF-209

SUMMARY

line %s: %s %s not defined.

DESCRIPTION

This error message happens when a CPF object is used without defining or fails to define it. Check the CPF file for the definition/creating of the object. And also look for any error/warn messages prior to this error.
For example, if 'create_power_domain' command errors out due to some reason, the later 'update_power_domain' will give this error because the power domain it tries to update is not defined. Please also pay attention to the command order in the CPF file. If some object is defined after it's used, tool will also give this error message.
Example:

**ERROR: (IMPCPF-209): line 453: power_domain PD_off is not defined.

**ERROR: (IMPCPF-209): line 735: power_mode PMdvfs2 is not defined

**ERROR: (IMPCPF-209): line 740: global net VDDw is not defined

IMPCPF-235

NAME

IMPCPF-235

SUMMARY

domain '%s' not specified in the -domain_conditions list in default power_mode%s.

DESCRIPTION

The message is reported when a power domain (Example: PD_C2) is given in the domain conditions but the power domain is not defined by create_power_domain,means there is no power domain PD_c2.

Example:

In the given example only PD_C1 is defined but there is no PD_C2. The below sequence issue the message.

create_power_domain -name PD_C1

create_power_mode -name M1 -default -domain_conditions {PD_C1@off PD_C2@on}

IMPCPF-237

NAME

IMPCPF-237

SUMMARY

library set not specified for nominal condition %s in default power_mode %s.Please use CPF

update_nominal_condition -library_set to specify its library set.

DESCRIPTION

Encounter 13.1 release onwards, tool issues above error message if library sets are not defined in CPF. The library sets can be defined either using viewdefinition.tcl file or using define_library_set command in CPF. The library sets defined in CPF can be further associated to nominal condition as shown below:
create_nominal_condition -name off -voltage 0 -ground_voltage 0.0 -state_off
update_nominal_condition -name off -library_set <lib set name >
But, if the library sets are not defined in CPF, then CPF will issue above error message while executing create_power_mode command:
create_power_mode -name cpu_off -domain_conditions {pd_1@off pd_2@on}
To resolve this error message and use the library sets defined with viewdefinition.tcl, please set below variable before read_power_intent:
setMsvMode -useViewDefLibSet true
This makes CPF to recognize the libray sets defined in viewdefinition.tcl and do not require update_nominal_condition command in CPF to have library sets defined.

IMPCPF-238

NAME

IMPCPF-238

SUMMARY

lLibrary file %s of library_set %s used in the CPF file is not loaded from viewDefinition file. It's caused by inconsistent library_set definition in CPF and viewDefinition file.

DESCRIPTION

Library set in the CPF file needs to contain the same library files as in the viewDefinition file.

This message is reported when CPF file loads a library file that is not loaded into Innovus

by viewDefinition file during design initialization.

To solve it, check the library set definitions in CPF and viewDefinition files and

make sure them consistent.

A good practice is to define library file paths in a separate file and use variable

in CPF and viewDefinition file so that they will always be consistent.

IMPCPF-239

NAME

IMPCPF-239

SUMMARY

The default power mode is not defined. Please check if CPF has create_power_mode with -default option.

DESCRIPTION

CPF needs a default power mode. Please define a CPF power mode as a default by

create_power_mode -default.

Example:

**ERROR: (IMPCPF-239): The default power mode is not defined.

IMPCPF-243

NAME

IMPCPF-243

SUMMARY

Cannot bind power domain %s to a library_set.

DESCRIPTION

Power domain library binding is through either MMMC file(viewDefinition.tcl) or CPF power mode and nominal condition as follows:

a. viewDefinition.tcl: update_delay_corner -name dc1 -power_domain PD1 -library_set libSet1

b. CPF: create_power_mode -name PM1 -default -domain_conditions{PD_FOOBAR@1.08v} where nominal condition 1.08v is associated to a lib by update_nominal_condition -name nc1 -library_set libSet1

IMPCPF-246

NAME

IMPCPF-246

SUMMARY

Must specify sdc_files for power_mode %s to be used in analysis_view %s. Use 'update_power_mode -sdc_files' in the CPF file to specify.

DESCRIPTION

In the CPF file, power mode used in 'create_analysis_view' command must have

SDC file specified. Because commit_power_intent will convert the power mode into

constraint mode and it needs to know the SDC file. To specify, use the
update_power_mode command.
Example:
create_power_mode -name PM_HL_FUNC -domain_conditions \\
{AO@high_ao PLL@high_pll TDSPCore@low_tdsp TDSPCore_R@low_tdsp}
update_power_mode -name PM_HL_FUNC -sdc_files \\
dtmf_recvr_core_gate_wc.sdc
Example:

**ERROR: (IMPCPF-246): Must specify sdc_files for power_mode PM_LO_FUNC to be used in analysis_view AV_LO_FUNC_MAX_RC1. Use 'update_power_mode -sdc_files' in the CPF file to specify.

IMPCPF-247

NAME

IMPCPF-247

SUMMARY

The operating_corner %s %s not specified; the default value %g is used.

DESCRIPTION

The message is issued when operating corner is not defined in CPF.
Example:
Add below command to CPF to avoid this warning
create_operating_corner -name qc_max_corner -process 3 -temperature 125
-voltage 0.99 -library_set max_timing

IMPCPF-249

NAME

IMPCPF-249

SUMMARY

The CPF file is incomplete.

DESCRIPTION

The CPF file is missing the definition of some key objects. Usually the error message shows up along with some other error messages. Check those error and fix them before loading the CPF.

Example:

Checking CPF file ...

**ERROR: (IMPCPF-243): Cannot bind power domain VDD1 to a library_set.

**ERROR: (IMPCPF-243): Cannot bind power domain VDD2 to a library_set.

**ERROR: (IMPCPF-243): Cannot bind power domain VDD to a library_set.

**ERROR: (IMPCPF-239): The default power mode not defined.

**ERROR: (IMPCPF-249): The CPF file is incomplete

IMPCPF-251

NAME

IMPCPF-251

SUMMARY

line %s: create_isolation_rule -name %s: Can not find an isolation cell with a valid location domain %s and with the isolation output state %s. The possible reasons are: 1) the specified location in update_isolation_rule is different from the location in define_isolation_cell, or 2) the output state for the valid isolation cell does not match to its output state specified in create_isolation_rule.

DESCRIPTION

The message shows that Innovus cannot insert an isolation cell with a valid

location and with required isolation_output state. The reasons could be:

1. The rule-specified location is different from the valid location

specified in define_isolation_cell. For example:

define_isolation_cell -cells isoandlow_f2_pm -valid_location on

create_isolation_rule -name VDD2LSW1_iso_low_from \\

-from PD_VDD2LSW1

update_isolation_rules -names VDD2LSW1_iso_low_from \\

-location from -cells {isoandlow_f*_pm}

The rule specifies "-location from" (PD_VDD2LSW1 is a switchable power

domain) and "-cells isoandlow_f*_pm". But all the isolation cells

isoandlow_f*_pm are specified as "-valid_location on" which means the

isolation cells are to be placed in an unswitched domain.

Therefore these isoandlow_f*_pm cells do not fit this rule.

If the rule specifies "-location to" in this case, then these cells

would fit the rule.

2. No valid cell can match the rule's output state requirement when

the isolation_condition is asserted. For example,

create_isolation_rule -name iso_low -isolation_output low

update_isolation_rules -names iso_low -cells {isonandhigh*_pm}

There are no isolation cells matching the name isonandhigh*_pm with

isolation_output low. Therefore the message of CPF-251 is issued.

Verify the cell name and confirm a cell exists which matches the cell

specified and also matches the required isolation_output state.

IMPCPF-253

NAME

IMPCPF-253

SUMMARY

line %s: create_isolation_rule -name %s can not insert an inverter in power domain %s to generate the inverted isolation enable signal %s. Most likely, the net is set to 'dont_touch' or the inverter is not bound to this domain. Please remove the 'dont_touch' constraint or correct the power domain library binding.

DESCRIPTION

This error message was seen either because the net has dont_touch attribute or

the inverter is not available. For the unavailable inverter reason, starting

from Encounter 14.1, we recommend users to use viewDefinition.tcl to do the domain

binding in a specific domain. check if the specific domain's library binding

has the available inverter.

IMPCPF-289

NAME

IMPCPF-289

SUMMARY

library file %s in library set %s is not loaded, it will be skipped in determining temperature or process of operating corner %s.

DESCRIPTION

The message is issued when the library set is not loaded properly. Check viewdefinition.tcl and correct the library set

IMPCPF-310

NAME

IMPCPF-310

SUMMARY

line %s: create_isolation_rule -name %s: location domain %s does not have hinst to insert isolation in the location domain. check if the option in update_isolation_rules is specified correctly.

DESCRIPTION

commit_power_intent will insert the isolation cell based on the isolation rule.

If a rule tells the tool to insert the isolation in a particular domain,

the users need to make sure that this particular domain has a hierarchical instance

for the isolation to be inserted logically.

IMPCPF-311

NAME

IMPCPF-311

SUMMARY

line %s: create_level_shifter_rule -name %s: location domain %s does not have hinst to insert level_shifter in the location domain.check if the location option in update_level_shifter_rules is specified correctly.

DESCRIPTION

commit_power_intent will insert the level shifter cell based on the level shifter rule.

If a rule tells the tool to insert the level shifter in a particular domain,

the users need to make sure that this particular domain has a hierarchical instance

for the level shifter to be inserted logically

IMPCPF-312

NAME

IMPCPF-312

SUMMARY

line %s: create_%s_rule -name %s: valid %s cells (%s) are not bound to location domain %s; or the library defining those cells are not loaded while executing init_design. Please check this domain library binding.

DESCRIPTION

This is caused by library which defining those cells are not loaded or binding to domain.

you need to check domain's library binding in view_definition.tcl file.

In view_definition.tcl file, we use command "update_delay_corner -power_domain -library_set"

to specify domain's library.

Example:

In view_definition.tcl:

Only have : "create_delay_corner -name -library_set -rc_corner"

No "update_delay_corner -power_domain -library_set"

There are two solutions:

1. You need to modify this mmmc file by adding "update_delay_corner

-power_domain -library_set" to specify the domain's library binding.

or

2. In foundation flow,do NOT specify the mmmc file and let CPF to set up the

MMMC. in the file FF/init.tcl,specify the init_mmmc_file to an empty string "".

then commit_power_intent will setup the MMMC based on the CPF spec and the domain library binding.

IMPCPF-350

NAME

IMPCPF-350

SUMMARY

Found undefined variable while restoring CPF db, this might be a problem if CPF content is used by certain commands.

DESCRIPTION

The design might be moved from other location which depends on some user defined variables to complete its content. Problem might arise if users run some commands that will use CPF data in the design, such as runCLP. In that case, users need to define those variables that are referenced by this design,and start over. This message will only be reported once, but there may be more than one undefined varaiable.

Example:

set cpf_isolation_rules

set cpf_level_shifter_rules

set cpf_pd_boundary_ports($name) cpf_pd_boundary_ports(load)

IMPCPF-390

NAME

IMPCPF-390

SUMMARY

define_always_on_cell: same %s and %s pins of always_on cell %s

DESCRIPTION

This error is due to wrong pin definition in CPF define_always_on. The options -power_switchalbe and -power (-ground_switchable and -ground) in this command should not have the same pin name if it is power switchable (ground_switchable) always on cell as follows:

define_always_on_cell -cells { AlwaysOnCell } -power_switchable VDD -power VDD -ground VSS

Please check the .lib for the correct pin names for -power_switchable and-power.

IMPCPF-402

NAME

IMPCPF-402

SUMMARY

Cannot find any matching instance for domain %s -instances name %s.

DESCRIPTION

Innovus issue warning during commit_power_intent when the instance provided in the CPF for a

powerdomain is not present in the netlist.

Example:

Assume "DTMF/WAON/ping_mod/inst1" instance is not present in the netlist,

but is provided in the CPF, Innovus will issue this warning during commit_power_intent.

create_power_domain -name PD_AON -instances {DTMF/WAON/ping_mod/inst1}

IMPCPF-403

NAME

IMPCPF-403

SUMMARY

Cannot find any matching port for domain %s -boundary_ports name %s defined in create_power_domain -boundary_ports. Check if this boundary port exists in the netlist.

DESCRIPTION

Sometimes, users use create_power_domain -boundary_ports <listOfports> to

define the boundary ports' power domain. Users need to make sure the specified

list of ports exist in the netlist. Otherwise, commit_power_intent will issue the above

Error when it can not find the port.

IMPCPF-701

NAME

IMPCPF-701

SUMMARY

%s inst %s(cell %s) is not in the valid_location '%s', any 2nd P/G pin will not be connected.

DESCRIPTION

This message is issued when an iso/shifter instance is found at invalid location.

Such issue might result in no P/G connection of 2nd P/G pin of the cell.

An iso/shifter cell can be limited to be inserted in the power domain of signal's

source or sink, if not inserted correctly, its 2nd P/G pins can not be correctly connected.

IMPCPF-980

NAME

IMPCPF-980

SUMMARY

Power domain %s is not bound to any library. Power domain library binding is through 'update_delay_corner -power_domain' in the MMMC file viewDefinition.tcl. Please make sure that 'update_delay_corner -power_domain %s' is specified for each delay corner in the MMMC file.

DESCRIPTION

The WARN happens when CPF does not contain MMMC definition and power domain is not bound to

library through 'update_delay_corner -power_domain' in MMMC file viewDefinition.tcl.

User need to check the sanity of viewDefinition.tcl file and fix the problem by adding

'update_delay_corner -power_domain %s'.

The WARN on non-virtual power domain is critical for whole flow.

Example

**WARN: (IMPCPF-980): Power domain PD3 is not bound to any library. Power domain library

binding is through 'update_delay_corner -power_domain' in the MMMC file viewDefinition.tcl.

Please make sure that 'update_delay_corner -power_domain PD3' is specified for each delay corner in the MMMC file.

IMPCPF-2011

NAME

IMPCPF-2011

SUMMARY

The switchable power domain %s shutoff condition is not specified in CPF.

DESCRIPTION

When dumping out cpf file using command saveCPF or write_power_intent, there is no "-shutoff_condition" saved out for switchable power domain.
The case may be non-standard msv flow case, for example, the power domain in the DB are defined but did not follow the "standard" msv flow which uses CPF.
This case need to be converted to CPF case in order for it to be officially supported.
For example, the case is 1801 based case. After "saveCPF top.cpf" after init design:
<CMD> saveCPF top.cpf
**WARN: (IMPCPF-2011): The switchable power domain PD2 shutoff condition is not specified.
**INFO: constraint mode func_mode is specified in multiple analysis view, the nominal condition for analysis view setup_func_m40 is used to create corresponding power mode.

IMPCPF-2204

NAME

IMPCPF-2204

SUMMARY

Cannot get the primary power net for the power domain %s, using first power net %s specified in connections as primary power net.

DESCRIPTION

This warning message comes when CPF does not define the primary power net for the %s domain.

Example:

Something similar to the following needs to be added:

update_power_mode -name PM1 -primary_power_net VDD1

IMPCPF-2210

NAME

IMPCPF-2210

SUMMARY

The partition CPF %s references the toplevel SDC files. Modify the partition CPF to reference the correct SDC files if necessary.

DESCRIPTION

The message is reported when the SDC's in CPF are not point to correct SDC

Example:

Correct SDC path of below command in the CPF

update_power_mode -name PD1 -sdc_files ${libDir}/cpf/Block1.sdc

IMPCPF-2303

NAME

IMPCPF-2303

SUMMARY

Using CPF is required to save the database. Please use "write_power_intent -cpf <filName>.cpf; read_power_intent -cpf <fileName>.cpf; commit_power_intent" to saveDesign again.For more information about CPF information or a backward compatibility mode, refer to the documentation.

DESCRIPTION

This message is issued when the design has power domains, but CPF or IEEE1801 or LP DB is not loaded. Please confirm the power domains are defined through CPF or IEEE1801 file.

IMPCPF-2500

NAME

IMPCPF-2500

SUMMARY

Cannot support disjoint power domain with leaf instance(s)

DESCRIPTION

This message is reported while creating disjoint power domain with option -disjointHInstBoxList of a PD which have a leaf instance given in CPF for"create_power_domain -instance <Hier_Instt Leaf_Inst>" along with Hier instance which is not a support model .Explicitly Hier instance should be part of create_power_domain PD -instances'of CPF file to create disjoint PD. Correct your CPF by providing only Hier instances and avoid leaf instances in the CPF.

Example:

modifyPowerDomainAttr PD -disjointHInstBoxList {

{A {ax0 ay0 ax1 ay1 ax2 ay2 ax3 ay3}}

{{B C} {bx0 by0 bx1 by1 bx2 by2 bx3 by3}} }

modifyPowerDomainAttr PD -addBlockBox {block1}

Note: disjointHInstBoxList: Specify a disjoint region for the hinsts as a pair of hinsts and region.The region is defined as box list.

IMPCPF-2510

NAME

IMPCPF-2510

SUMMARY

The box list specified is not disjoint.

DESCRIPTION

In real designs, an RTL or logical-level power domain may have to be implemented into different physical regions with unconnected local power supplies. Such implementation of a power domain is called a Disjoint Power Domain.

Example:

1. One box

modifyPowerDomainAttr PD1 -disjointBoxList {46 479 319 543}

**ERROR: (IMPCPF-2510): the box list specified is not disjoint

2. Abutted

modifyPowerDomainAttr PD1 -disjointBoxList {46 479 319 543 46 475 263 479}

**ERROR: (IMPCPF-2510): the box list specified is not disjoint

IMPCPF-2602

NAME

IMPCPF-2602

SUMMARY

Loading floorplan after commit_power_intent may cause inconsistency in power domains. The recommended low power flow is to load floorplan before read_power_intent.

DESCRIPTION

This message pops-up when the user tries to load floor-plan file after CPF is

loaded and committed to the design

Example:

In order to avoid this issue, the user shousld load floor-plan file in after design is imported,

then load and commit cpf file.

This will ensure correct power intent information being applied to the design

IMPCTE-104

NAME

IMPCTE-104

SUMMARY

The constraint mode of this inactive view '%s' has been modified and may need to be reanalyzed to ensure proper timing results. To reanalyze timing for this view make the view active using 'set_analysis_view' and run timing analysis.

DESCRIPTION

This warning message appears when 2 or more views are sharing the same constraint mode in the design and also the constraints are changed. For example, In a design, say totally 9 analysis views are created and all these views are sharing the same constraint mode "delay_constraints" and currently 2 views are in active state,Now, when there is a change in the constraint modes in form of some constraint change , tool is trying to make these changes to all of the inactive views. Hence the warning message clearly shows that the constraint mode has been modified and the particular inactive view should be re-analyzed to make proper timing analysis. There won't be any harm on proceeding further on the design steps.

IMPCTE-290

NAME

IMPCTE-290

SUMMARY

Could not locate cell %s in any library for view %s.

DESCRIPTION

This message is issued when cell could not be found in any library of the view. To find the list of libraries associated with the view, use command "report_analysis_views -type active".

IMPCTE-291

NAME

IMPCTE-291

SUMMARY

%s is a physical only instance and is ignored. This indicates that the instance is physical only (e.g. a filler/decap cell) and is in the database, but not in timing graph since physical cells do not have timing information. Verify the instance is a physical only cell to confirm that this warning can be ignored.

DESCRIPTION

This warnning is issued when tool tries to do timing analysis for physical only instance. Please check your lib cell whether has (e.g. is_filler_cell/is_decap_cell/is_tap_cell true) attribute.

IMPCTE-313

NAME

IMPCTE-313

SUMMARY

Paths not in the in2out domain will be added 1000ns slack adjustment.

DESCRIPTION

This warning is issued when path groups are set in input to output mode only.

For all the other paths that are not in the in2out domain, a positive slack of 1000ns is added so that they do not show up as critical paths during analysis.

IMPCTE-314

NAME

IMPCTE-314

SUMMARY

Paths not in the in2reg domain will be added 1000ns slack adjustment.

DESCRIPTION

This warning is issued when path groups are set in input to register mode only.

For all the other paths that are not in the in2reg domain, a positive slack of 1000ns is added so that they do not show up as critical paths during analysis.

IMPCTE-317

NAME

IMPCTE-317

SUMMARY

Paths not in the reg2out domain will be added 1000ns slack adjustment

DESCRIPTION

This warning is issued when path groups are set in register to output mode only.

For all the other paths that are not in the reg2out domain, a positive slack of 1000ns is added so that they do not show up as critical paths during analysis.

IMPCTE-318

NAME

IMPCTE-318

SUMMARY

Paths not in the reg2reg domain will be added 1000ns slack adjustment.

DESCRIPTION

This warning is issued when path groups are set in register to register mode only.

For all the other paths that are not in the reg2reg domain, a positive slack of 1000ns is added so that they do not show up as critical paths during analysis.

IMPCTE-337

NAME

IMPCTE-337

SUMMARY

An unsupported Liberty attribute: max_clock_tree_path - was found on pin %s of cell: %s in library: %s. This attribute is not supported by timing analysis and will be ignored. Type 'man IMPCTE-337' for more detailed information.

DESCRIPTION

Used in timing groups under a clock pin. Defines the maximum clock tree path constraint for a pin driving an internal clock tree for input transition. Please check lib to confirm that this warning can be ignored.

IMPCTE-432

NAME

IMPCTE-432

SUMMARY

Failed to convert the next state function %s of cell %s to BDD.

DESCRIPTION

This warning is issued when the function expression constains an undeclared variable or port. Please check the timing library where the next state function is defined for the cell.

IMPDB-1206

NAME

IMPDB-1206

SUMMARY

Global net name not specified.

DESCRIPTION

This error occured when empty name "" is specified for global net. Need to specify existing net name.

IMPDB-1216

NAME

IMPDB-1216

SUMMARY

The global net '%s' specified in the global net connection(GNC) rule doesn't exist in the design.

DESCRIPTION

This error occurs when power/ground nets are not defined before initializing/loading the design.

To resolve this error, define the power/ground nets before loading the design.

For example, power(VDD) and ground(VSS) nets can be declared as below before initializing the design

set init_pwr_net {VDD}

set init_pwr_net {VSS}

init_design

globalNetConnect VDD -type pgpin -pin VDD

globalNetConnect VSS -type pgpin -pin VSS

CUI equivalent example:

==========

set_db init_power_nets {VDD}

set_db init_ground_nets {VSS}

init_design

connect_global_net VDD -type pg_pin -pin_base_name VDD

connect_global_net VSS -type pg_pin -pin_base_name VSS

IMPDB-1220

NAME

IMPDB-1220

SUMMARY

A global net connection(GNC) rule for connecting pin '%s' of cell '%s' to global net '%s' was specified. The connection cannot be made because the %s pin and the %s net are not of the same polarity. Check the imported design and make sure the GNC rule is correctly specified or generated. If the polarity mismatch is required, use the 'init_ignore_pgpin_polarity_check' variable to ignore the polarity check.

DESCRIPTION

{Some polarity checks need to be ignored, like for back-bias in Silicon-On-Insulator (SOI) technologies. Please refer to the 'init_ignore_pgpin_polarity_check'" variable documentation}

IMPDB-1284

NAME

IMPDB-1284

SUMMARY

Using lower level net '%s' to connect to higher level instance pgTerm in module '%s' is not allowed. The net needs to be in the same level as instance or in the higher level.

DESCRIPTION

{Connect lower level net to higher level instance pg term is not allowed, ex: connect global net A/B/C/net1 to instance A/B/inst1 pg term won't be honored. Fixing the problem by replacing the net with higher level net A/net2}

IMPDB-2148

NAME

IMPDB-2148

SUMMARY

%sterm '%s' of %sinstance '%s' is tied to net '%s'. However, none of the instance's %s terms is connected to the net. Usually an instance's tieHi/Lo term and one of the Power/Ground (P/G) terms of the instance should connect to the same P/G net. Check the input netlist, and also make sure proper global net connections are applied to the instance's tieHi/Lo terms and P/G terms.

DESCRIPTION

Ensure that the global net connectivity for pgpins is defined.

globalNetConnect VDD -type pgpin -pin VDD -all

globalNetConnect VSS -type pgpin -pin VSS -all

Check if 'globalNetConnect' command is run to specify the tie high/low signal nets.

globalNetConnect VSS -type tielo -all

globalNetConnect VDD -type tiehi -all

IMPDB-2504

NAME

IMPDB-2504

SUMMARY

Cell '%s' is instantiated in the Verilog netlist, but it is not defined in the library or design data. Its pin directions may be derived incorrectly. Provide the cell definition or its pin information in the library or design data and reload the design to avoid potential issues.

DESCRIPTION

Check running the command 'check_instance_library_in_views' which checks for missing libraries for instances in the active view.

Check running the command 'check_library' which checks the problematic cells that cause issues.

Make sure if there should not mismatch between .lef and .lib for problematic cell, ex: definition or pin direction.

IMPDB-2532

NAME

IMPDB-2532

SUMMARY

RouteType '%s' already exists.

DESCRIPTION

This error occurs when the route type being created (create_route_type) already exists in the design database. You can query the existing route types using following command:

innovus> dbGet head.routeTypes.name

In Common UI:

innovus> db_db route_types .name

IMPDB-2550

NAME

IMPDB-2550

SUMMARY

VIARULE '%s' referenced in parameterized via '%s' was not found in technology LEF, but was soft-matched to VIARULE '%s' in technology LEF.

DESCRIPTION

Soft-matched means they have different VIARULE name but with the same content. You can ignore the warning to use the soft-matched VIARULE.

IMPDB-5029

NAME

IMPDB-5029

SUMMARY

This message is issued because one %s cannot belong to two groups at the same time. '%s' was already assigned to group '%s', so it cannot be assigned to another group '%s' again.

DESCRIPTION

Single instance cannot be assigned to multiple instance groups. To assign the instance to another group, you need to remove the instance from the current group. Please deleteInstFromInstGroup first and retry addInstToInstGroup.

IMPDB-7003

NAME

IMPDB-7003

SUMMARY

Line '%d' is syntax error, MASKSHIFTPATTERN value must be an number array and element is layer shift value combination, eg: 0000 0001 0010 0011.

DESCRIPTION

Define the MASKSHIFTPATTERN according MASKSHIFTLAYER metal layer sequence, only multi-mask layers need to be defined. 1st bit for 1st metal layer (routing or cut layer), 2nd bit for 2nd metal layer (routing or cut layer), and so on. 00 is required which mean the original mask.

IMPDBTCL-204

NAME

IMPDBTCL-204

SUMMARY

'%s' is not a recognized object/attribute for object type '%s'. For help use 'dbSchema %s' to get list of all supported (settable/unsettable) objects and attributes.

DESCRIPTION

The first field to dbGet must be {<obj>|<objList>|head|top|selected}. Obj or objlist is a pointer or list of pointer of a db object. "head" "top" and "selected" are keyword to the category of different db structure. Head point to the start of library related infomation. top point to start of design information and selected point to the start of selected objects.

Example:

Below command results in warning message IMPDBTCL-204

innovus 1> dbGet top.insts.wires

**WARN: (IMPDBTCL-204): 'wires' is not a recognized object/attribute for object type 'inst'. For help use 'dbSchema inst' to get list of all supported (settable/unsettable) objects and attributes.

"dbSchema inst" will output recognized object/attributes for 'inst' object type. Alternatively, you can also use "dbGet top.insts.<tab in>" or "dbGet top.insts.?" to know the recognized objects.

IMPDBTCL-205

NAME

IMPDBTCL-205

SUMMARY

Unknown or unsupported object pointer detected. See 'help dbGet' for more details.

DESCRIPTION

This can occur when dbGet is given a pointer which has been deleted from the database such as a wire segment, instance or net. You can verify the object pointer by selecting the object and running 'dbGet selected'. The Design Browser can also be used to search for and select the object. Note object pointers are unique to each session so scripts should retrieve the object pointers.

IMPDBTCL-229

NAME

IMPDBTCL-229

SUMMARY

'%s' is not a legal attribute name, you probably have a typo. If it was not intended as an attribute name, you can hide it inside a tcl variable and use the variable instead in the dbget expression. You can use 'dbGet <object>.?h' to get list of all supported objects and attributes.

DESCRIPTION

You may meet unexpected error in dbGet pattern matching if the pattern contains decimal point. For example:

> dbGet top.insts.instTerms.name {U1[0].test/SE}

**ERROR: (IMPDBTCL-229): 'test' is not a legal attribute name, you probably have a typo. If it was not intended as an attribute name, you can hide it inside a tcl variable and use the variable instead in the dbget expression. You can use 'dbGet <object>.?h' to get list of all supported objects and attributes.

0x0

If the decimal point is escaped it works:

> dbGet top.insts.instTerms.name {U1[0]\\.test/SE}

{U1[0].test/SE}

But problems arise again if the result is used in a variable:

> set termName [lindex [dbGet top.insts.instTerms.name {U1[0]\\.test/SE}] 0]

U1[0].test/SE

> puts $termName

U1[0].test/SE

> dbGet -p top.insts.instTerms.name $termName

**ERROR: (IMPDBTCL-229): 'test' is not a legal attribute name, you probably have a typo. If it was not intended as an attribute name, you can hide it inside a tcl variable and use the variable instead in the dbget expression. You can use 'dbGet <object>.?h' to get list of all supported objects and attributes.

0x0

Solution

The solution is to use regsub on $termName to escape the decimal point before using it with dbGet:

> set termName [lindex [dbGet top.insts.instTerms.name {U1[0]\\.test/SE}] 0]

U1[0].test/SE

> puts $termName

U1[0].test/SE

> regsub {\\.} $termName {\\\\.} termName

1

> dbGet -p top.insts.instTerms.name $termName

0x2aaab3f4e158

IMPDBTCL-271

NAME

IMPDBTCL-271

SUMMARY

The root attribute '%s' is not used in this application, so it is ignored.

DESCRIPTION

This warning occurs when read_db reads a root attribute that is not used in the current application. The most common reason is because the attribute was saved by an older release, and it is now obsolete and no longer needed. It is also possible an older release is trying to read a database saved by a newer release, and the older release does not understand the new attribute. In either case, the attribute will be ignored, and will not be saved by a subsequent write_db command.

IMPDBTCL-614

NAME

IMPDBTCL-614

SUMMARY

**INFO: (IMPDBTCL-614): Number of objects exceeds limit.Use setDbGetMode -displayLimit to control the number of objects evaluated by 'dbGet <object>.??' query.

DESCRIPTION

{DEATILMESSAGE}

IMPDC-1159

NAME

IMPDC-1159

SUMMARY

The input transition time value is less than 0.1ps. Ensure that the input transition time value is greater than or equal to 0.1ps.

DESCRIPTION

This warning is displayed when the value of input transition time specified by you is less than 0.1ps. When you specify an input transition time value that is less than 0.1ps, the software ignores this value and uses the default value of 0.1ps. To avoid this warning, ensure that the input transition time value is greater than or equal to 0.1ps.

IMPDC-3242

NAME

IMPDC-3242

SUMMARY

Total power of the design is not valid.

DESCRIPTION

{DETILMESSAGE}

IMPDC-3243

NAME

IMPDC-3243

SUMMARY

-powerDomain will be ignored in single PD flow.

DESCRIPTION

{DETILMESSAGE}

IMPDC-3245

NAME

IMPDC-3245

SUMMARY

The RC data is not in memory or the RC data in memory is for a different RC corner. RC data is being read.

DESCRIPTION

{DETILMESSAGE}

IMPDC-3246

NAME

IMPDC-3246

SUMMARY

Driver %s (cell %s) has different threshold value %s = %d from receiver %s (cell %s) threshold value %s = %d.

DESCRIPTION

{DETILMESSAGE}

IMPDC-3247

NAME

IMPDC-3247

SUMMARY

Driver %s (cell %s) has different slew derate value %s = %.3f from receiver %s (cell %s) slew derate value %s = %.3f.

DESCRIPTION

{DETILMESSAGE}

IMPDC-3248

NAME

IMPDC-3248

SUMMARY

This delay calculation is calculating IRMS data and may take longer run time than usual. If IRMS data is not needed, turn in off with setDelayCalMode -computeIrms false.

DESCRIPTION

{DETILMESSAGE}

IMPDC-3249

NAME

IMPDC-3249

SUMMARY

The delay calculation mode is AAE. In AAE mode, the delay is not calculated with effective capacitance and table lookup, option -delaytable will be ignored.

DESCRIPTION

{DETILMESSAGE}

IMPDF-2

NAME

IMPDF-2

SUMMARY

The errors found when reading the DEF file '%s' are too serious to continue. The rest of the DEF file will not be read. Refer to error messages above for details. Fix the errors, delete any partially read in data, and reread the corrected DEF file.

DESCRIPTION

If you have DEF syntax errors, you can look at the DEF manual to find the correct syntax. It can be accessed from the Innovus Help->Help Library... menu. Look under the Languages section for the latest LEF/DEF Language Reference Manual.

If there are other errors, check if you have the correct DEF file, and if you have the correct LEF or

OpenAccess libraries. Read the earlier error messages in detail to see exactly what went wrong.

Note, some data may have been read from the DEF file before the error occurred. You may need to delete it first, before reading a corrected DEF file. See documents for details about which sections of DEF are read in incrementally versus replacing the existing data.

IMPDF-30

NAME

IMPDF-30

SUMMARY

Line %ld: OffMGrid: %s (%d, %d) (%d, %d) %s %s is not on Manufacturing Grid.

DESCRIPTION

This error reports that a wire's coordinate in the DEF file are not on the manufacturing grid which will result in DRC errors.

The coordinates in the error message are in database units per micron (dbuPerMicron). Look for the following line in the DEF file to determine how many dbu's is 1 micron:

UNITS DISTANCE MICRONS dbuPerMicron ;

When reading DEF Innovus System will check that each edge and the center-line of wires is on the manufacturing grid defined in the technology LEF file (MANUFACTURINGGRID).

One possible scenario that could cause this issue is that the two edges of the wire are on manufacturing grid but the center line, which is what DEF syntax uses, may not be. To check if your dbu's have enough granularity, multiply dbuPerMicron * manufaturingGrid. The result should be an

integer quantity that is evenly divisible by two to ensure the center-line is on grid.

For example, if MANUFACTURINGGRID is 0.005, this is only achievable with a DBU of 2000.

- (1000*0.005)/2 = 2.5, (not evenly divisible by two), the result could be off manufacturing grid.
- (2000*0.005)/2 = 5, (evenly divisible by two), the result will be on manufacturing grid.

Or to say it another way:

If dbuPerMicron * manufacturingGrid is an odd number (e.g. 1000*0.005 = 5), you cannot create a path (center-line based) that has a width that is an odd number of manufacturing grids wide.

IMPDF-84

NAME

IMPDF-84

SUMMARY

The ROW '%s' is ignored because it references a site '%s' that has not been defined in the LEF/OpenAccess technology. Review the LEF files specified or the OA technology database, to see if the site is correctly defined.

DESCRIPTION

This error reports that a row references a site that has not been defined. The sites must be defined before they can be referenced from a row. Review the LEF files specified in the init_lef_file variable, or the OA technology database, and make sure the sites are correctly defined.

To determine the list of legal site names, use 'dbGet head.sites.name'.

While the design can be read in without rows and used for parasitic extraction and analysis, the loss of the rows will mean that placement and optimization functions will not work.

IMPDF-1008

NAME

IMPDF-1008

SUMMARY

The routing has wire-patches (that requires DEF 5.8 NETS RECT statements) in the signal routing that cannot be represented correctly in DEF 5.6 or 5.7. They will be converted to SPECIALNETS routing RECT shapes instead. This output is suitable for RC extraction tools, but this DEF should not be read back into Innovus as the routing data will not be correct. You should use DEF 5.8 to represent this routing data correctly by using "set dbgLefDefOutVersion 5.8".

DESCRIPTION

Wire-patches are a new DEF 5.8 concept that allows a rectangle to be added in the NETS symbolic routing section. They are commonly used to add a small amount of metal to fix minimum-area violations, or fill in notch violations, etc.

DEF 5.6 or 5.7 has no NETS syntax for these shapes, so they can only be written to the SPECIALNETS section using RECT syntax. If you read this DEF back into Innovus these shapes will be special-route shapes, and the signal router will not be able to rip up or repair them. You will need to remove them with a script.

IMPDF-1012

NAME

IMPDF-1012

SUMMARY

%s at (%d %d) on net '%s' has been found with unknown routing status so it is ignored.

DESCRIPTION

Routes or vias should have a route status (routed, fixed, cover, noshield) in order for defOut to write them to DEF. Routes with the unknown status are normally created by earlyGlobalRoute, and the net is marked isEarlyGlobalRouted and they are silently ignored by defOut unless you use the defOu -earlyGlobalRoutet option.

In some cases optimization may add some routes with the unknown status on nets that are not marked isEarlyGlobalRouted that will be repaired by the router later in the flow. It is also possible the user has added some routes manually or through scripts with the unknown status. This warning is caused by these types of routes, and defOut will not write them out by default.

You can avoid this warning by using the -earlyGlobalRoute option to force the unknown status routes to be written as "routed" status in the DEF, or by not using the -routing option so NETS section routing is not written at all.

IMPDF-1018

NAME

IMPDF-1018

SUMMARY

The routing has wire-patches (that require DEF 5.8 NETS RECT statements) in the signal routing that cannot be represented in DEF 5.5. They will be lost and the routing data will be incomplete with

missing shapes, because there is no DEF 5.5 syntax that can correctly represent them. You should use DEF 5.8 to represent this routing data correctly by using "set dbgLefDefOutVersion 5.8".

DESCRIPTION

Wire-patches are a new DEF 5.8 concept that allows a rectangle to be added in the NETS symbolic routing section. They are commonly used to add a small amount of metal to fix minimum-area violations, or fill in notch violations, etc.

DEF 5.5 has no NETS or SPECIALNETS syntax that can represent these shapes. If you read this DEF back into Innovus the missing shapes will cause DRC violations, and other problems. You will need to remove the signal routing and then run the router again or try to use ECO routing commands to repair them.

IMPECO-1

NAME

IMPECO-1

SUMMARY

Cannot %s the %s %s inside hierarchical instance %s. The hierarchical instance has a Verilog module %s that is used multiple times in the netlist, so directly modifying this hierarchical instance is not allowed. You must either use the –moduleBased option to modify the Verilog module instead, or set init_design_uniquify before init_design to force a unique module for each hierarchical instance.

DESCRIPTION

This message is issued when an ECO operation is applied on hierarchical instance and module is referenced multiple times in verilog netlist. ECO operations which do not support multiple referenced cells including changing instance name, changing an instancei's cell, deleting a net, adding a net, switching two terms of a net, and adding an instance.

To fix the issue, either use the -moduleBased option to modify the verilog module instead, or

uniquify the netlist by running command 'set init_design_uniquify 1' before init_design to force a unique module for each hierarchical instance.

IMPECO-37

NAME

IMPECO-37

SUMMARY

Net term hterm link incorrect after add term. Correct it.

DESCRIPTION

This message is issued when in the hierarchical design the link between instance and its immediate parent hierarchical instance is broken. Such link is set up during design load and needs to be fixed. Contact your Cadence Design System representative.

IMPECO-146

NAME

IMPECO-146

SUMMARY

Instance and net name must be unique in a module. The name '%s' is already used by an instance or a net in module '%s'. Use an unique name to avoid the problem. .

DESCRIPTION

This message is issued while adding a new net or changing an instance, the given new name for the net or instance is not unique. The name of net and instance must not be an existing name.

IMPECO-154

NAME

IMPECO-154

SUMMARY

Can not connect the net '%s' to the physical instance '%s' term '%s'.

DESCRIPTION

This message is issued because we don't allow connecting physical instance pins to logical net.

IMPECO-238

NAME

IMPECO-238

SUMMARY

Net (%s) term hterm link incorrect after attaching a term. Correct it.

DESCRIPTION

This message is issued when in the hierarchical design the link between instance and its immediate parent hierarchical instance is broken. Such link is set up during design loading and needs to be fixed. Contact your Cadence Design System representative.

IMPECO-521

NAME

IMPECO-521

SUMMARY

Cannot attach hterm to net (%s) without adding new port : different hierarchy.

DESCRIPTION

The specified term/port and net are in different hierarchy and cannot attach without creating a new port. To avoid this error, please try attachTerm/attachModule without -noNewPort.

IMPECO-560

NAME

IMPECO-560

SUMMARY

The netlist is not unique, because the module '%s' is instantiated multiple times. Make the netlist unique by running 'set init_design_uniquify 1' before loading the design to avoid the problem.

DESCRIPTION

This message is issued when the module is instantiated multiple times in a netlist. Current DB ECO commands need unique netlist. To make the netlist unique, run command 'set init_design_uniquify 1' before loading the design to avoid the problem.

IMPECO-570

NAME

IMPECO-570

SUMMARY

Assign is created by %s %s and %s %s.

DESCRIPTION

By default, init_no_new_assigns is set to 0, applications such as optimization can create Verilog assign statements during netlist ECOs. New assign creation is allowed by the tool. However, in this design, command "set init_no_new_assigns 1" was issued, creating any new assign is not allowed. Please report this issue to Cadence Customer Support.

As a work around, at the end of your run, use command remove_assigns to remove all assigns. Please note that this command removes all assigns including those assign statements contained in the incoming Verilog netlist except for the const tie (1'b1/1'b0) assigns.

IMPECO-620

NAME

IMPECO-620

SUMMARY

Cannot change the cell of instance '%s' to '%s' from '%s', because the pins of these two cells are not identical.

DESCRIPTION

This message is issued while changing the cell for an instance if the old cell and new cell do not have identical pins. This could be due to mismatch in number or name of the pins.

IMPESI-3086

NAME

IMPESI-3086

SUMMARY

The cell '%s' does not have characterized noise model(s) for '%s' lib(s). Missing noise information could compromise the accuracy of analysis.

DESCRIPTION

This message is aimed to highlight cells without CCSN/ECSMN/CDB models. check_noise command can be used to exhaustively check all the instances with missing noise models.

IMPESI-3140

NAME

IMPESI-3140

SUMMARY

Bumpy transitions may exist in the design which may lead to inaccurate delay computation. To report/analyze the nets having bumpy transition, please enable delay report and use command 'report_noise -bumpy_waveform -threshold 0' after timing analysis. Delay report is enabled by setting 'set_si_mode -enable_delay_report true' before timing analysis.

DESCRIPTION

The nets identified as having bumpy transitions are the nets which have a reverse swing of more than 30 percent of Vdd in their transitions. High crosstalk on such nets is the source of such bumpy transitions, and should be fixed to ensure accurate delay computation.

IMPESI-3188

NAME

IMPESI-3188

SUMMARY

Unable to interpolate for instance '%s' (cell: %s) view '%s'. The libraries '%s' %s.

DESCRIPTION

The analysis will snap to the library specified in IMPESI-3199 message. For proper analysis, make sure that you provide at least two libraries in the libset with different parameter values.

IMPESI-3189

NAME

IMPESI-3189

SUMMARY

Proper analysis will not take place since the cell, %s, is present in multiple noise library files(cdb): %s, %s and these files are bound to the same timing model file (.lib): %s. Make sure there is a one-to-one mapping between the noise and timing libraries. Check the ENCESI-3192 message for the names of the cdb files that are missing the timing library.

DESCRIPTION

For proper analysis, remove the extra noise library files or add the correct timing library files such that there is a one-to-one mapping between timing library and noise library files. The analysis tool can only bind one noise library to one timing library for proper analysis.

IMPESI-3190

NAME

IMPESI-3190

SUMMARY

Proper SI analysis cannot take place for net %s with driver instance %s and pin %s of reference cell %s beacuse there is no noise library data bound to the instance. Default parameters from the timing models will be used. Timing library mapped to this instance is %s at %s. Check that the proper noise libraries are being loaded in the design.

DESCRIPTION

Use the report_instance_library command to check the timing library binding for the instance. Use the report_instance_cdb command to check the cdB binding for the instance. Check that there is a noise library that matches the timing library power connections for the cell.

IMPESI-3191

NAME

IMPESI-3191

SUMMARY

Proper SI analysis cannot take place for net %s with receiver instance %s and pin %s with reference cell %s because there is no noise library data bound to the instance. Default parameters from the timing models will be used. Timing library mapped to this instance is %s at %s. Check that the proper noise libraries are being loaded in the design.

DESCRIPTION

Use the report_instance_library command to check the timing library binding for the instance. Use

the report_instance_cdb command to check the cdB binding for the instance. Check that there is a noise library that matches the timing library power connections for the cell.

IMPESI-3192

NAME

IMPESI-3192

SUMMARY

Could not find exact match of the timing model file (.lib) for cell %s of noise library file %s, and timing model library %s will be used for binding.

DESCRIPTION

For proper analysis, make sure there is a one-to-one mapping between timing library and noise library files.

IMPESI-3193

NAME

IMPESI-3193

SUMMARY

Could not find exact match between the noise library file, cdB, and the timing library file .lib for the cell %s of cdB %s, and the noise model for this cell will be ignored.

DESCRIPTION

For proper analysis, make sure there is a one-to-one mapping between timing library and noise library files.

IMPESI-3194

NAME

IMPESI-3194

SUMMARY

Unable to interpolate for instance '%s' (cell: %s) view '%s'. The libraries '%s' %s. Examine your libset and provide libraries to enable interpolation.

DESCRIPTION

The analysis will snap to the library specified in IMPESI-3199 message. For proper analysis, make sure that you provide at least two libraries in the libset with different parameter values.

IMPESI-3199

NAME

IMPESI-3199

SUMMARY

Unable to find proper library binding because there was no exact match and interpolation could not find appropriate libraries for instance '%s' (cell: %s) view '%s'. Using library '%s' for analysis.

DESCRIPTION

Use report_analysis_views, report_power_domain and report_instance_library commands to determine the design and library requirements. Also, check for IMPESI-3194 messages, if any, for interpolation related issues.

IMPESI-3352

NAME

IMPESI-3352

SUMMARY

Numerical instability detected on net %s during simulation of noisy transition. This may cause SI delay on this net to be more pessimistic than usual.

DESCRIPTION

A likely reason is poorly characterized timing model.

IMPESO-301

NAME

IMPESO-301

SUMMARY

The %s command requires design data to be loaded.

DESCRIPTION

The command could not be run because design data is not loaded. Load a database or design data.

IMPESO-303

NAME

IMPESO-303

SUMMARY

The Path Based Analysis (PBA) using retime %s is ignored %sbecause the AOCV analysis mode for timing analysis is not set. Configure the AOCV analysis mode by reading in the AOCV libraries, and set it using "set_analysis_mode -aocv true".

DESCRIPTION

AOCV based path based analysis (PBA) could not be done because AOCV analysis mode for timing analyis is not set. If you want to do AOCV based PBA analysis, then you need to configure the AOCV analysis mode by reading in AOCV libraries while loading the design, and set the AOCV mode using "set_analysis_mode -aocv true".

IMPESO-306

NAME

IMPESO-306

SUMMARY

Failed to open %s file %s for %s

DESCRIPTION

A file system error occurred when attempting to open a file. Usually this is because you do not have permission to read or write a file in the current working directory, or have specified a file for read which does not exist.

Example:

Use the operating system 'ls -l' command to check file permissions. Use the operating system 'chmod' command to change permissions.

The operating system 'df' command can be used to check available space. For example:

innovus 2> df -H

Filesystem Size Used Avail Use% Mounted on

/disk/directory 2.2T 2.0T 271G 88% /mount/mountpoint

IMPESO-309

NAME

IMPESO-309

SUMMARY

Error reading/writing file '%s'.

DESCRIPTION

The command was not able to read or write data from a file. Check available disk space and file permissions.

IMPESO-314

NAME

IMPESO-314

SUMMARY

Buffer cell '%s' will not be used because timing information for this cell is not available.

DESCRIPTION

The reported buffer cell cannot be used because there is no timing information available for it. This is most probably due to missing liberty files (.lib) in the design configuration.

To solve this, you should verify that buffers are part of each active library set inside the viewDefinition.tcl file.

IMPESO-317

NAME

IMPESO-317

SUMMARY

The hierarchical instance name '%s' provided in the partition list file is not found in the design.

DESCRIPTION

The partition list file should contain the names of all hierarchical module instances which should be treated as a partition. This error occurs when an entry in the partition list file could not be found in the design. Ensure the names in the file are correct.

IMPESO-320

NAME

IMPESO-320

SUMMARY

Cannot create directory '%s': %s.

DESCRIPTION

The current session does not have the write access to create a directory. Check the filesystem permissions for the current directory.

IMPESO-338

NAME

IMPESO-338

SUMMARY

Since number of unique setup and hold (active) views '%d' is greater than '%d', which is the amount of usable CPU set through %s command, some views will be timed sequentially and final summary report will be based on eco_opt_design internal estimated timing.

DESCRIPTION

When no ECO Timing DB are provided through the set_eco_opt_mode -load_eco_opt_db option, the eco_opt_design command will generate those automatically using the distributed MMMC infrastructure.

In case number of active views is greater than number of available hosts, some views will be timed sequentially, which will result in more runtime but also the final summary report will be based on eco_opt_design internal estimated timing.

To avoid this situation, it is recommended to enable equal or more hosts than the number of active views when relying on eco_opt_design to generate the ECO Timing DB.

Example:

Here is an example to enable 6 remote hosts, each one using 4 threads, for timing analysis :

set_multi_cpu_usage -remoteHost 6 -cpuPerRemoteHost 4

IMPESO-358

NAME

IMPESO-358

SUMMARY

Cell swapping transform requires multiple Vth libraries in the design.

DESCRIPTION

The tool was not able to detect multiple Vth libraries in this design which is a prerequesite to perform same size cell swapping.

Either you have provided only a single Vth library or all cells from other Vth libraries are set as dont_touch.

IMPESO-366

NAME

IMPESO-366

SUMMARY

setDontUse commands will be ignored by eco_opt_design.

DESCRIPTION

The eco_opt_design does support set_dont_use command in order to enable/disable the usage of a given cell.

The setDontUse command, is not supported by eco_opt_design.

To avoid this message, make sure that the setDontUse commands being part of the Innovus DB being loaded, or from your script, are replaced by set_dont_use command.

Example:

To disable usage of BUFX1 cell using set_dont_use command:

set_dont_use [get_lib_cells BUFX1] true

IMPESO-389

NAME

IMPESO-389

SUMMARY

Failed to open %s file %s for %s

DESCRIPTION

A file system error occurred when attempting to open a file. Usually this is because you do not have permission to read or write a file in the current working directory, or have specified a file for read which does not exist.

Example:

Use the operating system 'ls -l' command to check file permissions. Use the operating system 'chmod' command to change permissions.

The operating system 'df' command can be used to check available space. For example:

innovus 2> df -H

Filesystem Size Used Avail Use% Mounted on

/disk/directory 2.2T 2.0T 271G 88% /mount/mountpoint

IMPESO-396

NAME

IMPESO-396

SUMMARY

max_tran/max_cap data is not available for hold only views during timing analysis. This data is required for hold view DRV aware optimization (enabled with option -check_drv_for_hold_views) in TSO. View(s) needs to be specified as both active setup and active hold view during timing analysis to use this feature in TSO.

DESCRIPTION

To use the feature of hold view aware DRV optimization (enabled with option -check_drv_for_hold_views), ECO Timing DB needs late slews data (max_tran/max_cap). This data will be available only when the view is available as setup view as well. You can either specify the view(s) in setup list in current flow or use DMMMC/SMSC flow for ECO Timing DB generation.

IMPEXT-1023

NAME

IMPEXT-1023

SUMMARY

Failed to %s file or directory '%s' to '%s'. The system message is '%s'.

DESCRIPTION

This error occurs when a file system operation, such as copy or move, fails. This may be because of inadequate disk space or permission in the file system, such as the current directory or the TMPDIR, where the operation is being performed.

IMPEXT-1024

NAME

IMPEXT-1024

SUMMARY

File system operation %s(%s%s%s) failed. The system message is '%s'.

DESCRIPTION

This error occurs when a file system operation, such as mkdir or mkstemp, fails. This may be because of inadequate disk space or permission in the file system, such as the current directory or the TMPDIR, where the operation is being performed.

IMPEXT-1081

NAME

IMPEXT-1081

SUMMARY

setExtractRCMode -effortLevel %s is ignored for preRoute extraction. This setting is only applicable for postRoute extraction.

DESCRIPTION

Extraction supports two engine modes, preRoute and postRoute. These are specified using the engine parameter of the setExtractRCMode command. Effort-level selection is not supported in the preRoute mode. For more information on setting the effort level, see the documentation for the setExtractRCMode command.

IMPEXT-1197

NAME

IMPEXT-1197

SUMMARY

The '/tmp' directory has been specified for cache/temporary data storage. In distributed processing mode IQuantus expects cache/temporary data directory to be accessible on all hosts used for distributed processing. Therefore the current directory will be used instead of '/tmp'.

DESCRIPTION

This warning is issued when distributed processing is enabled for IQuantus and FE_TMPDIR or TMPDIR is set to /tmp. Distributed processing requires that the temporary storage area should be accessible to all hosts. The software will use the current directory instead.

You can specify a directory for temporary storage in any of the following ways, depending on what is available:

\t

1. \t Save in the directory defined by the environment variable, FE_TMPDIR.

\t

2. \t Save in the directory defined by the environment variable, TMPDIR.

\t

3. \t Save in the current directory, if it is writeable.

\t

4. \t Save in /tmp.

IMPEXT-1221

NAME

IMPEXT-1221

SUMMARY

No poly layer found in the technology file '%s'.

DESCRIPTION

No poly layer is found in the technology file. Check to ensure that the correct technology file is specified and check the technology file content.

IMPEXT-1222

NAME

IMPEXT-1222

SUMMARY

No CUT layer defined between the poly LAYER and first routing metal LAYER in LEF technology file '%s'.

DESCRIPTION

The CUT layer between the poly layer and the first routing metal layer is missing in the LEF technology file.

An example of a LEF outline showing CUT layer is as provided below:

\t

LAYER poly

\t \t \t

TYPE MASTERSLICE;

\t

END poly

\t

LAYER V0

\t \t \t

TYPE CUT;

\t

END V0

\t

LAYER M1

\t \t \t

TYPE ROUTING;

\t

END V1

IMPEXT-1241

NAME

IMPEXT-1241

SUMMARY

No poly layer found in the layermap file, '%s'.

DESCRIPTION

The layer mapping information for the poly layer is missing in the layermap file. This information is required for running extraction. Check the layermap file and rerun extraction.

IMPEXT-1245

NAME

IMPEXT-1245

SUMMARY

TCL array 'qxHiddenOption' is an internal variable that is provided only for developers.

DESCRIPTION

TCL array 'qxHiddenOption' is an internal variable that is provided only for developers. To avoid this message, remove the 'set qxHiddenOption' from your script.

IMPEXT-2773

NAME

IMPEXT-2773

SUMMARY

The via resistance between layers %s and %s could not be determined from the LEF technology file because the via resistance specification is missing. A default of 4 Ohms will be used as via resistance between these layers.

DESCRIPTION

This warning message is displayed when the capacitance table file is not specified for RC corners during a multi-corner setup and the via resistance between the specified layers is missing in the technology LEF file. In this case, a default of 4 Ohms will be used as via resistance between these layers. If capacitance table file is specified for all RC corners using the create_rc_corner or update_rc_corner command, the software uses RC data from this capacitance table file instead of accessing the LEF data.

IMPEXT-2776

NAME

IMPEXT-2776

SUMMARY

The via resistance between layers %s and %s is not defined in the capacitance table file. The via resistance of %g Ohms defined in the LEF technology file will be used as via resistance between these layers.

DESCRIPTION

This warning message is displayed when the capacitance table file is not specified for RC corners during a multi-corner setup. In this case, the software uses RC data from the LEF file. If capacitance table file is specified for all RC corners using the create_rc_corner or update_rc_corner command, the software uses RC data from this capacitance table file instead of using the LEF data.

IMPEXT-2827

NAME

IMPEXT-2827

SUMMARY

Found NONDEFAULT RULE for layer %d having wire width (%d), which is less than the minimum wire width (%d)" "for this layer. This may cause inaccuracy in the extraction results. Check the design for correctness.

DESCRIPTION

An example of where this error will be reported is shown below. In the default layer definition for M2, the width is 0.07um (1400 db units,) but in the non-default rule the width is 0.06um (1200 db units):

Default M2 definition

LAYER M2

TYPE ROUTING ;

DIRECTION VERTICAL ;

WIDTH 0.07 ;

END M2

Non-default rule test_ndr

NONDEFAULTRULE test_ndr

LAYER M2

WIDTH 0.06 ;

SPACING 0.7 ;

END M2

END test_ndr

In this case the non-default rule needs to be corrected so the width is greater than or equal to the default width of 0.07um.

IMPEXT-2884

NAME

IMPEXT-2884

SUMMARY

An unconnected wire is found at terminal %s of net %s. The wire connectivity of this net is broken because of which the parasitic data for this net may be incomplete.

DESCRIPTION

During RC extraction (extractRC) this message indicates the extractor found that the net is not properly connected to this terminal. If verifyConnectivity -net <net_name> or checkRoute reports an open net during RC extraction (extractRC), it means that the net is not properly connected. Connect this net, so that extraction is completed.

IMPEXT-2900

NAME

IMPEXT-2900

SUMMARY

Unable to find the rc-corner name '%s' in the active rc-corner list specified below. It could be due to an error in syntax, or because the corner is not an active one. To fix this, make sure the correct RC corner is bound to an active delay corner and analysis view.

DESCRIPTION

The RC corners considered active by the tool would be those which are referenced in at least one active analysis view. Defining an RC corner alone is not enough to activate that RC corner. You may follow the example below on defining an activate an RC corner.

The RC corners considered active are those that are referenced in at least one active analysis view. Defining an RC corner alone is not enough to activate that RC corner. See the example below on how to activate an RC corner.

create_rc_corner -name rc_typ -qx_tech_file rc_typ/qrcTechFile

create_constraint_mode -name dummyConstraint -sdc_files /dev/null

create_delay_corner -name dummyDelayCorner -library_set [lindex [all_library_sets] 0] -rc_corner rc_typ

create_analysis_view -name dummyAnalysisView -constraint_mode dummyConstraint -delay_corner dummyDelayCorner

set_analysis_view -setup {dummyAnalysisView} -hold {dummyAnalysisView}

IMPEXT-2989

NAME

IMPEXT-2989

SUMMARY

SPEF file reading will not be completed. This is because even though the option to read corner-specific SPEF file(s) has been specified, multi-corner RC extraction is not defined. Please ensure that the MMMC environment is set up and initialized correctly.

DESCRIPTION

The following example creates single-mode two-corner analysis in MMMC setup:

```
create_library_set -name lib_ff \\
\t \t
-timing \\
\t \t
[list /lib/ecsm/std_ff_ecsm.lib \\
\t \t
/lib/essm/macro_ff_ecsm.lib]

create_library_set -name lib_ss \\
\t \t
-timing \\
\t \t
[list /lib/ecsm/std_ss_ecsm.lib \\
\t \t
/lib/essm/macro_ss_ecsm.lib]

create_rc_corner -name rcworst \\
\t \t
-cap_table rcworst.capTbl

create_rc_corner -name rcbest \\
\t \t
-cap_table rcbest.capTbl

create_delay_corner -name setup_delay \\
```

```
\t \t
-library_set lib_ss \\
\t \t
-rc_corner rcworst

create_delay_corner -name hold_delay \\
\t \t
-library_set lib_ff \\
\t \t
-rc_corner rcbest

create_constraint_mode -name func \\
\t \t
-sdc_files \\
\t \t
[list /lib/SDC/func.tcl]

create_analysis_view -name func_setup -constraint_mode func -delay_corner delay_setup

create_analysis_view -name func_hold -constraint_mode func -delay_corner delay_hold

set_analysis_view -setup [list func_setup] -hold [list func_hold]
```

IMPEXT-3297

NAME

IMPEXT-3297

SUMMARY

The validation check on parasitic database '%s' has failed and cannot be restored. To continue the flow, choose one of the following options: extract the design, load the SPEF file(s), or load a compatible parasitic database.

DESCRIPTION

The validation check on the parasitic database has failed and, therefore, it cannot be restored. The most likely cause of validation failure is an unsupported parasitic database version. The parasitic database generated by the software generally holds good only for one base release and its ISR releases. A compatible parasitic database can be generated using the current version of the software by either extracting the design or loading the SPEF file(s).

IMPEXT-3423

NAME

IMPEXT-3423

SUMMARY

Detected %d nets with incomplete RC network. Low-value resistances have been added by the software to complete the RC network of these nets. Review the list of affected nets in the '%s' file to ensure they are not along the critical path because results of timing analysis performed on nets with incomplete RC network can be inaccurate.

DESCRIPTION

This warning is displayed when the SPEF file contains incomplete RC network connectivity for some nets. This can also happen if a net occurring before a given net in the SPEF file has a coupling capacitance to a node that is not referenced in the resistance section of the given net. While computing the delay of a net, if the RC network in the SPEF file is incomplete, there will be no resistance path from the driver to the receiver of the net. As a result, the receiver will never switch in simulation and this will result in incorrect delay computation. Therefore, the software adds a low-value resistance to establish a resistance path from the driver to the receiver of the net so that the delay of the net can be computed correctly. To avoid this warning, ensure that the SPEF file has

the complete RC network for all the nets.

IMPEXT-3493

NAME

IMPEXT-3493

SUMMARY

The design extraction status has been reset by set_analysis_view/update_rc_corner or setExtractRCMode command. The parasitic data can be regenerated either by extracting the design using the extractRC command or by loading the SPEF or RCDB file(s). To prevent resetting of the extraction status, avoid changing extraction modes.

DESCRIPTION

This message is printed when design extraction status is reset because of changes in the extraction mode settings. The parasitic data generated in the previous extraction run is no longer usable. However, the parasitic data will not be deleted if the previous extraction was done using the IQuantus extraction engine. In this case, the tool might use the previously extracted database to perform incremental extraction to save on the runtime or it might perform full-chip extraction.

IMPEXT-3496

NAME

IMPEXT-3496

SUMMARY

The specified options -best, -worst, -typical in 'rda_Input(ui_captbl_file)' of the configuration file for readCapTable are obsolete. For single-mode two-corner analysis and optimization, use MMMC setup instead of reading multiple captables through the readCapTable command. To ensure compatibility with future releases, update the script to use a MMMC viewDefinition.tcl file.

DESCRIPTION

The following example creates single-mode two-corner analysis in MMMC setup:

```
create_library_set -name lib_ff \\
\t \t
-timing \\
\t \t
[list /lib/ecsm/std_ff_ecsm.lib \\
\t \t
/lib/essm/macro_ff_ecsm.lib]

create_library_set -name lib_ss \\
\t \t
-timing \\
\t \t
[list /lib/ecsm/std_ss_ecsm.lib \\
\t \t
/lib/essm/macro_ss_ecsm.lib]

create_rc_corner -name rcworst \\
\t \t
-cap_table rcworst.capTbl

create_rc_corner -name rcbest \\
\t \t
-cap_table rcbest.capTbl

create_delay_corner -name setup_delay \\
```

```
\t \t
-library_set lib_ss \\
\t \t
-rc_corner rcworst

create_delay_corner -name hold_delay \\
\t \t
-library_set lib_ff \\
\t \t
-rc_corner rcbest

create_constraint_mode -name func \\
\t \t
-sdc_files \\
\t \t
[list /lib/SDC/func.tcl]

create_analysis_view -name func_setup -constraint_mode func -delay_corner delay_setup

create_analysis_view -name func_hold -constraint_mode func -delay_corner delay_hold

set_analysis_view -setup [list func_setup] -hold [list func_hold]
```

IMPEXT-3497

NAME

IMPEXT-3497

SUMMARY

The options -best or -worst or -typical for readCapTable are obsolete. For single-mode two-corner analysis and optimization, use the MMMC setup instead of reading multiple captables through the readCapTable command. To ensure compatibility with future releases, update the script to use an MMMC viewDefinition.tcl file.

DESCRIPTION

The following example creates a single-mode two-corner analysis in the MMMC setup:

```
create_library_set -name lib_ff \\
\t \t
-timing \\
\t \t
[list /lib/ecsm/std_ff_ecsm.lib \\
\t \t
/lib/essm/macro_ff_ecsm.lib]

create_library_set -name lib_ss \\
\t \t
-timing \\
\t \t
[list /lib/ecsm/std_ss_ecsm.lib \\
\t \t
/lib/essm/macro_ss_ecsm.lib]

create_rc_corner -name rcworst \\
\t \t
-cap_table rcworst.capTbl
```

```
create_rc_corner -name rcbest \\
\t \t
-cap_table rcbest.capTbl

create_delay_corner -name setup_delay \\
\t \t
-library_set lib_ss \\
\t \t
-rc_corner rcworst

create_delay_corner -name hold_delay \\
\t \t
-library_set lib_ff \\
\t \t
-rc_corner rcbest

create_constraint_mode -name func \\
\t \t
-sdc_files \\
\t \t
[list /lib/SDC/func.tcl]

create_analysis_view -name func_setup -constraint_mode func -delay_corner delay_setup

create_analysis_view -name func_hold -constraint_mode func -delay_corner delay_hold

set_analysis_view -setup [list func_setup] -hold [list func_hold]
```

IMPEXT-3530

NAME

IMPEXT-3530

SUMMARY

The process node is not set. Use the command setDesignMode -process <process node> prior to extraction for maximum accuracy and optimal automatic threshold setting.

DESCRIPTION

Cadence recommends always using setDesignMode to specify the process technology. It controls many default settings that are used by implementation and analysis engines within Innovus System. For analysis purposes, the best results depend on using different RC extraction thresholds going from 130nm to 90nm, or from 65nm to 45nm. setDesignMode -process recognizes nodes from 10 to 250 (nm), with 90 as the default. Use getDesignMode to query the current settings.

The -process setting will influence, for example, setExtractRCMode -engine and -effortLevel defaults.

IMPEXT-3534

NAME

IMPEXT-3534

SUMMARY

A multi-CPU setup has been provided in the tool to use '%d' CPUs, but licenses are only available for '%d' CPUs. Therefore, '%d' CPUs will be used for '%s'. Adjust the option with setMultiCpuUsage.

DESCRIPTION

To adjust the number of CPUs you want to use in your session:

setMultiCpuUsage -localCpu 8

Or run the following command for more detail:

innovus > setMultiCpuUsage -help

IMPEXT-3550

NAME

IMPEXT-3550

SUMMARY

The command setRCFactor is obsolete because the latest version of the software is using the Multi-Mode Multi-Corner (MMMC) architecture for design import. To ensure compatibility migrate to an MMMC environment and set RC factors using the create_rc_corner and update_rc_corner commands. For more information on creating MMMC configurations, refer to the "Configuring the Setup for Multi-Mode Multi-Corner Analysis" section in the "Importing and Exporting Designs" chapter in the Innovus System User Guide.

DESCRIPTION

The following command creates an RC corner called rc-cbest that uses the capacitance table rcbest.capTbl and derates the resistance values based on the temperature of 50 degree Celsius, and sets various factors for preRoute and postRoute:

create_rc_corner -name rc-cbest -cap_table rcbest.capTbl -T 50 \\

-postRoute_cap 1.06 \\

-postRoute_clkcap 0.96 \\

-postroute_clkres 0.95 \\

-postRoute_res 1.02 \\

-postRoute_xcap 1.04 \\

-preRoute_cap 1.03 \\

-preRoute_clkcap 0.99 \\

-preRoute_clkres 0.97 \\

-preRoute_res 1.05

The following command changes the capacitance table used by the RC corner rc-cbest to rcbest_2.capTbl and the temperature by which resistance values are derated to 25 celsius:

update_rc_corner -name rc-cbest -cap_table rcbest_2.capTbl -T 25

IMPEXT-3551

NAME

IMPEXT-3551

SUMMARY

The command readCapTable is obsolete because the latest version of the software is using the Multi-Mode/Multi-Corner (MMMC) architecture for design import. To ensure compatibility, migrate to an MMMC environment and set Cap tables using the -cap_table option of the MMMC commands: create_rc_corner and update_rc_corner. For more information on creating MMMC configurations, refer to the "Configuring the Setup for Multi-Mode Multi-Corner Analysis" section in the "Importing and Exporting Designs" chapter in Innovus System User Guide.

DESCRIPTION

Some examples of the MMMC commands are provided below:

The following command creates an RC corner called rc-cbest that uses the capacitance table rcbest.capTbl and derates the resistance values based on the temperature of 50 degree Celsius:

create_rc_corner -name rc-cbest -cap_table rcbest.capTbl -T 50

The following example changes the capacitance table used by the RC corner rc-cbest to rcbest_2.capTbl and the temperature by which resistance values are derated to 25 degree Celsius:

update_rc_corner -name rc-cbest -cap_table rcbest_2.capTbl -T 25

IMPEXT-5036

NAME

IMPEXT-5036

SUMMARY

The '%s' file '%s' is not readable. Either Quantus QRC failed to generate it, or Innovus failed to read it. See Innovus Text Command Reference for setExtractRCMode -qrcCmdType, correct the

command file, and retry extraction.

DESCRIPTION

The most common cause for this error is: the -directory_name being specified in the output_setup section of the command file. Remove the -directory_name option from the command file.

IMPEXT-5064

NAME

IMPEXT-5064

SUMMARY

Extraction could not be completed. This is because the syntax in the layermap file '%s' is incorrect since it does not use CCL syntax to define the layer mapping (using the -lefTechFileMap option). Correct the layermap file to use CCL syntax and run extraction again.

DESCRIPTION

The format required for -lefTechFileMap has changed. The old format was just a list of layers like:

PO poly \\

CO odcont \\

The new format should be in Quantus QRC CCL format and have the following general syntax:

extraction_setup -technology_layer_map \\

<design_layer_name1> <technology_layer_name1> \\

<design_layer_name2> <technology_layer_name2>

etc...

Following is an example of the new format:

extraction_setup -technology_layer_map \\

PO poly \\

CO odcont \\

M1 metal1 \\

VIA1 via1 \\

M2 metal2 \\

VIA2 via2 \\

M3 metal3 \\

VIA3 via3 \\

M4 metal4 \\

VIA4 via4 \\

M5 metal5 \\

VIA5 via5 \\

M6 metal6 \\

VIA6 via6 \\

M7 metal7 \\

VIA7 via7 \\

M8 metal8

Use the -lefTechFileMap option to point to the file.

IMPEXT-6013

NAME

IMPEXT-6013

SUMMARY

There is a gap or overlap between layer '%s' (h=%g t=%g) and layer '%s' (h=%g t=%g) in the ICT file.

DESCRIPTION

The following example shows properly defined ICT file.

dielectric "dielectric_0" {

\t

conformal FALSE

\t

height 0.000000

\t

thickness 0.500000

\t

dielectric_constant 3.900000

}

dielectric "dielectric_1" {

\t

conformal FALSE

\t

height 0.500000

\t

thickness 0.600000

\t

dielectric_constant 4.200000

}

dielectric "dielectric_2" {

\t

conformal FALSE

\t

height 1.100000

\t

thickness 0.050000

\t

dielectric_constant 8.100000

}

Notice above that:

height + thickness of dielectric_0 = height of dielectric_1

And:

height + thickness of dielectric_1 = height of dielectric_2

If the dielectric layer height and thicknesses do not meet this requirement, then there is an overlap or gap between the layers and this error is reported.

IMPEXT-6089

NAME

IMPEXT-6089

SUMMARY

The processing layer '%s' : delta_layer '%s' has not been defined. The ICT file needs to be modified. Ensure that the ICT files are ordered so that the lowest layers are defined first, followed by

higher layers. For example, POLY is defined before MET1. Call generateCapTbl again.

DESCRIPTION

For example, the generateCapTbl command would give a syntax error when processing the following ICT file containing the delta_layer construct:

```
conductor "MET1" {

min_spacing 0.30

min_width 0.30

delta_layer POLY <== Not Yet Defined

delta_height 0.30

}

conductor "POLY" {

min_spacing 0.25

min_width 0.16

height 0.35

upto 0.55
```

resistivity 8.6

gate_forming_layer true

}

IMPEXT-6159

NAME

IMPEXT-6159

SUMMARY

The annotated parasitics can not be reported because the command report_annotated_parasitics is issued before the design is loaded. Load the design before issuing report_annotated_parasitics.

DESCRIPTION

Load the design with either restoreDesign (or read_design in Tempus) or init_design and the parasitic data with one of the following: extractRC (or extract_rc in tempus), spefIn (or read_spef in Tempus), and read_parasitics, before issuing report_annotated_parasitics.

The following example loads a design from the test.imp.dat directory and reads the parasitic data into the Innovus session:

restoreDesign test.imp.dat TOP

read_parasitics -rc_corner C1 TOP_C1ef.gz -rc_corner C2 TOP_C2ef

report_annotated_parasitics -list_annotated -list_not_annotated -list_real_net -list_float_net -list_nodriver_net -list_noload_net -max_missing 3

IMPEXT-6166

NAME

IMPEXT-6166

SUMMARY

Capacitance table file(s) without the EXTENDED section is being used for RC extraction. This is not recommended because it results in lower accuracy for clock nets in preRoute extraction and for all nets in postRoute extraction using -effortLevel low. Regenerate capacitance table file(s) using the generateCapTbl command.

DESCRIPTION

To run the generateCapTbl command with Multi-CPU, specify the following commands:

setDistributeHost -local

setMultiCpuUsage -localCpu 4

generateCapTbl -ict sample.ict -output sample.capTbl

IMPEXT-6189

NAME

IMPEXT-6189

SUMMARY

Initialization for preRoute extraction mode using the technology file is being terminated since the technology file '%s' could not be read. This is because it is either an invalid file or an error occurred in importing it. Check the file and read it in again using create_rc_corner or update_rc_corner -qx_tech_file.

DESCRIPTION

The technology file (.tch) is generated by TechGen, a built-in functionality of Quantus. Users get it either directly from foundries, or can generate it themselves from an ICT file (an ASCII-format Interconnect Technology input file) using TechGen.

IMPEXT-6191

NAME

IMPEXT-6191

SUMMARY

Using a captable file is not recommended for process nodes less than or equal to %d nm due to parasitic accuracy concerns. The Quantus QRC technology file should be specified for all RC corners using the command create_rc_corner or update_rc_corner, which will then be used for preRoute and postRoute(effort level medium or high or signoff) extraction engines.

DESCRIPTION

For more information, see the "RC Extraction > PreRoute Extraction Flow without Capacitance Table data" User Guide.

IMPEXT-6195

NAME

IMPEXT-6195

SUMMARY

The low effort level for postRoute extraction mode will be ignored because it is not allowed for the current multi-corner setup. This is because either flow is without a cap table, or the design process node is less than or equal to 32 nm and cap tables are not specified for all the active RC corners. To avoid this, switch to -effortLevel medium or high or signoff, if Quantus QRC techfile(s) are available.

DESCRIPTION

For more information, see the "RC Extraction > PreRoute Extraction Flow without Capacitance Table data" User Guide.

IMPEXT-6197

NAME

IMPEXT-6197

SUMMARY

The Cap table file is not specified. This will result in lower parasitic accuracy when using preRoute extraction or postRoute extraction with effort level 'low'. It is recommended to generate the Cap table file using the 'generateCapTbl' command and specify it before extraction using 'create_rc_corner/update_rc_corner -cap_table'.

DESCRIPTION

If Cap table file is not available, user can generate it using 'generateCapTbl –ict [-lef]'. For preRoute

extraction on 32nm and below designs, or postRoute extraction under 65nm, Quantus QRC technology files are more accurate than the Cap table. User can specify them with 'create_rc_corner or update_rc_corner -qx_tech_file' if Quantus QRC technology files are available. For postRoute extraction with available Quantus QRC tech files the 'setExtractRCMode -effortLevel' should then be updated to 'medium or high or signoff'.

IMPEXT-6198

NAME

IMPEXT-6198

SUMMARY

Extraction will not take place because the technology file is not specified for all RC corners. Technology files are needed for preRoute extraction and effort level medium or high or signoff of postRoute extraction when the process node set using set setDesignMode -process is less than or equal to %d nm. Use the commands create_rc_corner or update_rc_corner to specify the technology file for all corners and run the extraction again.

DESCRIPTION

In MMMC based flow, the qrcTechFile is strongly recommended for preRoute and postRoute RC extraction in process nodes of 32nm and lower, because of the increased accuracy that is necessary at these nodes.

For further detail, see Innovus Digital Implementation System User Guide: "RC Extraction" > "PreRoute Extraction Flow without Capacitance Table Data.

IMPEXT-6202

NAME

IMPEXT-6202

SUMMARY

In addition to the technology file, the capacitance table file is specified for all the RC corners. If the technology file is already specified for all the RC corners, the capacitance table file is not required for preRoute and postRoute extraction. In a new session, the capacitance table files can be removed from the create_rc_corner command to enable the technology file to be used for preRoute and postRoute (effort level medium/high/signoff) extraction engines.

DESCRIPTION

This warning message is displayed when the process node set using setDesignMode is greater than 32nm and both technology and captable files are specified for all the RC corners. Using this setup, the captable file would be used for preRoute extraction. However, to enable preRoute extraction using the technology file, remove the captable file specification from create_rc_corner in a new session. This would change the default value of the effort level for postRoute extraction to medium, and the low effort level would not be allowed.

IMPEXT-7036

NAME

IMPEXT-7036

SUMMARY

The system call %s failed because of %s. Rerun the command or contact the Cadence support team for information.

DESCRIPTION

This is a system error for which some possible reasons could be; too many processes running on the system, insufficient memory available to create a child process, or the system call interrupted by a signal.

IMPFM-205

NAME

IMPFM-205

SUMMARY

Model %s does not exist.

DESCRIPTION

The specified model name does not exist in the current loaded design. Model name should be a logical module name in the netlist or an instance group name in the design. Double check the model name and re-specify it again.

Example:

<CMD> set_proto_mode -identify_exclude_module {tdsp_coore}

**WARN: (IMPFM-205): Module tdsp_coore does not exist.

<CMD> set_proto_mode -idenitfy_exclude_module {tdsp_core}

IMPFM-206

NAME

IMPFM-206

SUMMARY

Module %s and module %s are exclusive. Both cannot be specified as flexmodels and/or black boxes.

DESCRIPTION

Currently Innovus cannot support nested FlexModels. If a module is already being specified as FlexModel, its parent or children module cannot be specified as FlexModel again. Innovus issued the ERROR message IMPFM-206 for the specified modules where only one of them can be specified as FlexModel.

IMPFM-226

NAME

IMPFM-226

SUMMARY

Module %s cannot be a partition,In Innovus FlexModel technology you cannot have a flexmodel as a partition.

DESCRIPTION

In Innovus FlexModel technology you cannot have a flexmodel as a partition, the above message is indicating that.

Innovus will not have any errors during creation of %s as a flexmodel even though its declared as a partition in the original netlist.

However, if you load the design back after creating the flex models this errors appears.

Now, below is solution that you can trick Innovus to have a flex model as a partition:

SOLUTION after you hit this error:

#Save out a current floorplan for future use:

<CMD> saveFPlan current_Floopplan.fp

#Delete all existing Partitions.

<CMD> deletePartition -all

Restore the protomodels again

<CMD> source DBS/$DESIGN/$Name.protomodels

Read the previously saved floorplan to restore partitions

<CMD> loadFPlan current_Floopplan.fp

Now you should not see the above error.

IMPFM-235

NAME

IMPFM-235

SUMMARY

This design has less than 1M instances. It is recommend to use FlexModel for a design that has more than 1M instances since netlist reduction ratio may not be good for small FlexModels.

DESCRIPTION

It is recommended to use FlexModel for a large design that has more than 1 million instances to see the real benefit of it. Since the design size is small, netlist reduction ratio may not be good for this design.

IMPFM-318

NAME

IMPFM-318

SUMMARY

Model '%s' does not exist.

DESCRIPTION

Specified model does not exist in the current loaded design. Model can be a module or an instance group in the design. Double check the model name and re-run the command again.

IMPFM-333

NAME

IMPFM-333

SUMMARY

Option %s for command %s is obsolete and will be removed in future releases. Use %s instead.

DESCRIPTION

Specified option of the given command is obsolete and will be removed in future release. Use the new replaced command and/or update your run script to avoid warning message.

IMPFM-334

NAME

IMPFM-334

SUMMARY

Option %s of the command %s is obsolete and will be removed in future releases.

DESCRIPTION

Specified option of the given command is obsolete and will no longer be available in future release. Do not use this option and/or remove it from your run script to avoid this warning message.

IMPFM-353

NAME

IMPFM-353

SUMMARY

Model %s's standard cells and macros have a combined area of %7.2f, which is greater than specified value %7.2f for -create_total_area.

DESCRIPTION

Total area of standard cells and macros in the current netlist of the model is greater than specified value of the -create_total_area option. Innovus will use the user-specified value instead. If this is not the intention, re-specify the total area for the model with create_proto_model -create_total_area.

Example:

<CMD> set_proto_model -model tdsp_core -create_total_area 10

**WARN: (IMPFM-353): Model tdsp_core's standard cells and macros have a combined area of 7753.67, which is greater than specified value 10.00 for -create_total_area.

<CMD> set_proto_model -model tdsp_core -create_total_are 9000.0

IMPFM-706

NAME

IMPFM-706

SUMMARY

Model %s has been generated.

DESCRIPTION

create_proto_model outputs this warning message if the specified model already had been generated from previous run and was saved in the prototyping model directory specified by the -create_dir option of the set_proto_mode command. Innovus will reuse this model and will not re-generate it to save time. If model needs to be re-generated, either following choice can be used:

1. Remove existing prototyping model directory and rerun create_proto_model again.

2. Overwrite existing model by running create_proto_model with -overwrite and -model options.

IMPFM-709

NAME

IMPFM-709

SUMMARY

Model %s is incomplete. Re-generate the model.

DESCRIPTION

create_proto_model outputs this warning message if the specified model had been generated but not incomplete from previous run. The command will re-generate this model again. This is for information only.

IMPFM-725

NAME

IMPFM-725

SUMMARY

Command %s is obsolete and will be removed in future releases. Please use %s instead.

DESCRIPTION

Specified command is obsolete in the current release and will not be available in future release. Use the new replaced command and update your run script if needed to avoid warning message.

IMPFM-730

NAME

IMPFM-730

SUMMARY

Model %s already has physical constraint so it cannot be converted to soft guide. Unplace the model and rerun the command again.

DESCRIPTION

Specified FlexModel currently already has guide/fence/region boundary. In order to convert this FlexModel to a soft guide which does not have any physical constraint, unplace the model by manually moving it outside the core area or using the unplaceGuide command. Once the model is unplaced, rerun the set_proto_model_physical_constraint command again.

Example:

set_proto_model_physical_constraint -model spi -type soft_guide

**WARN: (IMPFM-730): Model SPI_INST already has physical constraint so it cannot be converted to soft guide. Unplace the model and rerun the command again.

unplaceGuide SPI_INST

set_proto_model_physical_constraint -model spi -type soft_guide

IMPFM-735

NAME

IMPFM-735

SUMMARY

Model %s does not have physical constraint so it cannot be converted to %s. Place the model and rerun the command again.

DESCRIPTION

Specified model cannot be converted to guide/fence/region since the model does not have any physical constraint. Move the model inside the core area and rerun the set_proto_model_physical_constraint command again.

Example:

setObjFPlanBoxList Module cORE/test_wrapper 12554.1900 15037.5500 13499.3250 15659.8000

set_proto_model_physical_constraint -model test_wrp -type fence

IMPFM-759

NAME

IMPFM-759

SUMMARY

create_proto_model currently cannot handle a design that has both module and instance group based FlexModels. Only module based models will be created with this run.

DESCRIPTION

Innovus supports both module and instance group based FlexModels. However create_proto_model currently does not create models for both modules and instance groups within one run. create_proto_model will only create module based FlexModels for this run. To work around this limitation, do two create_proto_model runs:

1. Specify instance group based models first and run create_proto_model for instance groups.

2. Specify module based FlexModels and then run second create_proto_model to generate models for modules.

IMPFM-760

NAME

IMPFM-760

SUMMARY

The design has no flexmodel, please specify planDesign seeds in a constraint file and do proto_design -constraints.

DESCRIPTION

Example:

<CMD> proto_design -constraints constraint_file_name

IMPFM-761

NAME

IMPFM-761

SUMMARY

Routing blockage characterization currently does not support a design that has both module and instance group based FlexModels. FlexFiller routing blockages will only be created for module based FlexModels.

DESCRIPTION

FlexFiller routing blockage characterization cannot handle a design that has both module and instance group based FlexModels. To work around this limitation use following flow:

1. Specify instance group based FlexModels only.

2. Run create_proto_model to create models for specified instance groups.

3. Run routing blockage characterization for these instance group based FlexModels. Only run this step if ART based model generation is used.

4. Specify module based Flexmodels

5. Run create_proto_model to crete models for the modules

6. Run routing blockage characterization for these module based FlexModels. Only run this step if ART based model generation is used.

IMPFM-790

NAME

IMPFM-790

SUMMARY

Cannot load FlexFiller route blockage since FlexFiller routing layers specified in file %s is '%d' which is not consistent with the current available routing layer number '%d'.

DESCRIPTION

routeBlkg.model file is created by the command create_flexfiller_route_blockage. The most likely reason for the error is that you set different routing layer when doing create_flexfiller_route_blockage and restoring FlexModel design. you can run mib::getMinNumMaxRouteLayerWireLayer to get available routing layer number. The solution is that you need redo create_flexfiller_route_blockage. If you do not want to model Flexfiller route blockage, you can safely ignore the error.

IMPFM-1206

NAME

IMPFM-1206

SUMMARY

Design has net(s) without routing. Best_layer_no_detour will be used for calculating delay for un-routed net(s).

DESCRIPTION

Current design contains nets that have partial or no routing. Prototyping timing analysis tool(timeDesign -proto) will calculate net delays for these net using Manhattan route with best routing layers. To obtain net delays for all nets in the design based on routing information, re-route the design and timing the design again.

IMPFM-1304

NAME

IMPFM-1304

SUMMARY

The design is not portable and power intent will not be updated.

DESCRIPTION

If you really want to update power intent data, please save the design as a portable design, and do createLogicHierarchy on the design.

IMPFP-40

NAME

IMPFP-40

SUMMARY

Cannot support data '%s' for '%s'. The data may be generated from new version of software which is not compatible with current version. Check the data or change the software version.

DESCRIPTION

Cannot support data '%s' for '%s'. The data may be generated from new version of software which is not compatible with current version. Check the data or change the software version.

IMPFP-104

NAME

IMPFP-104

SUMMARY

Cannot open %s. You may not have permission read a file or the file simply does not exist. Check the file name or contact administrator.

DESCRIPTION

The message occurs because you may not have permission read a file or the file simply does not exist.

IMPFP-172

NAME

IMPFP-172

SUMMARY

Row '%s' cannot accommodate all pad cells, needs %d sites > %d row sites. The floorplan needs to be enlarged to place the pads legally in the IO rows.setIoFlowFlag 0 to disable the IO row flow and avoid this message.

DESCRIPTION

If setIoFlowFlag is 1 when loading a design, a check is run to verify the IO rows can accommodate the pads in the design. This warning indicates there are more pad cells than the IO rows can accommodate so the floorplan needs to be enlarged. Run checkPlace to report overlapping pads and look for pads placed outside the IO rows. If you want to avoid this message disable the IO row flow by setting setIoFlowFlag 0 prior to loading the design.

IMPFP-175

NAME

IMPFP-175

SUMMARY

No IO rows in design. Use command "getIoFlowFlag" to get the current IO flow(with or without row). To avoid this error message, Use command"setIoFlowFlag" to change the IO flow.

DESCRIPTION

Innovus issues above error message on restoring the saved design. Though, I have no IO cells defined in my Verilog netlist and I am not reading in any IO cells in my libraries.Why does Innovus issue this error message? init_design or defIn issues this error message if IO rows are not defined in the design and below option is set to 1 in the globals file: set conf_use_io_row_flow 1 This variable is set to 1 for IO Row Flow in Innovus.

IMPFP-247

NAME

IMPFP-247

SUMMARY

Cannot create non-integral multiple height row. There is no site to generate rows inside the power domain. Check it has a SITE that is common to all the cells in the power domain.

DESCRIPTION

This warning is issued by createRow command when user tries to create standard cell row which is non-integral height of existing row's or default row.Highly recommend user to use a?? initCoreRowa?? for power domain/whole chip row creating, which fetch row setting from CPF. User even dona??t need specify tech site, just one command without option.

IMPFP-298

NAME

IMPFP-298

SUMMARY

Floorplan cannot be resized due to insufficient X spacing or illegal resize line. Edit floorplan to make room in X direction or re-specify resize line and re-run.

DESCRIPTION

Floorplan cannot be resized due to insufficient X spacing or illegal resize line. Edit floorplan to make room in X direction or re-specify resize line and re-run. This error is likely to occur, if user has not specified the"setResizeFPlanMode & setResizeLine" options correctly.

Example:

Floorplan cannot be resized due to insufficient X spacing or illegal resize line. Edit floorplan to make room in X direction or re-specify resize line and re-run. This error is likely to occur, if user has not specified the "setResizeFPlanMode & setResizeLine" options correctly. For example to increase floorplan in vertical direction, resizeLine must have the same x coordinate. For eg setResizeLine -direction V (-63 798) (-63 3878)

IMPFP-316

NAME

IMPFP-316

SUMMARY

Not enough space for floorplan resize. No change for floorplan.

DESCRIPTION

One of the possible reason for this warning could be that the Fplan_box and the Fplan_corebox areas are same. Try maintaining some difference among two will resolve the warning.

IMPFP-320

NAME

IMPFP-320

SUMMARY

The resize value needs at least bigger than one micron.

DESCRIPTION

The message is reported by resizeFP when user tried to resize floorplan with less than one micron.

Example:

resizeFP -xSize -0.9 -ySize -0.9

IMPFP-701

NAME

IMPFP-701

SUMMARY

The Design Boundary's lower left corner not on manufacture grid. The boundary must be on manufacture grid. Check the definition of manufacture grid. Check the definition of manufacture grid in the tech LEF/OA or re-specify floorplan.

DESCRIPTION

The Design Boundary's lower left corner not on manufacture grid. The boundary must be on manufacture grid. Check the definition of manufacture grid. Check the definition of manufacture grid in the tech LEF/OA or re-specify floorplan.

IMPFP-704

NAME

IMPFP-704

SUMMARY

IO box's upper right corner not on manufacture grid. IO box must be on manufacture grid. Check the definition of manufacture grid or re-specify floorplan.

DESCRIPTION

IO box's upper right corner not on manufacture grid. IO box must be on manufacture grid. Check the definition of manufacture grid or re-specify floorplan.

IMPFP-788

NAME

IMPFP-788

SUMMARY

Cell '%s' for IO '%s' has LEF/OA CLASS other than PAD or sub class Areal0.

DESCRIPTION

If a customer is using OA libraries instead of LEF, they are confused by the wording of the ERROR message. The message should automatically change to say OA instead of LEF if Innovus was started with OA libraries. If this is not possible at this time, then the ERROR message should say LEF/OA libraries and not just LEF.

Example:

Cell '%s' for IO '%s' has LEF CLASS other than PAD or sub class Areal0.

or when starting Innovus with OA libraries:

Cell '%s' for IO '%s' has OA CLASS other than PAD or sub class Areal0.

or

Cell '%s' for IO '%s' has LEF/OA CLASS other than PAD or sub class Areal0.

IMPFP-793

NAME

IMPFP-793

SUMMARY

IO cell '%s' doesn't overlap any IO row to snap to. When use IO row flow, tool will automatically check that if IO pads and IO rows are matching. Recreate IO rows and then try to snap IO cell on the row.

DESCRIPTION

This warning message will be generated if you choose the IO row flow for pad placement (setIoFlowFlag 1). When you use the IO row flow, tool will automatically check that if IO pads and IO rows are matching. These messages just warn you that there is some mismatches in the IO row flow.If you want to make the warning message disappear, please recreate IO rows and use defOut then defIn to check. Else, you can ignore them or you can go with normal flow without IO rows.setIoFlowFlag 0 #this will prompt to use the normal IO flow.Also, check for "setUserDataValue conf_use_io_row_flow 1" in the .globals file. If the value of this variable is set to 1, then change this to 0 to avoid these warnings.

IMPFP-903

NAME

IMPFP-903

SUMMARY

Bump %s is assigned to net %s. Not deleted.

DESCRIPTION

The specified bump cannot be deleted because a top level net is assigned to it. The net assignment must first be removed in order to delete the bump. The net assignment can be removed using either the unassignBump or unassignBumpByName commands.

Example:

The following commands will select a bump named "98", unassign its net and

delete it.

select_bump -bumps {98}

unassignBump -selected

deleteBumps -selected

IMPFP-905

NAME

IMPFP-905

SUMMARY

Constraints of HInst %s is out of die. Cannot output it to floorplan file.

DESCRIPTION

This message occurs when saveFPlan or saveDesign tries to save floorplan file but instance are placed outside of die area.

IMPFP-1594

NAME

IMPFP-1594

SUMMARY

No site specified. Check the LEF/OA file to make sure a site is specified for core cell.

DESCRIPTION

All designs require at least one core site to create rows with even if the design only contain hard blocks.So the user needs to load the tech LEF/OA which has SITE defined in it even if the blocks don't use the SITE

Example:

For example :

SITE site1

SYMMETRY y ;

CLASS core ;

SIZE 0.660 BY 5.040 ;

END site1

IMPFP-1871

NAME

IMPFP-1871

SUMMARY

Failed to run the command because it attempts to change the top cell bounding box. Use the 'floorPlan' command to modify top cell bounding box first before calling this command.

DESCRIPTION

When a user creates a floorplan let's say 100 by 100 and snapping to grid is enabled, the tool will automatically snap the FP to the grid and the FP will end up to be 99.987 by 99.95. Next, when the user wants to run a command like setObjFPlanBoxList (or several other command) with the original Fplan coordinates, the toll will complain that this is an attempts to change the top cell bounding box. This is true, because 100 is basically outside of the post-snapping bounding box (which is let's say 99.987). Either the user can turn off the auto-snap when creating the FP, do the operations he wants, then use snap_floorplan to snap the FP to grid, or he must use the coordinates stored in the DB after autosnap of the FP.

IMPFP-2101

NAME

IMPFP-2101

SUMMARY

Shifter for %s to %s is not defined in shifter table.

DESCRIPTION

Shifter for %s to %s is not defined.

It may be due to no shifter defined in CPF file or no standard cell found in the power domain.

Example:

**WARN: (IMPFP-2101): Shifter for _internal_VDD_SOC_VSS_ to PD_PD_AVE_CCH is

not defined in shifter table.

_internal_VDD_SOC_VSS_ is an empty power domain created automatically by

default. There is no shifter defined for this internal power domain.

IMPFP-3101

NAME

IMPFP-3101

SUMMARY

Skip don't touch net '%s'. When insert shifter for floating net & undriven net,the don't touch net should be ignored.

DESCRIPTION

In the design there were many ports that had been assigned as set_dont_touch. These ports were assigned to nets of the same name in the design. Based on the fact that these are dont_touch nets in the design, Innovus System will not insert logic onto those nets, even if they are suggested as necessary by the CPF for the design. With the SDC and CPF in conflict, Innovus System honors the SDC that the net should not be changed and gave the above warning.

Example:

The user should confirm that the ports/nets labeled as dont_touch should indeed

need to be dont_touch. And if it is necessary to create buffering, level shifting, or isolation on those ports/nets, then the setting the port/net as dont_touch in SDC should be removed.

IMPFP-3302

NAME

IMPFP-3302

SUMMARY

Rows for site '%s' cannot be created. The height of this site is non-integer multiple of default row type. Non-integer multiple-height rows and single height rows cannot overlap. Edit the library set to modify the default row type or remove the library.

DESCRIPTION

This message reports the error situation about Non-integer multiple-height rows. Edit the library set to modify the default row type or remove the library to resolve this issue.

IMPFP-3356

NAME

IMPFP-3356

SUMMARY

IO Inst %s is outside of design boundary. All placed IO instances must be located inside the design boundary. Move IO instance to a location within the design boundary.

DESCRIPTION

The above error is reported when restoring the design. Why is this error reported and how can I avoid it?

This error indicates there are instances placed outside the design boundary.All instances with placement status of placed, fixed or cover need to be placed within the design boundary. To resolve this:

Place all cells currently placed outside the design boundary within the boundary. If these cells are physical only cells (i.e. filler cells, decap cells,etc.) you can delete them from the database.

Example:

The following script can be used to delete and report all cells outside the

design boundary.

```
#####################################################
redirect { puts "" } > CellOutsideBoundary.txt
set x1 [lindex [lindex [dbGet top.fplan.box] 0] 0]
set y1 [lindex [lindex [dbGet top.fplan.box] 0] 1]
set x2 [lindex [lindex [dbGet top.fplan.box] 0] 2]
set y2 [lindex [lindex [dbGet top.fplan.box] 0] 3]
set num 0
deselectAll
selectInst *
foreach inst [dbGet selected] {
set box [dbGet $inst.box]
set lx [lindex [lindex $box 0] 0]
set ly [lindex [lindex $box 0] 1]
set ux [lindex [lindex $box 0] 2]
set uy [lindex [lindex $box 0] 3]
if { [expr $lx < $x1] || [expr $ly < $y1] || [expr $ux > $x2] || \
[expr $uy > $y2] } {
redirect { puts [dbGet $inst.name] } >> CellOutsideBoundary.txt
deleteInst [dbGet $inst.name]
```

```
set num [expr $num + 1]
}
}
echo "$num cells deleted and stored in CellOutsideBoundary.txt"
deselectAll
#####################################################
```

Please note that after Innovus 13.1 is is OK to have a COVER type macro which is

partially outside the prBoundary.

IMPFP-3361

NAME

IMPFP-3361

SUMMARY

The Cell %s has already set padding %d. Specify it again will overlap the original padding. Use reportCellPad command to query and check.

DESCRIPTION

This warning message is issued when the user tries to add cell padding again to a library cell which already has a cell padding defined. User can run reportCellPad command to report out previously defined cell padding to confirm.

IMPFP-3388

NAME

IMPFP-3388

SUMMARY

Block instance %s not found.

DESCRIPTION

This message is issued when loadFPlan could not find the corresponding Block instance accroding to the block name.

IMPFP-3761

NAME

IMPFP-3761

SUMMARY

The resolveSdpOverlap command is obsolete.

DESCRIPTION

The command 'resolvSdpOverlap' is no longer supported. Please update your scripts to use 'set_sdp_mode' and 'placeSdpGroup' instead.

Example:

The following command disables extension of the core boundary if the boundary

cannot accommodate all SDP placements:

set_sdp_mode -disable_extended_core true

The following commands place elements or instances of all defined SDP

groups and generate a detailed SDP placement report named

dtmf_chip.sdp.rpt:

set_sdp_mode -place_report dtmf_chip.sdp.rpt

placeSdpGroup

IMPFP-3780

NAME

IMPFP-3780

SUMMARY

Only orthogonal edges are allowed in blockage polygons. One or more edges is an odd-angle edge, including this one: {x1 y1} {x2 y2}. You must fix the polygon to only use orthogonal edges.

DESCRIPTION

Creates a routing blockage object that can be moved even outside the core area. The object area prevents routing of specified metal layers, signal routes, and hierarchical instances in this area. Currently only orthogonal edges are supported by this command. You must use DEF directly if you need to create a blockage with 45-degree edges. Use this command during partition floorplanning.

IMPFP-3803

NAME

IMPFP-3803

SUMMARY

Command "%s" is obsolete and has been replaced by "%s". The obsolete command still works in this release, but to avoid this warning and to ensure compatibility with future releases, update your script to use "%s".

DESCRIPTION

There is a change from Innovus '%s' release onwards. "%s" command is obsolete and has been replaced by "%s" command.

Example:

**WARN: (IMPFP-3803): Command "createObstruct" is obsolete and has been replaced by "createPlaceBlockage".
Use below 2 commands for this purpose:
setPlaceMode a??selectiveBlockage true
createPlaceBlockage a??type soft {-box {x1 y1 x2 y2 } | -polygon {{x1 y1 } {x2 y2 }...} | -boxList {{llx1 lly1 urx1 ury1} {llx2 lly2 ...}}
However, this option allows not only all buffers and inverters but also isolation cells and level shifters. If user wants to limit the size, type of cells or even instances that are allowed in the area, one more command can be used:
unspecifySelectiveBlkgGate
[-help]
[-cell cellName]
[-inst instName]
In addition, other types of cells or instances can be allowed through the following command:
specifySelectiveBlkgGate
[-help]
[-cell cellName]
[-inst instName]
This last 2 commands work when setPlaceMode -selectiveBlockage is set to true.

IMPFP-3823

NAME

IMPFP-3823

SUMMARY

Cannot find routing blockage with name: %s.

DESCRIPTION

You have this message because the routing blockage with the specified name does not exist. Please check your naming in your command options.

IMPFP-3824

NAME

IMPFP-3824

SUMMARY

Cannot find place blockage with name: %s.

DESCRIPTION

You have this message because the placement blockage with the specified name does not exist. Please check your naming in your command options.

IMPFP-3825

NAME

IMPFP-3825

SUMMARY

Cannot find place blockage with name: %s and type: %s. Check your naming in the command options and make sure a valid blockage type(hard, soft, or partial) is given.

DESCRIPTION

You have this message because the placement blockage with the specified name and type does not exist. Please check your naming in your command options and make sure a valid blockage type(hard, soft, or partial) is given.

IMPFP-3881

NAME

IMPFP-3881

SUMMARY

IO box is not equal to die box, which is not allowed in a block design.

DESCRIPTION

This message is issued when the IO box is not equal to the die box in a block design. Modify the boxes to be the same to resolve this issue.

Related commands: floorPlan

IMPFP-3929

NAME

IMPFP-3929

SUMMARY

The symmetry of instance '%s' does not allow the rotation or flipping as requested. symmetryX must be true to allow flipping about the X-axis, symmetryY must be true to flip about the Y-axis, and symmetryR90 to allow rotation. Check current cell symmetry with 'dbGet [dbGet -p head.libCells.name <cellName>].??'.

DESCRIPTION

{The symmetry is wrong and you need to update the library cell data to fix it permanently (LEF SYMMETRY statement). You can also change it with dbSet in the current session if you want to continue without reloading the libraries and design.}

IMPFP-3941

NAME

IMPFP-3941

SUMMARY

PreRoute (%f %f) (%f %f) not on manufacturing grid. It must be on manufacturing grid in order to be manufactured. Move the object so it is on the manufacturing grid.

DESCRIPTION

This message reports that an object is off the manufacturing grid. The manufacturing grid is defined in the technology LEF file. Look for MANUFACTURINGGRID in the LEF. An object must be on this grid in order for it to be manufactured. Some objects like partition boundaries or GCell Grids are not actually manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so it is on the manufacturing grid.

IMPFP-3957

NAME

IMPFP-3957

SUMMARY

Multi-Layer pin %s has metals not exactly stacking. Multi-Layer pin needs at least 2 metal shapes.

DESCRIPTION

This message is issued about multi-layer pins. They needs at least 2 metal shapes.

IMPFP-3960

NAME

IMPFP-3960

SUMMARY

The cell '%s' and cell '%s' are using same tech site %s, but they have different VDDonbotom attributes. Need to align VDD/GND pins of single height row/double height row when creating rows. Check and correct the LEF file or OA abstract view.

DESCRIPTION

If the customer is using OA libraries, this message should automatically switch to say OA abstract view instead of LEF. If Innovus does not have a mechanism to allow this type of dynamic response to the ERROR message, then the message should be changed to say OA abstract view or LEF file

Example:

The cell '%s' and cell '%s' are using same tech site %s, but they have

different VDDonbotom attributes. Need to align VDD/GND pins of single height

row/double height row when creating rows. Check and correct the LEF file.

or if starting Innovus with OA libraries:

The cell '%s' and cell '%s' are using same tech site %s, but they have

different VDDonbotom attributes. Need to align VDD/GND pins of single height

row/double height row when creating rows. Check and correct the OA abstract

view.

or

The cell '%s' and cell '%s' are using same tech site %s, but they have

different VDDonbotom attributes. Need to align VDD/GND pins of single height row/double height row when creating rows. Check and correct the LEF file or OA abstract view.

IMPFP-3961

NAME

IMPFP-3961

SUMMARY

The techSite '%s' has no related standard cells in LEF/OA library. Cannot make calculations for this site type unless standard cell models of this type exist in the LEF/OA library. If the SITE is not used by the library you can ignore this warning or remove the SITE definition from the LEF/OA to avoid this message.

DESCRIPTION

This warning occurs when a site is defined without being referenced by any cell in LEF/OA library. The tool uses the SITE definition along with the library cells which use the SITE to validate the power and ground pins are defined consistently so followpin routing will be successful.

Example:

* The following example shows a predefined SITE 'core' which is referenced by a cell 'AND0':

SITE core

SITE 0.180 BY 1.114 ;

SYMMETRY Y ;

CLASS CORE ;

END core

MACRO AND0

CLASS CORE ;

SIZE 0.360 BY 2.228 ;

SITE core;

...

END AND0

IMPFP-3966

NAME

IMPFP-3966

SUMMARY

%s is not on manufacturing grid (LL-%.4f %.4f). The object must be on manufacturing grid in order to be manufactured. Move the object so it is on the manufacturing grid.

DESCRIPTION

This message reports that an object is off the manufacturing grid. The manufacturing grid is defined under the MANUFACTURINGGRID section in the technology LEF file. An object must be on this grid for it to be manufactured.Some objects like partition boundaries or GCell Grids are not actually manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so that it is on the manufacturing grid.

IMPFP-3967

NAME

IMPFP-3967

SUMMARY

%s is not on manufacturing grid (UR-%.4f %.4f). The object must be on manufacturing grid in order

to be manufactured. Move the object so it is on the manufacturing grid.

DESCRIPTION

This message reports that an object is off the manufacturing grid. The manufacturing grid is defined under the MANUFACTURINGGRID section in the technology LEF file. An object must be on this grid for it to be manufactured.Some objects like partition boundaries or GCell Grids are not actually manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so that it is on the manufacturing grid.

IMPFP-3968

NAME

IMPFP-3968

SUMMARY

Horizontal Track is off manufacturing grid. It must be on manufacturing grid in order to be manufactured. Move the object so it is on the manufacturing grid.

DESCRIPTION

This message reports that an object is off the manufacturing grid. The manufacturing grid is defined under the MANUFACTURINGGRID section in the technology LEF file. An object must be on this grid for it to be manufactured.Some objects like partition boundaries or GCell Grids are not actually manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so that it is on the manufacturing grid.

IMPFP-3969

NAME

IMPFP-3969

SUMMARY

Vertical Track is off manufacturing grid. It must be on manufacturing grid in order to be manufactured. Move the object so it is on the manufacturing grid.

DESCRIPTION

This message reports that an object is off the manufacturing grid. The manufacturing grid is defined under the MANUFACTURINGGRID section in the technology LEF file. An object must be on this grid for it to be manufactured.Some objects like partition boundaries or GCell Grids are not actually manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so that it is on the manufacturing grid.

IMPFP-3970

NAME

IMPFP-3970

SUMMARY

Placement grid is not on manufacturing grid.

DESCRIPTION

This message reports that an object is off the manufacturing grid. The manufacturing grid is defined under the MANUFACTURINGGRID section in the technology LEF file. An object must be on this grid for it to be manufactured.Some objects like partition boundaries or GCell Grids are not actually manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so that it is on the manufacturing grid.

IMPFP-3971

NAME

IMPFP-3971

SUMMARY

The GCell Grid (%g %g) is not on manufacturing grid.

DESCRIPTION

{ This message reports that an object is off the manufacturing grid. The manufacturing grid is defined in the technology LEF file. Look for MANUFACTURINGGRID in the LEF. An object must be on this grid in order for it to be manufactured. Some objects like partition boundaries or GCell Grids are not actually manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so it is on the manufacturing grid. }

IMPFP-3972

NAME

IMPFP-3972

SUMMARY

Routing blockage((%f,%f),(%f,%f))is not on manufacturing grid. Check the routing blockage and move it on the manufacturing grid.

DESCRIPTION

This message reports that an object is off the manufacturing grid. The manufacturing grid is defined under the MANUFACTURINGGRID section in the technology LEF file. An object must be on this grid for it to be manufactured.Some objects like partition boundaries or GCell Grids are not actually

manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so it is on the manufacturing grid.

IMPFP-3973

NAME

IMPFP-3973

SUMMARY

Routing blockage not on manufacturing grid.

DESCRIPTION

This message reports that an object is off the manufacturing grid. The manufacturing grid is defined under the MANUFACTURINGGRID section in the technology LEF file. An object must be on this grid for it to be manufactured.Some objects like partition boundaries or GCell Grids are not actually manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so it is on the manufacturing grid.

IMPFP-3974

NAME

IMPFP-3974

SUMMARY

The object %p (name : %s) is off the manufacturing grid. The object must be on manufacturing grid in order to be manufactured. Move the object so it is on the manufacturing grid.

DESCRIPTION

{ This message reports that an object is off the manufacturing grid. The manufacturing grid is

defined in the technology LEF file. Look for MANUFACTURINGGRID in the LEF. An object must be on this grid in order for it to be manufactured. Some objects like partition boundaries or GCell Grids are not actually manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so it is on the manufacturing grid. }

IMPFP-3975

NAME

IMPFP-3975

SUMMARY

Instance %s not on manufacturing grid. It must be on manufacturing grid in order to be manufactured. Move the object so it is on the manufacturing grid.

DESCRIPTION

{ This message reports that an object is off the manufacturing grid. The manufacturing grid is defined in the technology LEF file. Look for MANUFACTURINGGRID in the LEF. An object must be on this grid in order for it to be manufactured. Some objects like partition boundaries or GCell Grids are not actually manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so it is on the manufacturing grid. }

IMPFP-3976

NAME

IMPFP-3976

SUMMARY

IO Pin %s, %s layer shape is not on the manufacturing grid. It must be on the manufacturing grid for it to be manufactured. Move the object so it is on the manufacturing grid.

DESCRIPTION

This message reports that an object is off the manufacturing grid. The manufacturing grid is defined under the MANUFACTURINGGRID section in the technology LEF file. An object must be on this grid for it to be manufactured.Some objects like partition boundaries or GCell Grids are not actually manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so it is on the manufacturing grid.

IMPFP-3977

NAME

IMPFP-3977

SUMMARY

Multi-Layer pin %s has via %s not on manufacturing grid. It must be on manufacturing grid in order to be manufactured. Move the object so it is on the manufacturing grid.

DESCRIPTION

{ This message reports that an object is off the manufacturing grid. The manufacturing grid is defined in the technology LEF file. Look for MANUFACTURINGGRID in the LEF. An object must be on this grid in order for it to be manufactured. Some objects like partition boundaries or GCell Grids are not actually manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so it is on the manufacturing grid. }

IMPFP-3978

NAME

IMPFP-3978

SUMMARY

Ptn %s Pin %s is not on manufacturing grid. It must be on manufacturing grid in order to be manufactured. Move the object so it is on the manufacturing grid.

DESCRIPTION

{ This message reports that an object is off the manufacturing grid. The manufacturing grid is defined in the technology LEF file. Look for MANUFACTURINGGRID in the LEF. An object must be on this grid in order for it to be manufactured. Some objects like partition boundaries or GCell Grids are not actually manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so it is on the manufacturing grid. }

IMPFP-3980

NAME

IMPFP-3980

SUMMARY

Polygon pre-route is not on manufacturing grid. It must be on manufacturing grid in order to be manufactured. Move the object so it is on the manufacturing grid.

DESCRIPTION

{ This message reports that an object is off the manufacturing grid. The manufacturing grid is defined in the technology LEF file. Look for MANUFACTURINGGRID in the LEF. An object must be on this grid in order for it to be manufactured. Some objects like partition boundaries or GCell Grids are not actually manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so it is on the manufacturing grid. }

IMPFP-3981

NAME

IMPFP-3981

SUMMARY

PreRoute Via %s (%f,%f) is not on manufacturing grid. It must be on manufacturing grid in order to be manufactured. Move the object so it is on the manufacturing grid.

DESCRIPTION

{ This message reports that an object is off the manufacturing grid. The manufacturing grid is defined in the technology LEF file. Look for MANUFACTURINGGRID in the LEF. An object must be on this grid in order for it to be manufactured. Some objects like partition boundaries or GCell Grids are not actually manufactured so this error may not be as serious as a via or other physical object being off grid. Overall, you should investigate the object and move it so it is on the manufacturing grid. }

IMPFP-4008

NAME

IMPFP-4008

SUMMARY

The ring number '%d' is specified at sides '%s' , so all IO pads defined in this ring honor margins for these sides to calculate the location.

DESCRIPTION

The ring number '%d' is specified at sides '%s' , so all IO pads defined in this ring honor margins for these sides to calculate the location.

Example:

(top

(io_row ring_number = 1 margin = 0)

)

(bottom

(io_row ring_number = 1 margin = 90)

)

(left

(io_row ring_number = 1 margin = 180)

)

IMPFP-4009

NAME

IMPFP-4009

SUMMARY

The specified ring_number '%d' exceeds the allowed max number 1000. Input correct ring_number or reduce the number of rings.

DESCRIPTION

The specified ring_number '%d' exceeds the allowed max number 1000. Input correct ring_number or reduce the number of rings.

Example:

(top

(io_row ring_number = 1001 margin = 0)

)

IMPFP-4010

NAME

IMPFP-4010

SUMMARY

The io_order '%s' defined for ring_number '%d' in local is different from the global setting '%s' . Tool will use the local setting for it.

DESCRIPTION

The io_order '%s' defined for ring_number '%d' in local is different from the global setting '%s' . Tool will use the local setting for it.

Example:

(globals

version=3

io_order = counterclockwise

)

(left

(locals

ring_number=1

io_order=clockwise

)

IMPFP-4011

NAME

IMPFP-4011

SUMMARY

There are more than one of space, offset, skip and endcap as constraints for IO instance '%s'. Use only one of them as the constraint.

DESCRIPTION

There are more than one of space, offset, skip and endcap as constraints for IO instance '%s'. Use only one of them as the constraint.

Example:

(inst name="ins_7" space = 0 offset = 1000)

IMPFP-7006

NAME

IMPFP-7006

SUMMARY

Follow pin (Pin Box:%s) routed over hard macro (%s) should be cut at macro boundary.

DESCRIPTION

{Follow pin cannot be routed over hard macros. So it should be cut at macro boundary.}

IMPFP-7007

NAME

IMPFP-7007

SUMMARY

Power / Ground [rail | via | followpin] %s on layer %d does not match expected track color at box %s.

DESCRIPTION

{The color of power/ground [rail | via | followpin] should be the same as layer track.}

IMPFP-7008

NAME

IMPFP-7008

SUMMARY

Follow pin for net %s should horizontally align with the row boundary and vertically align with row end. The follow pin's box is : %s.

DESCRIPTION

{Horizontal followpin should align with the row boundary. Vertical followpin should align with row end.}

IMPFP-7009

NAME

IMPFP-7009

SUMMARY

Follow pin for net %s should align with power pin of rows (cells) if the cell will be placed in same orientation as row orientation. The follow pin's box is : %s

DESCRIPTION

{The cell's followpin should align with power pin of rows if the cell is placed in the same orientation with row orientation.}

IMPFP-7012

NAME

IMPFP-7012

SUMMARY

%s has been chosen to fit to track. But it's pin(%s) on layer %d is not on track.

DESCRIPTION

{Pins should be on layer track.}

IMPFP-7013

NAME

IMPFP-7013

SUMMARY

%s has a pin(%s) on layer %d. Its shape is on track, but color is not the same. According our rule NON-FAT pin shape should have same color with track.

DESCRIPTION

{NON-FAT pin shape should have the same color with track.}

IMPFP-7014

NAME

IMPFP-7014

SUMMARY

%s has a pin(%s) on layer %d. Its shape is on track, but color is not the same. According our rule FAT pin shape should have same color with track.

DESCRIPTION

{FAT pin shape should have the same color with track.}

IMPFP-7015

NAME

IMPFP-7015

SUMMARY

%s has a pin(%s) on layer %d. Its shape is on track, but color is the same. According our rule FAT pin shape should have different color with track.

DESCRIPTION

{FAT pin shape should have the different color with track.}

IMPFP-7016

NAME

IMPFP-7016

SUMMARY

Instance %s of macro cell %s is not fixed. Please update the place_status to fixed prior to running placement.

DESCRIPTION

{Instance of macro cell should be fixed status before running placement.}

IMPFP-9998

NAME

IMPFP-9998

SUMMARY

The symmetry of instance '%s' does not allow the rotation or flipping as requested. x must be true to allow flipping about the X-axis, y must be true to flip about the Y-axis, xy must be true to flip about X or Y axis, and any must be true to allow rotation. Check current cell symmetry with 'get_db [get_db insts <cellName>].base_cell.symmetry'.

DESCRIPTION

{The symmetry is wrong and you need to update the library cell data to fix it permanently (LEF SYMMETRY statement). You can also change it with set_db in the current session if you want to continue without reloading the libraries and design.}

IMPILM-194

NAME

IMPILM-194

SUMMARY

Cannot flatten ILM modules due to preceding reported messages. All ILM modules will remain unflattening.

DESCRIPTION

All ILM modules cannot be flattened due to the preceding reported messages. Problem is detected during reading an ILM netlist. The ILM netlist may have mismatched ports, or have duplicate module definition. Check the preceding error messages, fix the reported problem, and rerun the command

again.

Example:

innovus> flattenIlm

...

...

**ERROR: (IMPILM-193): There's problem reading ilm netlist (tdsp_core.v). If the ILM netlist has mismatched port(s), you can either define an empty module definition for 'tdsp_core' based on the one in ILM netlist upfront in the top level design netlist, or modify the instantiation/module for the mismatched port(s) in the top netlist to be consistent. Then re-run the flow for using ILM. If ILM netlist has duplicate module, try to re-run createInterfaceLogic to recreate the ILM model or modify the duplicate modules to have unique name.

**ERROR: (IMPILM-194): Cannot flatten ILM modules due to preceding reported messages. All ILM modules will remain unflattening

IMPILM-203

NAME

IMPILM-203

SUMMARY

There is no ILM specified in the design. Nothing will be switched to ILM view.

DESCRIPTION

flattenIlm command will not do anything because the design does not have any specified ILM. An ILM should be specified first before running flattenIlm command. Users can specify an ILM using the specifyIlm command and rerun flattenIlm again. Otherwise, flattenIlm will not run for a design that does not have any specified ILM.

Example:

restoreDesign . dtmf_recvr_core

setIlmMode -keepFlatten true

specifyIlm -cell tdsp_core -dir ../../PTM/tdsp_core/ilm

specifyIlm -cell ram_256x16_test -dir ../../PTM/ram_256x16_test/ilm

update_constraint_mode -name setup_func -ilm_sdc_files design/mmmc/dtmf_recvr_core_func.sdc

flattenIlm

IMPILM-281

NAME

IMPILM-281

SUMMARY

There is no netlist associated with the intended ILM specification for cell: %s

DESCRIPTION

This ERROR usually occurs during flattenIlm . The netlist of the specified ILM cell is not available for loading. Run reportIlmStatus to find out the data location of the specified ILM block and check if the netlist is available.

IMPILM-298

NAME

IMPILM-298

SUMMARY

The cell of %s is not specified for ILM. Nothing to do with unspecifyIlm.

DESCRIPTION

unspecifyIlm command outputs the warning message ECNILM-298 due to the specified cell is not an ILM. This command should only be used for unspecifying an existing ILM cell.

IMPILM-334

NAME

IMPILM-334

SUMMARY

Specified ILM %s has non-empty module definition; no ILM created for it.

DESCRIPTION

This error simply means that there is still a module for the ILM in the verilog netlist, which is not empty. There may be gates, or at least assign statements in it.Currently, in the ILM flow, we don't allow the ILM as non-empty module definitions during design import phase. Only empty module definitions are supported. To fix this error, user can remove the module definitions in the top level netlist to proceed. In other words modify the design data such that there is no non-empty ILM module in the top netlist.

IMPILM-349

NAME

IMPILM-349

SUMMARY

*Info: setIlmMode -keepAsync false conflicts with setAnalysisMode -asyncChecks async setting. setIlmMode -keepAsync false will be used in the ILM flow.

DESCRIPTION

setIlmMode -keepAsync setting will override the setAnalysisMode -asyncChecks setting if there is a conflict. The -kepAsync option of setIlmMode is set to false while the design already has the setAnalysisMode -asyncChecks async setting so the -keepAsync false setting will be used in the ILM flow instead. Set the -keepAsync option of setIlmMode to true if you want setAnalysisMode -asyncChecks async to be honored.

Example:

When there is si_ilm_data, if you run flattenIlm, it will issue this ERROR message.

IMPILM-350

NAME

IMPILM-350

SUMMARY

setIlmMode -keepAsync true conflicts with setAnalysisMode -asyncChecks noAsync setting. setIlmMode -keepAsync true will be used in the ILM flow.

DESCRIPTION

setIlmMode -keepAsync setting will override the setAnalysisMode -asyncChecks setting if there is a conflict.The -keepAsync option of setIlmMode is set to true while the design already has the setAnalysisMode -asyncChecks noAsync setting so the -keepAsync true setting will be used in the ILM flow instead. Set the -keepAsync option of setIlmMode to false if you want setAnalysis -asyncChecks noAsync to be honored.

IMPILM-365

NAME

IMPILM-365

SUMMARY

SI data will not be generated in this run since extraction needs to be done in postRoute mode. To enable SI data creation, invoke SI aware optimization and then rerun createInterfaceLogic.

DESCRIPTION

createInterfaceLogic will not generate SI data since extraction needs to be done in postRoute mode . You need to firstly enable SI aware delay calculation by "setDelayCalMode -SIAware true" , secondly make sure coupling is present and perform postroute timing analysis with "timeDesign -postRoute" , then SI data could be generated by createInterfaceLogic.

IMPILM-380

NAME

IMPILM-380

SUMMARY

Command '%s' is not supported in unflattened state. Use the 'flattenIlm' command to put the design in flattened state before calling this command.

DESCRIPTION

This error message is seen while using ILMs in toplevel without flattening ILMs and any timing and/or optimization commands are executed.

eg., **ERROR: (IMPILM-380): Command 'createClockTreeSpec' is not supported in unflattened state. Please use the 'flattenIlm' command to put the design in flattened state, before calling this command.

Here, the the user tried to execute the command "createClockTreeSpec" before flattening the ILMs. All super commands such as optDesign, timeDesign, clockDesign etc., automatically take care of flattening and upon completion, leave the design in an unflattened state.

All other timing/optimization commands require you to run flattenIlm first so that the nets and instances internal to ILM are exposed to the timing engine.

You can refer to the ILM usage details in Innovus System User Guide.

IMPILM-402

NAME

IMPILM-402

SUMMARY

Interactive constraint is allowed only in flattened state of design. Specified interactive constraint '%s' would be lost.

DESCRIPTION

Why does Innovus System issue the above error message when I enter interactive constraints such as set_timing_derate?

How can one avoid this error?

In general, for ILMs constraints are supported through create_constraint_mode / update_constraint_mode specified in your mmmc setup. You may refer to our Foundation Flow scripts for detailed information. If specified interactively, they could only be done so in flattened mode and would be discarded in unflattened mode. However, the best way to specify your constraints is upfront through the above MMMC constructs and binded to -ilm_sdc_file argument, and they would thus be read automatically in the flow. If there are constraints that you need to specify which could not be done in an SDC file (e.g. setTimingDerate, group_path), then you need to provide them through setIlmNonSdcConstraintFile <fileName>.

You cannot specify the interactive constraints when ILMs are not flattened (unflattenIlm).In the flatten mode (flattenIlm), you can specify both interactive and modeless constraints and these constraints are used during various cycles of unflattenIlm to flattenIlm. During saveDesign, these constraints are honored.

To specify additional constraints while running unflattenIlm, set the following:

set_global timing_defer_mmmc_object_updates true

set_interactive_constraint_modes [all_constraint_modes -active|or your_own_list_of_modes]

foreach mode {list_of_modes_to_be_updated} {update_constraint_modes -name $mode -ilm_sdc_files

[concat get_constraint_modes -name $mode -ilm_sdc_files] additional.sdc]

}

Include all modeless constraints such as timing_derates and group_path in a separate file, and run:

setIlmNonSdcConstraintFile <fileName>

IMPILM-537

NAME

IMPILM-537

SUMMARY

The command %s has become obsolete. It will be removed in the next release and replaced by import_ilm_data.

DESCRIPTION

To support MMMC analysis, import_ilm_data command is added to replace the existing createILMDataDir command. The createILMDataDir command will be removed in the next release so the import_ilm_data command should be used instead.

Example:

innovus> import_ilm_data -cell blk1 -dir A -model_type timing -verilog V1.v -spef 1ef -rc_corner corner1 -sdc sdcfiles -timing_view view1

IMPILM-548

NAME

IMPILM-548

SUMMARY

'%s' is not supported in flattened ILM state. Internally Innovus will unflatten the ILMs in the design and will flatten them back before exiting the command. To improve run time, unflattenIlm command should be called explicitly for a group of commands that do not work in flattened state.

DESCRIPTION

When -keepFlatten option of setIlmMode is set to true, for non-related timing commands Innovus will automatically unflatten the design, run the command, and flatten the design back. However it may take more run time if Innovus run unflattenIlm/flattenIlm for each non-related timing command. It is recommended that the user explicitly runs unflattenIlm for a group of commands that do not work in flattened mode to improve run time.

Example:

At top-level design, verify the design after the design has been optimized

...

...

timeDesign -signoff -reportOnly -outDir RPT

timeDesign -signoff -reportOnly -hold -outDir RPT

unflattenIlm

summaryReport -outDir RPT

verifyConnectivity -noAntenna

verify_drc

verifyMetalDensity

verifyProcessAntenna

IMPIMEX-1

NAME

IMPIMEX-1

SUMMARY

Failed to find target of link '%s' in given library directory '%s'.

DESCRIPTION

Check and correct the library path specified with \'-lib_dir\' option.

IMPIMEX-3

NAME

IMPIMEX-3

SUMMARY

There is no verilog netlist found in init_verilog. The variable is either not specified or specified incorrectly. Check the location of Verilog file in the global file.

DESCRIPTION

This issue can be resolved as one of the following scenarios:

1. Check the location of Verilog file; if you had created soft links, it might have been deleted.

2. When restoring a design, an error might have occurred in sourcing the design.globals file, check the log for this error:

This error indicates certain variables in the global file no longer exist or have been replaced with newer ones; this error prevents the rest of the globals file from being read, and hence the Verilog netlist cannot be accessed.

Update to a new EDI System version OR make sure you maintain a version consistency in saving and restoring designs.

IMPIO-1

NAME

IMPIO-1

SUMMARY

No active selection. Select one cell to shift up.

DESCRIPTION

{DETAIL_MESSAGE}

IMPIO-2

NAME

IMPIO-2

SUMMARY

Too many selections. Shift one cell at a time.

DESCRIPTION

{DETAIL_MESSAGE}

IMPIO-3

NAME

IMPIO-3

SUMMARY

Reached end of table. No more cell to swap.

DESCRIPTION

{DETAIL_MESSAGE}

IMPIO-4

NAME

IMPIO-4

SUMMARY

Cannot swap io cells from side to corner, or vice versa.

DESCRIPTION

{DETAIL_MESSAGE}

IMPLF-3

NAME

IMPLF-3

SUMMARY

Error found when processing LEF file '%s'. The subsequent file content is ignored. Refer to error messages above for details. Fix the errors, and restart '%s' again.

DESCRIPTION

If you have LEF syntax errors, you can look at the LEF manual to find the correct syntax. It can be accessed from the Innovus Help->Help Library... menu. Look under the Languages section for the latest LEF/DEF Language Reference Manual.

If there are semantic errors, check if you have the correct LEF technology file (the first file listed in the init_lef_file variable), or that you are not mistakenly including a LEF file with macros from some other technology node. You can also look at the manual for more information about specific statements.

IMPLF-27

NAME

IMPLF-27

SUMMARY

TAPERRULE '%s' referenced in pin '%s' in macro '%s' is not found in the database, and will be ignored. The rule must be defined in the LEF NONDEFAULTRULE section before it can be referenced from a macro. Review the LEF files to see if the rule does not exist or is specified after the one that defines the macro.

DESCRIPTION

TAPERRULE must be defined in the LEF NONDEFAULTRULE section before it can be referenced from a macro. The rule is either missing from the LEF files that were read or it was defined in a LEF that was specified after the one that contained the macro. Review the LEF files to see if the rule is defined and, if so, reorder the LEF files so that the LEF file that contains the rule is read before the one that contains the macro.

IMPLF-40

NAME

IMPLF-40

SUMMARY

Macro '%s' references a site '%s' that has not been defined. The sites must be defined before they can be referenced from a macro. Review the LEF files specified in the init_lef_file variable to see if the site does not exist or is specified after the one that defines the macro.

DESCRIPTION

This error reports that a macro references a site that has not been defined. The sites must be defined before they can be referenced from a macro. The site is either missing from the LEF files that were read or it was defined in a LEF that was specified after the one that contained the macro. Review the LEF files specified in the init_lef_file variable to see if the site is defined and, if so, reorder the LEF files in the init_lef_file variable so that the LEF file that contains the site is read before the one that contains the macro.

The following example shows the SITE CORE0 and CORE2 are defined but CORE1 is not defined and referenced by the MACRO PLL which will lead to this error message:

SITE CORE0

SYMMETRY Y ;

CLASS CORE ;

SIZE 0.045 BY 1.200 ;

END CORE0

SITE CORE2

SYMMETRY X Y ;

CLASS CORE ;

SIZE 0.045 BY 2.400 ;

END CORE2

MACRO PLL

SITE CORE1 ;

SYMMETRY X Y ;

...

IMPLF-53

NAME

IMPLF-53

SUMMARY

The layer '%s' referenced %s is not found in the database. A layer must be defined in the LEF technology LAYER section before it can be referenced from a macro. Review the LEF files specified in the init_lef_file variable to see if the layer does not exist or is specified after the one that defines the macro.

DESCRIPTION

This error reports that a macro PIN references a layer that has not been defined. The layer must be defined before they can be referenced from a macro. The layer is either missing from the LEF files that were read or it was defined in a LEF that was specified after the one that contained the macro. Review the LEF files specified in the init_lef_file variable to see if the layer is defined and, if so, reorder the LEF files in the init_lef_file variable so that the LEF file that contains the layer is read before the one that contains the macro.

IMPLF-58

NAME

IMPLF-58

SUMMARY

MACRO '%s' has been found in the database. Its content except DENSITY and PIN ANTENNA* data, and certain properties, will be ignored." "Review the LEF files specified in the init_lef_file variable and remove redundant definitions.

DESCRIPTION

This message reports that a MACRO has already been defined in another LEF file, or earlier in this LEF file. All MACROs must be defined only once in LEF files. The only exception is the DENSITY and PIN ANTENNA* data, and certain properties, which may be defined subsequently. If the data in both MACRO definitions is needed, manually merge the data into one definition.

Review the LEF files specified in the init_lef_file variable to see if a MACRO has been defined more than once, or if a LEF file has been mistakenly included more than once.

IMPLF-61

NAME

IMPLF-61

SUMMARY

%d duplicated MACRO definitions have been found in the LEF file(s). Their content except DENSITY and PIN ANTENNA* data, and certain properties, have been ignored." "Review the LEF files specified in the init_lef_file variable and remove redundant definitions.

DESCRIPTION

This message reports duplicated LEF MACRO definitions in the LEF file(s). If more than the default display limit of 20 has been reported, increase the display limit of warning message ENCLF-58 to see complete list of names.

All MACROs must be defined only once in LEF files. The only exception is the DENSITY and PIN ANTENNA* data, and certain properties, which may be defined subsequently. If the data in all MACRO definitions is needed, manually merge the data into one definition.

Review the LEF files specified in the init_lef_file variable to see if a MACRO has been defined more than once, or if a LEF file has been mistakenly included more than once.

IMPLF-63

NAME

IMPLF-63

SUMMARY

The layer '%s' referenced %s is not found in the database. The obstruction geometries specified on the layer are being ignored. A layer must be defined in the LEF technology LAYER section before it can be referenced from a macro. Review the LEF files specified in the init_lef_file variable to see if the layer does not exist or is specified after the one that defines the macro.

DESCRIPTION

This error reports that a macro OBS references a layer that has not been defined. The layer must be defined before they can be referenced from a macro. The layer is either missing from the LEF files that were read or it was defined in a LEF that was specified after the one that contained the macro. Review the LEF files specified in the init_lef_file variable to see if the layer is defined and, if so, reorder the LEF files in the init_lef_file variable so that the LEF file that contains the layer is read before the one that contains the macro.

IMPLF-80

NAME

IMPLF-80

SUMMARY

%s is not an even number of manufacturing grids which will result in DRC errors. Check the manufacturing grid definition in the technology LEF file and make sure the value is an even multiple of the grid.

DESCRIPTION

When reading LEF Innovus System will check that WIDTH value on routing layer is an even number of manufacturing grids defined in the technology LEF file (MANUFACTURINGGRID). This will ensure that both the edge and the center-line of the wires will stay on the manufacturing grid.

Look for the following line in the LEF file to determine how many database units is 1 micron (dbuPerMicron):

UNITS DATABASE MICRONS dbuPerMicron ;

To check if your dbu's have enough granularity, multiply dbuPerMicron * manufaturingGrid. The result should be an integer quantity that is evenly divisible by two to ensure the center-line is on grid.

For example, if MANUFACTURINGGRID is 0.005, this is only achievable with a DBU of 2000.

- (1000*0.005)/2 = 2.5, (not evenly divisible by two), the result could be off manufacturing grid.
- (2000*0.005)/2 = 5, (evenly divisible by two), the result will be on manufacturing grid.

Or to say it another way:

If dbuPerMicron * manufacturingGrid is an odd number (e.g. 1000*0.005 = 5), you cannot create a path (center-line based) that has a width that is an odd number of manufacturing grids wide.

IMPLF-119

NAME

IMPLF-119

SUMMARY

LAYER '%s' has been found in the database. Its content%s will be ignored." "Review the LEF files specified in the init_lef_file variable and remove redundant definitions.

DESCRIPTION

This message reports that a LAYER has already been defined in another LEF file, or earlier in this LEF file. All LAYERs must be defined only once in the technology LEF file (the first LEF file defined in the init_lef_file variable). The only exception is the ANTENNA* data which may be defined in subsequent LEF files.

Review the LEF files specified in the init_lef_file variable to see if a LAYER has been defined more than once, or if a LEF file has been mistakenly included more than once.

If the data in both LAYER definitions is needed, manually merge the data into one definition.

IMPLF-200

NAME

IMPLF-200

SUMMARY

Pin '%s' in macro '%s' has no ANTENNAGATEAREA value defined. The library data is incomplete and some process antenna rules will not be checked correctly.

DESCRIPTION

This warning is triggered when the technology data has process antenna rules, and a signal pin is missing process antenna data needed to check the rules. In this case, a signal pin that is either an input or inout pin is missing the gate-area data.

In CMOS, every signal pin that is an input or inout pin connects to a transistor gate. If there is no gate-area associated with this pin, then the library data is incomplete and process antenna rules cannot be checked for this pin correctly. The router and verification commands will assume this pin has no transistor gate attached, and therefore does not need to be protected from process antenna violations, which may result in real violations that are not fixed by the router or seen by the verification commands.

The best way to avoid this warning is to add the correct antenna gate-area data to the library data.

You can also use the suppressMessage command to turn off this warning message. This might be appropriate if you know the only library cells without antenna data are already protected by internal diode cells (e.g. some blocks might be built this way). In that case, you would lose the possible benefit of those internal diode cells for any nets connected to the block input, which might cause the router to add some unnecessary diode cells to protect other inputs attached to the same net. This is somewhat dangerous, because you might suppress messages for pins that are not protected.

You can also turn off the warning if you believe antenna errors are rare for these pins in practice, and you will depend on final sign-off physical verification tools to find any errors, and repair them

manually.

The following example shows the definition of antenna gate area in a LEF PIN statement:

```
MACRO AND2
CLASS CORE;
SIZE 0.90 BY 1.114 ;
SYMETRY X Y ;
SITE CORE ;
PIN A1
DIRECTION INPUT ;
ANTENNAGATEAREA 0.002320 ; #antenna gate area in um^2
PORT
LAYER M1 ;
RECT 0.188 0.196 0.234 0.426 ;
END
END A1
...

END AND2
```

IMPLF-201

NAME

IMPLF-201

SUMMARY

Pin '%s' in macro '%s' has no ANTENNADIFFAREA value defined. The library data is incomplete and some process antenna rules will not be checked correctly.

DESCRIPTION

This warning is triggered when the technology data has process antenna rules, and a signal pin is missing process antenna data needed to check the rules. In this case, a signal pin that is either an output or inout pin is missing the diffusion-area data.

In CMOS, every signal pin that is an output or inout pin connects to a transistor diffusion. If there is no diffusion-area associated with this pin, then the library data is incomplete and process antenna rules cannot be checked for this pin correctly. In that case, the router may try to protect other input pins connected to the same net with extra routing and vias ('layer-hopping'), or add extra diode cells to avoid 'false' antenna violations. The verification commands may flag false violations also.

The best way to avoid this warning is to add the correct antenna diffusion-area data to the library data.

You can also use the suppressMessage command to turn off this warning message. This might be appropriate if you know that antenna violations are rare in this technology, and you are willing to tolerate some extra layer-hopping, or extra diode cells that are not really necessary.

The following example shows the definition of antenna gate area in a LEF PIN statement:

```
MACRO AND2
CLASS CORE;
SIZE 0.90 BY 1.114 ;
SYMETRY X Y ;
SITE CORE ;
PIN A1
```

```
DIRECTION INPUT ;
ANTENNADIFFAREA 0.008320 ; #antenna diff area in um^2
PORT
LAYER M1 ;
RECT 0.188 0.196 0.234 0.426 ;
END
END A1
...

END AND2
```

IMPLF-223

NAME

IMPLF-223

SUMMARY

The LEF via '%s' has been defined and found in the database. The current definition will be ignored. Review the LEF files to ensure that you have not specified duplicate LEF files, or LEF files with duplicate VIA definitions.

DESCRIPTION

This error reports that a LEF via is defined with the same name as a LEF via that has been previously defined and read into the database. The new definition is therefore ignored. The via name can not be the same if the via geometry is different. Make sure different via definitions have different via names. Otherwise, it may cause incorrect and undesired result. Review the LEF files to ensure that you have not specified duplicate LEF files, or LEF files with duplicate VIA definitions.

IMPLF-345

NAME

IMPLF-345

SUMMARY

The EXACTWIDTH attribute is specified in ENDOFLINE" "phrase in SPACING statement in layer '%s'. This attribute is intended to" "be used with WIDTHTABLE or SPANLENGTHTABLE but there is no WIDTHTABLE nor" "SPANLENGTHTABLE statement defined in this layer. Make sure this rule is" "specified as intended.

DESCRIPTION

This is to specify that this end-of-line spacing rule only applies if the edge width/length is exactly equal to eolWidth. This construct would typically make sense only if WIDTHTABLE or SPANLENGTHTABLE is also defined on the layer, and the end-of-line spacing rule will only be triggered for one of the discrete widths.

Example:

PROPERTY LEF58_WIDTHTABLE

"WIDTHTABLE 0.05 0.10 0.15 ;" ;

SPACING 0.09 ENDOFLINE 0.051 WITHIN 0.02 ;

PROPERTY LEF58_SPACING

"SPACING 0.07 ENDOFLINE 0.10 EXACTWIDTH WITHIN 0.04 ;" ;

IMPMP-1001

NAME

IMPMP-1001

SUMMARY

Invalid factor value '%s' for module '%s', and will be ignored during placement. Usage: -modulePadding <modulename> <factor>

DESCRIPTION

This warning message is issued while running placeDesign command if there are some issues with '-modulePadding' option of setPlacemode command.

Example:

Module padding is a means of reducing localized congestion (hotspots) by spreading out cell instances in the specified modules. The correct usage of the command is as below

setPlaceMode -modulePadding <modulename> <factor>

setPlaceMode -modulePadding <modulename> <factor>

A factor of 1.2 means the placer will increases the area of module A factor of 1.2 means the placer will increases the area of module and default value is 1.0.

IMPMSMV-1006

NAME

IMPMSMV-1006

SUMMARY

The number of areas exceed %d.

DESCRIPTION

he error message usually happens when setNanoRouteMode -routeHonorPowerDomain is true while the # of power domains and minGap areas exceed 64. Nanoroute will not honor some of the domains. Since the above mode is a soft constraint, you can ignore it if your design has more than 64 domains and mingaps.

Example:

**ERROR: (IMPMSMV-1006): Number of areas exceed 64

IMPMSMV-1007

NAME

IMPMSMV-1007

SUMMARY

The default power domain is not defined. Check the CPF file and make sure default power domain is created with -default option.

DESCRIPTION

Default power domain must be defined in the power intent file. When restoring an old DB saved without CPF by previous Innovus release, please prepare a CPF file correctly describing your power intent. Then use read_power_intent -cpf and commit_power_intent to load it into Innovus.

IMPMSMV-1015

NAME

IMPMSMV-1015

SUMMARY

The cell %s is defined in power intent file but is not defined in library or lef. Check the LEF and timing library files to make sure the cell's library is loaded.

DESCRIPTION

Cells defined in power intent file by 'define_*_cell' command must have their LEF and timing library loaded into Innovus.

Example:

**WARN: (IMPMSMV-1015): The cell SRDFFX1 is defined in power intent

file but is not defined in library or lef.

IMPMSMV-1051

NAME

IMPMSMV-1051

SUMMARY

AOB cell type different along the signal path instance %s(cell:%s) drives instance %s(cell:%).

DESCRIPTION

Both AOB and its driver cell should have same number of bia pin and connected to same bias net.

IMPMSMV-1052

NAME

IMPMSMV-1052

SUMMARY

AOB instance %s(cell:%s) has bias pin while its driver %s(cell:%s) has not.

DESCRIPTION

The AOB instance has bia pin connection, so its driver should have bias pin connected to same net or driver's location domain shouold have PMOS/NMOS bias pin specified.

IMPMSMV-1053

NAME

IMPMSMV-1053

SUMMARY

AO inst %s has cell type %s, doesn't match the best type (%s) for Domain %s.

DESCRIPTION

With share well AO buffering, each domain has its best fit AO type according to user defined power intent.

This message states that a non-best fit AO type is found in the netlist.

IMPMSMV-1054

NAME

IMPMSMV-1054

SUMMARY

inst %s is AO type %s, because its AO power net %s is no covered by domain nwell net %s.

DESCRIPTION

It is found that this AO instance fails on power net coverage requirement.

Location domain's nwell net must cover (more on) instance AO power net.

IMPMSMV-1116

NAME

IMPMSMV-1116

SUMMARY

Failed to create powerDomain '%s', because the powerDomain name conflicts with the hinst name.

DESCRIPTION

The name of the power domain cannot be the same as its member hinst.

For example, this is wrong:

create_power_domain -name TDSP_CORE_INST -instances TDSP_CORE_INST

and this is fine:

create_power_domain -name TDSPCore -instances TDSP_CORE_INST

Example:

**ERROR: (IMPMSMV-1116): Failed to create powerDomain 'TDSP_CORE_INST',

because the powerDomain name conflicts with the hinst name.

IMPMSMV-1123

NAME

IMPMSMV-1123

SUMMARY

(H)Inst '%s' belongs to instGroups '%s', it cannot be assigned to any power domain.

DESCRIPTION

Any domain's direct member cannot be a member of any other inst group.

If you have list this (H)Inst in power intent domain element list, it is a direct member.

User needs to resolve this before read/commit power intent by deleting such inst group.

IMPMSMV-1211

NAME

IMPMSMV-1211

SUMMARY

The pg term %s of inst %s is not connected to any net. Use reportPowerDomain -inst to check its driver and receiver and pg connection information.

DESCRIPTION

The pg terms of instances are connected according to the power intent file: CPF or IEEE1801. There are implicit connection and explicit connection. Most of the pg connections are done implicitly. Such as connecting the primary power/ground pin of a standard cell to its power domain's primary power/ground net. Or connecting always-on buffer's secondary power pin to its driving instance's power pin. Or connecting level shifter's input and output power pin according to its

driving and receiving power domain. As long as the power domain, primary pg net and iso/shifter rules are properly defined in the power intent file,Innovus can derive the pg connection automatically. Explicit pg connection are necessary when there is no way for the tool to derive connection from the power intent file. For example, the pg pins of an analog block. In this case,user needs to add explicit pg connection, such as 'create_global_connection'command.

Example:

**WARN: (IMPMSMV-1211): The pg term BIASNW of inst UPF_ISO__0_out is not connected to any net.

IMPMSMV-1212

NAME

IMPMSMV-1212

SUMMARY

The gnd term %s of inst %s is connected to WRONG net - %s. According to the instance power domain PG connection specification defined in CPF or IEEE1801,it should be connected to net - %s.

DESCRIPTION

In CPF or IEEE1801 flow, most of the PG connection specification is automatically derived from instance's relationship with power domain and rules.

IMPMSMV-1213

NAME

IMPMSMV-1213

SUMMARY

The pwr term %s of inst %s is connected to WRONG net - %s. According to the instance power domain PG connection specification defined in CPF or IEEE1801,it should be connected to net - %s.

DESCRIPTION

In CPF or IEEE1801 flow, most of the PG connection specification is automatically derived from instance's relationship with power domain and rules.

IMPMSMV-1215

NAME

IMPMSMV-1215

SUMMARY

The tielo term %s of inst %s is connected to WRONG net - %s. Check the inst's PG connection and the term's related PG pin using reportPowerDomain -inst command.

DESCRIPTION

Basically an instance's tie-off term should be connected based on the term's related PG pin and the net this PG pin is connected to.

For example:

For example:

For regular cell, tie-off term should be connected to its primary PG net.

For example:

For always-on cell, tie-off term should be connected its secondary PG net.

For example:

For level shifer cell, tie-off term should be connected to its input power net.

For example:

For hard macro, check the term's related pg attribute in *.lib to decide.

IMPMSMV-1219

NAME

IMPMSMV-1219

SUMMARY

The AOB inst %s in domain %s has its P/G terms connected to P/G nets (pwr:%s, gnd:%s) of disabled domain %s.

DESCRIPTION

The AOB instance is in a domain which has attribute 'disbale_secondary_domain' to disallow AOB in it to connect 2nd P/G pins to primary P/G nets of disbaled domains.

IMPMSMV-1226

NAME

IMPMSMV-1226

SUMMARY

AO inst (%s) is used in domain %s by shorting primary and secondary power term.

DESCRIPTION

The message exists after CMD verifypowerdomain means that there is always on buffer used in the design and its primary and secondary power is connected to the same supply power net.

The issue maybe caused by wrong behavior of Innovus if the buffer is added by GPS, always on buffer is used as regular buffer. Or the AON buffer is added for some design purpose by designer.

User can replace the AOB by a regular buffer to save area, and file a CCR against this issue if it is not added for any particular purpose.

Example:

<CMD> verifypowerdomain -bind -isoNetPD ./RPT/prects.isonets.rpt -xNetPD ./RPT/prects.xnets.rpt -gconn

Verifying P/G connection of power domain - 'PD_AON_LOGIC'.

Verifying P/G connection of power domain - 'PD_ON_OFF'.

**WARN: (IMPMSMV-1226): AO inst (usb30_core/u_onoff_top/u_pib_top/prects_i_FE_OFC9162_partial_rst_no) is used in domain PD_ON_OFF by shorting primary and secondary power term.

IMPMSMV-1243

NAME

IMPMSMV-1243

SUMMARY

Default powerDomain doesn't need minGap, option -minGaps is ignored.

DESCRIPTION

Unlike non default power domains, the default power domain does not need a fence constraint specified for it. The default power domain covers all the remaining core area except th non-default domain fences.

IMPMSMV-1245

NAME

IMPMSMV-1245

SUMMARY

Default powerDomain doesn't need routeSearchExtension, option -rsExts is ignored in modifypowerdomainattr command.

DESCRIPTION

The default power domain doesn't have a fence constraint specified for it, hence routeSearchExtension is meaningless in this case.

IMPMSMV-1246

NAME

IMPMSMV-1246

SUMMARY

Cannot modify default power domain rowFlip, option -rowFlip is ignored in modifypowerdomainattr command.

DESCRIPTION

The default power domain doesn't have a fence constraint specified for it, please use 'floorplan' or 'createRow' commands to change default domain row attributes.

IMPMSMV-1247

NAME

IMPMSMV-1247

SUMMARY

Cannot modify default power domain rowSpaceType, -rowSpaceType option is ignored in modifypowerdomainattr.

DESCRIPTION

Unlike non default power domains, the default power domain cannot have a fence constraint specified for it; please use 'setFPlanRowSpacingAndType' or'createRow' commands to change default domain row spacing attributes.

IMPMSMV-1248

NAME

IMPMSMV-1248

SUMMARY

Cannot modify default power domain rowSpacing, -rowSpacing option is ignored in modifypowerdomainattr.

DESCRIPTION

Unlike non default power domains, the default power domain cannot have a fence constraint with dedicated rows specified for it; please use 'setFPlanRowSpacingAndType' or 'createRow' commands to change default domain row spacing attributes.

IMPMSMV-1249

NAME

IMPMSMV-1249

SUMMARY

Cannot modify default power domain bbox, ignores -box option.

DESCRIPTION

This message happens when 'modifypowerdomainattr -box' is used on a default power domain. Only non-default power domain is allowed to change the bounding box by -box option.

Example:

<CMD> modifypowerdomainattr PD1 -box 0 0 100 100

**WARN: (IMPMSMV-1249): Cannot modify default power domain bbox, ignores -box option.

IMPMSMV-1264

NAME

IMPMSMV-1264

SUMMARY

minGap 0 set for powerDomain '%s' edge %d.

DESCRIPTION

Be cautious setting min gap zero for power domain, which might cause power shortage in the flow.

Designer must make sure power separation is done correctly.

IMPMSMV-1267

NAME

IMPMSMV-1267

SUMMARY

Option '%s' needs %d values in {...} and match domain's number of edges.

DESCRIPTION

The problem could be that user is not putting all edge values in {}, or

the number of values doesn't match number of edge of the domain.

Please check option -help for command synatx.

IMPMSMV-1314

NAME

IMPMSMV-1314

SUMMARY

Cannot find cell '%s'. Check the LEF and timing library files to make sure the cell's library is loaded.

DESCRIPTION

Cells defined in the CPF by 'define_*_cell' command must have its LEF and timing library loaded into Innovus.

Example:

**WARN: (IMPMSMV-1314): Cannot find cell 'SRDFFX1'.

IMPMSMV-1315

NAME

IMPMSMV-1315

SUMMARY

Cell %s is a standard cell. The cell for ioPin (-boundary_port) cannot be a standard cell.

DESCRIPTION

IMPMSMV-1315 is issued when users try to assign standard cell's IO pins' power

domain through CPF create_power_domain -boundary_ports.

Please check if the cell is defined as standard cell (CLASS CORE) in LEF.

Example:

Pad cell for A_1/IO1 is defined as following:

cell(PAD_CELL) {

sec_external_voltage_type : voltage_07001800 ;

dont_use : true;

dont_touch : true;

sec_class : pad;

sec_cell_type : ringcell;

"sec_class : pad;" is not standard pad cell declaration.

Liberty Guide uses pad_cell : true;

IMPMSMV-1501

NAME

IMPMSMV-1501

SUMMARY

No connection specification for shifter '%s' in power domain '%s'. \Power/Ground terms are not connected.

DESCRIPTION

During commit_power_intent the above message is reported because it can not connection the shifter PG pins. One of the reason is that the shifter is float and commit_power_intent can not make its non-follow-pin PG connection.

Example:

To specify the power and ground connections for the power domain add something like the following to the CPF:

create_power_nets -nets VDD -voltage 1.080

create_ground_nets -nets VSS -voltage 0.000

update_power_domain -name AO -primary_power_net VDD -primary_ground_net VSS

IMPMSMV-1504

NAME

IMPMSMV-1504

SUMMARY

Failed to get pin '%s' for cell '%s'.

DESCRIPTION

Please check if the pin is defined in LEF file for the cell.

A possible reason is the cell pin is defined in timing library but

not defined in LEF file.

IMPMSMV-1531

NAME

IMPMSMV-1531

SUMMARY

Failed to get power and ground connection specification for powerDomain '%s' instance '%s' (Cell:%s, Pwr:%s, Gnd:%s). Use reportPowerDomain -inst to check if its PG connection information is implicitly or explicitly defined in CPF or IEEE1801.

DESCRIPTION

The message normally happens on the Nwell/Pwell pin connections. Those Nwell/Pwell connections should be defined in CPF or IEEE1801.

IMPMSMV-1592

NAME

IMPMSMV-1592

SUMMARY

No default tech site found for power domain '%s'. Power domain must be empty (no standard cells, and I/O cells).

DESCRIPTION

This warning is issued when a virtual power domain is defined in the CPF i.e a power domain is created without -instances and -default options (create_power_domain -name VDDAR_virtual)
Example:

Below example shows a Power domain created without -instances and -default options in CPF. Innovus issues this warning when CPF contains below definition.
create_power_domain -name VDDAR_virtual
**WARN: (IMPMSMV-1592): No default tech site found for power domain 'VDDAR_virtual'. Power domain must be empty (no standard cells, and I/O cells).
Check if PowerDomain contains any stdcells :
> llength [dbget -e [dbget -e top.insts.pd.name VDDAR_virtual -p2].cell.subClass core]
If the powerdomain is not empty make sure visually that it's fence is placed inside the DIE area and rows are cut inside its fence for the site to which its stdcells belong to .

IMPMSMV-1595

NAME

IMPMSMV-1595

SUMMARY

Failed to find spare instance for cell:%s from spare list in PostMask ECO mode.

DESCRIPTION

This error indicates that the command tried to find a spare component

to use, but failed to find a proper one.

This happens if there is no more spare one, or the applicable ones

are not specified with ecoDesign command.

Please check ecoDesign command -spareCell option to make sure

spare cell are provided correctly.

IMPMSMV-1636

NAME

IMPMSMV-1636

SUMMARY

No library found for level shifter cell '%s' with input '%f' and output '%f' volts, placed in power domain '%s'. The first available library cell of the same name will be used, irrespective of input and output voltages.

DESCRIPTION

Why is this message issued during timing analysis?

Following are excerpts from the library showing a level shifter and associated

pins and their voltage. If a level shifter with the appropriate voltages is not

found the error above will be issued.

At the top of the file the voltage levels are defined using voltage_map

statements:

voltage_map (VDD, 1.08);

voltage_map (ExtVDD, 0.9);

voltage_map (VSS, 0);

voltage_map (GND, 0);

voltage_map (ExtVSS, 0);

Example:

Within the cell definition define power pins and respective voltage names

within a pg_pin statement:

cell (LSHLX1_FROM) {

is_level_shifter : "true";

level_shifter_type : "HL";

area : 0;

pg_pin (VSS) {

pg_type : primary_ground;

voltage_name : "VSS";

}

pg_pin (VDD) {

pg_type : primary_power;

std_cell_main_rail : true;

voltage_name : "VDD";

}

pg_pin (ExtVDD) {

pg_type : backup_power;

voltage_name : "ExtVDD";

}

Lastly, define the signal_level and related power and ground pins for the input

and output pins:

pin (Y) {

output_signal_level : ExtVDD;

direction : output;

function : "A";

related_ground_pin : VSS;

related_power_pin : ExtVDD;

pin (A) {

input_signal_level : VDD;

direction : input;

related_ground_pin : VSS;

related_power_pin : VDD;

IMPMSMV-1780

NAME

IMPMSMV-1780

SUMMARY

Power net '%s' is not specified in command line.

DESCRIPTION

This message is issued when the power net present in the design but not specified with command "set_lib_binding_by_voltage -power_net_voltages". To fix the issue, all power nets present in the design must be specified with command "set_lib_binding_by_voltage".

IMPMSMV-1781

NAME

IMPMSMV-1781

SUMMARY

Cannot find net '%s' in design, skip it.

DESCRIPTION

This message is issued when power net specified in the command "set_lib_binding_by_voltage -power_net_voltages" is not present in the design. The net will be ignored. To fix the issue, specify the correct power net.

IMPMSMV-1783

NAME

IMPMSMV-1783

SUMMARY

Cannot find a matching library for inst %s (cell %s), use library %s.

DESCRIPTION

This message is issued when session does not have any library with the pg pin voltage that matches with the power net voltage specified in command "set_lib_binding_by_voltage -power_net_voltages". In such case, software binds the instance to available library. This may impact analysis accuracy. To fix the issue, load the libraies with matching power net voltages.

IMPMSMV-1792

NAME

IMPMSMV-1792

SUMMARY

Power domain is not created for pg net %s because it is not connected to any standard cell's primary/backup/internal pg_pin The voltage might not be assigned correctly because it is not associated with a power domain.

DESCRIPTION

This message is issued when there is an unconnected pg net in design. There will not be any power domain creation corresponding to such pg net. The voltage might not be assigned correctly because it is not associated with a power domain. To fix the issue, specify the voltage for such pg net(s) explicitly in set_lib_binding_by_voltage command.

IMPMSMV-1798

NAME

IMPMSMV-1798

SUMMARY

Power net '%s' is not specified in -pg_net_voltages of create_delay_corner or update_delay_corner.

DESCRIPTION

This message is issued when the power net present in the design but not specified with -power_net_voltages option of create_delay_corner or update_delay_corner. To fix the issue, all power nets used in the design must be specified.

IMPMSMV-1800

NAME

IMPMSMV-1800

SUMMARY

Pin '%s' of multi-supply cell '%s' (%s) does not have related_power_pin attribute.

DESCRIPTION

Signal pin in multi-supply cell should have related_power_pin attribute so correct power supply can be determined.

IMPMSMV-1801

NAME

IMPMSMV-1801

SUMMARY

The power or ground pin, '%s' (pg_type '%s') of cell '%s' (instance '%s') is not connected to power or ground net. Please fix the Verilog file by connecting this pin to a power or ground net.

DESCRIPTION

pg_pin should be connected to have correct voltage.

IMPMSMV-1802

NAME

IMPMSMV-1802

SUMMARY

Voltage of term '%s', %gv, does not match the voltage of multi-driver net '%s', %gv.

DESCRIPTION

Please check all the inputs of multi-dirver net to make sure they have the same related power supply and voltage.

IMPMSMV-1804

NAME

IMPMSMV-1804

SUMMARY

Cell '%s' does not have timing library defined in default library set of analysis view '%s'.

DESCRIPTION

This message is issued when the cell is used in the design but its corresponding timing library is not present. To fix the issue, timing library corresponding to each cell must be loaded.

If the cell is physical only, the message can be ignored.

If timing is needed, please add a library containing the missing cell and restart the run, or update the library set using update_library_set.

IMPMSMV-1805

NAME

IMPMSMV-1805

SUMMARY

Pin '%s' of inst '%s' (cell %s) does not have related_power_pin attribute, voltage %g is assigned.

DESCRIPTION

Signal pin in multi-supply cell should have related_power_pin attribute so correct power supply can be determined.

IMPMSMV-1806

NAME

IMPMSMV-1806

SUMMARY

Pin '%s' of inst '%s' (cell %s) is related to internal_power_pin %s which does not have pg_function attribute, voltage %g is assigned.

DESCRIPTION

Signal pin in multi-supply cell should have related_power_pin attribute so correct power supply can be determined.

IMPMSMV-1820

NAME

IMPMSMV-1820

SUMMARY

Detected design has ILM(s) and is in unflattened state, read/commit power intent must run after flettenIlm.

DESCRIPTION

The correct flow for design with ILM is to flatten all ILMs then read/commit power intent, this chip level

power intent contains information covering inside ILM netlist. Fail to follow the recommended flow might

induce down stream design issue.

IMPMSMV-3101

NAME

IMPMSMV-3101

SUMMARY

replaceWithAlwaysOnBuffer: No always-on buffer specified in CPF. Make sure always-on buffers are defined properly in the CPF and they are not set dont_use. Use 'dbGet' comamnd to check and 'setDontUse' to change setting.

DESCRIPTION

In assign scenario, after commit_power_intent, regular feed though assign buffer in off domain will be replaced by always on buffer(when turn on do assign in case).But if there is no always on buffer defined by define_always_on_cell in CPF file, or the always on cell has dont_use attribute in lib or in tcl file, above ERROR will exist.

Example:

(1) In below CPF file, all define_always_on_cell attribute is commented and "setMsvMode -useLibraryLowPowerCell false", WARN(IMPMSMV-3101) will exist after commit_power_intent.

#define_always_on_cell -cells { GPGBUF_X8M_A9TH } -power_switchable VDD -power VDDG -ground_switchable VSS -ground VSSG

(2) In below case tcl, if only one always on buffer exist in design, after "setDontUse GPGBUF_X8M_A9TH true", WARN(IMPMSMV-3101) will exist after commit_power_intent.

setDontUse GPGBUF_X8M_A9TH true

read_power_intent -cpf top.cpf

commit_power_intent -verbose

IMPMSMV-3502

NAME

IMPMSMV-3502

SUMMARY

Power net %s is not associated with any power domain. It is probably because this power net is not specified as any domain's primary power net. You need to modify CPF to create a virtual power domain using 'create_power_domain' without -instances and -default options then specify this power net as its primary power net using 'update_power_domain'.

DESCRIPTION

This warning is issued when a power net is defined in CPF by "create_power_nets -nets < >" and is not associated with any power domain by "update_power_domain -primary_power_net".

When you see this warning, Please check CPF file to see if all of power nets are associated with power domain.

Example:

User need to modify CPF file to create a virtual power domain using "create_power_domain" without -instances and -default options then specify this power net as its primary power net using "update_power_domain".

create_power_nets -nets vddar2 -voltage 1.2

update_power_domain -name VDDAR_virthttp -primary_power_net vddar2

IMPMSMV-3700

NAME

IMPMSMV-3700

SUMMARY

Isolation instance %s input is tied to power/ground.

DESCRIPTION

The message exist after CMD verifypowerdomain and means that there input of some isolation instance ties to power/ground.

This kind of isolation always added by other tool not Innovus for particular purpose. (Cross domain tie high/low)

User should get to know the usage of this kind of isolation and check if its power connection is right.

Example:

<CMD> verifypowerdomain -isoNetPD

... ...

**WARN: (IMPMSMV-3700): Isolation instance CPF_ISO_out1 input is tied to power/ground.

**WARN: (IMPMSMV-3700): Isolation instance CPF_ISO_out1 input is tied to power/ground.

In the design, CPF_ISO_out1's input is connected directly to power.

IMPMSMV-3701

NAME

IMPMSMV-3701

SUMMARY

Isolation instance %s input and output are of the same power domain %s. Please make sure that the isolation driver and receivers are in different domains. Use reportPowerDomain -inst to check its driver and receiver connections.

DESCRIPTION

Effective power domain of input and output of the specified isolation instance is the same.

Most Likely Cause:

(1) Redundant isolation is added

(2) Isolation cell's power connection changed

(3) In IEEE1801 flow, it may caused by not detailed isolation strategy (no -source/-sink)

What to Do Next:

(1) If the isolation is redundant, user can eco delete the isolation as workaround and file CCR against the issue

(2) Use globalNetConnect to change the connection as workaround and file CCR against the issue

(3) Complete isolation strategy in 1801 file

IMPMSMV-3910

NAME

IMPMSMV-3910

SUMMARY

Creating new supply port %s for module %s to connect supply net %s, this will cause inconsistency on physical netlist and power intent. check message help for detail.

DESCRIPTION

A new P/G port is added for a supply net to go into a module. This is most likely to connect new buffers added by application.

This will cause inconsistency of physical netlist and power intent which defines all P/G connection of a design.

Do either of following steps will prevent new port being created during the design process.

For hierarchical power intent, user should define supply ports for all connecting nets of a scope, and connect all of them

with connect_supply_net -ports.

To prevent a P/G net being used to connect into a scope, user should utilize extra_supplies option to control P/G connection.

IMPMSMV-3920

NAME

IMPMSMV-3920

SUMMARY

Failed to connect net %s into instance in ILM module %s, because no existing PG port to connect.

DESCRIPTION

The connection cannot be done, because ILM moduel cannot be modified.

User needs to check netlist of ILM instance, or P/G connection spec. in power intent.

IMPMSMV-4001

NAME

IMPMSMV-4001

SUMMARY

The '-fromPowerDomain' option is obsolete. Please use '-from' instead.

DESCRIPTION

The option '-fromPowerDomain' of reportIsolation and reportShifter is obsolete and has been replaced by '-from'. The obsolete option still works in this release but to avoid this warning and to ensure compatibility with future releases, update your script to use '-from'

Example:

<CMD> reportIsolation -fromPowerDomain PDtdsp

**WARN: (IMPMSMV-4001): The '-fromPowerDomain' option is obsolete. Please use '-from'

instead.

INFO: Isolation instances will be reported to file dtmf_chip.isolation.rpt.

INFO: 102 isolation instances reported.

IMPMSMV-4002

NAME

IMPMSMV-4002

SUMMARY

The '-toPowerDomain' option is obsolete. Please use '-to' instead.

DESCRIPTION

The option '-toPowerDomain' of reportIsolation and reportShifter is obsolete and has been replaced by '-to'. The obsolete option still works in this release but to avoid this warning and to ensure compatibility with future releases, update your script to use '-to'

Example:

<CMD> reportIsolation -toPowerDomain PDtdsp

**WARN: (IMPMSMV-4002): The '-toPowerDomain' option is obsolete. Please use '-to' instead.

INFO: Isolation instances will be reported to file dtmf_chip.isolation.rpt.

INFO: 32 isolation instances reported.

IMPMSMV-4100

NAME

IMPMSMV-4100

SUMMARY

Domain member (%s -> %s) is not inside specified domain %s

DESCRIPTION

The named domain member is not inside logical hierarchy of any member of specified parent domain.

This feature requires all domains and its members must be under same logical hierarchy of the specified parent domain.

IMPMSMV-4110

NAME

IMPMSMV-4110

SUMMARY

P/G nets are different, physical Domain %s has P/G nets (%s, %s), but domain %s has (%s, %s)

DESCRIPTION

All logical domains must have same P/G nets as its parent physical domain.

Please reset marking with mark_physical_power_domains commands.

IMPMSMV-4111

NAME

IMPMSMV-4111

SUMMARY

N/Pwell nets are different, physical Domain %s has N/Pwell nets (%s, %s), but domain %s has (%s, %s)

DESCRIPTION

All logical domains must have same Pwell/Nwell nets as its parent physical domain.

Please reset marking with mark_physical_power_domains commands.

IMPMSMV-4112

NAME

IMPMSMV-4112

SUMMARY

Failed to find domain to share fence for domain %s, power (%s), ground (%s)

DESCRIPTION

User should check if mamrked physical domain cover all logical domains.

Innovus will search higher hierarchy for physical domain from logical domain level.

IMPMSMV-4113

NAME

IMPMSMV-4113

SUMMARY

Available supplies are different, physical PD %s, logical PD %s

DESCRIPTION

All domains share same fence must have same available supplies.

Check input power intent, or report of power domains.

IMPMSMV-4115

NAME

IMPMSMV-4115

SUMMARY

Found domain (%s) has P/G nets (%s,%s) which are different from previous set (%s,%s).

DESCRIPTION

There are at least one domain has different P/G nets with others in the input domain list.

it is required that all domains to share fence or to be merged have same P/G nets defined.

IMPMSMV-4120

NAME

IMPMSMV-4120

SUMMARY

Domain::Hinst (%s::%s) and (%s::%s) violates paren/child restriction.

DESCRIPTION

To merge physical power domains, all domains must not in parent/child logical hierarchy from its members.

Review and update domains list in command line.

Use -domains for domains which have parent/child hierarchy members.

IMPMSMV-4200

NAME

IMPMSMV-4200

SUMMARY

Power Domain (%s) is virtual, set a fence for it has no effect and will not be saved.

DESCRIPTION

A virtual domain has no member, the fence will not be saved.

IMPMSMV-4201

NAME

IMPMSMV-4201

SUMMARY

Power Domain (%s) is logical, should not have fence.

DESCRIPTION

Setting boundary for logical will be deleted later if this domain is set to share fence

of a physical domain.

IMPMSMV-6600

NAME

IMPMSMV-6600

SUMMARY

Command '%s' is not allowed after '%s'

DESCRIPTION

There are commands that are not allowed to run after a certain stage
in the design flow. This is one of them.

IMPMSMV-7101

NAME

IMPMSMV-7101

SUMMARY

error parsing IEEE1801 power intent file.

DESCRIPTION

This error is a general message issued when parsing of IEEE1801 fails.
This is typically due to syntax errors in the file. When you receive
this message, review the log file for warning and error messages which
precede the ENC1801-201 message. You should see messages which report

the specific lines in IEEE1801 which Innovus System is complaining about.

Correct the IEEE1801 and then try loading it in again.

IMPMSMV-7510

NAME

IMPMSMV-7510

SUMMARY

Power Switch rule %s for domain %s specifies input supply net %s, but no connecting net found on ptn %s.

DESCRIPTION

Partition will only create such port if the net connects to partition boundary.

Check power intent for such connection being specified or if power plan has been done correctly.

IMPMSMV-7511

NAME

IMPMSMV-7511

SUMMARY

Per power intent, Power Switch rule %s output supply net %s will connect to outside, but no port found on ptn instance %s.

DESCRIPTION

Partition will only create such port if the net connects to partition boundary.

Check power intent for such connection being specified or if power plan has been done correctly.

IMPMSMV-7512

NAME

IMPMSMV-7512

SUMMARY

Partition %s has PG pin %s, but it is not connected, it might need to be connected to net %s.

DESCRIPTION

Partition is not connected to the net. However, partition cell has same name port exists.

It is highly possible that the net should be connected to this port. Need to check why connection is missing.

IMPMSMV-7515

NAME

IMPMSMV-7515

SUMMARY

Partition %s rule %s has specified net %s, but has no such port found.

DESCRIPTION

Partition has power intent rule where a net is specified, but cannot find such net connecting into partition.

User might need to update power intent to connect it or use power plan or power route to connect it.

IMPMSMV-7520

NAME

IMPMSMV-7520

SUMMARY

Partition %s Domain %s has power switch rule %s, control signal %s is not connected to partition.

DESCRIPTION

This message warns that power switch rule control signal is not connected to partition, this is probably

because there is no power switch added, if power switch is to be added in partition,

then this signal should be manually connected to partition.

IMPMSMV-8003

NAME

IMPMSMV-8003

SUMMARY

skip element %s because it is not at the domain interface

DESCRIPTION

For the IEEE1801 isolation and level shifter insertion, the element listed in

the IEEE1801 set_isolation and set_level_shifter should be either domain

boundary ports or IO port or domain member. Please check the specified element

in the IEEE1801 file.

IMPMSMV-8304

NAME

IMPMSMV-8304

SUMMARY

rule %s: isolation inst %s has wrong isolation_signal; the ISO's enable pin is driven by a source which doesn't match the isolation signal specified in the IEEE1801 rule.

DESCRIPTION

please check if the ISO's source matches to the one specified in

-isolation_signal option in the IEEE1801 set_isolation command.

For example,

set_isolation rule1 -domain PD1 -isolation_signal I1/isoCtrl \

-isolation_sense low -location self

Example:

From Innovus, you can trace the connection of the instance's enable pin by:

innovus 1> reportPowerDomain -inst U_TOP_IO/U_PD_IO/UPF_ISO_1

Analyzing U_TOP_IO/U_PD_IO/UPF_ISO_1 (Cell: ISO_CELL) power domain: PD_IO

------- from side --------

Pin sdn33 (related power pin vdd33) => Net n6

U_TOP_IO/U_PD_IO/pdft_51/z in power domain PD_IO

innovus 4> all_fanin -to n6

A/z A/i iso/z33 iso/i U_TOP_ANALOG/U_TA_ANA/U37/z U_TOP_ANALOG/U_TA_ANA/U37/i

...

all_fanin returns pin chain, the last pin of which name contains

U_TOP_ANALOG is U_TOP_ANALOG/U_TA_ANA/U37/z.

innovus 7> get_nets -of U_TOP_ANALOG/U_TA_ANA/U37/z

n3

without -leaf, the following command returns the highest level HTerm on the net

innovus 8> get_pins -of n3

U_TOP_ANALOG/sul_iso_core2ana U_TOP_IO/iso

So the fanin is U_TOP_ANALOG/sul_iso_core2ana not

U_TOP_ANALOG/sul_iso_core2io specified in the UPF rule.

It means the connectivity in the Verilog doesn't match the rule in the UPF.

IMPMSMV-8401

NAME

IMPMSMV-8401

SUMMARY

Internal power domain %s is created for supply nets %s %s. Users need to define its PVT using MMMC command 'update_delay_corner -power_domain'.

DESCRIPTION

In IEEE1801 flow, there are more supply sets than power domains. Innovus will create an "internal power domain" for the supply set which is not primary PG nets for a domain.

- commit_power_intent will issue a WARN when it creates "internal" domain.

- Signal pin can be assigned to an internal domain if the signal pin is related the supply set without any associated domain in IEEE1801

Users need to define the internal domain's PVT so that a signal pin can be assigned to the correct voltage.

Voltage assignment flow:

Signal pin -> related pg pin -> supply_set -> domain -> domain's PVT definition in each view

To define the PVT, use MMMC command:

update_delay_corner -name <delay_corner>

-power_domain <internal_domain_name> -opcond <op_cond_you_defined>

IMPMSMV-8600

NAME

IMPMSMV-8600

SUMMARY

Power Intent is Not committed yet.

DESCRIPTION

Power Intent has been read, but has not been committed according to db.

User should run command - commit_power_intent to commit it before checking it.

IMPMSMV-8610

NAME

IMPMSMV-8610

SUMMARY

Power domain (%s) has no %s net defined.

DESCRIPTION

Power Domain has no power or ground net defined, and no supply set associated with it.

Check input power intent and correct it, then redo read_power_intent and commit_power_intent before proceeding.

IMPMSMV-8620

NAME

IMPMSMV-8620

SUMMARY

Power domain (%s) has not given a legal fence.

DESCRIPTION

All physical power domain must have fence defined and inside design boundary.

Use floorplan command or GUI to define power domain boundary.

IMPMSMV-8623

NAME

IMPMSMV-8623

SUMMARY

Primary PG term %s of Instance %s is connected to net %s which conflicts with primary power net %s of the domain %s specified in UPF. This can impact the run time and quality of results.

DESCRIPTION

This error might lead to power shortage, and need to be fixed.

Use reportPowerDomain -inst <inst_name> -verbose to see connection details.

IMPMSMV-8630

NAME

IMPMSMV-8630

SUMMARY

Power domain (%s) in view (%s) has no user defined operating condition.

DESCRIPTION

To achieve the best QoR of design, it is recommended that user to define complete operating condition in MMMC definition file.

IMPMSMV-8631

NAME

IMPMSMV-8631

SUMMARY

Power domain (%s) in view (%s) is using op. cond from timing library set.

DESCRIPTION

Every power domain should have user defined operating condition or a valid definition from its timing library.

The check shows user has not defined operating condition, and using the setting from domain's timing library.

User can modify view definition file to define operating condition.

IMPMSMV-8632

NAME

IMPMSMV-8632

SUMMARY

Power domain (%s) in view (%s) has no default op. cond.

DESCRIPTION

No user defined or default op. cond. can be found from power intent for this power domain.

This could lead to incorrect timing evaluation of the design.

It is recommended that user to modify view definition file and define complete operating condiditon for each domain.

IMPMSMV-8640

NAME

IMPMSMV-8640

SUMMARY

No timing library set found for domain %s in view %s.

DESCRIPTION

Check MMMC configuration file for timing library definition for power domains and views.

It is recommended to define power domain specific library set in all views.

IMPMSMV-8650

NAME

IMPMSMV-8650

SUMMARY

Cell (%s) Pin (%s) has no related power/ground pin defined in timing library.

DESCRIPTION

Reported pin of cell has no related power/ground pin defined in timing library.

IMPMSMV-8656

NAME

IMPMSMV-8656

SUMMARY

Domain (%s) do not allow feedthrough being added in it.

DESCRIPTION

All modules inside this domain are not allowed to add new port, so no feedthrough can go thru it.

This is to warn user that no feedthru can be added to reported domain, as this might affect timing result.

IMPMSMV-8660

NAME

IMPMSMV-8660

SUMMARY

No available AO buffer for power domain (%s) in view (%s).

DESCRIPTION

There is no AO buffer found for the reported domain and view, either no buffer found in domain's library set

or some buffers might be marked as don't use. If AO buffer is expected to be used in this domain, user must

correct this issue before proceed in the design flow.

IMPMSMV-8670

NAME

IMPMSMV-8670

SUMMARY

Instance (%s) of power domain (%s) is placed inside fence of power domain (%s).

DESCRIPTION

Reported instance is fixed and placed in other domain's fence, this is placement violation that needs to be corrected.

User can manually move or unplace the reported instances, and redo placement to correct the issues.

IMPOAX-124

NAME

IMPOAX-124

SUMMARY

OpenAccess (OA) shared library installation is older than the one that was used to build this %s version. For using the OA installation built and tested with this %s version, unset the shell variable OA_HOME. For using '%s' or higher version of OA, reset OA_HOME to point to that installation.

DESCRIPTION

These errors are only reported when you point to an OpenAccess (OA) installation which is older than the tool version was built with. By default, tool will use the OA version in the tool installation unless the environment variable OA_HOME is set to point to another OA installation. To resolve this issue, the recommendation is to use 'unsetenv OA_HOME' so tool will use the local OA installation. Alternatively, set OA_HOME to a compatible OA installation.

OA versions are signified using three sets of numbers separated by a period (i.e. XX.YY.ZZZ) or sometimes the third number is separated with a dash (i.e. XX.YY-ZZZ). OA versions are compatible if the first two sets of numbers are the same.

To determine what OA version an IC610 or tool installation was compiled with by going to http://downloads.cadence.com and clicking on the README or README.OA file. This is listed next to each release.

Overall, Cadence recommends you run your application with the version of OA that it was built, tested and shipped with. Otherwise, unforeseen compatibility issues may arise.

For example, any 22.04.abc version is compatible with any other 22.04.xyz version.

IMPOAX-148

NAME

IMPOAX-148

SUMMARY

Error in getting path for %s/%s/%s. OA Exception : %s.

DESCRIPTION

Check if you have permission to access the OpenAccess database.

IMPOAX-252

NAME

IMPOAX-252

SUMMARY

Found busBit terminals of bus '%s' of cell '%s' without bus ordering information in OpenAccess library '%s'. There could be more such terminals without bus order information. This may lead to problems during saveDesign. It is recommended to run verilogAnnotate on the library for annotating bus ordering information to such terminals.

DESCRIPTION

The issue occurs because the bus ordering information for cell’s busBit terminals is not present.

The OpenAccess (OA) libraries were created using lef2oa. LEF file contains no information about bus order of busBit terminals. When using this tool with OA, the bus ordering information must be annotated into the abstract using the verilogAnnotate utility.

To run verilogAnnotate for the cell to update the existing OA data with

terminal ordering information from a Verilog file.

verilogAnnotate -refLibs libraryList -verilog fileList [Optional Arguments]

For example:

restoreDesign -cellview {lib cell view}

If you only have the top level design netlist but no this cell's netlist,

you need to generate leafOnly.v.

saveNetlist leafOnly.v -onlyLeafCell

Make sure you have write permission to update the OA file

verilogAnnotate -refLibs library_1 -verilog leafOnly.v

exit

restart tool

restoreDesign -cellview {lib cell view}

attachTerm ...

saveDesign ...

The saved design will have the changes saved.

IMPOAX-332

NAME

IMPOAX-332

SUMMARY

Failed to initialize OpenAccess (OA) database. OA related commands cannot be run in this session. Confirm that the OA shared library is installed and OA_HOME is set correctly. Typically the OA_HOME environment variable should not be set.

DESCRIPTION

The environment variable OA_HOME should not typically be set as the correct OpenAccess shared library should be automatically loaded. If the OA_HOME environment variable is set, confirm that it is set intentionally and unset it if not. If the requirement is to load a newer shared library, then confirm that the path name specified in OA_HOME is correct.

Example:

Manual override of default shared library location:

setenv OA_HOME /xx/xx/<tool_name>/toolxxx/xx.xx/lnx86/oa_vxx.4x

IMPOAX-335

NAME

IMPOAX-335

SUMMARY

Could not open technology data. Refer to any earlier error messages.

DESCRIPTION

It is a common and generic error message that comes during init_design or restoreDesign steps and may have numerous specific causes due to which the technology data is not being read. Check the warnings and errors above it in logfile to troubleshoot this error further.

IMPOAX-392

NAME

IMPOAX-392

SUMMARY

Destination library '%s' already exists and is in correct state as it would be if created with the given command. If a new library is desired, then a different library name must be specified, otherwise use

the library that already exists.

DESCRIPTION

The library creation only works if a library with the specified name does not already exist in the cds.lib. So, if createLib indicates that the library already exists, then rerun the command with a different library name or remove the existing library from the cds.lib and disk before running the createLib command.

IMPOAX-433

NAME

IMPOAX-433

SUMMARY

Saving design to (%s/%s/%s) which is using technology from lib '%s', doesn't contain any valid LEFDefaultRouteSpec. Aborting saveDesign.

DESCRIPTION

LEFDefaultRouteSpec could not be found, either by definition or by name in the technology. Please create an interoperable PDK before proceeding. test test test.

if starting point is LEF file do:

1.Load the design into the tool

2.write_oa_techfile <filename>.tf

3.create OpenAccess lib using techLoadDump <filename>.tf

4.add place and route data to the lib from <filename>.lef using lef2oa -pnrLibDataOnly.

if virtuoso PDK is already there do only step 4 mentioned above to create interoperable PDK.

IMPOAX-503

NAME

IMPOAX-503

SUMMARY

Cannot open OpenAccess library '%s'. Make sure the library exists on disk and its entry is present correctly in the library definition file.

DESCRIPTION

Why do I receive the error above when importing my design into tool?

This error indicates tool is unable to find an OpenAccess (OA) library.

For example, if your .globals file defines:

set init_oa_ref_lib {oaLib1 oaLib2}

But your cds.lib (or lib.defs) file only defines oaLib1:

DEFINE oaLib1 ./oaLib1

Correct this by removing the reference for oaLib2 or specifying the path to oaLib2 in your cds.lib file:

DEFINE oaLib1 ./oaLib1
DEFINE oaLib2 ./oaLib2

Also, make sure you are not confusing the syntax for the cds.lib file and the lib.defs file. We recommend using a cds.lib file. Its syntax is:

DEFINE libName libPath

If the error is preceded by the following warning then there is not a cds.lib file in the run directory to define the location of the libraries:

**WARN: (IMPOAX-791): Error reading library definition file : No default library definition file found.

IMPOAX-571

NAME

IMPOAX-571

SUMMARY

Property '%s' on %s %s is a hierarchical property which is not supported in %s. This property is not translated and it will be lost in round trip unless updateMode is enabled.

DESCRIPTION

Virtuoso and OpenAccess (OA) allow creation of hierarchical properties. For instance, value of a hierarchical property can itself be another hierarchical property. So there can be a multi-level tree of properties on a object in OA. "Multi-level tree like properties" are not supported and hence not read.

Example:

If the following setting is used, these properties are preserved on the original object, so when the design is saved, these properties are not lost :

setOaxMode -updateMode true

If you want to preserve these properties, please use this setting.

IMPOAX-606

NAME

IMPOAX-606

SUMMARY

Failed to add edge %s/%s - %s/%s to scan chain '%s'. The design being read from OpenAccess during oaIn is out of sync with the design in memory. This scan chain contains logical instances which are not present in current design. So, some of the scan chain edges are not being created. Please oaIn consistent desgin with current design.

DESCRIPTION

This message is issued when any logical instance in scan chain being read from OpenAccess during oaIn is not present in current design. Adding additional logical instances may cause LVS

problem, scan chain edges with unknown logical instances will be dropped. Possibly, the design being oaIn is out of sync with the restored DB. Please update the designs to be consistent with current design and oaIn again.

IMPOAX-618

NAME

IMPOAX-618

SUMMARY

Custom via definition for via '%s' cannot be created in the technology database, because the technology database associated with library '%s' is readonly.

DESCRIPTION

In the tool's Flow new vias may be created during
power routing. These are typically via arrays created from VIARULE GENERATE
statements in the technology LEF. When saving the design to OpenAccess (saveDesign or
oaOut) via definitions of these vias need to be added to the technology library if they cannot
be defined in a parameterized form using standard vias from the OpenAccess technology file. To
see if the via is defined in parameterized form, use defOut to create a DEF
file and look for vias in the VIAS section that are defined using the + RECT
syntax instead of + VIARULE syntax.

If the vias cannot be represented by standard vias then a new custom via must be
created which requires writing to a technology file. Therefore, you must have
write permissions or allowed to do an incremental update of the technology
library.

Since the technology database needs to be incrementally updated, the recommended method is to create

local technology database in design library either using 'createLib -referenceTech' or 'setOaxMode -libCreateMode reference' option. For example:

createLib myLib -referenceTech myRefLib

set init_oa_design_lib myLib

Or

setOaxMode -libCreateMode reference

Then define the place and route technology rules in myRefLib by importing a technology LEF. This creates a local technology database in the design library that can be modified incrementally. Overall, when setting up your mixed-signal design environment we recommend using a Base PDK which contains the base technology file and an incremental technology database (ITDB) which references the Base PDK. The ITDB contains the information for physical design and can be updated, while the Base PDK can remain read-only.

IMPOAX-683

NAME

IMPOAX-683

SUMMARY

Unable to find module terminal '%s' for module '%s' in '%s/%s/%s'. Connectivity cannot be

maintained if the terminal does not exist for module.

DESCRIPTION

One of the possible reason can be - If the design is re-mastered from abstract views that were used by tool and layout views that can be used by verification tools, the re-mastered view does not have any terminals. The oaOut -noConnectivity option must be specified to be able to save the database. As the database will not have connectivity information it will not be able to be reloaded if no connectivity exists in the cellview that was written. A cellview created using the -noConnectivity option is designed to be used with verification tools that do not need the OpenAccess database to contain connectivity information.

IMPOAX-684

NAME

IMPOAX-684

SUMMARY

Cannot find definition of BUS Terminal '%s' of Cell '%s' in reference library. This could lead to further errors while saving the OpenAccess (OA) database. Possible reasons could be that verilogAnnotate was not run on the OA reference library that has the definition for this cell. Either run verilogAnnotate on the reference library to fix this problem or use command 'setOaxMode -allowBitConnection true' before saving design to make bitwise connection of terminals.

DESCRIPTION

The message is issued when saving a design to OpenAccess (OA) by running saveDesign. The OA libraries were created using lef2oa.
When using tool with OA, the bus pin order must be annotated into the abstract using the verilogAnnotate utility. This step is done after

importing the LEF macro data and prior to running saveDesign .
Failure to complete this step on macros with the bus pins causes tool to
display this warning message.

Example:

To prevent this warning, a Verilog stub file is needed for each macro with bus
pins. This might be derived from the symbol view using the 'Create-Cellview-From'
in Cellview menu command. Once you have a stub file for each macro which has bus
pins run verilogAnnotate at the Linux command line using the following steps:

$CDSHOME/share/oa/bin/verilogAnnotate \

-refLibs reference_library_name \

-verilog stub.v

where, stub.v contains the module definitions with only port list, input/output
direction and bus definitions of the referenced blocks.

Alternatively, you can set "setOaxMode -allowBitConnection true" prior to
saveDesign in place of running verilogAnnotate.

IMPOAX-720

NAME

IMPOAX-720

SUMMARY

The layer '%s' has inconsistent preferred routing direction. Check the layer information in OpenAccess technology database.

DESCRIPTION

This message is issued when the Open Access (OA) technology
is read in and consecutive layers have the same preferred direction. In some
technologies Metal1 and Metal2 will both be horizontal to allow for power rails
on both layers.

Example:

Example OpenAccess technology file where Metal1 and Metal2 are both horizontal:

```
routingDirections(
;( layer direction )
;( ----- --------- )
( Metal1 "horizontal" )
( Metal2 "horizontal" )
( Metal3 "vertical" )
( Metal4 "horizontal" )
( Metal5 "vertical" )
( Metal6 "horizontal" )
( Metal7 "vertical" )
( Metal8 "horizontal" )
( Metal9 "vertical" )
) ;routingDirections
```

IMPOAX-745

NAME

IMPOAX-745

SUMMARY

Cell '%s' from cellview '%s' has already been read in from '%s'. The cell can only be read once, so the second version will be ignored. Review the value of the init_oa_ref_lib variable and update to remove the library that has the copy of the cell that should not be read.

DESCRIPTION

Each library cell can only be read once. In the case where the same cell is found in multiple libraries, the first one read being will be the one that is used to create the cell data within software. The library cells are read based on the settings of the init_oa_ref_lib and init_abstract_view variables. Anytime a library cell is found in multiple libraries, that is likely not intended and the values variables should be updated to prevent the duplicate cell from being found.

IMPOAX-750

NAME

IMPOAX-750

SUMMARY

Tech site '%s' used in macro '%s' is not found. Check if this macro in OpenAccess (OA) database has correct site information, and if the site is defined in OA technology database.

DESCRIPTION

Standard cells (CLASS CORE) require sites to be placed properly. If no site definition is found then the cell cannot be legally placed. Either the site definition is missing from the library that contains the standard cells or another library that contains the site definition was not included in the init_oa_ref_lib variable's reference library list.

If the site was missing from the library that contains the standard cells, modify the <technology file>.tf (ASCII technology file) file used in Virtuoso and compile again your technology library in Virtuoso.

Please follow these steps :

- Open the <technology file>.tf file :

- Look for the following "SITEDEFS" and modify like this :

```
;*******************************

; SITEDEFS

;*******************************

siteDefs(

scalarSiteDefs(

;( siteDefName type width height symInX symInY symInR90)
```

;(---------- ---- ----- ------ ------ ------ -------)

(CoreSite core 0.512 5.12 t nil nil)

) ;scalarSiteDefs

) ;siteDefs

- If you modified the technology file, please re-compile the technology file to OpenAccess DB.

IMPOAX-755

NAME

IMPOAX-755

SUMMARY

Macro '%s' has no SITE statement and it is a class CORE macro that requires a SITE statement. The SITE %s is chosen because it is a core site with height %.4f that matches the macro SIZE height.

DESCRIPTION

This message indicates this cell is defined with CLASS CORE which means it is a standard cell. Standard cells require a SITE to be defined for them. In a floorplan, rows are created which are made of SITES which define the placement grid for standard cells. The placer must know what SITE each standard cell is allowed to use. If a SITE is not defined for a standard cell,tool will try to find a SITE with the same height and use that. To specify the correct

SITE, open the Abstract view in Virtuoso and display the cells properties. At the bottom of the Attributes it will have Site Definition where you can select the cor- rect site. If you created your Open Access (OA) library from LEF you can add the SITE name to the MACRO definition and re-import the LEF into OpenAccess.

This message indicates this cell is defined with CLASS CORE which means it is a standard cell. Standard cells require a SITE to be defined for them.

MACRO FILL8
CLASS CORE ;
FOREIGN FILL8 0 0 ;
ORIGIN 0.0000 0.0000 ;
SIZE 1.2 BY 1.71 ;
SYMMETRY X Y ;
SITE CoreSite ;

IMPOAX-757

NAME

IMPOAX-757

SUMMARY

Can not find sitePattern '%s' for macro '%s' in %s database. Check if the site is defined correctly in OpenAccess technology database.

DESCRIPTION

This message indicates that a cell (typically an abstract view)

for example, 'DEL1' has SITE coreABC specified but that the site is not defined in the technology file. An equivalent LEF representation would be:

MACRO DEL1

- - -

- - -

SITE coreABC

- - -

- - -

Verify if the SITE name is correct, then verify its definition. This can be verified by dumping out the technology file by Virtuoso. The SITE information is defined in the scalarSiteDefs section of the technology file, or export a LEF file using oa2lef and search for the site with the given name. Below are examples of site definitions in the open access technology file and in LEF file.

In OpenAccess technology File

scalarSiteDefs(

(siteDefName type width height symInX symInY symInR90)

;(----------- ---- ----- ------ ------ ------ -------)

(coreABC core 0.5 5.0 nil nil nil)

) ;scalarSiteDefs

In LEF file

SITE coreABC

CLASS CORE

SIZE 0.5 BY 5.0

END coreABC

IMPOAX-773

NAME

IMPOAX-773

SUMMARY

Pin '%s' in macro '%s' has no ANTENNAGATEAREA value defined. The library data is incomplete and some process antenna rules will not be checked correctly.

DESCRIPTION

This warning is triggered when the technology data has process antenna rules,

and a signal pin is missing process antenna data needed to check the rules. In

this case, a signal pin that is either an input or inout pin is missing the gate-area data.

In CMOS, every signal pin that is an input or inout pin connects to a transistor gate. If there is no gate-area associated with this pin, then the library data is incomplete and process antenna rules cannot be checked for this pin correctly. The router and verification commands will assume this pin has no transistor gate attached, and therefore does not need to be protected from process antenna violations, which may result in real violations that are not fixed by the router or seen by the verification commands.

The best way to avoid this warning is to add the correct antenna gate- area data to the library data.

You can also use the suppressMessage command to turn off this warning message. This might be appropriate if you know the only library cells without antenna data are already protected by internal diode cells (e.g. some blocks might be built this way). In that case, you would lose the possible benefit of those internal diode cells for any nets connected to the block input, which might cause the router to add some unnecessary diode cells to protect other inputs attached to the same net. This is somewhat dangerous, because you might suppress messages for pins that are not protected.

You can also turn off the warning if you believe antenna errors are rare for these pins in practice, and you will depend on final sign-off physical verification tools to find any errors, and repair them manually.

IMPOAX-774

NAME

IMPOAX-774

SUMMARY

Pin '%s' in macro '%s' has no ANTENNADIFFAREA value defined. The library data is incomplete and some process antenna rules will not be checked correctly.

DESCRIPTION

This warning is triggered when the technology data has process antenna rules, and a signal pin is missing process antenna data needed to check the rules. In this case, a signal pin that is either an output or inout pin is missing the diffusion-area data.

In CMOS, every signal pin that is an output or inout pin connects to a transistor diffusion. If there is no diffusion-area associated with this pin, then the library data is incomplete and process antenna rules cannot be checked for this pin correctly. In that case, the router may try to protect other input pins connected to the same net with extra routing and vias ('layer-hopping'), or add extra diode cells to avoid 'false' antenna violations. The verification commands may flag false violations also.

The best way to avoid this warning is to add the correct antenna diffusion-area data to the library data.

You can also use the suppressMessage command to turn off this warning message. This might be appropriate if you know that antenna violations are rare in this technology, and you are willing to tolerate some extra layer-hopping, or extra diode cells that are not really necessary.

IMPOAX-923

NAME

IMPOAX-923

SUMMARY

Found unsupported shape with type '%s' in the OpenAccess (OA) database. The shape has bounding box co-ordinates from (%.11g,%.11g) to (%.11g,%.11g) and is on layer '%s'. In non-update mode these shapes will be lost in round trip. However, in update mode these shapes will be preserved in the OA database.

DESCRIPTION

When text information is attached to pin shapes, a warning like the following will appear.

**WARN: (IMPOAX-923): Found shape with unsupported type 'AttrDisplay' in the OpenAccess (OA) database. The shape has bounding box co-ordinates from (1063.911,1022.813) to (1064.826,1029.3) and it is lying on layer 'PIN'. In non-update mode these shapes will be lost in round trip. However, in update mode these shapes will be preserved in the OA database.

First, follow all the settings required for Virtuoso and this tool interoperability as explained in the Mixed-Signal Interoperability Guide. For this specific message make sure "setOaxMode -updateMode true" is set.

The reason in this case for the "**WARN: (IMPOAX-923):" is that shapes with unsupported types like "AttrDisplay", "Arc", "Dot" and "Line" are not read in OA DB. These object types should not be used in OA DB intended for

interoperability with tool.

IMPOAX-931

NAME

IMPOAX-931

SUMMARY

Found Pcell vias/instances in the design but Express Pcells are not enabled (Environment variable CDS_ENABLE_EXP_PCELL is not defined). Layout data for the pcell instances cannot be read from the pcell cache directory. Enable Express Pcells in the environment and retry.

DESCRIPTION

The error above is reported when importing an OpenAccess (OA) design from Virtuoso to

tool that contains Pcells. When I open the design in tool the Pcells

are not the proper size. What setup is required to transfer the Pcells

properly?

Prior to saving the design to OA in Virtuoso, make sure the following is done:

1. At the Linux prompt set the following:

setenv CDS_ENABLE_EXP_PCELL true

setenv CDS_EXP_PCELL_DIR ./.expressPcells

2. Invoke Virtuoso and open the design. Note in Virtuoso versions before

IC6.1.4.500.1 VLS-XL or VLS-GXL is required to save the express PCell cache. In

IC6.1.4.500.1 and later version all Virtuoso products support this.

3. Select Tools->Express Pcell Manager. Fill out all the details and Enable Caching of the Pcells check box with Auto Save option. Press Save Copy to save the Pcell Layout Cache. This step is necessary to enable inter-operation of the data between this tool and Virtuoso.

4. Save the design to OA and exit Virtuoso.

5. Prior to invoking tool set the following:

setenv CDS_ENABLE_EXP_PCELL true

setenv CDS_EXP_PCELL_DIR ./.expressPcells

IMPOAX-956

NAME

IMPOAX-956

SUMMARY

While annotating the placement data from %s/%s/%s, the logical instance '%s' was not found in the OpenAccess (OA) design. One reason for this could be that logical netlist data read during init_design is different from the OA cellview's embedded module hierarchy (EMH) data created from a previously read OA design. The OA database used to read physical information should be consistent with the verilog file or the OA database used for reading logical netlist.

DESCRIPTION

This message comes when any instance being read from OpenAccess (OA) during oaIn process is

not present in FEDB.

If you are planning to merge floorplan data from OA to tool or
incrementally loading the floorplan data then oaln has a new option "-filter
{boundary pin_shapes}" that tells tool to read only the information specified,
and ignore any mismatches. So for
example, if you used -filter pin_shapes, any existing pin shapes would be
replaced by the ones read from the OA cellview. Please refer the documentation for more details.

If you are using a prior version of tool than 13.2 , the -filter option isn't available and
a workaround is required:

1)load the config file in tool.
2)save OA design
3)Load the design in Virtuoso Layout-XL
4)File->Load Physical View (Be sure to load the pins in "update" mode)
5)Save the new/updated design
6)Restore this design in tool and continue with the P&R flow.

IMPOAX-986

NAME

IMPOAX-986

SUMMARY

%s can't support a MUSTJOIN terminal in bus bit format." "The terminal '%s' is renamed to '%s'.

DESCRIPTION

Loading LEF with below MUSTJOIN definition in the LEF issues IMPOAX-986 warning in OpenAccess based flow.The reason for this warning is that master pins can be a bus bit, but the slave cannot. Only pins that exist in the logical netlist can be bus bits.

The P/G and MUSTJOIN terminals (physical side only) cannot be bus bits.

Example :

==========

PIN pad_mj1

DIRECTION INPUT ;

USE SIGNAL ;

PORT

LAYER Metal2 ;

RECT 2.97 4.3 3.53 4.72 ;

END

END pad_mj1

PIN pad[1]

DIRECTION INPUT ;

USE SIGNAL ;

MUSTJOIN pad_mj2 ;

PORT

LAYER Metal2 ;

RECT 2.92 1.3 3.48 0.72 ;

END

END pad[1]

==========

In the above example

PIN pad[1] # this is not allowed, needs to be a simple name like pad_1

MUSTJOIN pad_mj2 ;

IMPOAX-1017

NAME

IMPOAX-1017

SUMMARY

Creating a database with the '-noConnectivity' option will result in a database that cannot be read back into %s.

DESCRIPTION

The OpenAccess database created with '-noConnectivity' option will not contain any nets, terms and instterms. The design created with this option will contain only physical shapes. This type of database is for use with tools that do not require connectivity in the database.

Some 'layout' views may not contain terminals and if the design references any cells that will be bound to those cellViews, then the '-noConnectivity' option should be specified.

By default, 'oaOut' will maintain connectivity, but that requires that terminals to exist on all cellViews that referenced from the instances within the design.

IMPOAX-1034

NAME

IMPOAX-1034

SUMMARY

Cannot open report file %s.oaread.rpt for writing. Check if you have correct permissions to write into this file.

DESCRIPTION

You have this message because you may not have write permission on current

working directory or have run out of disk space.

Example:

Check if you have permission on current working directory:

20> file writable [pwd]

1

Check if you have necessary disk space:

16> df -kH [pwd]

Filesystem Size Used Avail Use% Mounted on

/disk/subDirectory/case/case11189 2.2T 2.0T 271G 88%

/disk/subDirectory/case/case11189

IMPOAX-1050

NAME

IMPOAX-1050

SUMMARY

Type of trim layer '%s' is not identified as TRIMPOLY/TRIMMETAL layer. Tool only supports TRIMPOLY and TRIMMETAL layers. This layer will be read as MASTERSLICE layer.

DESCRIPTION

Either the layer is missing trim function or it belongs to diffusion/substrate cutting. You can use "techLoadDump -d <libName> <technology file name>" to check the technology.

IMPOAX-1092

NAME

IMPOAX-1092

SUMMARY

Logical instance '%s' of cell '%s' cannot be created in the OpenAccess database. It could be a problem in EMH (Embedded Module Hierarchy) data creation. Refer to any earlier error messages. Confirm that cell '%s' exists in the reference libraries.

DESCRIPTION

When attempting to save an OpenAccess database, the tool gives above error

messages and does not save the design.

What is the reason for tool giving above error messages?

This problem occurs if the reference library attached to the design library is

not present in the cds.lib or path to access this library is incorrect.

Please check your cds.lib file and correct the path. If the paths are correct,

then you need to check that you have defined following variables before saving

your design:

set init_oa_design_lib TEST

set init_oa_design_cell row_dec

set init_oa_ref_lib gsclib090

set init_oa_design_view layout

set init_abstract_view abstract

set init_layout_view layout

IMPOAX-1151

NAME

IMPOAX-1151

SUMMARY

Non-leaf cell %s will be treated as a leaf cell.

DESCRIPTION

Non-leaf cells are determined by LEF MACRO and dotlib definitions. If this is a hierarchical design, remove LEFs and dotlibs for flattened partitions. These are referenced in <design>.globals, viewDefinition.tcl, and tcl scripts with init_design. Ignoring this message can result in unexpected results when restoring a saved OpenAccess database.

IMPOAX-1255

NAME

IMPOAX-1255

SUMMARY

No VIARULE GENERATE statement between routing layers '%s' and '%s' while reading technology information from the library.

DESCRIPTION

VIARULE GENERATE (standardViaDef from technology database) defines formulas for generating via arrays. User can use the VIARULE GENERATE statement to cover special wiring that is not explicitly defined in the VIARULE statement.
Rather than specifying a list of vias for the situation, you can create a formula to specify how to generate the cut layer geometries.

Example:

The following example describes a formula for generating via cuts:

VIARULE via12 GENERATE

LAYER m1 ;

ENCLOSURE 0.05 0.01 ; #2 sides must be >=0.05, 2 other sides must be >=0.01

WIDTH 0.2 TO 100.0 ; #(optional)for m1, between 0.2 to 100 microns wide

LAYER m2 ;

ENCLOSURE 0.05 0.01 ; #2 sides must be >=0.05, 2 other sides must be
>=0.01

WIDTH 0.2 TO 100.0 ; #(optional)for m2, between 0.2 to 100 microns wide

LAYER cut12

RECT -0.07 -0.07 0.07 0.07 ; #cut is .14 by .14

SPACING 0.30 BY 0.30 ; #center-to-center spacing

END via12

IMPOAX-1257

NAME

IMPOAX-1257

SUMMARY

Allowing saveDesign to create OpenAccess (OA) based reference library data on-the-fly is not recommended.

DESCRIPTION

Allowing saveDesign to create OpenAccess (OA) based reference library data

(FEOAreflib) on-the-fly can result in multiple copies of reference library information as well as increase the run time of the saveDesign process. Externally translating the LEF information into OA reference libraries is recommended using lef2oa/verilogAnnotate or LEF-to-OA migration scripts.

IMPOAX-1265

NAME

IMPOAX-1265

SUMMARY

Some of the library data inside '%s %s %s' has data on invalid layers %s that will be ignored.

DESCRIPTION

This is most likely because the OpenAccess technology has multiple metal-stack options and the init_oa_extractor_setup that defines the valid layers for this design was not set correctly. See the init_design Tcl documentation for more details. In some methodologies this is allowed, in which case you should add (suppressMessage 1265) to turn off these warnings.

IMPOAX-1266

NAME

IMPOAX-1266

SUMMARY

Some of the library data inside cell "%s" has data on invalid layer "%s" that will be ignored.

DESCRIPTION

This is most likely because the OpenAccess technology has multiple metal-stack options and the init_oa_extractor_setup that defines the valid-layers for this design was not set correctly. See the init_design Tcl documentation for more details. In some methodologies this is allowed, in which case you should add (suppressMessage 1266) to turn off these warnings.

IMPOAX-1274

NAME

IMPOAX-1274

SUMMARY

Terminal %s is not on the interface of cell %s, the OpenAccess (OA) cellview terminal's isInterface bit is set to false. Logical connectivity of this terminal to corresponding net may get lost upon reading the data. In order to fix the problem, either run the VerilogAnnotate command on the layout view of the cell or recreate the reference libraries with interface bit set for this terminal.

DESCRIPTION

The issue occurs because the mentioned bit is not on the interface of the
cell. The isInterface bit is meant to align to the
Verilog modules. So, if a OpenAccess abstract terminal has isInterface = nil, that
means that it should not appear in the Verilog netlist when running saveNetlist
unless the -includePowerGround or -phys options are used. Terminals with
isInterface = nil should only be connected to a USE POWER/GROUND net, not a
regular signal net. Assuming that the Verilog module (and .lib) has port, then
running verilogAnnotate will set the bit on the abstract's terminal to true
instead of nil.

To run verilogAnnotate :

verilogAnnotate -refLibs libraryList -verilog fileList [Optional Arguments]

Example:

restoreDesign -cellview {lib cell view}

If you only have the top level design netlist but no this cell's netlist,
you need to generate leafOnly.v.

saveNetlist leafOnly.v -onlyLeafCell

Make sure you have write permission to update the OpenAccess database

verilogAnnotate -refLibs library_1 -verilog leafOnly.v

exit
restart tool

restoreDesign -cellview {lib cell view}

attachTerm ...

saveDesign ...

The saved design will have the changes saved.

IMPOAX-1275

NAME

IMPOAX-1275

SUMMARY

Interface bit for term %s of instance %s is not set. Dropping connection of this terminal with its corresponding net %s. In order to fix the problem, set the interface bit for these terminals in the reference libraries and recreate the OpenAccess database.

DESCRIPTION

The issue occurs because the mentioned bit is not on the interface of the
cell. The isInterface bit is meant to align to the
Verilog modules. So, if a OpenAccess abstract terminal has isInterface = nil, that
means that it should not appear in the Verilog netlist when running saveNetlist
unless the -includePowerGround or -phys options are used. Terminals with
isInterface = nil should only be connected to a USE POWER/GROUND net, not a
regular signal net. Assuming that the Verilog module (and .lib) has port, then
running verilogAnnotate will set the bit on the abstract's terminal to true
instead of nil.

To run verilogAnnotate :

verilogAnnotate -refLibs libraryList -verilog fileList [Optional Arguments]

Example:

restoreDesign -cellview {lib cell view}

If you only have the top level design netlist but no this cell's netlist,
you need to generate leafOnly.v.

saveNetlist leafOnly.v -onlyLeafCell

Make sure you have write permission to update the OpenAccess file

verilogAnnotate -refLibs library_1 -verilog leafOnly.v

exit
restart tool

restoreDesign -cellview {lib cell view}

attachTerm ...

saveDesign ...

The saved design will have the changes saved.

IMPOAX-1307

NAME

IMPOAX-1307

SUMMARY

Via definition for std via '%s' is not found in the OpenAccess (OA) technology database associated with the design. Possible reason could be that this design has been read or created using a different OA technology database or LEF and these two database are out of sync. This serious issue should be fixed before proceeding further. To save the design, %s is creating custom via definition in current OA technology database for the std via '%s'.

DESCRIPTION

If a VIA in the tool database is parameterized and refers to a LEF rule

VIARULE .. GENERATE, then oaOut will expect a matching (by name) oaStdViaDef to

use for the parameterized via. If the oaStdViaDef is not found, then a fixed

via (oaCustomViaDef) will be created instead which means that the parameterized

form is lost in the roundtrip (oaOut -> OpenAccess (OA) -> oaIn).

If the creation succeeds and the user doesn't need the Vias remain

parameterized, the message can be ignored.

If the user would want to have the Vias remain parameterized, they should

compare their "technology" data to see why the oaStdViaDef name does not match

the LEF VIARULE GENERATE name.

IMPOAX-1313

NAME

IMPOAX-1313

SUMMARY

The library '%s' has its data compression level set to '%d', while the compression level for this %s session is %d. Any new data being saved into this library will be saved with its compression

settings, irrespective of the global value.

DESCRIPTION

When user brings a design from virtuoso and save it, tool gives
following warning message:
In OpenAccess data model 4, you have an option to compress the library and save it. By default, virtuoso saves design in uncompressed mode, whereas, tool saves in compressed mode. So when you open a design initialized in virtuoso and save it in, you will get this warning message.To change compression level in tool use command
setOaxMode -compressLevel 0
Virtuoso IC 616 and tool version 11.1 and above can read and save compressed design library.
However, IC 615 cannot handle the compressed design.
Therefore you need to run oazip -decompress before restoring compressed design in virtuoso 615.

IMPOAX-1609

NAME

IMPOAX-1609

SUMMARY

pull_pin_constraint is unable to pull pin constraint from cell '%s' because it has no layout cellview bound to it. If the cell is bound to abstract cellview, use option -cellview to specify the 'lib cell view' name for pull_pin_constraint to find the target layout cellview.

DESCRIPTION

When any of the options (-cell, -inst or -all_blocks) is specified, this command pulls the pin constraints from the layout cellview that is bound to the cell(s). This error is displayed when there is no layout cellview bound to the cell itself. One possibility could be that the master cellview of the cell is an abstract cell and tool can't find its corresponding layout cellview. In such case, by default, tool expects the view name of the layout cellview to be 'layout' and its location to be under the same library/cell directory as the abstract cellview. Use the option -cellview to specify the 'lib cell view' name for pull_pin_constraint to find the target layout cellview.

IMPOAX-1625

NAME

IMPOAX-1625

SUMMARY

The tech graph in '%s' is different from the library '%s' which was used to create the %s technology information. This can result in problems during the save process if the vias, layer rules, etc are different in the two cases. The simplest solution to the problem is to have the '%s' reference the refLib of current design for technology information. To create a new library, use createLib with the -referenceTech option.

DESCRIPTION

The technology information in the design library that the cellview is being

saved into must be the same as the original library technology that was used to

create the in session technology information.

You need to set this library as design library so that tool understands the

hierarchy library/cell/view.

To set the library as design library use following command

set init_oa_design_lib "test1"

After this setting, tool will not give the warning message (IMPOAX-1625) during saveDesign.

Example:

**WARN: (IMPOAX-1625): The tech graph in 'designLibOA' is different from the library 'ref_lib' which was used to create the technology
information. This can result in problems during the save process if the vias, layer rules, etc are different in the two cases. The simplest solution to the problem is to have the 'designLibOA' reference the refLib of current design for technology information. To create a new library, use createLib with the -referenceTech option.

In the globals file used to invoke the design, you have following entries

++++++++++++++++++++++++++++++

set oareflib "tech1"

set DATA_DIR "./inputs"

set init_verilog "${DATA_DIR}/conf.v"

set init_top_cell sar10b_v2

set init_oa_ref_lib $oareflib

++++++++++++++++++++++++++++++

After that you create a library called "test1", in which you will be saving the
design after placement etc.

You need to set this library as design library so that tool understands the
hierarchy library/cell/view.

To set the library as design library use following command

set init_oa_design_lib "test1"

After this setting, tool will not give the warning message (IMPOAX-1625) during saveDesign.

IMPOAX-1751

NAME

IMPOAX-1751

SUMMARY

The WSP purpose '%s' specified by user through 'setOaxMode -wsspdPurpose' is not found in OpenAccess technology. default global WSP will be read from cellview or technology.

DESCRIPTION

Tool reads WSP with purpose either specified through 'setOaxMode -wsspdPurpose' or read default WSP. Make sure either you provide correct purpose or default WSP will be read.

IMPOAX-1753

NAME

IMPOAX-1753

SUMMARY

WSPs can not be saved in OpenAccess database. We can not create purpose '%s' in technology, because the technology database associated with library '%s' is readonly.

DESCRIPTION

Since the technology database needs to be incrementally updated, the recommended method is to create

local technology database in design library either using 'createLib -referenceTech' or 'setOaxMode -libCreateMode reference' option. For example:

createLib myLib -referenceTech myRefLib

set init_oa_design_lib myLib

Or

setOaxMode -libCreateMode reference

Then define the place and route technology rules in myRefLib by importing a technology LEF. This creates a local technology database in the design library that can be modified incrementally. Overall, when setting up your mixed-signal design environment we recommend using a Base PDK which contains the base technology file and an incremental technology database (ITDB) which references the

Base PDK. The ITDB contains the information for physical design and can be updated, while the Base PDK can remain read-only.

IMPOAX-5110

NAME

IMPOAX-5110

SUMMARY

Default Rule '%s' is not found in the technology library (%s). The default rule was specified using the global variable init_oa_default_rule, check the spelling to confirm that constraint group exists in the technology library. Either correct the init_oa_default_rule specification or update the technology library to contain a valid LEFDefaultRouteSpec.

DESCRIPTION

This error is caused by a missing LEFDefaultRouteSpec or not properly referencing the library which defines the LEFDefaultRouteSpec. To debug this do the following.

First, use Virtuoso to output an ascii version of the technology file from the ITDB (techLoadDump -d gsclib090 output.ascii). It should contain a LEFDefaultRouteSpec constraint group as shown below. This defines the rules for physical design:

;(group [override])

;(----- ----------)

```
( "LEFDefaultRouteSpec" nil


spacings(

( minWidth "Cont" 0.12 )

) ;spacings


routingGrids(

( horizontalPitch "Metal1" 0.29 )

( verticalPitch "Metal1" 0.29 )

( horizontalOffset "Metal1" 0.145 )

( verticalOffset "Metal1" 0.145 )

) ;routingGrids

...
```

Also, verify it references the base technology file. For example, you can see it references gpdk090 below:

```
controls(

techVersion("1.0")

refTechLibs(

; techLibName

; -----------

"gpdk090"

) ;refTechLibs


) ;controls
```

Lastly, when reading the design into tool, make sure you specify the OpenAccess reference library:

In *.global file:

```
set init_oa_ref_lib {gsclib090}
```

IMPOAX-6022

NAME

IMPOAX-6022

SUMMARY

The value 'VCE' for the -viewSubType argument is obsolete.

DESCRIPTION

The value 'VCE' for the -viewSubType argument is no longer supported. To avoid this warning and to ensure compatibility with future releases, update your script to use '-viewSubType VXL'.

IMPOAX-6024

NAME

IMPOAX-6024

SUMMARY

Error while %s %s. OA Exception: %s.

DESCRIPTION

This error often happens when you try to write an OpenAccess view while design is open in other session or Virtuoso, thus the database is locked. Use different view name or close other session or Virtuoso that open the same view.

IMPOGDS-391

NAME

IMPOGDS-391

SUMMARY

Line %d: Object Type '%s' specified with layer '%s' is not legal. The map file maybe being a DFII/Virtuoso map file. For a list of legal object types refer to the map file syntax in the User Guide.

DESCRIPTION

This error can occur due to the wrong layer Map file or the incorrect inputs specified to the StreamOut command. To resolve this warning, try few things:

1. Use the supported layer map file from the foundry.

2. Generate the generic layer map file from the Innovus.

Note: A generic mapping file from Innovus can be generated by running streamOut command without specifying a mapping file. It will create a generic map file named streamOut.map which you can then edit to map the layers to the required GDS layers.

IMPOGDS-392

NAME

IMPOGDS-392

SUMMARY

Unknown layer %s

DESCRIPTION

This message is triggered during command streamOut <filename> -mapFile <string> . If in the

specified map file a layer name is used that is not known from the LAYER statement of the LEF (or the respective the OA) technology file or GUI customer layer, then this warning is issued.

IMPOGDS-399

NAME

IMPOGDS-399

SUMMARY

Only %d layer(s) (%s) of a %s object is(are) specified in map file '%s'. A %s object needs 3 layers (%s %s %s) being specified at the same time in the map file. Add %s contruct(s) to the map file for the following layer(s): %s or remove %s construct(s) from the map file for the following layer(s): %s.

DESCRIPTION

While streaming out GDS, innovus streamOut reports the message. streamOut uses the object type VIA to map the bottom, top and via layer of via cells to GDS. So the map file must define VIA object types for all metal and via layers.

IMPOPT-132

NAME

IMPOPT-132

SUMMARY

Inverter '%s' was not deleted because it is not part of a back-to-back inverter pair, or because it is not possible to delete the inverter(s) due to fixed/dont_touch attributes.

DESCRIPTION

ecoDeleteRepeater can only delete inverters in back-to-back pairs. This message occurs when the

user has specified an inverter to be deleted, but a second inverter as part of a back-to-back inverter pair could not be found in the design, or any/both of the inverters have fixed/dont_touch attributes. Please refer to the documentation for ecoDeleteRepeater for more information.

IMPOPT-136

NAME

IMPOPT-136

SUMMARY

Cell '%s' does not exist in power domain '%s'.

DESCRIPTION

Possible reasons are :-

1. View definition does not bound the timing libraries containing this cell to this power domain.

2. CPF does not bound the timing libraries containing this cell to this power domain.

Use update_delay_corner command or modify CPF to update the timing libraries of this power domain.

IMPOPT-306

NAME

IMPOPT-306

SUMMARY

Found placement violations in the postRoute mode.

DESCRIPTION

This warning is issued when the tool while checking placement detects any placement violations during postRoute optimization flow.

In order to fix this issue the user needs to run 'checkPlace' command and correct all placement violations in specific and also it is advisable to correct the other remaining violations in general before proceeding further.

IMPOPT-310

NAME

IMPOPT-310

SUMMARY

Design density (%.2f%%) exceeds/equals limit (%.2f%%).

DESCRIPTION

This error comes when Design Global density exceeds the default or user limit.User can get rid of this error depending upon design stage.

1. If this error message comes during preCTS then most likely either the die area needs to increase or user needs to look at improving the placement in design.

2. If this error message comes during CTS (or postCTS) then quality of Clock Tree needs to be debugged specially if density increases a lot from preCTS to postCTS.

3. If this error message comes during postRoute user should specify list of Fillers and Decaps before optimization. This will ensure that optDesign swap filler/decap cells with other cells and do not use filler/decap cells during global density calculation.

IMPOPT-393

NAME

IMPOPT-393

SUMMARY

No noise libraries are specified, timing libraries will be used instead in order to perform the noise analysis which are not as accurate. To load the noise libraries use the 'create_library_set/update_library_set -si' command.

DESCRIPTION

Example:

An example of how to use the commands:

create_library_set -name lsCOM-1V \\

-timing [list stdcell_F_1V.lib ram_F.lib pad.lib] \\

-si [list stdcell_F_2.cdb ram_F.cdb pad.cdb]

update_library_set -name minLibs \\

-si {stdcell_CVF_1V.lib ram_CVF.lib pad.lib}

IMPOPT-519

NAME

IMPOPT-519

SUMMARY

No cells matching pattern '%s' were found.

DESCRIPTION

The setDontUse command could not find any cells matching the specified cell name pattern. Please check and correct the pattern.

Example:

The following example sets all library cells matching the sub-string 'BUFF' as don't use:

setDontUse *BUFF* true

IMPOPT-569

NAME

IMPOPT-569

SUMMARY

Design data is not loaded.

DESCRIPTION

A design must be loaded before running any optimization command.

Example:

The following command loads the saved design files from the test.enc database:

"source test.enc"

Alternatively see 'man restoreDesign' for further information.

IMPOPT-576

NAME

IMPOPT-576

SUMMARY

%d nets have unplaced terms.

DESCRIPTION

This message is issued when I/O pins connecting to signal nets are not placed or instances

connecting to nets are not placed. user can report unplaced I/O pins by running "checkPinAssignment -report_violating_pin -outFile viol_pins.rpt"

To report un-placed Instance user can run "checkPlace checkPlace.rpt" and review the file.

IMPOPT-600

NAME

IMPOPT-600

SUMMARY

No usable buffer and inverter has been found. At least one of them have to.

DESCRIPTION

You should check if the buffer(s)/inverter(s) are available in the timing libraries. If yes ensure footprint and function of buffer(s)/inverter(s) are defined properly in the library. To make buffer(s)/inverter(s) usable:

- define buffer(s)/inverter(s) in libraries

- do not set buffer(s)/inverter(s) as dont_use, both in libraries and in constraint file(.sdc file)

You can use reportDontUseCells command to reports cells that cannot be used for timing optimization. This command also reports the source of the timing constraint: the timing library file, timing constraint file, or the user (by specifying the setDontUse command).

In lower power designs verify the proper power domain binding has been done as following:

1. If your analysis views are defined in your CPF then commitCPF automatically creates delay corners for each analysis view of the name analysis_view_dc. For example, "create_analysis_view -name slow_PM01" will have a delay corner created named slow_PM01_dc. Innovus will automatically create the viewDefinition.tcl according to the CPF and bind the libraries to the respective delay corner and power domain.

2. If you have defined the MMMC definitions in a viewDefinition.tcl, you must define the complete MMMC information in the viewDefinition.tcl, which means that each power domain has "update_delay_corner -power_domain" to associate the delay corner to the power domains. There is no need to define the view in CPF.

If CPF has the views, commitCPF will create the info which viewDefinition.tcl does not have.

Example:

In older releases you will get SOCOPT-600, SOCOPT-596, SOCOPT-3000 and

SOCOPT-3001 for ENCOPT-600, ENCOPT-596, ENCOPT-3000 and ENCOPT-3001 messages respectively.

IMPOPT-616

NAME

IMPOPT-616

SUMMARY

Buffer insertion not successful. Reason: %s

DESCRIPTION

The error is generated when buffer insertion is not successful.

Possible reasons are :

-The buffer insertion affects a net which cannot be optimized. You can run"reportIgnoredNets -outfile ignored.rpt" to get a list of nets which cannot be optimized because they are clock nets, marked dont_touch, etc.

-The buffer insertion will change the port boundaries of a hierarchical instance which has hierarchical port constraints set by "setOptMode -keepPort keepPortHinstFile". You can run "getOptMode -keepPort#get_db opt_keep_ports" to see the setting.

-The default location for the added buffer is not compatible with the driver power domain. If you want to specify the location manually, you can use the -loc option.

-There may be an existing MSV violation on the net (the driver PD is incompatible with the sink PD). Maybe you want to insert an always on buffer,you can try and insert it with setting "setOptMode -addAOFeedThruBuffer true".

IMPOPT-622

NAME

IMPOPT-622

SUMMARY

Failed to open file %s!

DESCRIPTION

This is related to "setOptMode -sizeOnlyFile dont_touch.txt_003" ; This file is missing. Please make sure the file exist before running this command.

Example:

**ERROR: (ENCOPT-622): Failed to open file dont_touch.txt_003!

IMPOPT-624

NAME

IMPOPT-624

SUMMARY

No option provided for timeDesign. Use either -reportOnly or -prePlace | -preCTS | -postCTS | -postRoute| -signoff

DESCRIPTION

This error occurs when the timeDesign command is run without any option

To get rid of this error message user should do the following

Provide one of the following options :

-prePlace | -preCTS | -postCTS | -postRoute| -signoff

or -reportOnly

-reportOnly specifies the use of existing extraction and timing analysis data to generate timing reports. When you use this parameter, the software does not run extraction; instead it uses data that is already in memory.

* -reportOnly is not honored when used with -prePlace.

* -idealClock is not honored when used with -reportOnly.

* -signOff is honored when used with -reportOnly. This is used to run a signoff timing analysis based on external SPEF files.

Note: Specifying -preCts, -postCts, or -postRoute is optional with -reportOnly.

Example:

<CMD> timeDesign -hold -outDir tmp

**ERROR: (ENCOPT-624): You have to add either -reportOnly or -prePlace | -preCTS | -postCTS | -postRoute| -signoff option.

Usage: timeDesign [-help] [-batch] [-drvReports] [-expandReg2Reg]

[-expandedViews] [-hold] [-idealClock] [-ilm]

[-noIlm] [-numPaths <integer>] [-outDir <string>]

[-pathreports] [-prefix <string>] [-proto]

[-reportOnly] [-si] [-slackReports]

[-timingDebugReport] [-useTransitionFiles]

[-prePlace | -preCTS | -postCTS | -postRoute |

-signOff]

IMPOPT-628

NAME

IMPOPT-628

SUMMARY

No equivalent cell found in the library for the substitution. Use "%s false" to allow the swapping of cells if the two cells are of different functionality.

DESCRIPTION

User is trying to swap the existing cell with the new cell having different functionality (characterized by footprint) using the change_cell command.

E.g. Buffer to inverter, buffer to delay cells having different footprints.

IMPOPT-629

NAME

IMPOPT-629

SUMMARY

No alternate cell exists in the library for current power domain. To ignore MSV checks, specify '%s false'.

DESCRIPTION

This error comes during ECO resize when tool looks for the correct library cell.

The problem is occurring because of missing definition of the cell in liberty file.

Possible reasons :

Wrong cell function.

Wrong observable power domains.

IMPOPT-655

NAME

IMPOPT-655

SUMMARY

No usable delay or buf cells with footprint "%s" or "%s".

DESCRIPTION

This warning message pops-up when the user tries to run optDesign without specifying holdFixingCells list through setOptMode command and the tool finds that there are no usable delay or buffer cells in the library that can be used for hold fixing. The reason could be that these cells have a "dont_use" attribute assigned to them.

Example:

In order to resolve this issue and to avoid this warning message the user needs to specify hold fixing cells through "setOptMode -holdFixingCells" and make sure the specified cells in this list doesn't have a "dont_use" attribute

IMPOPT-661

NAME

IMPOPT-661

SUMMARY

The netlist is not uniquified. Optimization requires that hierarchical modules to be optimized have unique instances.

DESCRIPTION

Optimization requires unique instances of hierarchical modules. To uniquify the netlist run the uniquifyNetlist executable outside of Innovus then import the resulting uniquified netlist into Innovus.

If you are running the post-assembly closure (PAC) flow using master/clone partitions the master/clone partitions must either be ILM modeled or set to read only. You can use 'setModuleView -partition partitionName -type readOnly' to do this.

Example:

To uniquify a netlist the separate uniquifyNetlist command can be used as follows:

uniquifyNetlist -top top unique_output.v non_unique_input.v

IMPOPT-665

NAME

IMPOPT-665

SUMMARY

%s : Net has unplaced terms or is connected to uplaced instances in design.

DESCRIPTION

This warning message is issued during optimization if there are nets connected to any unplaced I/O pins or unplaced instances in the design. The unplaced instances can be reported by running checkPlace command and unplaced I/O's can be reported by running 'checkPinAssignment -report_violating_pin' command.Once these issues are fixed the warning message will not be reported.

IMPOPT-800

NAME

IMPOPT-800

SUMMARY

Turning off Critical Region Resynthesis. Reason: %s

DESCRIPTION

Either genus is not available in the path, or the version is not compatible with this innovus version or the genus licensing is not properly setup or some other error (detailed after "Reason:") caused the genus workers to not be properly setup.

A valid genus executable must be setup in the path for this feature to work.

IMPOPT-801

NAME

IMPOPT-801

SUMMARY

Genus executable not found in the path%s.

DESCRIPTION

Unix variable $path or $PATH (depending on your shell) must include a directory containing a genus executable; alternatively, you can specify it in the innovus shell as:

append env(PATH) ":<directory>

IMPOPT-802

NAME

IMPOPT-802

SUMMARY

Genus returned unmapped primitive '%s'.

DESCRIPTION

A genus worker was not able to properly remap some logic. The error is gracefully handled by the tool and the move causing it will be discarded. No bad logic or adverse side effect should be expected.

However, this can be considered an internal error and should be notified to Cadence support.

IMPOPT-803

NAME

IMPOPT-803

SUMMARY

Cannot synchronize with genus workers after %d seconds.

DESCRIPTION

The initial handshake with the genus workers did not complete successfully. This can occur if the genus process is killed or there is some error processing the libraries in genus.

This can be considered an internal error and should be notified to Cadence support.

IMPOPT-2901

NAME

IMPOPT-2901

SUMMARY

Design is not placed. Place the design before running

DESCRIPTION

Use place_design or place_opt_design to place the design.

IMPOPT-2902

NAME

IMPOPT-2902

SUMMARY

Insufficient number of usable buffers %s

DESCRIPTION

Please use get_db to make sure the .dont_use attribute is set to false for the buffer cells you want to use

IMPOPT-2903

NAME

IMPOPT-2903

SUMMARY

Insufficient number of usable inverters %s

DESCRIPTION

Please use get_db to make sure the .dont_use attribute is set to false for the inverter cells you want to use

IMPOPT-2904

NAME

IMPOPT-2904

SUMMARY

Power domain %s does not have available always-on buffers to use.

DESCRIPTION

It is because either always-on buffer is set to don't use/don't touch, or the 2nd power/ground is disabled in power intent file, or always-on buffer liberty is not bound to the domain. Fix it accordingly if always-on buffer is needed in this domain for buffering.

IMPOPT-2907

NAME

IMPOPT-2907

SUMMARY

hInst %s Is marked dont_touch, no buffers can be added in the hInst.

DESCRIPTION

Please use set_db to update the .dont_touch attribute

IMPOPT-2909

NAME

IMPOPT-2909

SUMMARY

Maximum length %.3f is too short. It is less than the optimal drive distance of %.3f and may result in excessive buffering.

DESCRIPTION

Check the optimal drive distance for each layer, and check that the maxLength is greater than the value with some margin built in.

IMPOPT-3000

NAME

IMPOPT-3000

SUMMARY

Buffer footprint is not defined or is an invalid buffer footprint.

DESCRIPTION

This warning message is issued when optimization engine does not find any buffers.

In order to fix this warning message the following things should be checked.

1. Buffer(s) are available in the timing libraries.

2. Footprint and function of buffer(s) are defined correctly in the library.

Buffers should contain only two signal pins. The power and ground pins should be defined properly

with USE POWER and USE GROUND in the LEF.

3. Buffer(s) are not set to dont_use in libraries or in constraint file(.sdc file).

Use "get_db lib_cells -if {.is_dont_use == true }" or run "report_preserves" command.

4. In low power designs proper binding of buffer libraries to the respective delay corner and power domain is done.

IMPOPT-3001

NAME

IMPOPT-3001

SUMMARY

Inverter footprint is not defined or is an invalid inverter footprint.

DESCRIPTION

This warning message is issued if optimization didn&'t find any Inverter.

In order to fix this warning message the following things can be checked.

1. Inverter(s) are available in the timing libraries.

2. Footprint and Function of inverter(s) are defined properly in the library.

Inverter(s) should contain only two signal pins. The power and ground pins should be defined properly with USE POWER and USE GROUND in the LEF.

3. Inverter(s) are not set to dont_use in libraries or in constraint file(.sdc file).

Use "get_db lib_cells -if {.is_dont_use == true }" or run "report_preserves" command.

4. In low power designs inverter libraries are binded to the respective delay corner and power domain is done.

IMPOPT-3025

NAME

IMPOPT-3025

SUMMARY

Optimization Restructuring is disabled because the tool cannot find cells needed for this type of optimization.

DESCRIPTION

Optimization restructuring need to have access to cells functionalities such as ANDs/ORs/Inverters.

Check the functions of the cells that are available to the tool; you can double check the dont_use settings for example.

IMPOPT-3034

NAME

IMPOPT-3034

SUMMARY

Optimization process capabilities limited due to %d assigned nets.

DESCRIPTION

The message is to inform the user that there are assign statements in the netlist which optDesign cannot optimize. If these are not on timing critical paths then it is likely okay assuming your flow allows for assign statements. Often designers do not want assign statements and therefore remove them during synthesis or in Innovus System using the setDoAssign command.

IMPOPT-3035

NAME

IMPOPT-3035

SUMMARY

Optimization process capabilities limited due to 1 assigned net.

DESCRIPTION

This warning message is issued by optDesign in case there is one assign net in the design and there is no way to optimize it.

setDoAssign command can be used to remove assign statements in the design and replace them with a buffer when importing the netlist.

IMPOPT-3040

NAME

IMPOPT-3040

SUMMARY

skewClock will overwrite scheduling file %s

DESCRIPTION

This warning comes when skewClock is run in preCTS mode. To get rid of this warning user should specify a scheduling file name using setSchedulingFile command.

Example:

setSchedulingFile scheduling_file.cts

skewClock

IMPOPT-3050

NAME

IMPOPT-3050

SUMMARY

setUsefulSkewMode -useCells is pointing to the cell %s which is set as dont_use in the library

DESCRIPTION

SkewClock command is potentially going to insert a cell which has been marked as dont_use in the library. You should double check that this is your intent.

Example:

setUsefulSkewMode -useCells {CLKBUFX8 CLKBUFX12 CLKINVX8 CLKINVX12}

setOptMode -usefulSkew true

optDesign

check for all don't use cells : get_lib_cells * -filter "is_dont_use == true" or dbGet [dbGet head.allCells.isDontUse 1 -p].name

IMPOPT-3058

NAME

IMPOPT-3058

SUMMARY

Cell %s/%s already has a dont_use attribute %s.

DESCRIPTION

This message occurs because you set dont_use attribute on a cell that has same value as what you are specifying.

This is not harmful and can be ignored if the value of dont_use attribute is what you want it to be.

Example:

* The following example sets library cell AND2 as dont_use:

innovus> setDontUse libSlow/AND2 true

innovus> set_dont_use libSlow/AND2 true

* The following example turns off dont_use attribute of library cell AND2:

innovus> setDontUse libSlow/AND2 false

innovus> set_dont_use libSlow/AND2 false

IMPOPT-3080

NAME

IMPOPT-3080

SUMMARY

All delay cells are dont_use. Buffers will be used to fix hold violations.

DESCRIPTION

This Warning message means all delay cells in the loaded libraries have "dont_use" attribute and the tool will use only Buffer cells to fix hold violations

Example:

To fix this issue and to avoid the Warning message the user can either set "set_dont_use false *dlylibCell*" in the SDC or if he wants do the same in the Innovus shell for MMMC design can run "set_interactive_constraint_modes [all_constraint_modes -active]" followed by "set_dont_use" command and then re-run "optDesign -hold

IMPOPT-3115

NAME

IMPOPT-3115

SUMMARY

Netlist is not uniquified, optimization will be ignoring nets around modules that are not uniquified.

DESCRIPTION

Nets connected to non uniquified modules will be ignore for optimization.

You can Run uniquifyNetlist outside Innovus environment in a unix shell to generate a uniquified netlist. You can also direct the tool to automatically uniquify the design after flattening by setting global variable init_design_uniquify to 1.

To see if the design is uniquified run checkUnique.

IMPOPT-3121

NAME

IMPOPT-3121

SUMMARY

No usable buffer cell.

DESCRIPTION

This warning message is related to MMMC setup. If the standard cell library is missing from any library set or when creating a delay corner the "-library_set" option is missing, then any active view that uses the library set will not have a buffer cell defined. So while running optDesign the tool issues a warning saying no usable buffer cell is found.

Example:

In order to avoid this Warning message the user needs to make sure that when library sets are defined in the viewDefinition.tcl, make sure that the library set for all active views are properly defined and all libraries are included.

IMPOPT-3129

NAME

IMPOPT-3129

SUMMARY

Unable to delete instance %s.

DESCRIPTION

This warning message is issued when the user tries to delete a buffer using 'ecoDeleteRepeater' command.

Possible causes for the error:

- inst is dont_touch'ed or FIXED

- any net connect to the inst is dont_touch'ed

- library cell of the inst is dont_touch'ed

- the inst is an inverter.

Example:

In order to brute force the deletion: feedthrough buffer can be deleted using dbDeleteBuffer command. An example command would be 'dbDeleteBuffer [dbGetInstByName inst_name]'

IMPOPT-3135

NAME

IMPOPT-3135

SUMMARY

ecoAddRepeater -relativeDistToSink works with -term or -net with 1-sink net on routed design.

DESCRIPTION

This error message comes when user runs ecoAddRepeater -relativeDistToSink with value other than 1 on a multi fanout net for buffering multiple sink terms.

Example:

ecoAddRepeater -cell C12T32_LL_BFX33_P10 -net SOCE_PRECTS_NET_INCR_SETUP_DRV_FE_OFCN1278_SOCE_INPUT_BOUNDARY_ISOLATION_4949_tst_io_testmode_N -relativeDistToSink 0.5

**ERROR: (ENCOPT-3135): ecoAddRepeater -relativeDistToSink works with -term or -net with 1-sink net on routed design.

IMPOPT-3142

NAME

IMPOPT-3142

SUMMARY

Could not open the file %s. Option '-reportIgnoredNets' will be ignored.

DESCRIPTION

The message occurs because Innovus can not write the file that you have specified with '-

reportIgnoredNets'. Please check if you have necessary permission to write the file on target directory (usually working directory) and have sufficient disk space or if you specify sub-directory - that it exists.

Example:

* The following example checks if you have permission to write on current working directory:

innovus 20> file writable [pwd]

1

* The following example checks if you have sufficient disk space:

innovus 21> df -kH [pwd]

Filesystem Size Used Avail Use% Mounted on

/disk/dir 2.2T 2.0T 271G 88% /disk/dir

IMPOPT-3144

NAME

IMPOPT-3144

SUMMARY

Could not open the file %s. Option '-outFile' will be ignored.

DESCRIPTION

The message occurs because Innovus can not write the file that you have specified with '-outFile'. Please check if you have necessary permission to write the file on target directory and have sufficient disk space or if you specify sub-directory - that it exists.

Example:

* The following example checks if you have permission to write on current working directory:

innovus 20> file writable [pwd]

1

* The following example checks if you have sufficient disk space:

innovus 21> df -kH [pwd]

Filesystem Size Used Avail Use% Mounted on

/disk/dir 2.2T 2.0T 271G 88% /disk/dir

IMPOPT-3180

NAME

IMPOPT-3180

SUMMARY

Could not open the file %s to report ignored nets.

DESCRIPTION

The message occurs because you may not have permission to write a file or run out of disk space. Please check if you have necessary permission to write a file on target directory (usually the working directory) and have sufficient disk space or if you specify sub-directory - that it exists.

Example:

* The following example checks if you have permission to write on current working directory:

innovus 20> file writable [pwd]

1

* The following example checks if you have sufficient disk space:

innovus 21> df -kH [pwd]

Filesystem Size Used Avail Use% Mounted on

/disk/dir 2.2T 2.0T 271G 88% /disk/dir

IMPOPT-3186

NAME

IMPOPT-3186

SUMMARY

*** switching analysis mode to "setAnalysisMode -usefulskew true" so that newly generated latencies are taken in account by the timing engine***

DESCRIPTION

This warning message is issued when 'setOptMode -usefulSkew true' and the user tries to run optDesign command.

Example:

When usefulSkew is set to true the tool produces scheduling and latency files before CTS runs, or adds buffers and inverters after CTS, just as skewClock does. This parameter sets 'setAnalysisMode -usefulSkew true', so that timing analysis can read the latency file.

IMPOPT-3195

NAME

IMPOPT-3195

SUMMARY

Analysis mode has changed.

DESCRIPTION

You have this message because Innovus temporarily changes the analysis mode for optimization use. This is usually not harmful and you may ignore this message.

One of these 5 analysis mode changes will cause this:

-clkSrcPath true

-clockPropagation sdcControl

-usefulSkew false

-virtualIPO false

-skew true

IMPOPT-3213

NAME

IMPOPT-3213

SUMMARY

The netlist contains multi-instanciated modules. The optimization engine will consider these modules as dont touch. Uniquify the netlist to get better quality of results.

DESCRIPTION

optDesign requires the netlist to be unique. If you are running the post-assembly closure (PAC) flow using master/clone partitions, the master/clone partitions must either be ILMs or set to read only (setModuleView -partition partitionName -type readOnly).

To uniquify the netlist, run uniquifyNetlist outside of Innovus System. Then import the resulting, uniquified netlist into Innovus System.

Example:

uniquifyNetlist -top top non_unique.v unique.v

From 10.1USR2 the ordering of input and output files are different. In other words first the output file and then non-unique input file:

uniquifyNetlist -top top unique.v non_unique.v

IMPOPT-3225

NAME

IMPOPT-3225

SUMMARY

SpefIn flow is used. Re-extract RC and spefIn for accuracy.

DESCRIPTION

This warning message is issued when the user tries to run optimization through spef based flow. For each corer spef needs to be read in separately, if spef is missing for any corner tool will issue above warning and will re-extract Parasitics.

spefIn command has an option to read corner spef file using '-rc_corner' option. For each of the corner in the design user needs to read in separate spef files before performing spef based optimization.

IMPOPT-3313

NAME

IMPOPT-3313

SUMMARY

Skipping %s which is an assign net.

DESCRIPTION

This message pops-up when the user tries to run 'attachIOBuffer' command on an assigned net.

In order to avoid this Warning message the user needs to first set 'setDoAssign on -buffer buf_name' before importing the design and then run 'attachIOBuffer' command.

IMPOPT-3314

NAME

IMPOPT-3314

SUMMARY

Skipping net '%s' which has fewer than two connected pins.

DESCRIPTION

This warning is issued by the 'attachIOBuffer' command when nets with only one or zero connected pins are encountered. 'attachIOBuffer' does not add buffers on such nets.

IMPOPT-3315

NAME

IMPOPT-3315

SUMMARY

Common path pessimism removal is not enabled even though timing derates are applied. This can cause optimization to see more pessimistic timing than expected. To enable CCPR for both setup and hold use "setAnalysisMode -cppr both".

DESCRIPTION

CPPR (Common Path Pessimism Removal) removes pessimism from clock paths that have a portion of the clock network in common between launch and capture paths. This error message indicates that timing derates are applied, so that the clock part of the launch and capture paths may be timed differently, but that removal of resulting pessimism in the common clock path is not enabled.

Example:

setAnalysisMode -analysisType onChipVariation

setAnalysisMode -cppr both

IMPOPT-3318

NAME

IMPOPT-3318

SUMMARY

Missing -preCTS|-postCTS|-postRoute option.

DESCRIPTION

This warning message is issued when the user tries to run optDesign command without specifying the design stage, meaning preCTS, postCTS or postRoute.

Example:

This message can be avoided by running optDesign with correct options depending upon on the stage of the design. As an example if the clock tree is not placed in the design then 'optDesign -preCTS' can be run to optimize the design for the set-up.

IMPOPT-3319

NAME

IMPOPT-3319

SUMMARY

The -hold option is not available with -preCTS.

DESCRIPTION

This warning message is issued when the user tries to run -preCTS optimization in hold mode and the command exits without running preCTS optimization. The '-hold' option cannot be specified with preCTS optimization.

In order to avoid this warning message '-hold' option should be removed while running preCTS optimization meaning only setup optimization makes sense at preCTS stage.

IMPOPT-3326

NAME

IMPOPT-3326

SUMMARY

The -drv option not allowed in -hold mode.

DESCRIPTION

This warning message is issued when the user tries to run optDesign in hold mode with '-drv' option. The tool issues the warning and comes out without running optimization.

When running hold fixing, optDesign will maintain exiting setup and drv in the setup recovery step.

Example:

This issue can be fixed by removing '-drv' option. As an example the user cannot run 'optDesign -postCTS -hold -drv', the correct command options are 'optDesign -postCTS -hold'

IMPOPT-3327

NAME

IMPOPT-3327

SUMMARY

The -drv option not allowed with -incr option.

DESCRIPTION

This warning message is issued when user tries to run drv fixing with -incr option and the command exits without performing DRV fixing. The DRV fixing cannot be run with -incr option.

Example:

The correct command will be 'optDesign -postCTS -drv' or running DRV fixing on selected nets/terms by specifying them in a file.

IMPOPT-3328

NAME

IMPOPT-3328

SUMMARY

The -incr option is ignored with -hold option.

DESCRIPTION

This warning message is issued when hold optimization is run with '-incr' option. The tool issues this warning message and performs regular hold fixing on the design.

Example:

In order to avoid this warning message '-incr' option can be avoided while running hold fixing.

IMPOPT-3396

NAME

IMPOPT-3396

SUMMARY

Cannot determine how to connect %s. There is a mismatch in number of pins between the cells being swapped.

DESCRIPTION

Here is no direct way to do this in Innovus System currently. The recommendation is to handle this in RTL Compiler.

IMPOPT-3465

NAME

IMPOPT-3465

SUMMARY

The buffer cells were automatically identified. The command setBufFootPrint is ignored. If you want to force the tool to honor this setting, you have to load a footprint file through the loadFootPrint command.

DESCRIPTION

This warning message is issued when the user uses footprintless flow and tries to run the command setBufFootPrint to specify the buffer cell footprint. In order to use footprint flow the user needs to specify the footprints using loadFootPrint command and then run setBufFootPrint command, this will fix the warning issue.

IMPOPT-3466

NAME

IMPOPT-3466

SUMMARY

The inverter cells were automatically identified. The command setInvFootPrint is ignored. If you want to force the tool to honor this setting, you have to load a footprint file through the loadFootPrint command.

DESCRIPTION

This warning message is issued when the user uses footprintless flow and tries to run the command setInvFootPrint to specify the Inverter cell footprint. In order to use footprint flow the user needs to specify the footprints using loadFootPrint command and then run setInvFootPrint command, this will fix the warning issue.

IMPOPT-3467

NAME

IMPOPT-3467

SUMMARY

The delay cells were automatically identified. The command setDelayFootPrint is ignored. If you want to force the tool to honor this setting, you have to load a footprint file through the loadFootPrint command.

DESCRIPTION

This warning message is issued when the user uses footprintless flow and then tries to runs setDelayFootPrint command to specifies the delay cell footprints. In order to use footprint flow the

user needs to specify footprints using loadFootPrint command and then run setDelayFootPrint command, this will remove the warning issued.

IMPOPT-3468

NAME

IMPOPT-3468

SUMMARY

The command loadFootPrint has disabled the footprintless flow. Now using the classes of equivalence defined in the footprint file.

DESCRIPTION

This message is seen when the command "loadFootPrint" is executed. Innovus by default follows the footprintless flow. If the user want to define the foot prints and disable the footprintless flow, it can be done using the command"loadFootPrint".

Example:

<CMD> loadFootPrint -infile modified_foot_print.file

**WARN: (ENCOPT-3468): The command loadFootPrint has disabled the footprintless flow. Now using the classes of equivalence defined in the footprint file.

Clearing footprints for all libraries

Loading footprints for all corners.

IMPOPT-3481

NAME

IMPOPT-3481

SUMMARY

There is no buffer defined for the following power domain(s):%s.

DESCRIPTION

This warning message is issued while running optDesign command in preCTS/postCTS/etc..., if there are library binding issues with power domain and the cells have dont_use attribute

Example:

In order to fix this issue the user needs to check if the library binding with respective Power domain is o.k, this can be verified by running &'verifyPowerDomain -bind &' and also ensure that the required cells are available for optimization, meaning there are no dont_use attribute associated to them

IMPOPT-3531

NAME

IMPOPT-3531

SUMMARY

No usable inverter has been found. It could be that there are no inverters defined in the libraries or all inverters are set as dont-use. Ensure that allrequired libraries have been loaded & check the dont-use settings for inverter cells.

DESCRIPTION

Example:

To get a list of all cells marked dont-use: reportDontUseCells To disable a dont-use? on a library cell: setDontUse <cell-name> false

IMPOPT-3532

NAME

IMPOPT-3532

SUMMARY

No usable buffer has been found. It could be that there are no buffers defined in the libraries or all buffers are set as dont-use. Ensure that all required libraries have been loaded & check the dont-use settings for buffer cells.

DESCRIPTION

To get a list of all cells marked dont-use: reportDontUseCells

To disable a dont-use? on a library cell: setDontUse <cell-name> false

IMPOPT-3535

NAME

IMPOPT-3535

SUMMARY

OptDesign command could not find any buffers which could be used for optimization. It could be that" "a) There are no buffers in libraries (Ensure that all required libraries have been loaded) OR " "b) All buffers are set as dont use (Check the dont use settings for buffer cells within the libraries).

DESCRIPTION

For example:

To get a list of all cells marked dont-use, issue command:

reportDontUseCells

To disable a dont-use on a library cell, issue command:

setDontUse <cell_name> false

IMPOPT-3543

NAME

IMPOPT-3543

SUMMARY

Option setOptMode -resizeShifterAndIsoInsts is set to true (default false).

DESCRIPTION

This warning message is issued when 'resizeShifterAndIsoInsts' is set to true in setOptMode. This means even if they are marked as dont_touch, optDesign may resize some shifter and isolation cells for timing optimization

Example:

Don't touch instances and are not changed during timing optimization. When this parameter is set to true, the shifters and isolation cells are resized for timing optimization by using optDesign.

IMPOPT-3547

NAME

IMPOPT-3547

SUMMARY

Net %s is connected to unplaced instance(s). Drv(s) cannot be fixed on it.

DESCRIPTION

Please ensure that the design is legally placed before running optimization.

Use the checkPlace command.

Example:

To report the instances to which a net connects:

dbGet [dbGet -p top.nets.name <net-name>].instTerms.inst.name.

To report a list of unplaced instances:

dbGet [dbGet -p top.insts.pStatus unplaced].name.

IMPOPT-3560

NAME

IMPOPT-3560

SUMMARY

SDF based flow is used. The final timing report summary cannot be printed out in this mode.

DESCRIPTION

SDF based flow does not report the final timing summary after optimization. This is due to the fact the original SDF(s) are not valid after optimization and have to be regenerated after optimization.

Example:

To report the timing after optimization, regenerate the SDFs, load them and time the design:

read_sdf -view <view1> ...

read_sdf -view <view2> ...

timeDesign -reportOnly

IMPOPT-3563

NAME

IMPOPT-3563

SUMMARY

"setTrialRouteMode -keepExistingRoutes true" is not supported by optDesign/timeDesign. This trialRoute option will be disabled.

DESCRIPTION

The optDesign or timeDesign commands cannot honour "setTrialRouteMode -keepExistingRoutes true", the reason being the design is at pre-route stage and these commands are going to re-run trialRoute and estimate parasitics hence existing routes in the design cannot be preserved. In order to avoid this message either the user needs to change "setTrialRouteMode -keepExistingRoutes false" before running optDesign or timeDesign command or else the tool will automatically disable it.

IMPOPT-3579

NAME

IMPOPT-3579

SUMMARY

Cell '%s' is marked as dont_touch. %s command will skip this cell.

DESCRIPTION

This warning message is issued by an attempt to run the interactive ECO command on a dont_touch library cell. This can be overridden with "setEcoMode -honorDontTouch false". Alternatively adjust the dont_touch status on the cell.

IMPOPT-3580

NAME

IMPOPT-3580

SUMMARY

Cell '%s' is marked as dont_use. %s command will skip this cell.

DESCRIPTION

This warning message is issued by an attempt to run the interactive ECO command on a dont_use library cell. This can be overridden with "setEcoMode -honorDontUse false". Alternatively adjust the dont_use status on the cell.

IMPOPT-3581

NAME

IMPOPT-3581

SUMMARY

Instance '%s' is marked as dont_touch. %s command will skip this instance.

DESCRIPTION

This warning message is issued by an attempt to run the interactive ECO command on a dont_touch instance. This can be overridden with "setEcoMode -honorDontTouch false". Alternatively adjust the dont_touch status on the instance.

IMPOPT-3585

NAME

IMPOPT-3585

SUMMARY

Instance '%s' is marked as fixed. %s command will skip this instance.

DESCRIPTION

This error comes when user runs an ECO command on a FIXED instance. To get rid of this error message user should specify instance whose placement status is not FIXED. User can also use dbSet command to change placement status of instance from FIXED to PLACED.

IMPOPT-3588

NAME

IMPOPT-3588

SUMMARY

%s is not a cell!

DESCRIPTION

When trying to change the cell for a specific instance using ecoChangeCell. It reports that the specific cell "is not a cell!"

The cell exists in the LEF. ecoChangeCell requires that the cell you specify, cellXYZ in this example, must be defined in the timing library. If it does not have a timing definition for it then this message will get issued. Create a timing definition in the .lib for this cell to resolve this issue.

Use checkDesign to confirm if all cells in the design has all timing library bounded.

IMPOPT-3593

NAME

IMPOPT-3593

SUMMARY

The cell %s is not defined in any library file. If you wish to use this cell please ensure a timing library file defining this cell is bound to each timing analysis-view.

DESCRIPTION

Example:

To see a list of defined timing analysis-views:

all_analysis_views | all_setup_analysis_views | all_hold_analysis_views

To see the library-sets defined for each analysis-view:

get_delay_corner [get_analysis_view <analysis-view> -delay_corner] -library_set | -early_library_set | -late_library_set

To see the list of library files defined for each library-set:

get_library_set <library-set> -timing

Alternatively check your &'viewDefinition.tcl&' file.

IMPOPT-3594

NAME

IMPOPT-3594

SUMMARY

'%s' is inside ILM block. %s command will skip it.

DESCRIPTION

This message comes when user tries to use an ECO command on an ILM object. ILM objects are read-only and cannot be modified by ECO commands.

Example:

<CMD> ecoDeleteRepeater -inst FE_OFC4333_des_interface_n_3736

**ERROR: (IMPOPT-3594):

'FE_OFC4333_des_interface_n_3736' is inside ILM block. ecoDeleteRepeater command will skip it.

IMPOPT-3596

NAME

IMPOPT-3596

SUMMARY

Running 'timeDesign -postRoute -si (-hold)' with 'setAnalysisMode -analysisType bcwc' is not recommended.

DESCRIPTION

Running &'timeDesign -postRoute -si (-hold)&' with &'setAnalysisMode -analysisType bcwc&' might lead to incorrect timing analysis results. This is because the SI delay push-outs (or pull-ins for -hold mode) on the clock nets get annotated to both the launch and the capture clock paths resulting in optimistic slacks to be reported. To get accurate timing analysis results, use &'setAnalysisMode -analysisType onChipVariation&', which requires the design to be run in either in multi-mode multi-corner (MMMC) or single-mode single-corner (SMSC) mode. For more information, see the &'Specifying the MMMC Environment&' section in the &'Optimizing Timing&' chapter of the Innovus User Guide.

IMPOPT-3600

NAME

IMPOPT-3600

SUMMARY

The setSiMode "-analysisType pessimistic" can only be set in conjonction with the setAnalysisMode -analysisMode -onChipVariation

DESCRIPTION

To get accurate SI timing analysis results, use &"setAnalysisMode -analysisMode onChipVariation&", which requires the design to be set either in multi-mode multi-corner (MMMC) or single-mode single-corner (SMSC) mode. If the MMMC and OCV modes are not enabled, and if the &"optDesign -postRoute -si&" and &"timeDesign -postRoute -si&" commands will exit with an error.

Example:

<CMD> setDelayCalMode -engine Aae

<CMD> setAnalysisMode -analysisType single

<CMD> setSiMode -analysisType pessimistic

Should be changed to :

<CMD> setDelayCalMode -engine Aae

<CMD> setAnalysisMode -analysisType onChipVariation

<CMD> setSiMode -analysisType pessimistic

IMPOPT-3602

NAME

IMPOPT-3602

SUMMARY

The specified path group name %s is not defined.

DESCRIPTION

This error occurs when an unknown path group name is specified to

setPathGroupOptions. Check the name or create the path group as required.

Example:

The following example defines a path group and sets the path group optimization effort level to high:

group_path -name PATH_GROUP_A -to [get_pins ff1/D]

setPathGroupOptions PATH_GROUP_A -effortLevel high

IMPOPT-3610

NAME

IMPOPT-3610

SUMMARY

Multi-CPU optimization is only supported in setDistributeHost -local mode.

DESCRIPTION

Multi-Cpu optimization supports multi-threading on the local host only. This can be setup using setDistributeHost -local and setMultiCpuUsage -localCpu <num of cpus>

Example:

setDistributeHost -local

setMultiCpuUsage -localCpu <num of cpus>

IMPOPT-3611

NAME

IMPOPT-3611

SUMMARY

Multi-CPU optimization is disabled.

DESCRIPTION

This option is for internal use only. To enable the multi-cpu optimization use setMultiCpuUsage -enable opt

Example:

To enable multi-cpu optimization use: setMultiCpuUsage -enable opt

To disable multi-cpu optimization use: setMultiCpuUsage -disable opt

IMPOPT-3626

NAME

IMPOPT-3626

SUMMARY

NanoRoute option "-routeWithTimingDriven" is set to "false" by user."optDesign" will automatically set this option to "true" in nanoRoute based flow.

DESCRIPTION

This warning message is issued while running preCTS optimization in NRGR based flow when '-routeWithTimingDriven' is set to false

IMPOPT-3629

NAME

IMPOPT-3629

SUMMARY

Option "-criticalRange <value>" for command setOptMode is obsolete and has been replaced by "-allEndPoints true|false".

DESCRIPTION

This message comes when user tries to use option "-criticalRange <value>" of setOptMode command with the latest version of the tool. In order to get rid of this message user should use setOptMode -allEndPoints true|false

IMPOPT-3631

NAME

IMPOPT-3631

SUMMARY

Option -criticalRange for the command setPathGroupOptions is obsolete and is being ignored.

DESCRIPTION

The message occurs because the option '-criticalRange <value>' for the command setPathGroupOptions is obsolete. Please update your script with 'setOptMode -allEndPoints <boolean>'.

Example:

The following example enables WNS/TNS optimization:

setOptMode -allEndPoints true

The following example enable WNS optimization only:

setOptMode -allEndPoints false

IMPOPT-3634

NAME

IMPOPT-3634

SUMMARY

reg2reg optimization will not be run because there are no reg2reg paths in the design.

DESCRIPTION

This warning message is issued during optimization when the design doesn't have clock definition meaning there are no &"create_clock&" statements in the SDC file. The issue can be resolved by fixing this problem.

IMPOPT-3638

NAME

IMPOPT-3638

SUMMARY

Cell %s is not defined in any timing analysis view. This cell will be marked dont_use.

DESCRIPTION

This warning comes when the cell %s defined by user does not exist in any timing analysis view.

To remove the warning user needs to check the following

1. Correct cell name is used.

2. Cell library is added to at least one timing analysis view. To review the library binding user can either check viewDefinition.tcl file or run the following commands

a) Use all_analysis_views | all_setup_analysis_views | all_hold_analysis_views to get the name of all analysis views.

b) Use get_delay_corner [get_analysis_view <analysis-view> -delay_corner]

-library_set | -early_library_set | -late_library_set to see the library-sets defined for each analysis-view.

c) Use get_library_set <library-set> -timing to see the list of library files defined for each library-set.

IMPOPT-3649

NAME

IMPOPT-3649

SUMMARY

Reset VT partitioning data

DESCRIPTION

Info message shown upon "setOptMode -reset -defineVtPartition"

Example:

innovus 23> setOptMode -reset -defineVtPartition

Reset VT partitioning data

0

IMPOPT-3654

NAME

IMPOPT-3654

SUMMARY

Could not find lib: %s, specified in custom VT file: %s, in the libset for power view (%s).

DESCRIPTION

User defined vt partitioning has a different name other than LVT, SVT and HVT.When user specifies a vt partition name as anything other these names, for example, MVT or OSVT or FVT , are not acceptable. The user defined vt partition names have to be either LVT, SVT or HVT only.

Example:

Could not find lib: OSVT, specified in custom VT file:

my_user_defined_VT_partitioning.txt, in the libset for power view (view_FUNC_MODE).

IMPOPT-3655

NAME

IMPOPT-3655

SUMMARY

%d standard cell libs (listed below) are missing in custom VT file. Please review, correct the custom VT file and try again. Cells in these libs will not be part of any VT partition:

DESCRIPTION

Example:

Assume the design has the below libs set:

Lib set:

GS70_S_105_1.1_1.1_CORE.db

GS70_S_105_1.1_1.1_CORE_CUSTOM.db

GS70_S_105_1.1_1.1_CORE_PM.db

GS70_S_105_1.1_1.1_CORE_PM_XSVT.db

GS70_S_105_1.1_1.1_CORE_XSVT.db

GS70_S_105_1.1_1.1_CORE_CUSTOM_XSVT.db

GS70_S_105_1.1_1.1_CORE_CUSTOM_OSVT.db

GS70_S_105_1.1_1.1_CORE_OSVT.db

GS70_S_105_1.1_1.1_CORE_PM_OSVT.db

They should be partitioned as follows in the custom VT file with no lib missing:

Custom VT file:

LVT

GS70_S_105_1.1_1.1_CORE.db

GS70_S_105_1.1_1.1_CORE_CUSTOM.db

GS70_S_105_1.1_1.1_CORE_PM.db

SVT

GS70_S_105_1.1_1.1_CORE_PM_XSVT.db

GS70_S_105_1.1_1.1_CORE_XSVT.db

GS70_S_105_1.1_1.1_CORE_CUSTOM_XSVT.db

HVT

GS70_S_105_1.1_1.1_CORE_CUSTOM_OSVT.db

GS70_S_105_1.1_1.1_CORE_OSVT.db

GS70_S_105_1.1_1.1_CORE_PM_OSVT.db

IMPOPT-3657

NAME

IMPOPT-3657

SUMMARY

"-layerAwareOpt" setOptMode option will be obsoleted. This option still works in this release, but to avoid this warning and to ensure compatibility with future releases, updating your script is recommended.

DESCRIPTION

This warning message is issued when the user tries to set 'setOptMode -layerAwareOpt true" in Innovus-14.1 to perform layer aware optimization while running optDesign command.

Example:

In Innovus-14.1 onwards layer aware optimization is made default, there is no need for the user to set this option separately. Hence it's recommended to update the user scripts accordingly to avoid this warning message.

IMPOPT-3663

NAME

IMPOPT-3663

SUMMARY

Power view is not set. First setup analysis view (%s) will be treated as power view and VT partitioning will be done on basis of leakage specified in this view. If this is incorrect, specify correct power view via command "set_power_analysis_mode -analysis_view <view_name>".

DESCRIPTION

Before executing the command "setOptMode -defineVtPartition my_vt_partition_file.txt ", "set_power_analysis_mode -analysis_view my_power_view" has to be set. This warning is given when vt partitioning is mentioned without setting the power analysis view.

Example:

**WARN: (ENCOPT-3663): Power view is not set. First setup analysis view (view_FUNC_MODE) will be treated as power view and VT partitioning will be done on basis of leakage specified in this view. If this is incorrect, specify correct power view via command "set_power_analysis_mode -analysis_view <view_name>".

IMPOPT-3665

NAME

IMPOPT-3665

SUMMARY

VT partitioning could not complete due to above error(s). Fix the error(s) and rerun the command.

DESCRIPTION

There are some problems when "setOptMode -defineVtPartition my_vt_partition_file.txt " and tool started doing vt partitioning, but could not complete it because of some errors may be in the file my_vt_partition_file.txt ; Please check the syntax of the vt partitin file and correct it.

Example:

**ERROR: (ENCOPT-3665): VT partitioning could not complete due to above error(s). Fix the error(s) and rerun the command.

Number of VT partitions : 0

Power view : view_FUNC_MODE

Cells in design : 1443

Instances in design : 331073

Instance distribution across the VT partitions:

Reporting took 2 sec

IMPOPT-3714

NAME

IMPOPT-3714

SUMMARY

Cannot add buffer inside hierarchy '%s' as it is don't touch.

DESCRIPTION

The error is generated when tool is not allowed to add instances inside this hierarchy.

Possible reasons are: -

-The hierarchy is marked dont_touch using set_dont_touch command.

-The hierarchy belongs to (or is present inside) a multi-instantiated cell and ECO inside multi-instantiated cells is not allowed.

-The hierarchy is present inside an ILM.

IMPOPT-6022

NAME

IMPOPT-6022

SUMMARY

%s will not do any insertions on %s as this net has been set to dont_touch.

DESCRIPTION

Please confirm if it was intentional to set this net as "dont_touch".

Example:

To alter the "dont_touch" setting on a net:

set_dont_touch [get_nets <net_name>] false|true

IMPOPT-6055

NAME

IMPOPT-6055

SUMMARY

The following cells have a "dont-touch" property but without being "dont-use". This could lead to optimization problems if a cell is inserted by the tool but then cannot be modified. Please check the dont-touch and dont-use settings for these cells within your libraries.

DESCRIPTION

Example:

To alter these settings on library cells use:

setDontUse <cell-name> false | true

set_dont_touch [get_lib_cells <cell-name>] false | true

IMPOPT-6056

NAME

IMPOPT-6056

SUMMARY

Option "-extractionEngine" for command setSIMode is obsolete. This option has been mapped to the following option based on your selection of extraction engine for use in SI flow: %s Modify your script to use the above setting instead of setSIMode -extractionEngine.

DESCRIPTION

How do I control which extractor is used to generate spef file?

It seems the behavior of setExtractRCMode -engine and -effortLevel have changed indicated by the warnings above. Using set_db options -engine and -effortLevel to control which extractor is used by extractRC is described below.

The -engine option indicates whether to use the preRoute or postRoute extraction engine. The -engine values default, detail and CCE are now obsolete.

Use -engine preRoute when the design has not been detail routed by NanoRoute yet. This is equivalent to -enginee default in previous versions of Innovus. When -engine preRoute is set RC extraction is done by the fast density measurements of the surrounding wires; coupling is not reported.

Use -engine postRoute after the design has been detail routed by NanoRoute.RC extraction is done by the detailed measurement of the distance to the surrounding wires; coupling is reported. The effortLevel parameter further specifies which postRoute engine is used for balancing performance versus accuracy needs.

The -effortLevel value controls which extractor is used when the postRoute engine is used.

low - Invokes the native detailed extraction engine. This is the same as specifying the -engine postRoute setting.

medium - Invokes the Turbo QRC (TQRC) extraction mode. TQRC performance and accuracy falls between native detailed extraction and IQRC engine. This engine supports distributed processing. TQRC engine is recommended for process nodes < 65nm. Note: This setting does not require a QRC license.

high - Invokes the Integrated QRC (IQRC) extraction engine. IQRC provides superior accuracy compared to TQRC. IQRC is recommended for extraction after ECO. In addition, IQRC supports distributed processing.Note: IQRC requires a QRC license.

signoff - Invokes the Standalone QRC extraction engine. This engine choice provides the highest accuracy. The engine has several runModes, thereby,providing maximum flexibility.

The default value depends on the value of setDesignMode. The default for nodes above 65nm is

low. TQRC (effortLevel medium) is the default extraction engine in the postroute flow for 65 nm and below design. However, TQRC and lQRC do not support the obsoleted 3 corner flow (defineRCCorner flow) and require a QRCTechfile. Therefore, Native Detailed (effortLevel low) engine remains the default engine if no QRCTechfile has been defined or if the defineRCCorner command has been used.

Should you use Turbo QRC (tQRC) or standalone QRC?

The extraction time with tQRC is typically a small percentage of the total flow time. With standalone QRC, the runtime would be longer.

Standalone QRC requires the usage of a QRC license (tQRC uses the Innovus license). It writes out a DEF and invokes the standalone tool. It is slower than tQRC. It is not incremental like tQRC, so the runtime impact may be high. tQRC is incremental and if changes are small, extraction runtime drops to almost zero. The delta between standalone QRC and tQRC in terms of accuracy is typically small, so there is usually no flow advantage or end QoR gain by doing it.

Cadence's suggestion is to use TurboQRC for 65nm and below nodes in the postRoute flow, and for signoff use standalone QRC.

Note: setSIMode -extractionEngine is obsolete and extraction during SI fixing will use the values of setExtractRCMode -engine and -effortLevel to determine the extractor to use.

IMPOPT-6064

NAME

IMPOPT-6064

SUMMARY

honorFixedStatus is set to false. Fixed instance %s will be deleted.

DESCRIPTION

This warning message is issued when the user tries to delete a fixed instance using 'ecoDeleteRepeater' command.

Example:

When the 'setEcoMode -honorFixedStatus false' and the user tries to delete a fixed Buffer/Inverter using 'ecoDeleteRepeater -inst <inst_name>' command the tool issues above warning and deletes

the specified Buffer/Inverter.

IMPOPT-6072

NAME

IMPOPT-6072

SUMMARY

Timing after commit may not match evaluate timing as spef for net %s is disabled with "evaluateOnly".

DESCRIPTION

This warning message in Innovus indicates that the RC for this particular net is not available, even if the SPEF is loaded. Please note that in the absence of SPEF, evaluation timings might not match the timing that you get after commit.

Example:

**WARN: (ENCOPT-6072): Timing after commit may not match evaluate timing as spef for net n1 is disabled.

---- Cell: BUFX1 ----

Through-object Slack: 8.067

Global Slack: 4.913

Max Tran Slack: 2.2547

0

For example, in this case the net &'n1&' does not have detail parasitics:

> get_property [get_net n1] has_detailed_parasitics

false

You would not get this warning message if you read the parasitics for this net, like using below example:

> rcOut -spef testef

> spefln testef

You can also check the parasitics for this net is now available.

> get_property [get_net n1] has_detailed_parasitics

true

Running ecoAddRepeater now would not issue above warning message:

> ecoAddRepeater -net n1 -cell BUFX1 -evaluateOnly

Using master clock &'ck&' for generated clock &'gck&'

Calculate delays in Single mode...

Topological Sorting (CPU = 0:00:00.0, MEM = 325.7M)

Number of Loop : 0

Start delay calculation (mem=325.660M)...

Delay calculation completed. (cpu=0:00:00.0 real=0:00:00.0 mem=325.660M 0)

*** CDM Built up (cpu=0:00:00.0 real=0:00:00.0 mem= 325.7M) ***

---- Cell: BUFX1 ----

Through-object Slack: 8.067

Global Slack: 4.913

Max Tran Slack: 2.2547

0

IMPOPT-6080

NAME

IMPOPT-6080

SUMMARY

AAE-SI Optimization can only be turned on when the timing analysis mode is set to OCV.

DESCRIPTION

The Advanced Analysis Engine (AAE) requires timing analysis to be run in On-Chip Variation (OCV) mode. To enable OCV mode run:

setAnalysisMode -analysisType onChipVariation

With OCV mode you typically want to enable Common Path Pessimism Removal (CPPR) as well:

setAnalysisMode -cppr both

IMPOPT-6089

NAME

IMPOPT-6089

SUMMARY

Cannot delete instance '%s' as instance is resize only.

DESCRIPTION

This message is reported when user tried to delete an instance which have"ResizeOnly" attribute. This property was set by optDesign with the option setOptMode -sizeOnlyFile <file>, where <file> is user define list of cell to have this attribute.

Remove ResizeOnly property for the instance to delete.

The property can be removed as follows:

set inst B1

dbDelProp [dbGet -p [dbGet -p top.insts.name $inst].props.name ResizeOnly]

Note : starting 14.2 these property will be revised to a new scheme.

Example:

Once the "resizeOnly" attributes get removed , we can now delete the buffer using "ecoDeleteRepeater" command , as shown below:

ecoDeleteRepeater -inst B1

IMPOPT-6095

NAME

IMPOPT-6095

SUMMARY

Cannot delete instance '%s' as cell '%s' is neither a buffer nor an inverter. Only buffers & inverters can be deleted with this command.

DESCRIPTION

This error comes when tool does not find the specified instance as a buffer/inverter.

In order to get rid of this error: -

1. Check the name of buffer/inverter instance specified.

2. Dump out the footprint of the cell using reportFootPrint command. If the cell is not interpreted as a buffer/inverter, check library for buffer/inverter footprint and function.

IMPOPT-6108

NAME

IMPOPT-6108

SUMMARY

Used -term with -relativeDistToSink option set to value 1. Ignoring -relativeDistToSink option.

DESCRIPTION

This warning message is issued when the user tries to run ecoAddRepeater command with '-term' option and using '-relativeDistToSink 1'. Relative distance to sink 1 means that the repeater needs to be placed close to driver. If not all sink terms of the net are specified with -term option, -

relativeDistToSink option is ignored.

IMPOPT-6111

NAME

IMPOPT-6111

SUMMARY

The location {%.2f %.2f} specified in %s option is outside the design boundary. Command %s will ignore this option.

DESCRIPTION

This message comes when user specifies a location outside the design boundary.

In order to get rid of this message user should make sure the specified location lies within the design boundary. The design boundary can be checked using dbGet top.fplan.box.

IMPOPT-6115

NAME

IMPOPT-6115

SUMMARY

ECO batch mode has been activated, and '(batch mode)' has been added to the prompt as a reminder of that situation. Specify '%s false' after all ECOs are over.

DESCRIPTION

This warning is seen if the initial innovus db itself has batch mode enabled or the user has set it intentionally. Multiple ECO changes can be done in batch mode. This takes lesser run time when

compared to batch mode false. Once all the ECOs are done, we must exit batch mode, because optimization and many other commands do not work properly in batch mode. Timing updates for all ECOs done inside batch mode are done at once when batch mode is exited.

Example:

setEcoMode -batchMode true

ecoAddRepeater/ecoDeleteRepeater/ecoChangCell ...; # No timing update is done during these ECOs.

setEcoMode -batchMode false; # This would update timing incrementally for all the above ECOs at once.

report_timing ...; # Timing should be up-to-date here.

#For more details, please look into the COS "Speeding up ecoAddRepeater runtime when in batch mode

IMPOPT-6116

NAME

IMPOPT-6116

SUMMARY

ECO operation to delete a buffer fails if the buffer is a feedthrough buffer.

DESCRIPTION

Feedthrough buffers deletion is prohibited by the tool as in some cases, this will result in an assign statement, which is prohibited by default. This check is strict and will also prevent feedthrough buffer deletion on cases that don't require assign creation.

To remove this error in 13.x, user should add -allowCreateAssign option to ecoDeleteRepeater (source is CCR 1043429)

In 14.1, this should apparently be fixed through HECO, still according to the same CCR.

Example:

[DEV]innovus 3> ecoDeleteRepeater -inst

physical_lake_3/digrf_1/digrf_core_inst/regsp_top/digrf_regsp/FE_MHHOLD_ECO_DB100o_6489

**ERROR: (ENCOPT-6116): Cannot delete instance physical_lake_3/digrf_1/digrf_core_inst/regsp_top/digrf_regsp/FE_MHHOLD_ECO_DB100o_6489 as instance is a feed through buffer.

**WARN: (ENCOPT-3129): Unable to delete instance physical_lake_3/digrf_1/digrf_core_inst/regsp_top/digrf_regsp/FE_MHHOLD_ECO_DB100o_6489.

IMPOPT-6135

NAME

IMPOPT-6135

SUMMARY

Multiple instances with multiple cells are not supported with command %s.

DESCRIPTION

This message is issued when multiple cells are specified with multiple instances during resize. The possible combinations are: a single instance with multiple cells (evaluation only), or a single cell with multiple instances (commit only).

IMPOPT-6206

NAME

IMPOPT-6206

SUMMARY

Net %s is a special net.

DESCRIPTION

This Warning message is issued when user tries to run interactive ECO using ecoChangeCell, ecoDeleteRepeater or ecoAddRepeater commands when one of the pins of the cell is connected to a special net.

IMPOPT-6249

NAME

IMPOPT-6249

SUMMARY

Routing for net %s is not clean/complete. The terms to be buffered cannot be identified based on %s option. Use option -term or -net to add buffer on the net.

DESCRIPTION

Buffer addition to offload the net could not be done using specified options because software has identified some issues with the net routing. It could be that net has opens, shorts or incomplete routing etc. Review the routing of this net.

IMPOPT-7071

NAME

IMPOPT-7071

SUMMARY

The distributed optimization engine is obsolete and has been replaced by the GigaOpt optimization engine which is default in this release. Please update your scripts to remove any explicit settings of 'setDelayCalMode -engine feDc'or 'setDelayCalMode -engine signalStorm' so you get the default Advanced Analysis Engine (AAE) delay calculator to enable the GigaOpt engine.

DESCRIPTION

feDC delay calculation engine is not available in Innovus 14.1. When"setDelayCalMode -engine feDC" is executed, this error is seen. In Innovus 14.1,default delay calculation engine is AAE. If feDC delay calculation is required,revert to Innovus 13.2.

Example:

**ERROR: (ENCOPT-7071): The distributed optimization engine is obsolete and has been replaced by the GigaOpt optimization engine which is default in this release. Please update your scripts to remove any explicit settings of 'setDelayCalMode -engine feDc' or 'setDelayCalMode -engine signalStorm' so you get the default Advanced Analysis Engine (AAE) delay calculator to enable the GigaOpt engine.

**ERROR: Batch process failed.

IMPOPT-7075

NAME

IMPOPT-7075

SUMMARY

Timing data-to-data checks are present and will be disabled during optimization. To enable data-to-data checks during optimization use'setOptMode -enableDataToDataChecks true'.

DESCRIPTION

Timing data-to-data checks are found in the design and are disabled during optimization so that optimization focuses on regular data-to-clock timing checks. To enable data-to-data checks during optimization use 'setOptMode -enableDataToDataChecks true'.

IMPOPT-7077

NAME

IMPOPT-7077

SUMMARY

Some of the LEF equivalent cells have different ANTENNAGATEAREA/ANTENNADIFFAREA/PINS etc... attributes. They will not be swapped for fixed instances and for lefsafe operations like optLeakagePower in postroute mode. To find out what cells are LEF equivalent use the findLefEquivalentCells command.

DESCRIPTION

Due to differences between cells in the design physical library such as OBS,PINS, ANTENNAGATE, ANTENNADIFF etc... swapping is not allowed for such instances. For more information use the new findLefEquivalentCells command. It requires the name of a LEF cell to check, and optionally an output file for the results:

findLefEquivalentCells -cells <lib_cell> -outfile <out_file>

During normal timing optimization, optDesign will resize instances as required.Cells of different sizes but the same function are not equivalent, because you cannot safely swap one for the other without risk of overlap or other DRV.Commands like optLeakagePower, or timing optimization on fixed instances, will attempt what is known as "lefsafe" swapping, where you replace one cell with another of the same size, pin geometry, antenna gate area, etc. You can do this postRoute without risk of overlaps or need to re-legalize the placement.If two cells have the same function and size but are not lefsafe,findLefEquivalentCells will explain why.

Example:

findLefEquivalentCells -cells INVXL -outfile myfile

LEF Equivalent cells { INVXL }

Non-LEF Equivalent cells of same size but different pin geometries { INVX1 }

---

findLefEquivalentCells -cells DFND4BWP22P90

LEF Equivalent cells { DFND4BWP22P90 DFND4BWP22P90ULVT }

IMPOPT-7085

NAME

IMPOPT-7085

SUMMARY

optVirtual is now using the GigaOpt optimization engine which is default in this release. Please update your scripts to remove any explicit settings of 'setDelayCalMode -engine feDc'or 'setDelayCalMode -engine signalStorm' so you get the default Advanced Analysis Engine (AAE) delay calculator to enable the GigaOpt engine.

DESCRIPTION

feDC delay calculation engine is not available in Innovus 14.2. When "setDelayCalMode -engine feDC" is executed, this error is seen. In Innovus 14.2,default delay calculation engine is AAE. If feDC delay calculation is required,revert to Innovus 13.2.

Example:

**ERROR: (ENCOPT-7085): optVirtual is now using the GigaOpt optimization engine which is default in this release. Please update your scripts to remove any explicit settings of 'setDelayCalMode -engine feDc' or 'setDelayCalMode -engine signalStorm' so you get the default Advanced Analysis Engine (AAE) delay calculator to enable the GigaOpt engine.

**ERROR: Batch process failed.

IMPOPT-7253

NAME

IMPOPT-7253

SUMMARY

The standard cell <%s> is part of the timing library but does not have a physical definition. Please

ensure that this cell is described in the LEF.

DESCRIPTION

Please provide the LEF for the cell or mark the cell don't use (setDontUse <cell> true)

IMPOPT-7254

NAME

IMPOPT-7254

SUMMARY

The standard cell <%s> cannot be legally placed. optDesign will consider the cell don't use.

DESCRIPTION

Cell without row defined cannot be legally placed and should be marked don't use. Please add setDontUse on the cell or define row for the cell.

IMPOPT-7255

NAME

IMPOPT-7255

SUMMARY

The net <%s> is marked don't touch and has %d fanout. Timing and drv optimization of such nets are limited.

DESCRIPTION

The don't touch property can be removed using the command set_dont_touch

IMPOPT-7256

NAME

IMPOPT-7256

SUMMARY

The net <%s> is ideal and has %d fanout. Timing and drv optimization of such nets are limited.

DESCRIPTION

The ideal net property can be removed using the command reset_ideal_net/reset_ideal_network

IMPOPT-7257

NAME

IMPOPT-7257

SUMMARY

The net <%s> has msv violation. Timing and drv optimization of such nets are limited.

DESCRIPTION

To get more information about net with MSV violation, please run verifyPowerDomain -xNetPD -isoNetPD

IMPOPT-7261

NAME

IMPOPT-7261

SUMMARY

The drcMargin %f with internal margin of %f is less than 0 and so DRV will not be fixed up to the library/sdc defined target

DESCRIPTION

The drcMargin considering the margin should be equal or greater than 0. A negative value will lead to underfixing DRVs.

IMPOPT-7262

NAME

IMPOPT-7262

SUMMARY

Net %s has a bottom preferred layer defined on layer z=%d but the maximum route layer is lower and defined on layer z=%d.

DESCRIPTION

A bottom preferred layer cannot be defined on a layer higher than the maxRouteLayer. It is recommended for the bottom preferred layer to be lower or equal to maxRouteLayer -1. It can be changed using setAttribute

IMPOPT-7263

NAME

IMPOPT-7263

SUMMARY

Net %s has a bottom preferred layer defined on layer z=%d but the maximum route layer is defined same layer.

DESCRIPTION

A bottom preferred layer should be a layer <= maxRouteLayer - 1. We need 2 layers to route the net. It can be changed using setAttribute

IMPOPT-7264

NAME

IMPOPT-7264

SUMMARY

Running power optimization flow with leakage to dynamic ratio of %f but without activity file loaded.

DESCRIPTION

Please provide activity file.

IMPOPT-7266

NAME

IMPOPT-7266

SUMMARY

Running power optimization flow but no leakage power view provided.

DESCRIPTION

Please use set_analysis_view -leakage <>.

IMPOPT-7267

NAME

IMPOPT-7267

SUMMARY

Running power optimization flow but no dynamic view provided.

DESCRIPTION

Please use set_analysis_view -dynamic <>.

IMPOPT-7268

NAME

IMPOPT-7268

SUMMARY

Running power optimization flow but the leakage power analysis view '%s' is not part of the active analysis views.

DESCRIPTION

The list of active view can be found using all_setup_analysis_view and all_hold_analysis_view. Please change the power view or make the power view active.

IMPOPT-7269

NAME

IMPOPT-7269

SUMMARY

Running power optimization flow but the dynamic power analysis view '%s' is not part of the active analysis views.

DESCRIPTION

The list of active view can be found using all_setup_analysis_view and all_hold_analysis_view. Please change the power view or make the power view active.

IMPOPT-7271

NAME

IMPOPT-7271

SUMMARY

NDR %s doesn't exist in the database and will be ignored by gigaOpt.

DESCRIPTION

The list of all available non default rule in the design can be found by using the following query dbGet head.rules.name

IMPOPT-7273

NAME

IMPOPT-7273

SUMMARY

check_design cannot continue checking opt category due to invalid trialRoute maxRouteLayer value

DESCRIPTION

The max route layer can be specified via the command setMaxRouteLayer.

IMPOPT-7275

NAME

IMPOPT-7275

SUMMARY

The net <%s> will not be routed due to skip_routing property defined on the net.

DESCRIPTION

Verify if the skip routing attribute is necessary or not. If it is not necessary, please use setAttribute to disable the skip routing attribute.

IMPPP-133

NAME

IMPPP-133

SUMMARY

The block boundary of instance '%s' was increased to (%f %f) (%f %f) because cell geometry (%f %f) (%f %f) was outside the original block boundary.

DESCRIPTION

Some blocks have pins or obstructions outside block boundary. The block boundary will be extended which may have influence on power planning around block area.

IMPPP-188

NAME

IMPPP-188

SUMMARY

The nets "%s" does not exist in the domain %s.

DESCRIPTION

Make sure the nets specified have been connected to PG pin of the domain.

IMPPP-190

NAME

IMPPP-190

SUMMARY

The net '%s' does not exist in design.

DESCRIPTION

Make sure if the power nets have been defined in the globals file.

The power and ground nets are declared in the globals file using the following commands:

set init_pwr_net {VDD}

set init_gnd_net {VSS}

IMPPP-333

NAME

IMPPP-333

SUMMARY

%s can not be selected at the same time as stripe boundary. The power planner will generate stripes only over %s.

DESCRIPTION

Selected objects can not be stripe boundary at the same time in one addStripe command. Check the selected objects if stripes are not generated in desired one.

IMPPP-354

NAME

IMPPP-354

SUMMARY

The power planner did not generate %s stripe at %f %f %f %f with width %f either because the stripe would merge with rings, or because stripe could not be connected to any legal targets, or because stripe would break design rule.

DESCRIPTION

To debug the cause,first you can check if the stripe is removed because of obstruction or no target; then you can check the error/warning message in log file; at last you can add the stripe manually and run verify_drc to check the drc violation. For further help, please contact Cadence Support.

IMPPP-362

NAME

IMPPP-362

SUMMARY

The area specified in option -area intersects both the default and nondefault power domains. The power planner will create stripes only over the default power domain.

DESCRIPTION

When area specified in option -area intersects both the default domain and nondefault domains, power planner only creates stripes over default domain. If stripes are desired to be generated in nondefault domain, the specified area should be refined.

IMPPP-527

NAME

IMPPP-527

SUMMARY

ViaGen failed to modify via %s.

DESCRIPTION

This message may be reported because specified via size violates rules. Reasonable values should be specified.

IMPPP-543

NAME

IMPPP-543

SUMMARY

Inconsistent cut size definition in VIARULE '%s' and '%s'.

DESCRIPTION

This warning indicates that there are multiple via sizes on the same cut layer without cut class definition.

IMPPP-557

NAME

IMPPP-557

SUMMARY

A single-layer VIARULE GENERATE for turn-vias is obsolete and is being ignored. Remove this statement from the technology file: VIARULE %s GENERATE.

DESCRIPTION

In old versions, special turn vias were defined to fill the corner with metal when a special route changed directions. Turn vias are no longer required in Innovus System as the router automatically makes a proper connection.

IMPPP-4033

NAME

IMPPP-4033

SUMMARY

The net '%s' is not a primary but secondary net of the power domain %s.

DESCRIPTION

Tool can generate stripes of secondary net of a power domain. This message is to warn user for checking whether the net setting is right.

IMPPP-4051

NAME

IMPPP-4051

SUMMARY

Fail to add rings. Gaps among IO cells may exist. Execute command addIoFiller to fill gaps among cells before addRing.

DESCRIPTION

If working on top level implementation, use "-follow io" switch to addRing command which creates the rings abutting to the boundary.

IMPPP-4055

NAME

IMPPP-4055

SUMMARY

The run time of addStripe will degrade with multiple cpu setting according to the number of stripe sets, ignore the setting of setMultiCpuUsage in addStripe.

DESCRIPTION

addStripe uses multiple cpu feature dynamically according to the number of stripes to generate and the cpu on this machine. If the number of stripes is less, it's not recommended to use multiple cpu which may cost more runtime.

IMPPP-4500

NAME

IMPPP-4500

SUMMARY

Large amount of geometries exist around {%f, %f} between Layer %s and %s. Long running time might be introduced.

DESCRIPTION

This warning will typically be seen where a macro has very complex power pins. In turn these may be a result of mistakes in the creation of the abstract view for the macro.

IMPPP-5000

NAME

IMPPP-5000

SUMMARY

The valude of -pattern contains illegal character, or the length is more than %d.

DESCRIPTION

The legal characters for option -pattern are '1', '0', and ' '. And it has the maximum length restriction.

IMPPPR-638

NAME

IMPPPR-638

SUMMARY

In line %d of constraint file '%s', the PAIR constraint does not have available bump or instance name, so it will be ignored.

DESCRIPTION

At least a PAIR constraint should have one available bump and one available instance for the net.

IMPPPR-641

NAME

IMPPPR-641

SUMMARY

In line %d of constraint file '%s', bump or IO instance '%s' cannot be found or not suitable for viewBumpConnection, so it will be ignored for net '%s'.

DESCRIPTION

The instance or bump name, pin name or port number does not exist; the net of IO port is different from PAIR net; or the IO port is too small or narrow.

IMPPSO-123

NAME

IMPPSO-123

SUMMARY

Option -continuePattern must be specified with -globalPattern option.

DESCRIPTION

In power switch ring insertion, Option "-continuePattern 1" should be used along with -globalPattern option so that the power switch insertion pattern continues along the power domain edges. If "-continePattern 1" option is not specified, the pattern specified by -globalPattern stops at the edge and a new pattern starts from next edge.

Example:

In below example, a global pattern of switches is defined using -globalPattern

and same will continue around the power domain switch_pd as option

-continuePattern is specified.

```
addPowerSwitch -ring \
-powerDomain switch_pd \
-enablePinIn {enIn} -enablePinOut {enOut} \
-enableNetIn "Ctrl1_ip_0" \
-enableNetOut "power_en_out" \
-globalSwitchCellName {{PSW65_1 sw1} {PSW65_2 sw2}} \
-globalPattern {sw1 sw2 sw2 sw1} \
-globalFillerCellName {FILLERcell} \
-continuePattern 1
```

IMPPSO-133

NAME

IMPPSO-133

SUMMARY

Power and/or Ground pin of inserted power switches might not be connected power or ground nets. Please check the CPF/power intent.

DESCRIPTION

When power switches are added in design, the power and ground pins are also logically connected to power and ground nets based on CPF/power intent specification. In case this specification is found to be missing during power switch insertion using addPowerSwitch this warning message is shown.

Example:

To debug this issue, user should check below CPF specifications for debug:

Example :

create_power_domain -name PD_VIRTUAL

update_power_domain -name PD_VIRTUAL -primary_power_net VDDR

-primary_ground_net VSS

create_power_domain -name PD3 -instances inst1/b -shutoff_condition {pse3}

-base_domains PD_VIRTUAL

create_power_switch_rule -name psr_pd3 -domain PD3 -external_power_net VDDR

update_power_switch_rule -name psr_pd3 -cells HDRDID1BWPHVT -prefix

CDN_SW_PD3_

IMPPSO-134

NAME

IMPPSO-134

SUMMARY

Adding power switches to an always on power domain.

DESCRIPTION

The power switches are supposed to be added for a switchable power domain for which -shufoff_condition is defined in the CPF. This warning message is showed in case where power domain specified in-powerDomain option of addPowerSwitch does not have shutoff condition specified in CPF file.

Example:

To debug this issue, please check create_power_domain specification of the

power domain specified in addPowerSwich.

addPowerSwitch -powerDomain PD2 -column ...

In CPF , there is no shutoff condition.

create_power_domain -name PD2 -instances inst1/a

IMPPSO-155

NAME

IMPPSO-155

SUMMARY

CPF option -acknowledge_receiver of update_power_switch_rule ignored due to -enableNetOut option specified.

DESCRIPTION

This warning will be seen when there is -acknowledge_receiver_pin is defined in update_power_switch_rule for the power domain specified in addPowerSwitch command. In case -enableNetOut is not specified in addPowerSwitch command, then the last enable net out from last power switch cell will get auto connected to the pin specified in acknowledge_receiver_pin. (Here assumption is that there will be single enable net out from power switches) Since user is overriding this spec by giving -enableNetOut, this warning is given.

Example:

addPowerSwitch -powerDomain PD -ring -globalSwitchCellName CDN_RING_SW \

-enablePinIn NSLEEPIN -enableNetIn Net1 -enablePinOut NSLEEPOUT \

-enableNetOut n_5 -globalOffset 10 -switchModuleInstance mod11

**WARN: (IMPPSO-155): CPF option -acknowledge_receiver update_power_switch_rule ignored due to

-enableNetOut option specified.

If you intended for the CPF -acknowledge_receiver definition to be honored, do

not

use the -enableNetOut option.

IMPPSO-170

NAME

IMPPSO-170

SUMMARY

Fewer power switches inserted than specified on side: %s

DESCRIPTION

This warning message is seen during power switch ring insertion when user specifies number power switches to be inserted per power domain side. In case user specifies more number of power switches than the number that can be placed on a specific power domain edge/side, this warning

message will be seen.

Example:

Here user did ring type power switch insertion on power domain HEAD and

specified 4 switches per side.

But on top and bottom edge only 3 switches were inserted and so the warning

message.

Number of switches inserted for all sides: 4 3 4 3

**WARN: (IMPPSO-170): Fewer switches inserted than specified on

side: 2 (Top) : 3 < 4

**WARN: (IMPPSO-170): Fewer switches inserted than specified on

side: 4 (Bottom) : 3 < 4

Total number of switches added to HEAD : 14

IMPPSO-186

NAME

IMPPSO-186

SUMMARY

The specified module in -switchModuleInstance is in a different domain: %s

DESCRIPTION

From the warning message it means that, the module user specified in-switchModuleInstance does not belong to the power domain user want to add using addPowerSwitch -powerDomain. User need to correct the '-switchModuleInstancea' or update your CPF if user miss defining the instance in power domain.

Example:

addPowerSwitch -powerDomain PD_sw1 -column \

-globalSwitchCellName HDswHVT \

-switchModuleInstance INST/U_CPU_core/u_wrapper1 \

(Where PD_sw1a's hier. instance name is: INST/U_CPU_core/u_wrapper, see the 1

at the end)

**WARN: (IMPPSO-186): The specified module in -switchModuleInstance is in a

different domain: PD_default != PD_sw1 ...

IMPPSO-187

NAME

IMPPSO-187

SUMMARY

The specified module in -switchModuleInstance domain and -powerDomain are different: %s

DESCRIPTION

From the warning message, the module user specified does not belong to the power domain user want to add power switches i.e. as specified in addPowerSwitch -powerDomain. User need to correct the '-switchModuleInstancea', or update CPF if used missed defining the instance in power domain.

Example:

addPowerSwitch -powerDomain PD_sw1 -ring \

-globalSwitchCellName HDswHVT \

-switchModuleInstance INST/soc_core/u_wrapper1 \

(Where PD_sw1a's hierarchical instance name is: INST/soc_core/u_wrapper , see

the 1 in end of instance)

**WARN: (IMPPSO-187): The specified -switchModuleInstance domain and

-powerDomain are different: PD_default != PD_sw1.

IMPPSO-188

NAME

IMPPSO-188

SUMMARY

The power switches are added in domain %s which is different from the -powerDomain %s. You can use -switchModuleInstance to specify a correct module hierachy of the power domain.

DESCRIPTION

By default , addPowerSwitch will insert power switch instances into top design if user doesn't provide -switchModuleInstance . When the default domain of the top design is not equal to -powerDomain , we will meet this message that the power switch instance is added into a domain which is different from-powerDomain . It's required to specify -switchModuleInstance to ensure that the power switch instances are inserted to the correct logic of the power domain.

IMPPSO-192

NAME

IMPPSO-192

SUMMARY

The specified -enableNetIn is different from the power intent rule net: %s. The net name defined in cpf rule will be ignored. Please correct the net name if it's not the expected enable input net.

DESCRIPTION

If you have already specified update_power_switch_rule -enable_condition or create_power_domain -shutoff_condition in your CPF file, you do not need to specify this parameter. update_power_switch_rule -enable_condition takes precedence over

create_power_domain -shutoff_condition for enable net In connection. This message appears when the net name defined in -enableNetIn is different from the net in the power switch rule in the cpf file. You need to check if it's a correct net and correct it either in -enableNetIn or update_power_switch_rule in cpf file.

IMPPSO-206

NAME

IMPPSO-206

SUMMARY

First instance is not placed because it was blocked at location: %s. Please use offset options in addPowerSwitch to place the power switch instance in an availabe location.

DESCRIPTION

addPowerSwitch will try to insert the power switch instances according to the offset options in addPowerSwitch. The issue usually appears when the offset value is not suitable. Please check the location in the message and tune the offset value to fix the issue.

IMPPSO-306

NAME

IMPPSO-306

SUMMARY

row @%s with site %s is not covered by a switch. Type 'man IMPPSO-306' for more details.

DESCRIPTION

The message could happen in addPowerSwitch or verifyPowerSwitch. addPowerSwitch will verify

row coverage at end of a column insertion and print which row is not covered by a switch. You can turn it off with the option "-noRowVerify" in addPowerSwitch. You can use "addPowerSwitch -incremental -area" to insert the power switch to the location if you need the row to be covered by a switch.

IMPPSO-627

NAME

IMPPSO-627

SUMMARY

Option '-reportViolationsOnly' for optPowerSwitch command is obsolete and has been replaced by '-reportOnly'. The obsolete option still works in this release, but to avoid this warning and to ensure compatibility with future releases, update your script to use '-reportOnly'.

DESCRIPTION

This option '-reportViolationsOnly' of CMD 'optPowerSwitch' still works in this release(14.1), but to avoid this warning and to ensure compatibility with future releases, user should update the script to use option '-reportOnly'.

Example:

If use below CMD and option in TCL file, IMPPSO-627 will exist.

<CMD> optPowerSwitch -reportViolationsOnly

WARNING (IMPPSO-627): Option '-reportViolationsOnly' for optPowerSwitch

command is obsolete and has been replaced by '-reportOnly'. The obsolete option

still works in this release, but to avoid this warning and to ensure

compatibility with future releases, update your script to use '-reportOnly'.

... ...

This WARN will disappear after modify the TCL file to below:

<CMD> optPowerSwitch -reportOnly

IMPPSO-800

NAME

IMPPSO-800

SUMMARY

Power switch verification completed with %s. Please check the issue in above messages.

DESCRIPTION

verifyPowerSwitch will print all the warning messages after verification is completed and will summarize the total warning numbers. Please check the issues in the above messages.

IMPPSO-806

NAME

IMPPSO-806

SUMMARY

Number of warnings on domain %s. Please check the issues in above warning messages.

DESCRIPTION

Print the total number of warnings in the end of verifyPowerSwitch. User can check the issues in above warning messages.

IMPPSO-808

NAME

IMPPSO-808

SUMMARY

Power switch instance pin is floating: %s. It's usually caused by addPowerSwitch could not find a available enable net to connect to the pin. Please use rechainPowerSwitch to reconnect the power switch instance pins.

DESCRIPTION

The warning message usually appears when addPowerSwitch is completed. Please check the enable net connections of the power switch instances in the message. Use rechainPowerSwitch or update options in addPowerSwitch to fix the issue.

IMPPSO-809

NAME

IMPPSO-809

SUMMARY

Power switch chain forms a loop involving the following: %s. The enable signal loops maybe formed accidently during enable net chaining. Please check the enable net connections of the power switch chain.

DESCRIPTION

The message appears when verifyPowerSwitch -checkLoop to report if power switch enable chain forms a loop.

IMPPSO-906

NAME

IMPPSO-906

SUMMARY

Option -unchainByInstances of command addPowerSwitch will become obsolete in the next major release as same option function is now available command rechainPowerSwitch -unchainByInstances. The obsolete option still works in this release, but to avoid this warning and to ensure compatibility with future release, update the scripts to use the command rechainPowerSwitch-unchainByInstances.

DESCRIPTION

The power switch enable chain and unchain feature was first implemented as part of addPowerSwitch command.Now the power switch chain and unchain feature options are available in command rechainPowerSwitch.

IMPPSO-907

NAME

IMPPSO-907

SUMMARY

Option -chainByInstances of command addPowerSwitch will become obsolete in the next major release as same option function is now available under command rechainPowerSwitch -chainByInstances. The obsolete option still works in this release, but to avoid this warning and to ensure compatibility with future release, update the scripts to use the command rechainPowerSwitch-chainByInstances.

DESCRIPTION

The power switch enable net chain and unchain feature options were previously made available using addPowerSwitch command. But later this functionality was moved to new command rechainPowerSwitch.So its recommended for user to use the feature with rechainPowerSwitch command

IMPPSO-1551

NAME

IMPPSO-1551

SUMMARY

IEEE1801 option -ack_port of create_power_switch ignored due to -enableNetOut option specified.

DESCRIPTION

This warning will be seen when there is -ack_port is defined in create_power_switch for the power domain specified in addPowerSwitch command. In case -enableNetOut is not specified in addPowerSwitch command, then the last enable net out from last power switch cell will get auto connected to the pin specified in -ack_port. (Here assumption is that there will be single enable net out from power switches) Since user is overriding this spec by giving -enableNetOut, this warning is given.

Example:

addPowerSwitch -powerDomain PD -ring -globalSwitchCellName CDN_RING_SW \

-enablePinIn NSLEEPIN -enableNetIn Net1 -enablePinOut NSLEEPOUT \

-enableNetOut n_5 -globalOffset 10 -switchModuleInstance mod11

**WARN: (IMPPSO-1551): IEEE1801 option -ack_port of create_power_switch ignored due to

-enableNetOut option specified.

If you intended for the IEEE1801 -ack_port definition to be honored, do

not

use the -enableNetOut option.

IMPPTN-90

NAME

IMPPTN-90

SUMMARY

Pin %s of abutted partition %s could not be assigned. Could not find a feasible slot for the pin. Create more feasible location before for pin assignment by inserting feedthrough buffers using insertPtnFeedthrough command or allowing more layers for assigning pins or using setPinAssignMode -strict_abutment false or using setPinAssignMode -allow_unconnected_in_abutted_edge true for relaxing this check.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1 In abutted designs, pins of following type can not be placed on common edges between two adjoining partitions.

.in +2

A. Pins of net not connected to adjacent partition (fences of the two partitions being connected are not touching each other in floorplan).

B. Pins of nets having connections to two or more partitions any pin belonging to net of above type will have to route over an unconnected partition and result in illegal routing.

Feedthrough step is required to get rid of pins which connect non-adjacent partitions or multiple partitions, by changing netlist and making all pins connect to only one pin on adjacent partition to make the routing of net feasible/legal

C. Floating pins

.in

#2. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

#3. Use setPinAssignMode -strict_abutment false to relax abutment violations checks for placing multi partition pin of a net, non neighbor pins of a net and floating pins on abutted edges.

#4. Use setPinAssignMode -allow_unconnected_in_abutted_edge true to relax abutment violations checks for placing floating pins on abutted edges.

Example:

---

eg. if pins are not assigned for a net which has more than two partition pins to connect use insertPtnFeedthrough command to change netlist to have new nets added and older net modified in way that, now nets only connect two pins of adjacent partitions only.

IMPPTN-100

NAME

IMPPTN-100

SUMMARY

The net %s is not connected to any terminal. This net will not be considered for feedthrough buffer insertion. Correct the netlist to get this net considered for feedthrough buffer insertion.

DESCRIPTION

An unconnected net will not be considered for feedthrough insertion. The net should be connected

to an output port and an input port to be considered for feedthrough insertion.

IMPPTN-233

NAME

IMPPTN-233

SUMMARY

No legal free slots available for %s of partition %s. Create additional slots using definePartition command or by removing blockage before pin assignment.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

IMPPTN-426

NAME

IMPPTN-426

SUMMARY

Adjusting partition %s core to left from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

This is happening because the core spacing values specified (I/O to core distance of partition block) are not multiple of placement grid. Same issue for IMPPTN-427, IMPPTN-428 and IMPPTN-429 based or the side.

Example:

<CMD> definePartition -hinst uCORE/uPKTSS/uPKTSS_PPCS_PMA_SYS -coreSpacing {2.7 2.7 1.9 1.9} -reservedLayer {1 2 3 4 5 6 7 8} -routingHalo 1.9 -routingHaloTopLayer 7 -routingHaloBottomLayer 1 -placementHalo {2.7 2.7 1.9 1.9} -railwidth 0.1 -minPitchLeft 3 -minPitchRight 3 -minPitchTop 3 -minPitchBottom 3 -pinLayerTop {3 5} -pinLayerBottom {3 5} -pinLayerLeft {4 6} -pinLayerRight {4 6}

Creating partition PKTSS_PPCS_PMA_SYS.

**WARN: (IMPPTN-426): Adjusting partition PKTSS_PPCS_PMA_SYS core to left from 1.900000 to 2.025000.

**WARN: (IMPPTN-427): Adjusting partition PKTSS_PPCS_PMA_SYS core to right from 1.900000 to 2.025000.

**WARN: (IMPPTN-428): Adjusting partition PKTSS_PPCS_PMA_SYS core to top from 2.700000 to 2.850000.

**WARN: (IMPPTN-429): Adjusting partition PKTSS_PPCS_PMA_SYS core to bottom from 2.700000 to 2.850000.

Placement grid is at 0.135 x-direction, 0.095 y-direction.

IMPPTN-427

NAME

IMPPTN-427

SUMMARY

Adjusting partition %s core to right from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

During partitioning, the warnings above are issued. How does Innovus determine these adjustments?

\t Innovus snaps the partition coreBox (area where rows are created and placement can be done) boundary to the placement grid. The remaining difference between coreBox and partition box is adjusted in core to right, core to top values.

Example:

**WARN: (IMPPTN-427): Adjusting partition lbrx_top_0 core to right from 0.000000 to 0.100000.

IMPPTN-428

NAME

IMPPTN-428

SUMMARY

Adjusting partition %s core to top from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

During partitioning, the warnings above are issued. How does Innovus determine these adjustments?

\t Innovus snaps the partition coreBox (area where rows are created and placement can be done) boundary to the placement grid. The remaining difference between coreBox and partition box is adjusted in core to right, core to top values.

Example:

**WARN: (IMPPTN-428): Adjusting partition lbrx_top_0 core to top from 0.000000 to 3.680000.

IMPPTN-429

NAME

IMPPTN-429

SUMMARY

Adjusting partition %s core to bottom from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

This is happening because the core spacing values specified (I/O to core distance of partition block) are not multiple of placement grid. Same issue for IMPPTN-427, IMPPTN-428 and IMPPTN-429 based or the side.

Example:

**WARN: (IMPPTN-429): Adjusting partition PKTSS_PPCS_PMA_SYS core to bottom from 2.700000 to 2.850000.

IMPPTN-555

NAME

IMPPTN-555

SUMMARY

A feasible legal location was not found for %d (out of %d) pins. Consequently, the following pins could not be assigned:

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

2. Insert feedthrough buffers using the insertPtnFeedthrough command.

IMPPTN-624

NAME

IMPPTN-624

SUMMARY

insertPtnFeedthrough could not find a path for net '%s' to reach '%s'. If the -topoFile option is being used, the topology specified for this net is incomplete.

DESCRIPTION

In case automatic feedthrough insertion is being done, it means that a path to some of the terminals could not be found. If the routeBased option is used, the routing may be incomplete. For the case the topology file is used an explanation follows.

Tool issues above warning during insertPtnFeedthrough command step, when topology file provided with -topoFile is used to guide the tool for creating the feedthrough in a specified partition for multi-fanout nets. You will get above warning if the topology file did not define for all the terminals for a multi-fanout net. Always follow the convention from_pin to to_pin for writing the topology file.

Example:

If the net goes to three partition A, B and C and you want to make a part of the net from A to D then to C, then you can use the following approach to write the topology file.

net n123

hinst-hinst A D;

hinst-hinst D C;

hinst-hinst A B;

end net

So, here all the combinations are covered where the net goes, instead of defining the A-D-C.

IMPPTN-646

NAME

IMPPTN-646

SUMMARY

insertPtnFeedthrough is trying to find a feedthrough path for net %s. It could not find a path to partition or terminal [%s]. Partitions connected to this net may not be adjacent to each other.

DESCRIPTION

Automatic feedthrough insertion derives the feedthrough topology using the placement. It assumes a channel-less design. The possibility of routing through channels is considered minimal. In this design a path to a partition or terminal connected to the above mentioned net could not be found without avoiding the channels.

IMPPTN-647

NAME

IMPPTN-647

SUMMARY

insertPtnFeedthrough skipping net [%s] because a path to some of the partitions or terminals could not be found. It might not be necessary to insert feedthrough buffers for this net. If you wish to insert feedthrough buffers for this net, then use the topology file for guided feedthrough buffer insertion or use the -routeBased option after routing the net.

DESCRIPTION

insertPtnFeedthrough assumes the design to be channel-less and partitions to be in the line of sight for feedthrough path to pass from one partition to another. In case of channel based designs where

this is not true, the named net is ignored. In case feedthrough insertion is required for the net, either route the design and used insertPtnFeedthrough -routeBased or define the path for the net in a topology file and use insertPtnFeedthrough -topoFile <filename>

Example:

---

earlyGlobalRoute

insertPtnFeedthrough -routeBased

Or

insertPtnFeedthrough -topoFile <filename>

IMPPTN-652

NAME

IMPPTN-652

SUMMARY

The pushdownBuffer command cannot create an instance with name [%s%s]. An instance with this name already exists in the design. Using default prefix and name [%s] for this instance.

DESCRIPTION

This message is issued if the pushdownBuffer uses the prefix provided with the -prefix option and the resulting name has a conflict with an existing instance name. No action needs to be taken as it will make another name with the default prefix.

IMPPTN-716

NAME

IMPPTN-716

SUMMARY

Partition %s constraint missing. Specify a Guide, Region, Fence constraint on the partition or place the blackbox instance.

DESCRIPTION

While committing partitions 1. Blackboxes should be placed inside core 2. Partitions fences must be core

IMPPTN-780

NAME

IMPPTN-780

SUMMARY

Selected pin assignment: could not assign %d (out of %d) pins because feasible legal location was not found for following pins, need legal locations for pin to be assigned.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

2. Insert feedthrough buffers using the insertPtnFeedthrough command.

IMPPTN-882

NAME

IMPPTN-882

SUMMARY

The insertPtnFeedthrough command was invoked with the -routeBased option, but the design has not yet been routed. The insertPtnFeedthrough command will skip the nets that are not routed. Route the design using earlyGlobalRoute for these nets to be considered for feedthrough insertion.

DESCRIPTION

The insertPtnFeedthrough command invoked with the -routeBased option requires routing for the net to find a path based on which it will insert the feedthrough ports.

The net reported is not routed so it gets ignored. Route the design prior to running this command. The earlyGlobalRoute command can be used to route the design.

Otherwise insertPtnFeedthrough should be invoked without using the -routeBased option in which case the command will try to find a path for the net based on the floorplan and placement (placement based feedthrough insertion).

Example:

---

earlyGlobalRoute

insertPtnFeedthrough -routeBased.

IMPPTN-946

NAME

IMPPTN-946

SUMMARY

Pin named [%s] does not exist in cell [%s]. Ignoring the pin. Check and correct the pin name.

DESCRIPTION

Pin name specified for the specified partition does not exist. Check the pin name and partition name and correct accordingly. Problem could be case sensitivity. Command requires exact name which is case sensitive or incorrect manipulation of "alphabet l or numeric 1" "likewise "alphabet o and numeric 0"

Example:

Pin name could be "isCaseSensitive" but pin name supplied could be "iscasesensitive

IMPPTN-1211

NAME

IMPPTN-1211

SUMMARY

Specified layer [%s] is not within the allowed pin layer range [%s] and [%s] of the partition %s. Re-specify a valid pin layer value or change the partition definition to allow this pin layer and rerun the command again.

DESCRIPTION

Specified layer is not within the allowed pin layer range of the specified partition. Use the Partition->Specify Partition GUI to view the current specified allowed layers. Edit the current allowed pin layers of the partition to include this specified pin layer or re-specify pin layer and rerun the

command again.

IMPPTN-1250

NAME

IMPPTN-1250

SUMMARY

Pin placement has been enabled on metal layer 1.

DESCRIPTION

You have this message because you have enabled metal layer 1 for pin placement. However, metal layer 1 is generally reserved for follow pins. Make sure follow pins are already routed, to ensure that the pins do not block follow pins creation.

Example:

---

setDesignMode -bottomRoutingLayer 1 enables pins in M1

IMPPTN-1520

NAME

IMPPTN-1520

SUMMARY

Pin '%s' of %s '%s' cannot be placed at the constrained location [%0.2f %0.2f] due to a blocked pin slot close to the location. Placing the pin at location [%0.2f %0.2f].

DESCRIPTION

Pin slot can be blocked because of the following reasons

\t 1. pin blockages

\t 2. routing blockages

\t 3. Power ground routing

\t 4. availability of layers to put pins

IMPPTN-1521

NAME

IMPPTN-1521

SUMMARY

Unable to get any valid location for the constrained pin [%s] at location [%0.2f %0.2f].

DESCRIPTION

Pin slot can be blocked because of the following reasons

\t 1. pin blockages

\t 2. routing blockages

\t 3. Power ground routing

\t 4. availability of layers to put pins

IMPPTN-1550

NAME

IMPPTN-1550

SUMMARY

Cell [%s] cannot be specified as a black box because the design does not have any instance associated with this cell or instance may create nested blackBox. Ensure the design has an instance referenced to this cell or specify correct name of cell and rerun %s again.

DESCRIPTION

Specified cell cannot be defined as a black box because the design does not have any instance that is referenced to this cell or instance may create nested blackBox. Ensure there is at least one instance that is associated with this cell and rerun the command again.

IMPPTN-1669

NAME

IMPPTN-1669

SUMMARY

Ptn %s does not have any reserved slots for assigning ptn pins. Check the allowed layers for the partition and make sure that layers based on preferred routing tracks are reserved.

DESCRIPTION

This warning message is issued while assigning pins on a partition using the Innovus GUI with Partition => Assign Pin... or when using the assignPtnPin Tcl command.

The floorplan likely contains a problem with routing tracks and/or pin layer definitions. The problem can be debugged graphically using: Partition => Specify Partition

Select the offending partition and review the Partition Pin Layer Used section. Make sure the layers defined for pins are included in the Layers Reserved For Partition. Corrections may be made and applied with this form. Check the min max layer allowed though getDesignMode another reason could be presence of route blockage or PG on partition edge blocking the routing tracks.

Next, confirm there are preferred routing tracks defined for the pin layers using the Layer Control =>

Track => Pref Track and the Wire&Via layer defined for the pins. If the tracks are incorrect, they may be regenerated using the "generateTracks" Tcl command.

Example:

getPinConstraint -cell c -side all -layer

Constraint on partition c :

Allowed layer on side [top] : 2 4 6

Allowed layer on side [left] : 3 5

Allowed layer on side [bottom] : 2 4 6

Allowed layer on side [right] : 3 5

getDesignMode -bottomRoutingLayer -topRoutingLayer

-bottomRoutingLayer 2 # string, default=""

-topRoutingLayer 15 # string, default=""

{bottomRoutingLayer 2} {topRoutingLayer 15}

Look for the Tracks in a section with: Track:

While corrections can be made to the tmp.fp file and reloaded with the "loadFPlan tmp.fp" Tcl command, it is generally easier to do make changes with the Innovus GUI.

IMPPTN-1671

NAME

IMPPTN-1671

SUMMARY

The option %s cannot be used for updating pin attribute. Correct the command options and run the command again.

DESCRIPTION

Specified option cannot be used for just updating pin attribute. This option is used with other options for assigning pin location. Check the reference manual for the legal specified options. Then

correct the command options and rerun the editPin command again.

IMPPTN-1699

NAME

IMPPTN-1699

SUMMARY

Selective-pin-assignment by specifying just partition name(s) to command assignPtnPin is obsolete and will be removed in future releases. The old usage still works in this release, but to avoid this warning and to ensure compatibility with future releases, replace the obsolete usage with "assignPtnPin -ptn -pin ".

DESCRIPTION

To avoid this warning and to ensure compatibility with future releases, replace the obsolete usage with 'assignPtnPin -ptn <ptnName> -pin <pinName>'

Example:

---

* The following command assign pins name starting with "in" of partition "A" and pins name starting with "out" of partition "B"

assignPtnPin -ptn {A} -pin {in*} -ptn {B} -pin {out*}

* The following command accept a file pinLst.txt that contains the list of pins to be placed for partition A and partition B.

assignPtnPin -ptn A -ptn B -pin_file pinLst.txt

IMPPTN-1704

NAME

IMPPTN-1704

SUMMARY

The options [-row] and [-bringBackRow] are obsolete. Rows are brought back automatically, without using any of these options. To avoid this warning and ensure compatibility with future releases, update your script to not use any of these options.

DESCRIPTION

This messages is issued when obsolete options are used.Using these options will have no impact in this case.

Example:

---

eg. use flattenPartition

IMPPTN-1717

NAME

IMPPTN-1717

SUMMARY

The specifyPartition command will be obsolete in the next release. Use the definePartition command to define the partitions.

DESCRIPTION

The message occurs because you are using 'specifyPartition' which is obsoletelease use the 'definePartition' command to define the partitions.

Example:

The following example defines a partition:

definePartition \

-hinst ctr_inst \

-coreSpacing 0.56 0.56 0.0 0.0 \

-railwidth 0.0 \

-minPitchLeft 2 \

-minPitchRight 2 \

-minPitchTop 2 \

-minPitchBottom 2 \

-reservedLayer {1 2 3 4} \

-pinLayerTop {2 4} \

-pinLayerLeft {3} \

-pinLayerBottom {2 4} \

-pinLayerRight {3} \

-placementHalo 1.0 1.0 1.0 1.0 \

-routingHalo 1.0 \

-routingHaloTopLayer 7 \

-routingHaloBottomLayer 1

IMPPTN-1755

NAME

IMPPTN-1755

SUMMARY

Pin [%s] of %s [%s] connected to net [%s] is [%s] at location (%8.3f, %8.3f) on layer %1d %s.

DESCRIPTION

Message reports specific error/violation on a partition pin.

Example of ABUTMENT violation on a pin:

Pin [pin_1] of partition [ptn_1] connected to net [net_1] is [PLACED] at location (210.452, 540.160) on layer 8 has ABUTMENT violation WITH partition chip.

In above example error/violation is being reported for partition “ptn_1” pin's “pin_1” which is connected to net “net_1” and is placed at location “210.452, 540.160” on layer “8” having assignment status as “placed”. Pin has abutment (is placed on adjoining boundary of “ptn_1” and “chip”) violation with partition named “chip”. Ideally the pin pair of two adjoining (abutting) partitions should be placed on same track on edge of partition boundaries, touching each other (abutting).

Abutment violation could be because of following two reasons:

1. Net has multi-partition-pins. Since all other pins of different partitions cannot be placed at same location (no electrical connection through any overlap of physical shape), so it is reported as abutment violation.

2. “pin_1” pin of net “net_1” is not connected to any pin of adjoining (abutted) partition “chip”.

List other violations on pin:

- pin min-width violation
- pin min-depth violation
- pin missing metal shape violation
- pin min-area violation
- pin-color violation
- pin not on routing track (or ndr-rule-routing-track) violation
- pin not on fence violation
- pin spacing (drc and spacing constraints) violation
- pin not on allowed layer violation
- For nested partition it checks for child fence area violation
- pin outside pin-guide or bus-guide violation
- Pin associated pin-group or net-group violation

IMPPTN-1802

NAME

IMPPTN-1802

SUMMARY

Route layer setting through routing modes [setRouteMode %s <value>] or [setNanoRouteMode %s <value>] setting will not be honored. Set the value using setDesignMode command [setDesignMode %s <value>] and run the command again.

DESCRIPTION

This message is reported related to IO pin routing if there are any IO pins falls above maxRouteLayer. Message ENCPTN-1802 is generated to correct the user expectation, when user had set either setRouteMode or setNanoRouteMode for minLayer but has missed to set setDesignMode for minLayer, and user would like to set min/max layer of pin that is different from earlyGlobalRoute. Innovus checks for this issue and generate the message as user may forget to set min/max layer of pin when it differs from earlyGlobalRoute.

Example:

Because of the following reason the ENCPTN-1802 is reported.

Message ENCPTN-1802 is generated to correct the user expectation, when user had set either setRouteMode or setNanoRouteMode for minLayer but has missed to set setDesignMode for minLayer.

Use "setDesignMode -topRoutingLayer <layer>" to placing IO pins, to avoid this problem.

IMPPTN-3207

NAME

IMPPTN-3207

SUMMARY

The hierarchical-PG net %s is connected to an instance term %s inside the partition hinst %s. However, it is not connected to any PG port of the partition hinst. This is erroneous data. As a consequence, instance term %s will become unconnected. To correct this error, ensure that the above net is connected to a partition PG port when connecting to an instance PG term inside the partition, and run the command again.

DESCRIPTION

Reason of such incorrect PG net connection is generally introduced by either incorrect UPF or incorrect GNC rule. To correct this error, ensure that the above net is connected to a partition PG port when connecting to an instance PG term inside partition. Or, if this connection is not needed inside the partition hinst, then ensure that the net does not connect to any of the PG terms inside the partition hinst.

IMPREPO-102

NAME

IMPREPO-102

SUMMARY

Instance %s of the cell %s has no physical library or has wrong dimen- sion values (<=0). Check your design setup to make sure the physical library is loaded in and the attributes specified in physical library are correct.

DESCRIPTION

Check LEF files to see if the cell is defined in LEF; if it is, then check if it's dimension is defined by number which is less than 0.

IMPRM-143

NAME

IMPRM-143

SUMMARY

%s is not defined on cut layer "%s" in the technology DB. VIARULE GENERATE values will be used instead. The generated vias, using the VIARULE GENERATE values, are probably not optimal for signal routing and pin access.

DESCRIPTION

This command requires correct enclosure rules to auto-generate correct vias. This warning reports that enclosure rules are not defined on the layer and/or for the cut class, so the cut enclosure values in the VIARULE GENERATE statement will be used. This is not recommended usage except for old technology (LEF version 5.5 and older), because the VIARULE values are often larger than the DRC rules require, which will cause the vias to be too large. Routing results with these vias will likely be more congested and produce longer wires. Check the LAYER section of the technology definitions (the first file listed in the init_lef_file variable), to ensure enclosure rules are defined correctlylease note: the ENCLOSURE rule is used by generateVias, not ENCLOSUREEDGE rule. You can look at the LEF/OA manual to find the correct syntax.

Example: **WARN: (ENCRM-143): ENCLOSURE ABOVE for CUTCLASS VSINGLECUT is not defined on cut layer "VIA4" in the technology DB. VIARULE GENERATE values will be used instead. The generated vias, using the VIARULE GENERATE values, are probably not optimal for signal routing and pin access.

Example:

Example of ENCLOSURE rule used by generateVias:

PROPERTY LEF58_ENCLOSURE

" ENCLOSURE CUTCLASS VX ABOVE 0 0.03 ;

ENCLOSURE CUTCLASS VX ABOVE 0.02 0.02 ;

ENCLOSURE CUTCLASS VX BELOW 0 0.03 ;

ENCLOSURE CUTCLASS VX BELOW 0.02 0.02 ;

ENCLOSURE CUTCLASS VXBAR ABOVE END 0.02 SIDE 0.02 ;

ENCLOSURE CUTCLASS VXBAR ABOVE END 0.03 SIDE 0.01 ;

ENCLOSURE CUTCLASS VXBAR ABOVE END 0.04 SIDE 0 ;

ENCLOSURE CUTCLASS VXBAR BELOW END 0.02 SIDE 0.02 ;

ENCLOSURE CUTCLASS VXBAR BELOW END 0.03 SIDE 0.01 ;

ENCLOSURE CUTCLASS VXBAR BELOW END 0.04 SIDE 0 ;

" ;

If the ENCLOSURE rule is missing, the VIARULE GENERATE value will be used:

VIARULE M2_M1 GENERATE

LAYER M1 ;

ENCLOSURE 0.03 0.03 ;

WIDTH 0.05 TO 4.5 ;

LAYER M2 ;

ENCLOSURE 0.03 0.03 ;

WIDTH 0.05 TO 4.5 ;

LAYER VIA1 ;

RECT -0.025 -0.025 0.025 0.025 ;

SPACING 0.13 BY 0.13 ;

END M2_M1

IMPRM-148

NAME

IMPRM-148

SUMMARY

Command 'generateVias' is normally used for debugging and testing. The vias are only generated in this Innovus session, and will not be kept during save/restore for nanoroute to use the next time. Use 'setGenerateViaMode -auto true' before 'init_design' or 'restoreDesign' if you want generated vias to be used by nanoroute in later Innovus sessions.

DESCRIPTION

Command 'generateVias' can generate all the vias for signal routing automatically, including single cut vias, double cut vias, MAR vias, and even DFM vias. It is used in the Innovus flow, to help insure good routing results. Users don't need to manually create vias to meet the complex rules in advanced technology, 'genereateVias' will consider the rules (including non-default rules) and create the vias needed for routing. Since the vias are only generated in current Innovus session, and will not be kept during save/restore for NanoRoute to use the next time, this command is only used for debugging and testing. The standard usage flow is to set 'setGenerateViaMode -auto true' before 'init_design' or 'restoreDesign'. It will call 'generateVias' whenever the design is initialized or restored in innovus. This mode option setting can be saved in database by saveDesign. You can get more information about 'setGenerateViaMode' by 'man setGenerateViaMode'.

Example:

Debug flow example:

restoreDesign

generateVias

routeDesign

Standard usage flow example:

setGenerateViaMode -auto true

restoreDesign

routeDesign

IMPSC-1001

NAME

IMPSC-1001

SUMMARY

Unable to trace scan chain "%s". Check the information during tracing.

DESCRIPTION

Possible reason for scan trace failure is that instance in the scan chain has multiple corresponding pins for scan tracing.

How to solve the problem:

1. Use a Scan DEF file to define the exact instance pins scanTrace should trace through. Most modern synthesis tools can export a Scan DEF file which can then be imported into Innovus System using the defIn command:

defIn scanchain.def

2. If the design contains bidirectional pads, try defining the start/stop points of the scan chain on the core side of the pad so the tracer does not have to trace through the pad.

3. If instances in the scan chain has complex logic, set "setScanReorderMode -compLogic true" before scanTrace.

Example:

If the message is preceded with the following warnings:

**WARN: (ENCSC-1020): Instance's output pin "reg_1/Z" (Cell "DFFX12") has multiple corresponding input pins for scan tracing.

Please either specify the instance in the DEF scanchain, or use "setScanReorderMode -compLogic true". Otherwise scan trace may not succeed.

Then set setScanRorderMode -compLogic true prior to scan tracing. This will enable an advanced algorithm for tracing complex logic (gates with multiple inputs)

IMPSC-1010

NAME

IMPSC-1010

SUMMARY

During incremental tracing, scan chain "%s" cannot trace from "%s" to "%s". Perform regular trace.

DESCRIPTION

Incremental tracing will perform register to register tracing without other scan flops in between.

Check if any other scan flops were inserted between them in the flow.

IMPSC-1022

NAME

IMPSC-1022

SUMMARY

Instance's output pin "%s/%s" (Cell "%s") has no corresponding input pin for scan tracing.

DESCRIPTION

After reading scandef file, Innovus system gives the message during scanTrace. The warning message here is due to fact that scandef file and the verilog netlist are not compatible with respect to the scan chain and so tool is not able to trace it.

Example:

**WARN: (ENCSC-1022): Instance's output pin "i_Scan/i_Core/i_inst/QN" (Cell "XXX") has no

corresponding input pin for scan tracing.

The relevant part in the scandef file is like below:

==========

+ ORDERED

i_Scan/i_Core/i_inst (IN SI) (OUT Q) ---> It should be QN here.

i_digitalScan/i_digitalCore/U9714 (IN B1) (OUT ZN)

==========

The output "QN" is reported by the tool for not having corresponding input pin for scan tracing because the scan chain is defined over the pin "Q" in scandef file.

The scan chain is defined at negated output QN of the Flop but scan def file points to pin Q of the flop (which is not the part of scan chain) and hence tool is not able to trace it. So, make sure that scandef file and the verilog netlist are compatible with respect to the scan chain for the tool to trace it successfully.

IMPSC-1138

NAME

IMPSC-1138

SUMMARY

In scan chain "%s" DEF ordered section, buffers or logics following scan instance "%s" are corrected to match the netlist.

DESCRIPTION

This message is generated when the original SCAN DEF does not match the design netlist. One possible reason this may happen is because of an ECO operation which adds a buffer to a scan chain for hold fixing.

Example

Sample SCAN DEF (excerpt) :

...

...

u1/u2/u3/reg_0_6 (IN SI) (OUT Q)

u1/u2/u3/reg_0_7 (IN SI) (OUT Q)

u1/u2/u3/reg_0_8 (IN SI) (OUT Q)

...

Adding a buffer between reg_0_7 and reg_0_8 (to possibly fix a hold violation) will generate the above message.

IMPSE-31

NAME

IMPSE-31

SUMMARY

Tool name list given is not a proper TCL list: '%s'.

DESCRIPTION

Please correct the list and try again.

IMPSE-32

NAME

IMPSE-32

SUMMARY

Failed to locate '%s' in Cadence Online Support documents.

DESCRIPTION

The documents may not be installed correctly, or the content you are searching for is not in the documents. Try searching for a command you know exists to see if the installation is correct. If that fails, look at the User Guide Installation chapter for how to install the documents.

IMPSE-34

NAME

IMPSE-34

SUMMARY

Metric snapshot stack is not at the top level.

DESCRIPTION

A metric report was generated while still within a nested snapshot. This suggests a missing pop_snapshot_stack.

IMPSE-35

NAME

IMPSE-35

SUMMARY

Attempt to set undefined metric: %s

DESCRIPTION

An attempt was made to set and undefined metric.

IMPSER-514

NAME

IMPSER-514

SUMMARY

Binary DB for leaf cell %s has extra terminal %s. This terminal is not found in the .lef/.lib library definition. Connectivity of this terminal will be lost while reading the binary DB.

DESCRIPTION

One possible reason could be that either .lef/.lib are edited after the design was saved OR

.lib is not being read that has the definition of missing terminal.

IMPSP-101

NAME

IMPSP-101

SUMMARY

setPlaceMode Option '%s' is obsolete in current release. Use setPlaceMode option '%s' instead to access the same functionality.

DESCRIPTION

In Innovus some setPlaceMode options are made obsolete because another setPlaceMode

option is developed to provide better functionality or usability. This message

tells user that equivalent setPlaceMode option %s should be used instead of

obsolete setPlaceMode option %s.

IMPSP-105

NAME

IMPSP-105

SUMMARY

'setPlaceMode -maxRouteLayer' will become obsolete from next release. Use 'setRouteMode -earlyGlobalMaxRouteLayer N' to set maximum routing layer.

DESCRIPTION

The message occurs because there is a command usage to set maximum routing layer, which is 'setRouteMode -earlyGlobalMaxRouteLayer N'. The original command 'setPlaceMode -maxRouteLayer' will become obsolete from next release. Please update your script with the new command usage.

Example:

The following example sets the maximum routing layer to metal 7:

.in +4

innovus> setRouteMode -earlyGlobalMaxRouteLayer 7

.in

IMPSP-157

NAME

IMPSP-157

SUMMARY

Macro '%s' is not placed within core boundary.

DESCRIPTION

Macro '%s' is not placed within core boundary with location (%d,%d). This will cause issues for placement and downstream flow. Either use placeInstance command to fix the macro inside core boundary or redo the floorplan using planDesign command.

Example:

**WARN: (IMPSP-157):

Macro 'u_rxb_wrapper/u_rxf/u_hm_0/u_hm_mem_edram_2port_3/u_edram/

WRAPBRCD/INTWRAP/DRAMT' is not placed within core boundary

To fix this warning use placeInstance command to place macro inside the core.

placeInstance

u_rxb_wrapper/u_rxf/u_hm_0/u_hm_mem_edram_2port_3/u_edram/WRAPBRCD/INTWRAP/DRAMT 398.7 1480.2 -fixed

IMPSP-167

NAME

IMPSP-167

SUMMARY

Layer Number Provided for MaxRouteLayer option exceeds the MaxLayerNumber for the design. Current option '%s' is ignored.

DESCRIPTION

Need to get rid of this warning as we have deprecated MaxRouteLayer in setPlaceMode.

Example:

IMPSP-182

NAME

IMPSP-182

SUMMARY

Placeable area is 0. Stopping placement.

DESCRIPTION

This error is issued during placeDesign. Placement does not proceed when the available space for placing instances is zero.

This can be confirmed through the following message from placeDesign which shows the allocated area is 0:

Density for the design = 2311140.000.

= stdcell_area 2311140 (330225 um^2) / alloc_area 0 (0 um^2).

Please check if the design is completely blocked by placement blockage. User may find that

a placement blockage cover the block. Also, make sure that there are sites / rows defined in the design.

IMPSP-183

NAME

IMPSP-183

SUMMARY

Design has %s associated with some modules." " So software will override the current '0' value of '-keepEmptyModule'" " of import_mode. Empty modules will not be deleted.

DESCRIPTION

Default value 1 of -keepEmptyModule, is being applied to this mode option,

as deleting an empty module which has constraint or power-domain associated

with it can result in DB integrity issues. Hence, to ensure that software

does not seg-fault, this option is being reverted back to its default value.

IMPSP-185

NAME

IMPSP-185

SUMMARY

Found user set 'fastPolygon' mode for placement legalization API.

DESCRIPTION

LEF MACRO geometries (PORT, OBS) are defined using POLYgon shapes,

rather than RECT shapes. As DRV checking works with RECTs, these

polygons need to be broken down to rectangle during checks. This can

effect run-time, and in current implementation, is not thread-safe.

This may have an effect on GigaOpt Engine.

IMPSP-259

NAME

IMPSP-259

SUMMARY

**Info: (IMPSP-259): %s %s was not on the placement grid. It has been moved from (%d,%d) to (%d,%d).

DESCRIPTION

Example:

**Info (IMPSP-259): Cell icg_f16_dh_12t_svt is not on the placement grid. It has been moved from (2181212,1019656) to (2181060,1019200).

IMPSP-260

NAME

IMPSP-260

SUMMARY

Inst %s (cell %s) cannot be legally placed in constraint %s.

DESCRIPTION

Inst %s (cell %s) cannot be legally placed in constraint %s. Most probably there is not enough space available in the constraint %s to legally place the cell. Increase the area of constraint %s and re-run placement again.

Example:

IMPSP-263

NAME

IMPSP-263

SUMMARY

Cannot find access pin for fterm '%s' (cell '%s').

DESCRIPTION

This warning message is generated when there is no pin geometry for a cell's

pin defined in the LEF file. This needs to be corrected so the router can route

to the pin. Review the LEF being read in for this cell and confirm the physical

shape of the pin is described in the PORT statement.

Example:

Warning message was generated when running placeDesign.

The RECT statement below describes the geometry of the pin shape. If this is missing, the warning above is issued:

MACRO INVD1

.in +2

...

PIN I

.in

.in +4

DIRECTION INPUT ;

PORT

LAYER M1 ;

RECT .5 2 1 2.5 ;

END

.in

.in +2

END I

.in

If the pin is defined properly in the LEF, confirm this LEF file is specified in the configuration file and is read in before an antenna LEF files for this cell.

IMPSP-270

NAME

IMPSP-270

SUMMARY

Cannot find a legal location for MASTER CELL '%s'.

DESCRIPTION

Possible reasons for not finding any legal location for a cell are:

1. Cell's techSite has no rows in floorplan. To fix - re-init floorplan
2. Width of cell is too large for the dense power stripes' pitch. Make sure that stripe's layer is not being treated as obstruction - setPlaceMode -prerouteAsObs setting may need to change.

IMPSP-288

NAME

IMPSP-288

SUMMARY

Power domain %s has no fence constraint. Placement will ignore this power domain ...

DESCRIPTION

Given Power Domain does not have an area specified for restricting placement of its members. If this power domain needs level-shifters or isolation from other power domains, then tool will not be able to place these shifters/isolation cells to the power domain area boundary, to properly isolate.
Use command modifyPowerDomainAttr to specify a box for this domain.

IMPSP-300

NAME

IMPSP-300

SUMMARY

No layer1-to-layer2 spacing rule specified for any Implant layer in-use. Ignoring -honorImplantSpacing option.

DESCRIPTION

-honorImplantSpacing has no effect unless there is more than one Implant layer, and there is a spacing rule between different Implant layers, and your cell data has the corresponding Implant layer shapes in them.
Placer does not look at same-layer spacing rules for implant layers. It only enforces rules for spacing between different implant layers.
-honorImplantSpacing will be ignored until spacing rules between different implant layers are added to your technology rules.
For LEF, look for SPACING rules on the TYPE IMPLANT layers; and ensure that a spacing rule to a different layer exists as per syntax and example below:
.in +8
SPACING minSpacing [LAYER layerName2] ;
SPACING 0.28 LAYER HVT ;
.in
For OpenAccess rules, look for the oacMinClearanceRule on the implant layers.

IMPSP-305

NAME

IMPSP-305

SUMMARY

Cell:%s, Pin:%s geometry (<%d,%d> <%d,%d>) is sticking out of cell's " "boundary (<%d,%d> <%d,%d>). " "Placement will not be able to catch DRVs on the portion of pin " "outside the cell boundary. To avoid this, pin geom of the library cell " "model needs to be fixed.

DESCRIPTION

When doing Cell-to-Preroute design rule checks, the cell PR boundary is used as the search area, and as bounding box for insertion into search trees. Thus, spacing checks from a special wire geometry may see the PR boundary to be ok as a pre-check, and may not do detailed checking on each pin in this situation.
Thus, in this corner case, the pin outside the PR boundary may be causing a spacing violation, but will not be detected.
This is library cell modeling issue, and can not be fixed at design stage.

IMPSP-307

NAME

IMPSP-307

SUMMARY

**Info: (IMPSP-307): Design contains fractional %d cell%s.

DESCRIPTION

Fractional cells are cells where the width is not an integer multiple of the site and/or the height is not an integer multiple of the row height.

You can use command "checkDesign -physicalLibrary" to get a list of cells considered fractional.

IMPSP-308

NAME

IMPSP-308

SUMMARY

**Info: (IMPSP-308): Cell %s is fractional: %d:%d

DESCRIPTION

Given cell's width is not an integer multiple of its techSite width.

The values given are <cell-width % techSite-width> : <techSite-width>

IMPSP-309

NAME

IMPSP-309

SUMMARY

Pin %s in cell %s will cause issue in router access. Most probably the " "enclosure of via is larger than pin %s. Input the correct library cell %s " "and re-run placement.

DESCRIPTION

Example:

The via enclosure is larger than pin %s. Please correct the library cell %s and re-run placement.

IMPSP-315

NAME

IMPSP-315

SUMMARY

Found %d instances insts with no PG Term connections.

DESCRIPTION

Instances without PG connections, will fail legality check, as unconnected supply pins will short with followpins, if present. If followpin routing has not been done yet, although legality checks will not fail, design is still not in realizable state till these connections have been made.
One way to remedy the situation is to create global-net-connect rules, or if the rules exist, use command applyGlobalNet to make the connections.

IMPSP-357

NAME

IMPSP-357

SUMMARY

Could not initialize placement legalization data for power domain %s.

DESCRIPTION

The possible reasons for not initializing the placement legalization data for a power domain are:

1. The power domain has no tech site information.

2. The constraint box of the power domain is invalid.

3. The row information for the power domain is missed.

IMPSP-362

NAME

IMPSP-362

SUMMARY

Site '%s' has %s std.Cell height, so ignoring its X-symmetry.

DESCRIPTION

In a floorplan with flipped rows, with supply followpins being shared between rows, the cells of a single (or odd multiple) row height cannot be flipped

in Y-direction, as that would cause power to short with ground. As a result, the techSite needs to be defined with only symmetry Y, and must not have

symmetry X - allowing cells to be flipped around Y axis (R0->MY), but not X axis (R0->MX).

This message is reported when a core site definition includes the symmetry X which is typically not intended. SYMMETRY X means the site is symmetric about

the x axis. This means that N and FS sites are equivalent, and FN and S site are equivalent. A macro with an orientation of N matches N or FS rows.

Typically, this is not intended because it would allow the power rails to not align (i.e. the cell would be allowed to flip so a VDD rail aligns with a VSS

rail). Typically, only time X symmetry might be used for a site is with double height cells.

This message simply is indicating that Innovus does not believe the X symmetry was intended and

therefore ignoring it. To avoid this message remove

the X symmetry from the site.

For more information on defining symmetry, please refer to the "LEF language reference" manual.

Example:

Example site definition that causes this warning :

SITE core

.in +4

SYMMETRY x y ;

CLASS core ;

SIZE 0.660 BY 5.040 ;

.in

END core

IMPSP-365

NAME

IMPSP-365

SUMMARY

Design has inst(s) with SITE '%s', but the floorplan has no rows defined for this site. Any locations found for such insts will be illegal; create rows for this site to avoid this.

DESCRIPTION

This warning will be reported by commands such as checkFPlan and placeDesign

when the floorplan does not contain any rows for the specified site. Each

standard cell in the LEF should have a SITE defined for it. Instances of this

cell can only be placed in rows defined for this site.

Example:

Run the following command(replace RAM_site with your specific site name) to report the instances which use this site:

.in +2

dbGet [dbGet -p3 top.insts.cell.site.name RAM_site].name

.in

When you create the initial floorplan, it should automatically create rows for

the standard cells defined in the netlist. You can add additional rows using

Floorplan - Row - Create Core Row or using the createRow text command. If this

warning is occurring on standard cells you must define rows for them or else

they will not be placed.

If this problem occurs for hard macros such as memories you can ignore it.

Rows are not required by the hard macros. Remove the SITE definition in the LEF for the

hard macros to avoid this message for them.

If this occurs for IO pads you can also ignore it. Rows for IO pads are

optional. You can create IO rows using Floorplan - Row - Create I/O Row or

using the createIoRow text command.

IMPSP-372

NAME

IMPSP-372

SUMMARY

Found mismatched FollowPin in rows. Switching off DRC check from preroutes for this run. This

may cause illegal placement.

DESCRIPTION

Example:

There are missing tech SITE warnings when the design is being loaded. These messages are related to the IMPSP-372 warnings that are issued later.

_____

**WARN: (IMPFP-3961): techSite 'foo_SITE_IO_250000' has no related Cells, So Cannnot calculated VDDonbotom attributes. Need correct LEF filea?|a?|

**WARN: (IMPFP-3961): techSite 'foo_core2' has no related Cells, So Cannnot calculated VDDonbotom attributes. Need correct LEF filea?|a?|

**WARN: (IMPFP-3961): techSite 'foo_CORE3' has no related Cells, So Cannnot calculated VDDonbotom attributes. Need correct LEF filea?|a?|

**WARN: (EMS-63): Message has exceeded the default message display limit of 20. To avoid this warning, increase the display limit per unique message.

_____

If the site is not used in any standard cell macro, it can be ignored. The site should be removed from the LEF.

In Innovus it is assumed that all CLASS CORE site have standard cells associated with them, and we analyze the standard cells to identify power/ground followpins for consistency checks.

This results in the following message:

**WARN: (IMPSP-372): Found mismatched FollowPin in rows. Switch off DRC check from preroute. This may cause illegal placement.

IMPSP-373

NAME

IMPSP-373

SUMMARY

FollowPins in %d rows did not match the supply layout of the cells " "for that row orientation. This will result in power shorting to ground " "for all insts placed in these rows.

DESCRIPTION

Followpin pre-routes for some std-rows do not match the supply layout of

the cells for that row's orientation. That is, power pin of instances on

that row is shorted to ground followpin stripe, and vice versa.

In checkPlace results, this will show up as multiple 'Pre-route DRC' Violations.

Result of placeDesign/refinePlace may be "placement" legal, but will not

be DRC clean.

Delete and redo followpin routing, and rerun refinePlace to clean up

any remaining DRCs.

IMPSP-374

NAME

IMPSP-374

SUMMARY

Expected %s to have rows of basic site %s, but found %d rows only of other " "site(s). Check if the %s's row creation is correct before proceeding.

DESCRIPTION

A floorplan object's basic site is usually the smallest site of all instances to be placed within that object.

Here, a floorplan object can be a power-domain, a partition, or the entire core of a top-level or block design.

There should be at least one row of the basic site in a given floorplan object; while other rows can be of sites whose dimensions are integer multiples of those of its basic site.

In this case, the floorplan object has no rows of its basic site. Thus, instances of the cells using the basic site will find no legal location within the confines of this floorplan object.

IMPSP-452

NAME

IMPSP-452

SUMMARY

Density for module '%s' (%s = {%.3f %.3f %.3f %.3f}) is greater than 100% (%.3f) since the available site area for this module is smaller than sum of module instance area and blockage area. Most probably this is caused due to overlapping floorplan constraints such as guides, regions or fences. Correct the floorplanning constraints for this module and re-run placement again.

DESCRIPTION

This message is to check density of module. If the density of the module is greater than 100%, it will issue this message.

placeDesign handles differently based on whether the region is a fence or power domain. In both cases the user should increase the size of the fence or power domain (PD) to accommodate the cells.If a PD is not large enough to accommodate the standard cell logic then placeDesign will reports this message.

Example:

---

(1) Seed file

VERSION 1.0

BEGIN SEED

name=U_IOP/U_IOP_MPI createfence=true util=1.1

END SEED

(2)

<CMD> planDesign -constraints tn_seed.11

**WARN: (IMPSP-452): Density for module 'U_IOP/U_IOP_MPI' is greater than 100% (1.001) since the available site area for this module is smaller than sum of module instance area and blockage area. Most probably this is caused due to overlapping floorplan constraints such as guides, regions or fences. Correct the floorplanning constraints for this module and re-run placement again.

IMPSP-508

NAME

IMPSP-508

SUMMARY

Option -checkPinLayerForAccess takes a list of layer number, not layer name or boolean value. The default value 1 has been used for option -checkPinLayerForAccess.

DESCRIPTION

The recommended setting is to specify the layer number list like "setPlaceMode -checkPinLayerForAccess {1 2 3}". Default value 1 would be used for checking when boolean value is asserted; it's unpredictable when layer name is specified - "setPlaceMode -checkPinLayerForAccess {M1 M2 MET3}" would be presented as "setPlaceMode -checkPinLayerForAccess {1 2 3}" even MET3 doesn't be defined in LEF; "setPlaceMode -checkPinLayerForAccess {V12}" would be presented as "setPlaceMode -checkPinLayerForAccess {2}".

Example:

<CMD> setPlaceMode -checkPinLayerForAccess true

**WARN: (IMPSP-508): Option -checkPinLayerForAccess takes a list of layer number, not layer name or boolean value.

The default value 1 has been used for option -checkPinLayerForAccess.

IMPSP-514

NAME

IMPSP-514

SUMMARY

Turning OFF selective property of soft-blockages, as design restored had been saved by Encounter %s, and that version did not have this property turned on.

DESCRIPTION

The selective property of soft-blockages is now default true. If the design was saved by any version earlier then EDI14.1, then Innovus's behavior regards to soft blockage was different at the time design was saved. To not change the behavior, this selective property of soft-blockage is switched off when earlier DB version is detected.

To switch to the new default behavior, you can set place-mode as:

setPlaceMode -selectiveBlockage true

This will override the backward compatibility mode for this option, and soft blockages will only allow 1,2-pin cell instances.

IMPSP-1760

NAME

IMPSP-1760

SUMMARY

Buffer footprint does not have non-inverting buffers. Using inverter footprint for Virtual IPO. Verify you have buffers defined in the libraries you have read in and confirm they are usable by running reportDontUseCells. Run 'setDontUse bufferName false' to enable buffers which are currently unusable.

DESCRIPTION

This message is issued when placeDesign cannot find any usable buffers during timing driven placement.

Timing driven placement runs a virtual In-Place Optimization (VIPO) to predict how buffering will be done in order to achieve a better placement. If it cannot find any usable buffers it will use inverters instead.

Verify that you have:

1. Buffers defined in your library,

2. The timing libraries for the buffers have been read in,

3. The buffers are usable.

Run

.in +8

reportDontUseCells

.in

or

.in +8

reportFootPrint -dontTouchNUse -outfile footprint.rpt

.in

to report don't use cells.

Use the setDontUse command to control usability of cells. To enable a buffer which is currently unusable, run

.in +8

setDontUse bufferName false

IMPSP-2002

NAME

IMPSP-2002

SUMMARY

Density too high (%.1f%%), stopping detail placement.

DESCRIPTION

The most likely reasons for excessive density are:

1. The presence of unfixed hard macros in the design.

2. Too many instances being inserted without legal locations.

3. The design being filled with filler cells.

IMPSP-2020

NAME

IMPSP-2020

SUMMARY

Cannot find a legal location for instance '%s' (Cell %s).

DESCRIPTION

Possible reasons for no legal location found, are:

1. Width of instance's cell is too large for the dense power stripes'

pitch. Make sure that stripe's layer is not being treated as obstruction. Place-mode's -setPrerouteAsObs setting may need a change.

2. Floorplan rows are created incorrectly, making rows for this instance's cell not be placeable. Check correct basic site is set in floorplan creation.

3. Power/Ground followpin pre-routes do not match rows' orientations. Either re-create the rows, or re-route followpin wires.

This will cause run-time issues during detail placement step called by placeDesign or refinePlace.

Example:

This issue can be seen when there is a problem with globalNetConnects. If the power/ground pins are not properly connected to the rail, then the rail appears as obstruction and the cells cannot be legalized. The issue can be fixed by having proper orientation of rows in the floor-plan and by [having] or re-routing follow pin wires matching row orientation.

For example, M2 followpin width is too large which causes spacing violations with M2 pins/obs of certain cells no matter where these cells are placed. This causes long runtimes during legalization and the resulting placement will not be illegal.

In order to debug this turn off DRC checking during placeDesign or refinePlace using

.in +5

setPlaceMode -checkCellDRCFromPreRoute false.

.in

Once design is placed, turn DRC checking back-on and run checkPlace. Look for DRC violations on these cells between M2 pins/obs and follow pin. Correct the follow pin routing to make sure the DRC violations are gone between cells and follow pin. Rerun placeDesign/refinePlace again for legalized placement.

Check for verifyGeometry for Std. cell check and make sure your Std. cell is in Sync. with Tech file, to avoid legalization issues.

IMPSP-2021

NAME

IMPSP-2021

SUMMARY

Could not legalize <%d> instances in the design. Check warning message IMPSP-270, IMPSP-452, IMPSP-2024, IMPSP-2039, IMPSP-2040, IMPSP-2042 or IMPSP-2020 in log file for more details.

DESCRIPTION

If there are instances in design that could not be legalized,

refinePlace would give a warning for each of those instances (IMPSP-2020), or master-cell (IMPSP-270). There can be a number of reason why refinePlace could not find a legal location, such as:

* Cell may not have its site rows defined correctly in floorplan, or

* There may be a conflict between cell-library and power-planning structure such that some cells always have a spacing violation between thier pin or obs geometry and power net wires/vias/cuts.

* Some Region/Fence constraint may be over subscribed (IMPSP-452)

* Track offset and definition used may not allow for on-grid pin-access (for som advanced node libraries)

SEE ALSO

.in +5

Man-page for IMPSP-2020

.in

IMPSP-2022

NAME

IMPSP-2022

SUMMARY

No instances to legalize %s

DESCRIPTION

This message is issued by refinePlace if it does not find any instances to place. If command was invoked using '-inst' option, then some insts in the given list of instances should be valid for legalization.

refinePlace command will only legalize instances that are already in PLACED status. Thus, instances that are either in FIXED status, or UNPLACED status, are not counted.

IMPSP-2041

NAME

IMPSP-2041

SUMMARY

Found %d fixed insts that could not be colored.

DESCRIPTION

Design has instances fixed in locations where they are not considered legal. Due to same-mask spacing rules and adjacent colored geometries (such as PG nets wires and vias), the attempt to color them may result in incorrect color. Hence, these instances will not be colored till they are legalized.

You can run

.in 8

checkPlace

.in

to find the reason why the instance is not considered legal.

IMPSP-2044

NAME

IMPSP-2044

SUMMARY

The 'getDesignMode -addPhysicalCell' value is " "'flat' (not 'hier'). As such, physical insts added to the design will " "not be hierarchical, and will not have membership in fence/regions. " "If the design has fences, refinePlace will move placed physical " "insts out of the fences.

DESCRIPTION

Flat physical instances means that in the design hierarchy, they will
all be based on the top-level, and not inside the module hierarchy.
As fences/power-domains/partitions all are set on a module at a lower-
level then the top-of-the-design, the fillers will physically be
placed inside the bounding-box, but in DB, they will not belong
to the module associated with that placement-constraint. While
legalizing these physical instances, refinePlace will see
these instances as not having the fence membership, and will throw
them out to the top-level.
Just changing this mode setting is not enough, as any fillers
already added in the flow till this point (since the mode was set)
would already be inserted at the top-level. Hence those fillers will
need to also be deleted, and re-inserted after the mode has been
reset to 'hier'.

IMPSP-2702

NAME

IMPSP-2702

SUMMARY

There is no techSite '%s' in the library.

DESCRIPTION

The message is reported when a stand cell library does not have core site

definition. To fix the warning check std cell lef and correct the core site.

Example:

IMPSP-2704

NAME

IMPSP-2704

SUMMARY

No GA fillers have been detected in the design for replacement. Any new GA cells will remain unplaced.

DESCRIPTION

This error message is issued when no physical-only instances of the specified GA filler cell type(s) are present in the design. For ecoPlace to make use gate array fillers they must be physical-only.

Example:

IMPSP-2707

NAME

IMPSP-2707

SUMMARY

TechSite '%s' used by the GAFiller list does not have rows in the design.

DESCRIPTION

The message is reported when the corresponding core site rows are not created,

Check and create the corresponding rows to over come this warning. Use createRow -site <Site name>.

Example:

IMPSP-2717

NAME

IMPSP-2717

SUMMARY

There are %.2f\%(unplaced instance ratio) unplaced instances in the design, please run placeDesign instead of ecoPlace to avoid potential bad DRC and timing result.

DESCRIPTION

For timing-driven ecoPlace, the threshold of unplaced instance ratio is 15%.

For non timing-driven ecoPlace, the threshold of unplaced instance ratio is 5%.

IMPSP-2901

NAME

IMPSP-2901

SUMMARY

%i %s height segment%s too small to resolve.

DESCRIPTION

Segments that are too small to resolve are likely caused by fixed cells that are too close together. These cells must be manually adjusted, or unfixed so they may be moved by addFillerGap.

IMPSP-2902

NAME

IMPSP-2902

SUMMARY

%i %s height segment%s impossible to resolve.

DESCRIPTION

Segments that are impossible to resolve have an amount of free space that is nonzero and less than the provided minGap value. These segments

may be resolved by enabling the 'medium' effort mode of addFillerGap.
These segments may still be impossible to resolve under 'medium' effort
if no nearby segments can be found for cell movement or swapping.

IMPSP-2903

NAME

IMPSP-2903

SUMMARY

%i %s height segment%s too difficult to resolve.

DESCRIPTION

Segments that are too difficult to resolve are probably caused by pin
access constraints that interfered with the cell sliding mechanism.
The cells in these segments will probably have to be manually adjusted.

IMPSP-5101

NAME

IMPSP-5101

SUMMARY

The design must be completely placed before adding filler cell(s).

DESCRIPTION

When running addFiller the warnings or error above are issued.
When addFiller runs it checks whether the entire design is placed or not. If it is not, you will see this messages. When user would like to work on floorplan and want to run DRC checks on it in PVS or other tool, you may like to fill all the entire row area with fillers instead of running an entire placement.
If user receive the IMPSP-5101 warning it will still fill the rows with filler cells. It is simply warning you that the design is not entirely placed with below warnings.
**WARN: (IMPSP-5102): There 'are' 10 unplaced instances in the design..
OR
**ERROR: (IMPSP-503): Design must be placed before running "addFiller".
If you receive the IMPSP-503 error you can still place fillers by specifying the core area.
Example:

.in +2
addfiller -area [dbGet top.fplan.coreBox]
addfiller -area [dbGet top.fplan.coreBox]
.in

IMPSP-5106

NAME

IMPSP-5106

SUMMARY

AddEndCap cannot place end cap cells at the ends of the site rows. Most probably there are pre-placed std-cell inst%c at '%s' of '%s' row%c. Remove pre-placed instances and re-run addEndCap

again.

DESCRIPTION

The addEndCap command won't add end caps if there are existing cells at the end of rows, but if there are placement blockages and no existing cells it will add end caps next to the placement blockage.

Example:

IMPSP-5113

NAME

IMPSP-5113

SUMMARY

Maximum of only two tie-cells can only be provided.

DESCRIPTION

When user provides more than two cells for -cell < > option, Innovus will

error out with message IMPSP-5113.

User has to provide only two cells as in the example given below, Where

one cell must be a tie-high driver, and the other is a tie-low driver.

Example:

Right Approach:

addTieHiLo -cell "tieoff_hi tieoff_lo"

setTieHiLoMode -cell "tieoff_hi tieoff_lo"

Wrong Approach:

addTieHiLo -cell "tieoff_hi tieoff_lo tieoff_hi_pm tieoff_lo_pm"

setTieHiLoMode -cell "tieoff_hi tieoff_lo tieoff_hi_pm tieoff_lo_pm

IMPSP-5119

NAME

IMPSP-5119

SUMMARY

AddEndCap is unable to add %s-cap cell (%s) at (%0.3f, %0.3f).

DESCRIPTION

Most likely reason is:

The end location is already occupied by a fixed

instance or placement blockage.

It is illegal to add cap cell at this

location.

Fix these issues and re-run addEndCap command again.

Example:

IMPSP-5123

NAME

IMPSP-5123

SUMMARY

Cell %s is not found.

DESCRIPTION

The message occurs when the filler cell(s) your specified for setFillerMode or addFiller can not be found. Please make sure the cell(s) exist in the design.

Example:

---

* The following example checks the existence of cells with prefix 'FILL':

.in +4

innovus 20> get_lib_cells FILL*

lib1/FILL1 lib1/FILL2 lib1/FILL4

.in

IMPSP-5125

NAME

IMPSP-5125

SUMMARY

No filler cell provided.

DESCRIPTION

Previously in the ECO flows, the filler cells used to be deleted before ecoPlace and then they would be added back.

With the supercommand "ecoDesign", the filler cells have to be identified by the user so that internally the commands for addition and deletion of FILL cells can be called.

Example:

CMD> ecoDesign -noEcoRoute

FOO_RUNDIR/FOO_top.dat

FOO_top ../../../eco_v/FOO_top.v

Statistics of distance of Instance movement in

detailed placement:

.in +2

maximum (X+Y) = 0.00 um

mean (X+Y) = 0.00 um

.in

Total instances moved : 0

*** cpu=0:00:14.0 mem=2240.1M mem(used)=4.9M***

ERROR (SOCSP-5125): No filler cell provided.

To resolve use below approch :

The FILL cells are identified by setting this :

setFillerMode -core {corefill_3 corefill_2 corefill_1} -corePrefix xofiller_

If the design is being restored from a previously saved session, the .mode file

in the .dat dir will need to edited to add this command to it.

IMPSP-5131

NAME

IMPSP-5131

SUMMARY

%s '%s' has been marked dont_touch. %s %s will not be considered for tie-cell %s

DESCRIPTION

addTieHiLo is able to honor the don't touch property, this is controlled by

"setTieHiLoMode -honorDontTouch {true|false}"

Example:

In the design, there are four power nets: VDD, VSS, AVDD and AVSS. In the netlist, following connections are defined:

.in +4

module top (...);

...

.in

.in +8

analog_block a_inst(.A(AVDD), .B(AVSS), ...);

digital_block d_inst(.A(1'b1), .B(1'b0), ...);

.in

.in +4

endmodule

.in

If user have manually connected the analog tie high/low pins to AVDD and AVSS, use following flow to insert tie high/low cells for VDD and VSS without addTieHiLo inserting them for AVDD and

AVSS:

set_dont_touch [get_lib_cells TIEHI] false

set_dont_touch [get_lib_cells TIELO] false

set_dont_touch AVDD true

set_dont_touch AVSS true

setTieHiLoMode -cell {TIEHI TIELO} -honorDontTouch true

addTieHiLo

This will mark AVDD/AVSS as dont touch and tell addTieHiLo to honor the dont touch property.

The correct connections are shown in the resulting netlist:

.in +4

module top (...);

...

.in

.in +8

.TIELO LTIELO (.Y(LTIELO_NET));

.TIEHI LTIEHI (.Y(LTIEHI_NET));

analog_block a_inst (.B(AVSS), .A(AVDD), ...);

digital_block d_inst (.B(LTIELO_NET), .A(LTIEHI_NET), ...);

.in

.in +4

endmodule

.in

IMPSP-5134

NAME

IMPSP-5134

SUMMARY

Setting %s to %0.3f (microns) as a multiple of cell %s's techSite '%s' width of %0.3f microns

DESCRIPTION

Placement grid is based on the size of unit tech site. When the specified value is not multiple times of tech site size, it must be automatically adjusted to make sure all instances are placed on placement grid.

Example:

<CMD> addWellTap -cell WELLTAP -cellInterval 33

**WARN: (IMPSP-5134): Setting cellInterval to 32.900 microns as a multiple of cell WELLTAP's techSite 'core' width of 0.140 microns.

IMPSP-5140

NAME

IMPSP-5140

SUMMARY

Global net connect rules have not been created. Added %sinsts would have no supply connectivity, and would fail DRC.

DESCRIPTION

New instances created rely on Global-Net-Connect rules to determine which

supply net to connect the power and ground pins. With missing GNC rules,

the supply pins are left unconnected. When there are followpin stripes in

design, the followpin wires will be shorting to unconnected supply pins on

the instances. These instances will fail legality checking.

One way to add GNC rules is by using command globalNetConnect.

For example,

.in +8

globalNetConnect VDD -type pgpin -pin VDD

globalNetConnect VSS -type pgpin -pin VSS

.in

IMPSP-5144

NAME

IMPSP-5144

SUMMARY

The specified value of -reportGap is less than the basic tech site width. You should use" "a value equal to or greater than the basic tech site width to avoid this message.

DESCRIPTION

The command "checkFiller -reportGap" is used to check gaps with the specified gap size, especially for 1 site gaps.

As the placement grid is based on the tech site, the minimum -reportGap can be set to is the tech spec site width.

If the value of -reportGap is less than the basic tech site width, then the tool will continue but will use the

basic tech site width to check the gaps instead, reporting this warning message.

Example:

When running 'checkFiller -reportGap 0.10' for a design whose basic tech site is 0.14 micron,

checkFiller will report this warning message and continue to check gaps using the value 0.14 instead.

IMPSP-5157

NAME

IMPSP-5157

SUMMARY

Design has cells with user specified padding. This could result in gaps next to the instances of these cells.

DESCRIPTION

This warning message is issued while running addFiller command in a design that has cells with user specified cell padding. Since the cell padding is going to remain in the flow after placement also in order to avoid this message and to fill the gaps the user can delete cell padding using deleteCellPad command and rerun addFiller command.

Example:

IMPSP-5164

NAME

IMPSP-5164

SUMMARY

AON Tie cells insertion is not supported when createHierPort option is enabled.

DESCRIPTION

when setTieHiLoMode -createHierPort true, addTiHiLo can connect the tie pin

across hierarchical instance. In LP design, that means the tie cell can cross

the domain boundary to drive the tie pin whose location is in other domain.

Current addTiHiLo can only insert tie cell to drive the pins in the same location domain.

Example:

Add TiHiLo cells individually for each domain

addTieHiLo -powerDomain PD1

addTieHiLo -powerDomain PD2

addTieHiLo -powerDomain PD3

IMPSP-5169

NAME

IMPSP-5169

SUMMARY

No AON Tie-%s cell found for power domain %s.

DESCRIPTION

Design does not have AON Tie cells for the specified power domain. Check if the libary has AON Tie cells and

if the AON Tie Cells are specified in the CPF for the power domain.

IMPSP-5170

NAME

IMPSP-5170

SUMMARY

PowerDomain %s has no any module defined, stop %s in this powerdomain.

DESCRIPTION

Tool uses the module belong to specific power domain as the hierarchy when inserting physical cells, such as addEndCap, addWellTap, addFiller and addDeCap. These physical cell insertion commands error out if there is no any module defined under the target power domain, users need to modify the power domain definition with module to avoid this issue.

Example:

Incorrect CPF definition - leaf instances are specified to power domain PD_A:
create_power_domain -name PD_A -instances {mod1/inst1 mod1/inst2 mod1/inst3 mod2/inst1 mod2/inst2 mod2/inst3}

Correcting CPF to avoid IMPSP-5170:

create_power_domain -name PD_A -instances {mod1 mod2}

IMPSP-5178

NAME

IMPSP-5178

SUMMARY

Endcap cells for %s don't have same site.

DESCRIPTION

Endcap cells of the given type need to have the same techSite, as they
share the row they will be placed in. As such, if site type is different
than rows cannot be succesfully cap-ed on all required locations.

IMPSP-5216

NAME

IMPSP-5216

SUMMARY

A redundant edge type is found and will not be added.

DESCRIPTION

The warning is given when there are duplicated edge types assigned to the same cell. For example, the same edge type are added twice to the same cell "SDFFQ", you will get this message.

IMPSP-5217

NAME

IMPSP-5217

SUMMARY

addFiller command is running on a postRoute database. It is recommended to be followed by ecoRoute -target command to make the DRC clean.

DESCRIPTION

When -enableLeglizer is set to true, there might be DRC left if running addFiller command on a postRoute DB.

You can call ecoRoute command after addFiller to clean up the DRC,

or set setFillerMode -enableLeglizer to false to avoid this warning message.

IMPSP-5259

NAME

IMPSP-5259

SUMMARY

Options '-virtual_color_cell' and '-virtual_color_map' are obsolete, and have been replaced by command 'specify_cell_virtual_align'. These 'Mode' options still work in this release, but to ensure compatibility with future releases, updating your script is recommended.

DESCRIPTION

Filler mode options for virtual_color get applied during filler

insertion. But to ensure that this virtual_color is seen by all

placement commands (and API), use specify_cell_virtual_align.

The replacement command specify_cell_virtual_align, will ensure that

other placement command, such as checkPlace, refinePlace,

ecoPlace will also honor the virtual_color.

See Also:

.in +4

report_cell_virtual_align, delete_cell_virtual_align.

.in

IMPSP-6014

NAME

IMPSP-6014

SUMMARY

I/O pin '%s' does not connect to placed Area I/O instance or hard macro and will be ignored for bump assignment. Most likely reason is: 1. The Area I/O instance or hard macro is not placed. 2. I/O pin does not connect to I/O instance or hard macro in Verilog netlist. Fix these issues and re-run assignBump command again.

DESCRIPTION

assignBump command assigns the bumps closest to the I/O cells. For assigning I/O cells to bump, IO pads need to be with the Class type definition "PAD AREAIO"

Example:

MACRO iopad

CLASS PAD AREAIO ;

ORIGIN 0.000 0.000 ;

SIZE 35.000 BY 246.000 ;

SYMMETRY x y r90 ;

SITE pad ;

PIN PAD

PORT

CLASS BUMP

a?|a?|a?|a?|a?|

If the CLASS is not defined as "AREAIO" then tool will give WARN: (IMPSP-6014) warning message.

Users need to check the LEF file to make sure that CLASS type for that cell is specified as CLASS PAD AREAIO.

IMPSP-7207

NAME

IMPSP-7207

SUMMARY

Shifter '%s' has no connections outside its power domain.

DESCRIPTION

This message represents the detection of a level shifter or
isolation cell which is connected only to instances in the
same power domain (disregarding any enable nets).
The cell in question may have been improperly inserted
into the netlist, or may be a spare.
Use of the 'reportPowerDomain' command may be helpful
in analyzing the connectivity of this cell.
The level shifter placement algorithm will skip this cell
(i.e. not move it to the power domain boundary), and let it
be handled through normal processes.

IMPSP-7208

NAME

IMPSP-7208

SUMMARY

Term '%s' of %s '%s' is outside its power domain.

DESCRIPTION

This message represents the detection of a term that
is connected by a net to a level shifter or isolation cell,
but is physically outside the constraints of its expected
power domain.
This may be caused by a failure in floorplanning or an earlier
placement step, and analysis of the location of the reported
instance or block is recommended.

IMPSP-9025

NAME

IMPSP-9025

SUMMARY

No scan chain specified/traced.

DESCRIPTION

By default, scan chains are traced and reordered during place_opt_design and ccopt_design if it is specified by scan DEF or specifyScanChain command. If there is no scan chain specification, placer will skip this step and report the warning message.

IMPSP-9042

NAME

IMPSP-9042

SUMMARY

Scan chains were not defined, -place_global_ignore_scan option will be ignored. Define the scan chains before using this option.

DESCRIPTION

This warning occurs when setPlaceMode -place_global_ignore_scan true is set (default is true) but no scan chains are defined. Run getPlaceMode -place_global_ignore_scan to report its current setting. This option instructs placeDesign to disregard scan connections while running placement but it requires you to define scan chains first. Otherwise, the option is ignored. You can define scan chains by importing a scan DEF file using defIn or using the command specifyScanChain.

Example

The following command load scan specification from a DEF file:

defIn mySCAN.def

The following command sets scan chain test_si with a starting I/O pin name and a stopping pin name:

specifyScanChain test_si -start test23 -stop test_so

IMPSP-9053

NAME

IMPSP-9053

SUMMARY

Option -startRowNum assumes the frist row in design is '1', ignoring '%d'.

DESCRIPTION

Option -startRowNum of command addWellTap is used to specify the row number starting from the bottom or left side of the design on which the well-tap cells must be placed, which assumes the first row from the bottom as '1'. To avoid this message, the specified start row number must be equal or larger than '1'.
Example:

<CMD> addWellTap -cell FIIL1 -cellInterval 33 -startRowNum -1
**WARN: (IMPSP-9053): Option -startRowNum assumes frist row in design is '1', ignoring '-1'.

IMPSP-9514

NAME

IMPSP-9514

SUMMARY

Non-TimingDriven placement will be performed.

DESCRIPTION

Placement is being run without taking timing into account. Placement of instances on

timing critical paths may not be effiective.

Example:

To consider timing driven placmenet make sure constraints are loaded along with the following command:

.in +4

setPlaceMode -timingDriven true

.in

IMPSP-9516

NAME

IMPSP-9516

SUMMARY

-prePlaceOpt is disabled when -incremental option is on.

DESCRIPTION

placeDesign -incremental works on an already placed design and hence prePlaceOpt (buffer tree deleteion) is disabled.

Example:

To run Incremental placeDesign on an already placed data:

placeDesign -incremental

IMPSP-9528

NAME

IMPSP-9528

SUMMARY

Command '%s' is obsolete and will be removed in future release, use '%s' to replace it.

DESCRIPTION

The obsolete command still works in this release, but to avoid this warning and to ensure compatibility with future releases, please remove it from your script and use the recommended command to replace it.

Example:

<CMD> %s

**WARN: (IMPSYT-9528): Command '%s' is obsolete and will be removed in future release. The obsolete command still works in this release, but to avoid this warning and to ensure compatibility with future releases,

please remove the obsolete command from your script and use '%s' to replace it.

IMPSP-9542

NAME

IMPSP-9542

SUMMARY

check_design found some critical issues with the design. Please fix error(s) identified before re-running place_opt_design.

DESCRIPTION

Review report generated by check_design and fix the different errors before restarting place_opt_design.

IMPSP-15450

NAME

IMPSP-15450

SUMMARY

Cannot recognize this line correctly : %s

DESCRIPTION

Input row_num should be greater than 0, and less than the row height of the cell.

The summation of left and right cpp should be less than or equal to the width of the cell.

IMPSR-211

NAME

IMPSR-211

SUMMARY

Cannot find a bump named '%s' in Innovus DB.

DESCRIPTION

The macro of bump instance is 'CLASS COVER BUMP', but the 'Object Type' of bump instance is not 'Bump Cell'. Or attempting to optimize non-bump's assignment by "placePIO -assignBump",

such as TSV, pad, ...

IMPSR-212

NAME

IMPSR-212

SUMMARY

The bump shape is irregular, and not supported by global route. The bounding box of the bump is used in global route.

DESCRIPTION

Global route only supports rectangle or octangle bumps without merging. And for octangle bumps, the internal angles must be 135 degree and the edges must be vertical, horizontal or diagonal. Otherwise, bounding boxes are used in global route to represent the bumps.

IMPSR-215

NAME

IMPSR-215

SUMMARY

The value of maximum resistance for diff pair nets %s and %s is not proper. The two nets is routed with fixed routing width.

DESCRIPTION

Fcroute supports resistance driven diff pair routing in PIO mode. The value of maximum resistance for either net in one diff pair should be the same. Check the setting MAXRES for the diff pair nets in constraint file.

IMPSR-216

NAME

IMPSR-216

SUMMARY

The width range for diff pair nets %s and %s is not proper. The two nets is routed with fixed routing width.

DESCRIPTION

Fcroute supports resistance driven diff pair routing in PIO mode. The width range for either net in one diff pair should be the same. Check the setting WIDTHRANGE for the diff pair nets in constraint file.

IMPSR-217

NAME

IMPSR-217

SUMMARY

The net group %s cannot be found in the design. The tool will ignore it.

DESCRIPTION

Fcroute cannot find the net group specified by the keyword BUSGUIDE in the constraint file. Check the parameter of BUSGRUIDE for bus routing in constraint file, or create this net group by command createNetGroup.

IMPSR-218

NAME

IMPSR-218

SUMMARY

The nets in the net group %s are different between fcroute constraint file and createNetGroup. The tool will ignore net group %s.

DESCRIPTION

All the nets in the net group define by fcroute constraint file should be in the net list defined by createNetGroup and vice versa. Check the setting BUMP/SHIELDNET for bus routing in constraint file, or set srouteCheckNetinNetGroup to false to disable this check in extra configure file.

IMPSR-219

NAME

IMPSR-219

SUMMARY

Fcroute cannot find bus guide segments for the net group %s in the design. The tool will ignore net group %s.

DESCRIPTION

Fcroute cannot find any bus guide for net group. Check the setting BUSGUIDE for bus routing in constraint file, or create proper bus guide for the net group.

IMPSR-221

NAME

IMPSR-221

SUMMARY

Fcroute cannot get the end points of bus guides for net group %s. The tool will ignore net group %s.

DESCRIPTION

Fcroute fails to get the end points of bus guides. Normally this happens when the connected bus guids are ended by 45 degree bus guide, which is not supported. Try to add one orthogonal bus guide to the end point of the 45 degree bus guide.

IMPSR-222

NAME

IMPSR-222

SUMMARY

Fcroute cannot get two proper end points of bus guides for net group %s. The tool will ignore net group %s.

DESCRIPTION

Fcroute fails to get two proper end points of bus guides. Normally this happens when the connection styles of bus guides is too complex. Try to avoid T connection, and make sure that the connection between two bus guides are point-to-point connection, and the bus guides are ended on othogonal bus guides for two ends.

IMPSR-223

NAME

IMPSR-223

SUMMARY

Bus guides are touching the boundary box of bumps/pads in net group %s. The tool will ignore net group %s.

DESCRIPTION

Bus guides are touching the boundary box of bumps/pads in net group. Try to move the bus guides out of the boundary box of bumps/pads.

IMPSR-344

NAME

IMPSR-344

SUMMARY

The locations of bumps/pads in diff pair (%s %s) are too twisted for fcroute. The two nets are routed as normal nets.

DESCRIPTION

The connection line of two bump centers is crossing with that of two pad centers.

IMPSR-345

NAME

IMPSR-345

SUMMARY

The number of bumps/nets in net group %s is less than 3. The tool will ignore net group %s.

DESCRIPTION

The bumps/nets in one net group should be no less than 3. Try differential pair routing for two nets. And one net cannot form a net group.

IMPSR-346

NAME

IMPSR-346

SUMMARY

Cannot find bump %s specified in net group %s. The tool will ignore net group %s.

DESCRIPTION

Fcroute cannot find the bump with the bump name in constraint file. Confirm the bump to be routed in net group.

IMPSR-347

NAME

IMPSR-347

SUMMARY

Cannot find shield net %s specified in net group %s. The tool will ignore net group %s.

DESCRIPTION

Fcroute cannot find the shield net with the net name in constraint file. Confirm the shield net name in net group.

IMPSR-348

NAME

IMPSR-348

SUMMARY

Bump %s in net group %s belongs to a multi-term net. The tool will ignore net group %s.

DESCRIPTION

Fcroute cannot get the target pad for bump in multi-term net for bus routing. Try to use pair constraint, or bump property to specify the target pad for this bump.

IMPSR-349

NAME

IMPSR-349

SUMMARY

In net group %s, Bump %s is not selected to route. The tool will ignore net group %s.

DESCRIPTION

The bump is skipped in fcroute. If using with option '-selected_bump', check if the bump is in the list of the specified bumps. If using with option '-nets', check if the net of the bump is in the list of the specified nets.

IMPSR-794

NAME

IMPSR-794

SUMMARY

On bump '%s', IO port in '%s' is not found or suitable for routing to net '%s'. Check the bump property to correct it.

DESCRIPTION

The IO port is too small or narrow, blocked by obstruction, or has already been routed, or the port number does not exist, or there are typos on the bump property.

IMPSR-1256

NAME

IMPSR-1256

SUMMARY

Cannot find any CORE class pad pin of net %s. Change routing area or layer to include the expected pin, or check netlist, or change port class in the technology file.

DESCRIPTION

This message is reported when routing pad pins. Pad pins are power pins on the pad which should connect to the core power grid or ring. By default, sroute considers all power pins on the pads to connect to the power pad ring and not the core unless the pin's PORT definition is specified with CLASS CORE in the technology file. A power pin of a pad which is to drive the core power grid should be defined.

IMPSR-1972

NAME

IMPSR-1972

SUMMARY

***[%.3f %.3f] in '%s': Can't be routed because '%s' is blocked by cell or routing blockages (obstructions) preventing from routing.

DESCRIPTION

This message indicates the pin is blocked by cell or routing blockages (obstructions) preventing fcroute from routing to them.

Zoom to the pin and observe what blockages are at the same layer as the pin or above.

The blockages need to be removed from around and on top of the pin so fcroute can access it without creating a violation.

If the pin is blocked by a routing blockage, edit the blockage so the pin can be accessed.

If it is a cell blockage, you will need to update the LEF file or OA abstract view so the obstruction does not block the pin.

IMPSR-1974

NAME

IMPSR-1974

SUMMARY

%d port%s blocked by cell or routing blockages in M%d-M%d layer. Check the design if cell or routing blockages need be removed.

DESCRIPTION

This message indicates the pin is blocked by cell or routing blockages (obstructions) preventing fcroute from routing to them.

Zoom to the pin and observe what blockages are at the same layer as the pin or above.

The blockages need to be removed from around and on top of the pin so fcroute can access it without creating a violation.

If the pin is blocked by a routing blockage, edit the blockage so the pin can be accessed.

If it is a cell blockage, you will need to update the LEF file or OA abstract view so the obstruction does not block the pin.

IMPSR-2457

NAME

IMPSR-2457

SUMMARY

There is overlap of RANGE rules for SPACING on layer %s, spacing %.3f for [%.3f %.3f] and spacing %.3f for [%.3f %.3f]. The range values should not overlap. The router will use spacing %.3f for routing width no less than %.3f.

DESCRIPTION

The range values should not overlap if you specify multiple RANGE rules for SPACING.

IMPSR-2459

NAME

IMPSR-2459

SUMMARY

The geometry on layer %s in bump cell %s is too complicated for fcroute. The tool will try to replace the geometries with its circumscribed octagon.

DESCRIPTION

This may happen when there are too many complex geometries in bump pin. The circumscribed octagon can help fcroute to improve routability, but may cause design rule violations around bump in final routing result. User can manually set 'setFlipChipMode -bump_use_oct_shape false' to use the original geometries.

IMPSR-2617

NAME

IMPSR-2617

SUMMARY

The spacing value %s in line %d is smaller than allowed MINSPACING in layer %s in the technology file.

DESCRIPTION

When the spacing value in fcroute constraint file is smaller than allowed MINSPACING in that layer in the technology file, MINSPACING will be used.

IMPSR-4006

NAME

IMPSR-4006

SUMMARY

Failed to open extra config file %s to read.

DESCRIPTION

The message occurs because there is no reading permission or the file does not exist.

IMPSYC-2

NAME

IMPSYC-2

SUMMARY

Timing information is not defined for cell %s; Check the timing library (.lib) file and make sure the timing information exists for the cell and you can run the %s command to verify if the timing library

has complete information after the design is loaded.

DESCRIPTION

This is due to the timing information for cell %s is missing.

This warning could be shown even when the cell is physical cell

IMPSYC-179

NAME

IMPSYC-179

SUMMARY

The %s name '%s' is not a legal verilog identifier. If the identifier has special characters, use escaped format which start with backslash '\' and end with one space character ' '.

DESCRIPTION

This ERROR comes up with any command where instance/net name has special characters in it. Commands like addPowerSwitch, attachDiode.

1. Special character in the instance name :

attachDiode -diodeCell ANTENNA -pin xyz_F_1_o_reg[0] D

needs to be changed to

attachDiode -diodeCell ANTENNA -pin {xyz_F_1_o_reg\[2\] } D

2. Special character in the pin name :

attachDiode -diodeCell ANTENNA -pin hier.sub1/instance_1 D[2]

needs to be changed to

attachDiode -diodeCell ANTENNA -pin hier.sub1/instance_1 {D[2]}

IMPSYC-194

NAME

IMPSYC-194

SUMMARY

Incorrect usage for command '%s'.

DESCRIPTION

IMPSYC-194 is a common and generic error message for any command and may have numerous specific causes if the command has been incorrectly used. Check the man page of the command being reported in this error to know the correct usage of it.

IMPSYC-959

NAME

IMPSYC-959

SUMMARY

Inst '%s' in module '%s' has tie-high/low output pin '%s'. This can create a short circuit if the pin is not the driver of the power/ground net to be tied to, and the pin's output polarity is different from that of the power/ground net. Check the connectivity in the netlist.

DESCRIPTION

This error indicates that a OUTPUT/INOUT pin is tied high/low i.e. pin is driving the power network which might result in a short.

Check :

-> If the pin is defined with USE POWER or USE GROUND in the LEF which means the pin is PG

pin and its connectivity should not be defined in Verilog. The globalNetConnect command connects PG pins to the specified global net, which is either a power or ground net.

-> If the pin is a signal pin, properly define its DIRECTION in the LEF.

-> To avoid this error, You can set the following prior to init_design:

setCheckMode -vcelnetlist false

Note: Make sure that the sign-off LVS is run in your flow to verify the final power connections are correct.

IMPSYC-1636

NAME

IMPSYC-1636

SUMMARY

No library found for level shifter cell '%s' with input '%f' and output '%f' volts, placed in power domain '%s'. The first available library cell of the same name will be used, irrespective of input and output voltages.

DESCRIPTION

Why is this message issued during timing analysis?

Following are excerpts from the library showing a level shifter and associated

pins and their voltage. If a level shifter with the appropriate voltages is not

found the error above will be issued.

At the top of the file the voltage levels are defined using voltage_map

statements:

voltage_map (VDD, 1.08);

voltage_map (ExtVDD, 0.9);

voltage_map (VSS, 0);

voltage_map (GND, 0);

voltage_map (ExtVSS, 0);

Example:

Within the cell definition define power pins and respective voltage names

within a pg_pin statement:

cell (LSHLX1_FROM) {

is_level_shifter : "true";

level_shifter_type : "HL";

area : 0;

pg_pin (VSS) {

pg_type : primary_ground;

voltage_name : "VSS";

}

pg_pin (VDD) {

pg_type : primary_power;

std_cell_main_rail : true;

voltage_name : "VDD";

}

pg_pin (ExtVDD) {

pg_type : backup_power;

voltage_name : "ExtVDD";

}

Lastly, define the signal_level and related power and ground pins for the input

and output pins:

pin (Y) {

output_signal_level : ExtVDD;

direction : output;

function : "A";

related_ground_pin : VSS;

related_power_pin : ExtVDD;

pin (A) {

input_signal_level : VDD;

direction : input;

related_ground_pin : VSS;

related_power_pin : VDD;

IMPSYC-1816

NAME

IMPSYC-1816

SUMMARY

The connectivity of the net '%s' in saved routing file" "mismatches with the connectivity of the same net in memory.

DESCRIPTION

While running restoreRoute or restoreDesign, the above message is issued when the connectivity of a net recorded in the routing file of the EDI System database (*.route or *.route.gz file) does not match the connectivity of the net in memory (usually read from the Verilog during init_design or restoreDesign). Make sure the routing file correlates to the database in memory. If it does, try running the latest software release of EDI as this may be due to a software issue. If the error still is reported, please open a Case through http://support.cadence.com.

Overall, make sure you did not make any changes to the Verilog which are not reflected in the other database files. If you need to modify the Verilog file, you should then run one of the ECO Flows described in the EDI System User Guide.

IMPSYC-1919

NAME

IMPSYC-1919

SUMMARY

The connectivity mismatches to the routing data." "The wire at (%d %d) on net '%s' is associated to" "the instance pin '%s:%s'" "which is on a different net '%s'.

DESCRIPTION

This is a data integrity error. Review all previous steps to see how this is triggered and report it to Cadence.

IMPSYC-1921

NAME

IMPSYC-1921

SUMMARY

The connectivity mismatches to the routing data." "The wire at (%d %d) on net '%s' is associated to" "the IO pin '%s'" "which is on a different net '%s'.

DESCRIPTION

This is a data integrity error. Review all previous steps to see how this is triggered and report it to Cadence.

IMPSYC-1922

NAME

IMPSYC-1922

SUMMARY

The connectivity mismatches to the routing data." "The wire at (%d %d) on net '%s' is associated to" "the instance pin '%s:%s'" "which is not connected to any net.

DESCRIPTION

This is a data integrity error. Review all previous steps to see how this is triggered and report it to Cadence.

IMPSYC-1923

NAME

IMPSYC-1923

SUMMARY

The connectivity mismatches to the routing data." "The wire at (%d %d) on net '%s' is associated to" "the IO pin '%s'" "which is not connected to any net.

DESCRIPTION

This is a data integrity error. Review all previous steps to see how this is triggered and report it to Cadence.

IMPSYC-2100

NAME

IMPSYC-2100

SUMMARY

Instance %s added but could not find spare cell for it.

DESCRIPTION

Possible reasons for not finding a spare cell are:

1. Either the spare instance or the unplaced instance or both have region/fence placement constraints and no spare instance could be found that does not cause a constraint violation. To fix - remove the placement constraints on the spare instances or add new spare instances into the same region/fence hierarchy as the unplaced instances.

2. Spare instance having the same cell type as the unplaced instance is not available. Check if specifySpareGate command has been used to specify the spare instances. createSpareModule/placeSpareModule, addSpareInstance are some of the commands that could also be used to insert spare instances in the design.

3. ecoRemap and ecoSwapSpareCell commands could be used to map any remaining unplaced instances after ecoPlace -useSpareCells to spare instances of different cell types.

IMPSYC-3161

NAME

IMPSYC-3161

SUMMARY

Ignoring the -syncRelativePath setting in the configuration file. The -syncRelativePath parameter of the set_import_mode command is set to true in ETS by default. All relative paths in the configuration file will be synchronized to the current working directory. To avoid this warning, remove the syncRelativePath setting from the configuration file.

DESCRIPTION

{This warning is displayed because the ETS software ignores the -syncRelativePath setting in the configuration file and uses the default value (true) for the -syncRelativePath parameter of the set_import_mode command. When the -syncRelativePath parameter of the set_import_mode command is set to true, all the relative paths in the configuration file are synchronized to the current working directory. As a result, the configuration file can be loaded from any directory without changing the current working directory to the directory in which the configuration file was saved. You can use the set_import_mode -syncRelativePath false command in ETS if you do not want to synchronize the relative paths in the configuration file to the current working directory. Use this command after invoking ETS and before reading the design. To avoid this warning, remove the -syncRelativePath setting in the configuration file.}

IMPSYC-3166

NAME

IMPSYC-3166

SUMMARY

The use of '%s' with '%s' is not supported.

DESCRIPTION

At most only one of these can be used at a given time; correct your configuration.

IMPSYC-6114

NAME

IMPSYC-6114

SUMMARY

Could not add padding to given cell <%s>.

DESCRIPTION

Cell padding can only be added to standard cells of the library. Padding on hierarchical module, macro block, io pads, etc. is not supported.

IMPSYC-6152

NAME

IMPSYC-6152

SUMMARY

Net %s is marked as unrouteable by NanoRoute." "There may be an internal error or issue with the input data that triggers" "this net to be set as open. Please check the net objects for issues.

DESCRIPTION

If the pre route data contains issues, partial routes with FIXED vias, routes or other issues that will cause routing problems, NanoRoute sets the Nets attribute to skip the net and routes the other nets in the design. If the pre route is custom and complete the message can be ignored. If the preroute needs to be completed by NanoRoute the FIXED segments and vias may need to be converted to routed status. If you need the partial preroutes to be locked the preroutes may need to be converted to special nets for completion by the router.

Example:

convertNetToSNet $net1

setAttribute -net $net1 skip_routing false
setNanoRouteMode -routeWithEco true
ecoRoute

IMPSYC-6164

NAME

IMPSYC-6164

SUMMARY

Invalid padding value 0 is given, please correct usage with integer greater than 0.

DESCRIPTION

To clear the specified padding for a cell or list of cells, please use command deleteCellPad.

IMPSYC-6375

NAME

IMPSYC-6375

SUMMARY

Can't read hier pg file '%s' because hier pg feature is not on. To turn on hier pg feature please set

the variable 'upf_hier_pg_port_support'.

DESCRIPTION

If the variable is already set in your script file, but you still get this message, please check the file root.init in your design hierarchy, may be the variable got set in this file.

IMPSYC-6376

NAME

IMPSYC-6376

SUMMARY

Can't save hier pg file '%s' because hier pg feature is not on. To turn on hier pg feature please set the variable 'upf_hier_pg_port_support'.

DESCRIPTION

If the variable is already set in your script file, but you still get this message, please check the file root.init in your design hierarchy, may be the variable got set in this file.

IMPSYT-6260

NAME

IMPSYT-6260

SUMMARY

An error occurred while loading file %s/%s.globals. Review the messages above for reasons why loading the file failed. This often occurs when global variables have become obsolete. These variables will be ignored and the rest of the file will still be processed. To avoid this error remove these obsolete variables from the file.

DESCRIPTION

{This error will show if there is any error in the .globals file. It normally associates with GLOBAL errors.}

IMPSYT-6284

NAME

IMPSYT-6284

SUMMARY

Failed to open file %s for read.

DESCRIPTION

{This message is issued when the software is not able to open a file for read. This might happen due to file access permissions, or a transient NFS fault, or due to the file being accidentally deleted or corrupted.}

IMPSYT-7221

NAME

IMPSYT-7221

SUMMARY

restoreDesign failed: %s.globals file not found in '%s/%s/%s'.

DESCRIPTION

{If the cellview is a derivative of the one created by saveDesign -cellview,then use copyOaRestoreFiles to update the cellview from an earlier version. If the cellview was created by

another method use File->Import Design or set the init_ design variables (find_global init_*) as needed and then invoke the init_design command.}

IMPSYT-16038

NAME

IMPSYT-16038

SUMMARY

The specified file '%s' could not be found. Check your file system, correct the file name.

DESCRIPTION

This error occurs when a missing file is encountered during design parsing.

The tool cannot find a file if:

1. The file path name is incorrect.

2. A variable which is used in the path name is not correctly specified.

3. The read permission to the file path is disabled.

IMPSYT-40503

NAME

IMPSYT-40503

SUMMARY

Support for the loadConfig command and the configuration file based design import methodology for designs which are not configured as multi-mode/multi-corner (MMMC) has been discontinued in this release.

DESCRIPTION

This flow is replaced by the init_design based design import flow.

To import your design database to an 11.1 MMMC configuration,

you should perform a saveDesign using a 10.1 version of the software,

and then perform a restoreDesign using version 11.1 of the software.

You should refer to the 'Importing Designs Saved in Previous Versions'

section in the 'Importing and Exporting Designs' chapter in the EDI11

user guide for more detailed information.

IMPSYUTIL-96

NAME

IMPSYUTIL-96

SUMMARY

Cannot open (for %s) %s file: '%s'. The reason is: %s

DESCRIPTION

This error is reported when assembling a design because the topDir database does not contain a DEF file. For option -topDir specifies the path to the top-level design created by saveDesign -def. This design directory should contain the Verilog netlist and DEF files.

Load the top design and do a defOut to save the DEF or run for the top level so that topDir contains the DEF.

IMPSYUTIL-106

NAME

IMPSYUTIL-106

SUMMARY

Cannot allocate %ld bytes.

DESCRIPTION

Failed in memory allocation. It is likely that the machine run out of virtual memory.

IMPTB-2

NAME

IMPTB-2

SUMMARY

Cannot complete command %s, not able to open %s for write, provide a file path which can be opened for write to complete execution.

DESCRIPTION

The possible reasons you have this message might be:

1. You may not have necessary file operation permissions to create a file on current working directory.

2. There is a same-name file which you do not have write permission on it.

3. You may have run out of disk space.

Example:

Check whether you have permission to create a file on current working directory:

innovus 7> file writable [pwd]

1

Check whether you have a same-name file which you do not have write permission on it on current working directory:

set fileName innovus.log1

```
if {[file exists $fileName]} {
puts [file writable $fileName]
} else {
puts 0
}
```

Check if you have run out of disk space:

```
innovus 16> df -kH [pwd]
Filesystem Size Used Avail Use% Mounted on
/dir/subdirectory1/case/case11189 2.2T 2.0T 271G 88% /dir/subdirectory1/case/case11189
```

IMPTB-36

NAME

IMPTB-36

SUMMARY

Partition name %s does not match a hierarchical instance or a black box and will be ignored.

DESCRIPTION

The specified name does not match an uncommitted partition (hierarchical instance with a fence) or a black box (floorplan block object).

Example:

```
deriveTimingBudget -ptn ptnA
```

Warning: Partition name ptnA does not match a hierarchical instance or a black box and will be ignored.

IMPTB-178

NAME

IMPTB-178

SUMMARY

Command setFixedBudget cannot accept option "-fromFlopsOf" and "-toFlopsOf" together.

DESCRIPTION

setFixedBudget command can only be applied on a path segment. Please use it with pins at either "-from" or "-to" option.

IMPTB-521

NAME

IMPTB-521

SUMMARY

No SDC file found for analysis view %s. Make sure analysis views are properly constrained prior to running deriveTimingBudget.

DESCRIPTION

Check if viewDefinition file has correct SDC files (not a physical only flow or absent timing constraints).

IMPTB-522

NAME

IMPTB-522

SUMMARY

Partition %s's ports %s and %s are connected through verilog assign. Budgeting requires a physical pin inside partition in order to budget timing path inside partition.

DESCRIPTION

Verilog assign statements can be removed using 'remove_assigns -buffering' command before running deriveTimingBudget.

IMPTCM-42

NAME

IMPTCM-42

SUMMARY

"%s" is not a legal option for command "%s". Check the option whether is an existed option through command -help.

DESCRIPTION

This error is displayed when a command is entered with incorrect switch which is not supported by the command.

The message will also display the command and a list of switches which are legal to use for the command.

Review and use the command with the appropriate legal switch.

IMPTR-1107

NAME

IMPTR-1107

SUMMARY

Cannot find net %s, which is shown in the routing guide.

DESCRIPTION

When user set up trial route guides for certain nets by using "setTrialRouteMode -routeGuide <filename>", if a net or nets in the guide can not be found in the design, the warning message will be issued.

Related command is saveRouteGuide.

Example:

For example, in the netGuide.file below, the net "xyz" is defined but does not exist,

routeGuideNet xyz

wire 413.49 27.72 413.49 17.64 V 0.5 L 4

wire 413.49 17.64 413.49 12.04 V 0.5 L 4

wire 413.49 17.64 420.75 17.64 H 0.5 L 3

endRouteGuideNet

trialRoute will issue the warning message.

IMPTR-1109

NAME

IMPTR-1109

SUMMARY

Guide wires for net %s at line %d will be ignored because the net is prerouted/ignored.

DESCRIPTION

When route guides are used for certain nets and these nets are already prerouted, or they are to be ignored ("setAttribute -skip_routing true"), this WARN message will appear during trialRoute if "setTrialRouteMode -routeGuide <filename>" has these nets defined.

Example:

The clock net cclk is prerouted and this net is in route guide file as below,

routeGuideNet cclk__L1_N1

wire 324.39 243.88 324.39 274.68 V 0.5 L 4

wire 324.39 243.88 348.81 243.88 H 0.5 L 3

wire 324.39 274.68 324.39 279.72 V 0.5 L 4

wire 324.39 279.72 288.75 279.72 H 0.5 L 3

wire 348.81 243.88 350.79 243.88 H 0.5 L 1

wire 288.75 279.72 288.09 279.72 H 0.5 L 1

endRouteGuideNet

The message would be issued as,

**WARN: (INNTR-1109): Guide wires for net cclk__L1_N1 at line #% will be ignored because the net is prerouted or ignored.

IMPTR-2108

NAME

IMPTR-2108

SUMMARY

For layer M%d, the gaps of %d out of %d tracks are narrower than %0.3fum (space %0.3f + width %0.3f).

DESCRIPTION

The message occurs when gaps of track(s) of a layer are narrower than minimum allowed value (space + width) from the default routing rule. Those tracks might be initialized by a technology LEF which has values smaller than current one. Please make sure you have loaded the correct technology LEF or regenerate tracks to avoid this message.

Example:

The following commands generate new routing tracks:

\tinnovus> generateTracks

The following command generates tracks with a horizontal offset of 0.13, a horizontal pitch of 0.26, a vertical off set of 0.14, and a vertical pitch of 0.28 on layer m2:

\tinnovus> generateTracks -m2HOffset 0.13 m2HPitch 0.26 m2VOffset 0.14 -m2VPitch 0.28

IMPTR-2322

NAME

IMPTR-2322

SUMMARY

There are %d unplaced instances that will not be routed. Place all instances in the design before routing. TrialRoute will continue.

DESCRIPTION

This message pops-up while running &'trialRoute&' command if the design has any un-placed instances. The design will still be routed issuing this warning message.

Example:

In order to fix this warning message user needs to check if there are any unplaced instances in the design prior to running trialRoute command. The unplaced instances can be reported by running &'checkPlace checkPlace.rpt&' and verifying checkPlace.rpt file to find out unplaced instances and fixing this issue.

IMPTR-2325

NAME

IMPTR-2325

SUMMARY

There are %d nets connecting a pad term to a fterm without geometry and these nets will not be routed. A pad term is a pin of a pad logically connected to a top level module port (fterm). Type 'set trPrintIgnoredPadNets <limit>' prior to trialRoute to have it report each net up to <limit>. Review the list of nets and verify they do not require a physical route between the pad pin and fterm. Top level fterms connecting to pad pins typically do not require a physical route because the pad pin will connect to signals external to the design.

DESCRIPTION

This is referring to the top level ports that connect to the PAD pin of the IO pad. Since these signals

connect outside of the chip there is no port geometry to route to. For IO pins directly connected to IO pads, Innovus System implicitly considers the pin of the IO pad as an IO pin. Typically, you can ignore this warning.

Use &'set trPrintIgnoredPadNets <limit>&' prior to trialRoute to report each net up to <limit>.

Review the list of nets and verify they do not require a physical route between the pad pin and fterm. Top level fterms connecting to pad pins typically do not require a physical route because the pad pin will connect to signals external to the design.

Example:

You can set the following to have the warning list the nets it is ignoring:

\tset trPrintIgnoredPadNets 100

It will print up to 100 nets as:

PAD NET <net> is ignored.

Note:

The ignored net info can only be seen in innovus.logv file and not in the innovus.log file.

IMPTR-7111

NAME

IMPTR-7111

SUMMARY

There is no track for routing layer %s. Since the layer is not used, trialRoute will continue.

DESCRIPTION

This message pops-up in the design if the user tries to run trialRoute using &'setTrialRouteMode -useM1 true&' and there are no M1 tracks available to route.

Example:

In order to fix this issue user needs to define M1 tracks and then run trialRoute using

&'setTrialRouteMode -useM1 true&'.

IMPTR-7122

NAME

IMPTR-7122

SUMMARY

There is no selected net in file "%s" and trialRoute will continue.

DESCRIPTION

This message will pop-up when the user tries to set a file for &'setTrialRouteMode -selNet <fileName>&' option and there are no nets specified in the mentioned file.

Example:

In order to avoid this warning message the user needs to specify the nets he wanted to route one on each line in a file. This file can be inputted using &'setTrialRouteMode -selNetOnly <fileName>&' and then he can run &'trialRoute&' command to route specific nets.

IMPTR-8007

NAME

IMPTR-8007

SUMMARY

The "-useNanoRoute" option cannot be used for this design as it contains %s, and is therefore disabled. Regular trialRoute will be invoked.

DESCRIPTION

This message pops-up when the user tries to run trialRoute using NR global Route flow and the design contains partition and/or BB.

Example:

In order to avoid this warning message if the design has partition and/or BB NR global Route flow cannot be used. user needs to turn-off

"-useNanoRoute false" before invoking &'trialRoute&' command.

IMPTR-8015

NAME

IMPTR-8015

SUMMARY

trialRoute does not currently support option "%s" in this mode. Please set "-useNanoRoute false" if you require this option.

DESCRIPTION

This message pops-up when the user runs trialRoute in NRGR flow by using &'-skipTracks&' option in setTrialRouteMode. This is an info to user saying &'skipTracks&' option is not supported in NRGR flow. .

IMPTS-16

NAME

IMPTS-16

SUMMARY

Inconsistency detected in the time units specified among the timing libraries being used. Default system time unit of 1ns will be used. Use the '%s' command to set a specific time unit.

DESCRIPTION

This error is flagged during timing analysis when timing libraries with different time units are read into the software.

All timing library data is interpreted according to the native units of each individual library. When the library units differ across different libraries, this message is issued and all the time units are interpreted and reported with the default time unit.

However, you can use the '%s' command to set a specific time unit for the system. The system time unit will be used for reporting as well interpreting the constraints, which are either sourced from SDC files or entered interactively.

IMPTS-17

NAME

IMPTS-17

SUMMARY

Inconsistency detected in the capacitance units specified among the timing libraries being used. Default system capacitance unit of 1pF will be used. Use the '%s' command to set a specific capacitance unit.

DESCRIPTION

This error is flagged during timing analysis when timing libraries with different capacitance units are read into the software.

All timing library data is interpreted according to the native units of each individual library. When the library units differ across different libraries, this message is issued and all the capacitance units are interpreted and reported with the default capacitance unit.

However, you can use the '%s' command to set a specific capacitance unit for the system. The system capacitance unit will be for reporting as well as interpreting constraints, which are either sourced from SDC files or entered interactively.

IMPTS-282

NAME

IMPTS-282

SUMMARY

Cell '%s' is not a level shifter cell but has 'input_signal_level' and 'output_signal_level' specified on pins, or it has different related_power_pin specified on input and output pins. To mark this cell as level shifter, use 'is_level_shifter' attribute.

DESCRIPTION

This cell either has different related_power_pin defined for input and output pins, as per new liberty syntax, or it has 'input_signal_level' and 'output_signal_level' specified on pins, as per old liberty format. This can be specified for level_shifter_cells only. For a level shifter cell 'is_level_shifter' attribute is required.

IMPTS-302

NAME

IMPTS-302

SUMMARY

Min timing libraries are not specified, while max timing libraries are specified in configuration file. This may cause issues in hold analysis. Use rda_Input(ui_timelib) instead of rda_Input(ui_timelib,max) for timing library specification, or use setTimingLibrary command to set min timing libraries. By default max timing libraries will be used for hold analysis.

DESCRIPTION

For a non-MMMC setup it is mandatory to provide both min and max libraries. During timing analysis the max libraries are used during setup/late analysis and min libraries are used during early/hold analysis. When the min libraries are missing, the software will only use the max libraries for early/hold analysis, this may cause inaccurate timing results. It is, therefore, recommended that you provide both max and min libraries in the configuration file.

IMPTS-313

NAME

IMPTS-313

SUMMARY

Cell '%s' is missing in current active analysis view. No library found in MMMC library set corresponding to the cell. This can cause problem during optimization flow. The cell will therefore be marked as 'dont_use' during optimization.

DESCRIPTION

This message is issued when the cell is not defined for current active analysis view. Library is not present in library set corresponding to this cell for the active analysis view. This can cause problem during optimization flow. The cell will therefore be marked as 'dont_use' during optimization.

IMPTS-403

NAME

IMPTS-403

SUMMARY

Delay calculation was forced to extrapolate table data outside of the characterized range. In some cases, extrapolation can reduce the accuracy of the delay calculation. You can enable more detailed reporting of these cases by enabling the command 'setDelayCalMode -reportOutBound true'.

DESCRIPTION

This warning message is issued during Delay Calculation when the input transition or output load are falling beyond the library specified delay/slew table. This causes extrapolation of table values and may result in inaccurate reported values from Delay Calculation. It is recommended that you provide libraries for which the input transition/output capacitance of the design are within the library table boundaries. You can obtain a detailed report of outside range table boundaries by using the 'setDelayCalMode -reportOutBound true' command.

IMPTS-414

NAME

IMPTS-414

SUMMARY

There is mismatch in pin direction for the pin '%s' of cell '%s' specified in LEF or Verilog, and the timing library. The timing library value will be used.

DESCRIPTION

This message is issued when there is mismatch in the pin direction defined for cell between LEF/verilog and timing library. The timing library value will be used.

IMPTS-415

NAME

IMPTS-415

SUMMARY

Cell '%s' is not defined in all timing analysis view. This cell should be defined in all analysis views. Check the library binding of instances in active views using the command 'check_instance_library_in_views'.

DESCRIPTION

This message is issued when the cell is not present in all timing analysis view. Check the library binding of instances in active views using the command 'check_instance_library_in_views'.

IMPTS-423

NAME

IMPTS-423

SUMMARY

No library found for instance '%s', cell '%s', in powerdomain '%s', of view '%s'

DESCRIPTION

This message is issued when the library is missing for an instance in a power domain for an analysis view.

IMPTS-429

NAME

IMPTS-429

SUMMARY

The library specified at path '%s' with set_instance_library command is not loaded in the session. This command is ignored. Use 'update_library_set' command to add this library to any active library set and re-issue set_instance_library command.

DESCRIPTION

The library specified with command 'set_instance_library' must be an active library loaded in the session before this command is issued. Use 'update_library_set' command to add this library to any active library set and re-issue set_instance_library command.

IMPTS-451

NAME

IMPTS-451

SUMMARY

No matching library found in specified list for cell '%s' of instance '%s'. The set_instance_library command will be ignored for this instance.

DESCRIPTION

This message is issued when specified library list does not have any library containing the cell for an instance. In such cases, command is ignored only for the instance(s) for which library cells are not found.

IMPTS-452

NAME

IMPTS-452

SUMMARY

No matching instance/hinstance found for '%s'.

DESCRIPTION

This message is issued when instance or hinstance specified is not found in the design. In such cases, command is ignored only for invalid instance/hinstance.

IMPTS-455

NAME

IMPTS-455

SUMMARY

Design loading aborted due to library inconsistency. Refer to %s message(s) above for more details. Correct the library inconsistency and re-load.

DESCRIPTION

This message is issued when any library inconsistency(pin/cell mismatch across libraries) is found. In such cases design will be aborted.

IMPVAC-0

NAME

IMPVAC-0

SUMMARY

Skipping net %s as it has no defined frequency or a defined frequency of 0Hz. Check your design, or use verifyACLimitSetFreq/dbSetNetFrequency to specify the net frequency.

DESCRIPTION

Use 'verifyACLimitSetFreq -help' or 'dbSetNetFrequency -help' to get more usage for setting the net frequency.

IMPVAC-96

NAME

IMPVAC-96

SUMMARY

No EM rule is found in QRC tech file. Please check QRC tech file if it doesn't contain EM rule or incorrect layer stacking information.

DESCRIPTION

Use 'get_rc_corner <rc_corner_name> -qx_tech_file' to get the qrc tech file and check if it matches to the design.

IMPVAC-131

NAME

IMPVAC-131

SUMMARY

NET %s has no wire cap.

DESCRIPTION

Check if net %s is annotated in your parasitic file or if you had issues while reading such file.

You can run "report_annotated_parasitics -nets "..."" giving net's names to see if net is back-annotated.

Or run report_annotated_parasitics after reading parasitics file for a complete status report.

IMPVCM-7

NAME

IMPVCM-7

SUMMARY

Bad data in the QRC tech file or layer mapping file. Check your QRC tech setting.

DESCRIPTION

Use 'get_rc_corner <rc_corner_name> -qx_tech_file' to get the qrc tech file and check if it matches to the design.

IMPVFC-3

NAME

IMPVFC-3

SUMMARY

Verify Connectivity stopped: Number of errors exceeds the limit %d

DESCRIPTION

The defulat error number is 1000, please use "verifyConnectivity -error" to specify more error number.

For example, "verifyConnectivity -error 100000".

IMPVFC-16

NAME

IMPVFC-16

SUMMARY

%s is not attached to any terminal.

DESCRIPTION

The message is issued by VerifyConnectivity when a net is not connected to any terminal.

IMPVFC-92

NAME

IMPVFC-92

SUMMARY

Pieces of the net are not connected together

DESCRIPTION

This message is reported by verifyConnectivity when two metal pieces of a signal net wire segments are overlap each other and one among them is Floating Metal. This can be a valid scenario and the message to alert the user to cross check whether this is intended. If the user aware of the Floating Metal and would like to ignore such message/violation use following option. verifyConnectivity -noFloatingMetal

IMPVFC-93

NAME

IMPVFC-93

SUMMARY

Bump %s has not bump_conn_target property.

DESCRIPTION

This message is caused by that Bump %s doesn't have bump_conn_target property. If the bump is not assigned, first use assignBump to assign a net to this bump. If the bump is assigned, use addBumpConnectTargetConstraint to add the property to bump.

IMPVFC-200

NAME

IMPVFC-200

SUMMARY

Design must be in memory before running 'verifyPowerVia'. Use restoreDesign before call this command.

DESCRIPTION

The design has not been restored in memory before call 'verifyPowerVia', please use use 'restoreDesign' or 'init_design' to reatore the design in memory.

For example, use 'man restoreDesign' or man 'init_design' to get more information how to restore design in memory.

IMPVFC-250

NAME

IMPVFC-250

SUMMARY

Design must be in memory before running 'verifyWireGap'. Use resoreDesign before call this command.

DESCRIPTION

The design has not been restored in memory before call 'verifyWireGap', please use use 'resoreDesign' or 'init_design' to reatore the design in memory.

For example, use 'man resoreDesign' or man 'init_design' to get more information how to restore

design in memory.

IMPVFC-266

NAME

IMPVFC-266

SUMMARY

Design must be in memory before running 'verifyTieCell'. Use resoreDesign before call this command.

DESCRIPTION

The design has not been restored in memory before call 'verifyTieCell', please use use 'resoreDesign' or 'init_design' to reatore the design in memory.

For example, use 'man resoreDesign' or man 'init_design' to get more information how to restore design in memory.

IMPVFG-216

NAME

IMPVFG-216

SUMMARY

The invalid setting of setVerifyGeometryMode -layer will be ignored, since setVerifyGeometryMode -offSnapGrid option is false.

DESCRIPTION

The layer is only used for offGrid check. If you need limit the layer range for other check, please use

layerRange option. For example, verifyGeometry -layerRange {M1 M3}.

IMPVL-159

NAME

IMPVL-159

SUMMARY

Pin '%s' of cell '%s' is defined in LEF but not in the timing library.

DESCRIPTION

This message indicates, there are pins defined in the LEF abstract but not in the respective timing library files. In the example shown below, the pins that are missing in the timing library files are power/ground pins. This might cause Innovus not to recognize the buffer, inverter and delay cells properly.

**WARN: (IMPVL-159): Pin 'gnd' of cell 'BUFX2' is defined in LEF but not in the timing library.

IMPVL-209

NAME

IMPVL-209

SUMMARY

In Verilog file '%s', check line %d near the text %s for the issue: '%s'. Update the text accordingly.

DESCRIPTION

This message reports the location of the text causing a warning or error situation in the input netlist file, which is briefly described by the last argument text. Update the source text accordingly to

resolve the issue.

IMPVL-327

NAME

IMPVL-327

SUMMARY

Module %s has already been defined. Overwrite the previous one.

DESCRIPTION

The message occurs because EDI found a module conflicts with a same-name module which has been declared earlier. To resolve the conflict, EDI replace the old module definition with the new one. To avoid this message, please remove the duplicated module definition from your verilog netlist.

IMPVL-346

NAME

IMPVL-346

SUMMARY

Module '%s' is instantiated in the netlist, but is not defined in the LEF files. Since there is no real cell definition for such a cell, it will be treated as %s.

DESCRIPTION

The abstract view (LEF) for the macro was not defined but the instance is being instantiated in the netlist. This will cause the macro to be treated as black box or dummy cell.

To fix the problem, specify all the macro LEF files along with the timing .lib files through the init_lef_file list in the design.globals file and the library sets in the viewDefinition.tcl file respectively that are used in the netlist.

IMPVL-349

NAME

IMPVL-349

SUMMARY

In module '%s', for instance '%s' of '%s', implicit port connections (by position) are not allowed because module '%s' is not defined in the netlist. Either provide the module definition in the netlist, or use explicit port connections (by name) for the instance.

DESCRIPTION

A Verilog netlist is being read into EDI System, but it fails with the above message. This netlist can be read successfully by NC-Verilog but EDI System is rejecting it because it uses connection-by-position.

One workaround is to provide module stubs for whatever cells use connection by position. This Verilog stubs module is required in order to define the pin ordering for the module in case the implicit connections in the top level netlist are done.

IMPVL-356

NAME

IMPVL-356

SUMMARY

The macro cell '%s' is defined in LEF, but the pin '%s' used in the netlist is not defined in LEF. Check and correct the pin name or define the pin in LEF file.

DESCRIPTION

The message indicates that a pin is specified in a macro instantiation in the Verilog, but is not defined in the cell's LEF definition. The proper way to resolve this error is to correct the Verilog netlist or LEF so they are corresponding by checking for typos or inconsistencies in the name (lowercase vs. uppercase, different bus bit characters used, etc.)

If the netlist is in its early stages and still in development, and you just want to bypass these errors until the netlist matures, you can set the following hidden variables prior to loading the design:

set ::db::AllowSoftMatching 1

set ::db::AllowNewLefPorts 1

The AllowSoftMatching variable allows soft matching of ports. For example, it would match '\\A[0] ', a scalar, to A[0], a bus bit, and would match 'a' to 'A'. The AllowNewLefPort allows undefined ports in the instantiations of LEF-defined macros.

IMPVL-366

NAME

IMPVL-366

SUMMARY

The macro cell '%s' is LEF-defined, but the bus port '%s' used in the netlist is not defined in LEF. Check and correct the port name, or define the bus port in LEF file.

DESCRIPTION

This message indicates that the bus port is specified in a LEF macro instantiation in the Verilog, but is not defined in the cell's LEF definition. The proper way to resolve this error is to correct the Verilog netlist or LEF so they are corresponding by checking for typos or inconsistencies in the name (lowercase vs. uppercase, different bus bit characters used, etc.). If the netlist is in its early stages and still in development, and you just want to bypass these errors until the in development, and you just want to bypass these errors until the loading the design :

set ::db::AllowSoftMatching 1

set ::db::AllowNewLefPorts 1

The AllowSoftMatching variable allows soft matching of ports. For example, it would match "\\A[0] ", a scalar, to "A[0]", a bus bit, and would match "a" to "A".

The AllowNewLefPort variable allows undefined ports in the instantiations of LEF-defined macros.

IMPVL-377

NAME

IMPVL-377

SUMMARY

Matching port %s of instance %s in module %s to port %s of cell %s by case insensitivity. Check the input data files to ensure the correct case. Fix any case mismatches and re-run.

DESCRIPTION

The macro LEF has port is defined as scan_out[0] ... scan_out[29] which is not a bit blasted syntax. So there is the mismatch between Verilog and LEF.

Soft matching the bit-blasted scalars in the netlist is getting interpreted as the LEF-defined bus bits. That's why you are getting the bussed saveNetlistresult.

To retain the netlist bit-blasted scalars, you need to edit the LEF bus bits into bit-blasted scalars as below.

scan_out\\[0\\] .. scan_out\\[29\\]

IMPVL-503

NAME

IMPVL-503

SUMMARY

Logical pg nets are not connected to global pg nets.

DESCRIPTION

This message is issued when there are missing power and/or ground connections in the design. Please make sure that logical power/ground connections are properly defined using the globalNetConnect command.

IMPVL-520

NAME

IMPVL-520

SUMMARY

%s pin '%s' of instance '%s' is not connected to a power or ground net. Use globalNetConnect to connect it to a power or ground net. In a CPF-based flow, you can also use a create_global_connection command in the CPF to specify the connection.

DESCRIPTION

The warning indicates that a power or ground pin (identified by USE POWER or USE GROUND in the LEF) is not connected to a global power or ground net. In a CPF based flow make sure you have a create_global_connection command in the CPF to connect this instance pin to a global power/ground net. In a non-CPF based flow use globalNetConnect to specify the connection. Otherwise, this pin will be unconnected in the exported Verilog.

IMPVL-904

NAME

IMPVL-904

SUMMARY

Can't set top cell to "%s" because it does not exist. Exiting!

DESCRIPTION

This message is triggered when the module name specified by variable init_top_cell can not be found in the imported netlist.

During design import, Innovus can auto-detect the top level module. However, if there are multiple modules in the netlist that are not instantiated in other modules, then it is ambiguous what the top level module is. For that purpose, it should be specified using init_top_cell.

IMPVL-909

NAME

IMPVL-909

SUMMARY

Failed to flatten the design.

DESCRIPTION

This message indicates some issues occur during flatten design. Please check previous ERRORs before IMPVL-909 to get more details.

IMPVPA-1

NAME

IMPVPA-1

SUMMARY

Verify Process Antenna stopped:

DESCRIPTION

Verify Process Antenna stopped abnormally, please check the license, memory loading for possible root cause.

IMPVPA-22

NAME

IMPVPA-22

SUMMARY

verifyProcessAntenna failed to run because no process antenna information found for this design. Import the process antenna library data and run verifyProcessAntenna again.

DESCRIPTION

This error is reported because verifyProcessAntenna does not have the needed information to properly check for process antenna violations. To check for process antenna violations you need to define the antenna parameters in your technology LEF or Open Access (OA) technology. For more information see the chapter Calculating and Fixing Process Antenna Violations in the LEF/DEF Language Reference.

IMPVPA-55

NAME

IMPVPA-55

SUMMARY

Option "-leffile" for command verifyProcessAntenna is obsolete. Use 'lefOut -5.5 | -5.6 fileName' instead. The obsolete option still works in this release, but to avoid this warning and to ensure compatibility with future releases, remove "-leffile" from your script.

DESCRIPTION

lefOut supports antanna information dump out, please use lef 'lefOut -5.5 | -5.6 fileName' to write out antenna information after "verifyProcessAntenna". -leffile option is obsolete and will be retired in next release.

For example, please use 'man lefOut" to get help how to use lefOut to write out lef file.

NRDB-18

NAME

NRDB-18

SUMMARY

The binary Extended Cap Table file version (%f) is incompatible with the current version (%s)

DESCRIPTION

The binary Extended Cap Table file version is incompatible with the current version.

Regenerate captable using generateCapTbl command. Refer to the text command reference document on how to generate captable using generateCapTbl command.

NRDB-37

NAME

NRDB-37

SUMMARY

The number of %s exceeds the limit %d. Remove the excess definitions before proceeding.

DESCRIPTION

NanoRoute cannot proceed any further without reducing the number of LAYERs,

NONDEFAULTRULEs, VIARULEs or VIAs identified in the ERROR message. Fixing this error requires removing excess definitions from the technology file and/or imported design files.

NRDB-51

NAME

NRDB-51

SUMMARY

%s %s has no instance pin or special wire in its connectivity definition. %s with the same name will be routed but will not be connected to the empty %s.

DESCRIPTION

The root cause of this issue is that the net connectivity definition is incomplete.

It may have the net name in the special net section but no instance pin or wire. If the net has connectivity in the regular net section it will have no target in the special net section and warn of the inconsistancey. One of the possible reason could be manual editing done by user.

- Please corect the input data DEF/OA.

- To avoid this warning and route the net you can do the following :

1) convertSNetToNet -nets test/net1

2) Turn-off "-skip_routing" if exists through "setAttribute" command

3) Now do a selected net ecoRoute

NRDB-87

NAME

NRDB-87

SUMMARY

%s %s is partially routed in non-ECO mode and may be re-routed. If exiting wires are to be preserved, set the -routeWithEco option to true.

DESCRIPTION

This warning indicates a net is only partially routed and that if you want to preserve the pre-routed segments you should set "setNanoRouteMode -routeWithEco true". Otherwise, NanoRoute is free to re-route the net entirely based on the best solution it finds for the net. If you do not mind the net being re-routed you can ignore this warning.

NRDB-158

NAME

NRDB-158

SUMMARY

Missing via from %s %s to %s %s in %s %s. Add the missing via or remove all vias from %s %s so that NR can use the vias from the default %s.

DESCRIPTION

In an NonDefaultRule, it is optional to specify which vias the rule should use during routing. If no vias are defined then router will use the DEFAULT via's for the NonDefaultRule routing.

If NonDefaultRule has vias defined between some layers but not all, then this error is reported.

For example, if NonDefaultRule has vias defined between Metal1 and Metal2 but not between Metal2 and Metal3, this error is reported, you need to define or specify vias between each layer. See the NONDEFAULTRULE LEF syntax for more details on defining or specifying the vias to use.

NRDB-164

NAME

NRDB-164

SUMMARY

The number of layers between bottom routing layer (%d) and top routing layer (%d) is less than 2. Nanoroute cannot route with less than two routing layers.

DESCRIPTION

The number of layers between bottom routing layer and top routing layer is less than 2. Nanoroute cannot route with less than two routing layers. It requires at least two routing layers in order to route.

For example, NanoRoute need at least two routing layers:

setNanoRouteMode -routeTopRoutingLayer 4

setNanoRouteMode -routeBottomRoutingLayer 3

routeDesign

or

setAttribute -net reset -top_preferred_routing_layer 4 -bottom_preferred_routing_layer 3

routeDesign

NRDB-166

NAME

NRDB-166

SUMMARY

Boundary for %s %s is not properly defined. Correct the SIZE of the corresponding MACRO in the

library.

DESCRIPTION

Check the library if the size of stdcell/block is defined properly. If LEF format is used, make sure the SIZE statement exists in the MACRO definition, and the width/height values are not zero.

NRDB-319

NAME

NRDB-319

SUMMARY

MINIMUMCUT rule specifying %d (> %d) cuts for %s %s is ignored. Only up to %d is supported right now. NOTE TO RND : Please confirm if NR can support only MINIMUMCUT 8 ;

DESCRIPTION

Nanoroute cannot drop more than 8 cut vias, and hence cannot support below rule.

MINIMUMCUT 9 WIDTH 0.xxx ;

For example,

NanoRoute issues this message and leaves mincut violations when the following rule is specified in the technology LEF:

MINIMUMCUT 9 WIDTH 0.770 WITHIN 0.39 FROMBELOW ;

NRDB-331

NAME

NRDB-331

SUMMARY

LAYER OVERLAP cannot he defined in between layer definition in the LEF. An OVERLAP layer should be defined before or after other layers. Correct this in technology LEF before continuing.

DESCRIPTION

Layer "OVERLAP" cannot be defined in between the routing layers. It should be defined before or after defining the routing layers in the LEF file.

For example, Define LAYER OVERLAP before other LAYER definition in the LEF :

LAYER OVERLAP

\tTYPE OVERLAP

END OVERLAP

LAYER M1

\tTYPE ROUTING

...

END LAYER M1

..

or define LAYER OVERLAP at the end of all routing LAYER definitions:

LAYER M7

\tTYPE ROUTING

...

END M7

LAYER OVERLAP

\tTYPE OVERLAP

END OVERLAP

NRDB-605

NAME

NRDB-605

SUMMARY

Cannot set net attribute %s to %s for %s %s, as the net has pre-routed wires. Delete the pre-routed wires or convert them to SPECIAL wires, and then retry.

DESCRIPTION

NanoRoute does not support setting the rule of a net if the net has already been partially or fully routed. To set any attribute on a net, the prerouted wires must be deleted or converted to special wires.

For example:

convertNetToSNet -nets $n

editSelect -net $n

editSelectVia -net $n

editChangeStatus -to FIXED

setAttribute -net $n -non_default_rule CTS_RULE

NRDB-608

NAME

NRDB-608

SUMMARY

Cannot find special net %s for attribute %s. To reset an attribute to its default value specify the value "default".

DESCRIPTION

Cannot find special net default for attribute -shield_net To reset an attribute to its default value specify the value "default" with some exceptions (see below).

For example:

\tsetAttribute -net netName -non_default_rule default

\tsetAttribute -net netName -preferred_extra_space default

Exceptions:

1. The option -shield_net has a default of "none" which may cause confusion. So for -shield_net you must specify "none" to return it to its default value:

\tsetAttribute -net netName -shield_net none

2. You have a net with -top_preferred_routing_layer set to 7 and -bottom_preferred_routing_layer set to 6. You cannot reset -top_preferred_routing_layer first because its default value is 1 and the top preferred layer is not allowed to be less than or equal to the bottom preferred layer. You need to reset the bottom preferred layer first.

3. You cannot reset the non-default rule (NDR) on a routed wire. You must first delete the routing for the wire then re-route it after changing its rule.

NRDB-609

NAME

NRDB-609

SUMMARY

Cannot set attribute %s to %s on a net, since the value is not valid for this attribute. Specify a valid value and then retry.

DESCRIPTION

Net attributes cannot accept an arbitrary value. Each net attribute has a set of acceptable values. Type setAttribute -help for detailed information.

NRDB-628

NAME

NRDB-628

SUMMARY

Found non-default rules %s and %s in %s %s. Currently, only one default rule is supported on a net. Correct this configuration to ontinue .

DESCRIPTION

Non-default rule (NDR) is applied to nets using setAttribute -net netName -non_default_rule <ruleName>. You cannot have multiple non-default rule on a single net which need to be routed.

A non-default rule can be modified on a net using modify_ndr as long as the net is not routed. An error is reported if you try to modify a NONDEFAULTRULE of a routed net.

For example,

In order to change the non-default rule of a routed net you must delete the routing of the net, change the rule, then re-route the net.

Ex :

editDelete -net netName

setAttribute -net netName -non_default_rule newRule

setNanoRouteMode -routeSelectedNetOnly true

selectNet netName

routeDesign

If you have partially prerouted portions of the net, these sections must be defined as special nets. Use the command convertNetToSNet to convert these prerouted portions to special nets:

convertNetToSNet -nets netName

One exception to the above is if a net is already routed, you can use editChangeRule to change the non-default rule applied to the wire segments of the net. editChangeRule does not change the non-default rule attribute of the net, so if the net is re-routed or ECO routed, it will be routed with the widths and spacings of the original non-default rule applied to it. editChangeRule should only be

used if you don't intend to do any more routing. Example:

editChangeRule -net netName -from rule1 -to rule2

NRDB-629

NAME

NRDB-629

SUMMARY

NanoRoute cannot route PIN %s of INST %s for NET %s. The PIN does not have physical geometries. NR will ignore the PIN as if it does not exist in the NET. To fix the problem, add physical geometries to the PIN in the library.

DESCRIPTION

NanoRoute cannot route a PIN if it does not have physical geometries. Make sure the PIN of the corresponding MACRO has geometries defined.

For example:

EG:

MACRO <CELL_NAME>

\tCLASS CORE ;

\tORIGIN 0 0 ;

\tSIZE <n.nn> BY <n.nn> ;

\tSYMMETRY X Y ;

\tSITE <site_name> ;

\tPIN <pin_name>

\t\tDIRECTION INOUT ;

\t\tUSE POWER ;

\t\tPORT

\t\t\tLAYER <layer> ;

\t\t\tRECT <n.nn n.nn n.nn n.nn > ;

\t\tEND

NRDB-631

NAME

NRDB-631

SUMMARY

%s %s has more than one top-level logical pin which has no physical port (pin geometries) or has not been placed. Correct the pins before continue.

DESCRIPTION

A top level-pin is logical if it's not placed or it has no physical port (pin geometries. If a net has more than one such logical pin, NanoRoute will not route the design but error out. Create a physical pin geometries to such nets

NRDB-676

NAME

NRDB-676

SUMMARY

NET %s is marked as fully routed but NanoRoute detects that PIN %s of INST %s is not connected to the net.

DESCRIPTION

Each net has a set of flags to indicate its statuses. One of them is a flag to indicate if a net is fully routed. If this flag says a net is fully routed, but NanoRoute traverses every pin in the net and finds some pin is not connected to the net, this warning will be issued.

This issue could happen when a tie-net pin is tied to the special net by special vias/wires. The flag is set based on regular routing information, and it is possible that the pin does not exist in the regular routing information imported from reference DB. NanoRoute is aware of this mismatch issue, and performs a integrity check to detect it.

To fix the issue, check the warning pin if it is covered by STRIPE metal and connected by special vias. You can delete the special vias and set option setAddStripeMode to skip dropping via on this type of pins. Please reference command manual of setAddStripeMode and addStripe. The severity of this warning is not high.

NRDB-682

NAME

NRDB-682

SUMMARY

Connectivity is broken at PIN %s of INST %s connects to NET %s at location %s on LAYER %s. The location is not inside the pin geometry extraction.

DESCRIPTION

This could be due to moved wires or cells from design optimization.

If the user edited wires or if optDesign move cells the connectivity may be broken and need re-routing.

NanoRoute is capable of removing the problematic wires and reroute the PIN correctly.

If the wires are FIXED, you need to unfix them manually before routing.

NRDB-728

NAME

NRDB-728

SUMMARY

%s %s in %s %s does not have antenna diff area.

DESCRIPTION

This warning is reported when antenna fixing is enabled (setNanoRouteMode -drouteFixAntenna true) and an output or bi-directional pin is missing a value for AntennaDiffArea in the LEF. AntennaDiffArea defines the diffusion area for this pin. This value is then used when calculating the Process Antenna Effects (PAE) on the net connected to this pin. AntennaDiffArea defines the diffusion area connected to a net. Diffusion discharges a net and lessens the process antenna effect. If AntennaDiffArea is not defined then NanoRoute may perform unnecessary antenna fixing using layer hopping and diode insertion which would not be needed if AntennaDiffArea was properly defined for the pin.

If AntennaGateArea is not defined for input pins in LEF then it shows the warning for antenna gate area.

In a summary if you simply want to stop this warning you can add ANTENNAGATEAREA 0; to the input pin. While 0 is the default value if no statement is given, there is a difference between default, and "the gate area is really 0". Same as for output pin. Put ANTENNADIFFAREA 0 ; for LEF output pins without any diff area. In case of inout pin you have to add both ANTENNAGATEAREA and ANTENNADIFFAREA to 0.

NRDB-733

NAME

NRDB-733

SUMMARY

%s %s in %s %s does not have physical port.

DESCRIPTION

This warning indicates this pin does not have a physical shape defined properly in the LEF for MACRO or PAD cells.

The possible causes are:

- The pin does not have a RECT or POLY statement in the LEF to define its geometry.

- Another reason is the pin may be defined as USE POWER or GROUND. NanoRoute does not route power pins.

For example:

MACRO INVXL

...

PIN A

DIRECTION INPUT ;

USE POWER ;

PORT

LAYER metal6 ;

RECT 104.000 1549.940 104.800 1553.420 ; # Physical definition of pin END END A If a pin defined as a power or ground pin, and has SHAPE ABUTMENT or FEEDTHRU defined for it, then NanoRoute will treat the pin as a physical obstruction. If the power/ground pin is missing the SHAPE attribute then NanoRoute treats it as a logical pin and will report these warnings.

NRDB-741

NAME

NRDB-741

SUMMARY

Found shorts between two different ports on pin %s of cell_view %s. Loop detection and weak connectivity checking will be skipped for this pin. If loop is not an issue, you can disregard this message. Otherwise, pin geometries need to be corrected.

DESCRIPTION

This warning is issued when the geometries defined in separate PORT statements for a PIN in the LEF short together or create a loop.

When a PIN has multiple PORT statements it means the geometries within each PORT statement are weakly connected. So they typically should not overlap or touch. If they touch they are considered strongly connected and should be within the same PORT statement.

NanoRoute runs special checks to avoid loops. When it encounters geometries in different PORT statements which short together, it will disable this loop checking for this pin and issue the warning above. You should review the PIN definition in the LEF and correct it as needed.

For example the pin below has 4 PORT statements which create a loop:

PIN A

DIRECTION INPUT ;

PORT

LAYER Metal1 ;

RECT 0 0 10 1 ;

END

PORT

LAYER Metal1 ;

RECT 0 0 1 10 ;

END

END A

NRDB-778

NAME

NRDB-778

SUMMARY

No multicut vias which meet all area rules for LAYER %s are defined in RULE %s. When a LEF MINIMUMCUT rule is defined for a layer, you must define multicut vias for the layer in the LEF file. Edit your LEF file and read it in again.

DESCRIPTION

When a LEF MINIMUMCUT rule is defined for a layer, you must define multicut vias for the layer in the LEF file

For example,

The following minimum cut rule indicates that vias with 2 cuts are required,

PROPERTY LEF58_MINIMUMCUT

"MINIMUMCUT 2 WIDTH 0.09 WITHIN 0.05 AREA 2.0 ;" ;

NRDB-855

NAME

NRDB-855

SUMMARY

Illegal wire segment on NET %s near %s on LAYER %s. The shape is off %s manufacturing grid (%s), and must be corrected. Change the shape from FIXED to ROUTED status to allow NanoRoute to correct the issue.

DESCRIPTION

If a design has illegal wires/vias that are off manufacturing grid, Routing will delete the segments to correct the issue for sign-off verification. If they are of status "FIXED" NanoRoute can not change the segments. Please correct or remove the shapes or change their status to ROUTED so NanoRoute can correct the issue.

NRDB-874

NAME

NRDB-874

SUMMARY

There %s %d dangling wire%s/via%s in the fully routed NET %s. NanoRoute will correct the dangling wires/vias that are not of FIXED status.

DESCRIPTION

A dangling wire has one or more endpoints that are not connected to pins or other wires.

NanoRoute will check if there are any dangling wires that are not FIXED in the net if a net has been touched.

Common scenarios that introduce the dangling wires are:

\t1) Some instances are IPOed, but wires are marked FIXED

\t2) The nets are eco-routed, and some of the FIXED wires become dangling

\t3) Some wires status are changed and the design rerouted .

Note The wires in the frozen layers will not be deleted since the layers are locked.

The warning is given for informational purposes.

NRDB-897

NAME

NRDB-897

SUMMARY

The same MINSTEP ... MAXEDGES ... MINBETWEENLENGTH ... rule is specified more than once for layer %s.

DESCRIPTION

{DETAILMESSAGE]

NRDB-898

NAME

NRDB-898

SUMMARY

More than one MINSTEP ... MAXEDGES ... MINADJACENTLENGTH (MINBETWEENLENGTH) ... rule are specified for layer %s.

DESCRIPTION

{DETAILMESSAGE]

NRDB-899

NAME

NRDB-899

SUMMARY

More than one MINSTEP ... MAXEDGES 0 rule are specified, MINSTEP s% MAXEDGES 0 will be used for layer %s.

DESCRIPTION

{DETAILMESSAGE]

NRDB-900

NAME

NRDB-900

SUMMARY

The same MINSTEP s% MAXEDGES 1 rule is specified more than once for layer %s

DESCRIPTION

{DETAILMESSAGE]

NRDB-912

NAME

NRDB-912

SUMMARY

Internal error. Report this to Cadence. Pin (%f %f) of layer %d from net %s does not have boundary access in route region (%f %f %f %f). The net is now set as open net. You can try to delete this net and re-do the routing to see if this problem can be avoided with a different routing pattern.

DESCRIPTION

There is an internal error from the software or the data base and the net will be set to open.

If you receive this message, download and install the latest software version from http://downloads.cadence.com. If the warning still occurs, please open a case through http://support.cadence.com so the cause can be determined.

This message should not be ignored. To save a test case for Cadence use:

\tsaveTestCase -name NRDB-912

As a workaround you can try deleting the net and re-routing it.

\teditDelete -nets netName

\tselectNet netName

\tsetNanoRouteMode -routeSelectedNetOnly true

\trouteDesign

\tsetNanoRouteMode -routeSelectedNetOnly false

NRDB-944

NAME

NRDB-944

SUMMARY

The cut shape in VIA %s doesn't match any predefined cut dimension. Only the cuts that are defined in CUTCLASS can be used in VIA definition. %s

DESCRIPTION

This error occurs when Nanoroute finds a VIA definition which does not meet the defined CUTCLASS definitions.

To avoid the error you must either;

1) Define a new CUTCLASS for this via,

2) Remove the via

3) Edit the via cut size to match one of the cut classes.

NRDB-954

NAME

NRDB-954

SUMMARY

Invalid option value -routeTopRoutingLayer %d. It is in conflict with already existing routed wires on layer %d. The option must specify a layer equal to or above the top-most layer for existing routes.

DESCRIPTION

Pre-routed wires are not allowed above the routeTopRoutingLayer limit.

Please change the layer limit or remove the wires.

Alternatively you can relax the hard limit and add a preferred layer to all nets with setAttribute.

NRDB-955

NAME

NRDB-955

SUMMARY

Invalid option value -routeBottomRoutingLayer %d. It is in conflict with already existing routed wires on layer %d. The option must specify a layer equal to or below the bottom-most layer for existing routes.

DESCRIPTION

The design has pre existing routed or custom routed nets with a layer below the bottom routing layer set for detail route.

1) You can set all nets to prefer to stay off the layer

2) You can set "skip_routing" attribute on nets which are routed below your Bottom layer.

3) If you dont want routing below a certain layer you may want to delete the wires on those layers and let the router complete using the layer range requested.

4) Allow the the lower layer for the routing range.

For example,

setAttribute -net <net_name> -skip_routing true

NRDB-965

NAME

NRDB-965

SUMMARY

VIA GROUP %s in rule %s doesn't match any predefined via group. Only the via group that are

defined in VIAGROUP can be used. %s

DESCRIPTION

This error occurs when Nanoroute finds a VIAGROUP definition which does not meet the defined CUTCLASS definitions.

To avoid the error you must either;

1) Define a new VIAGROUP for this group,

2) Remove the rule

3) Edit the via group name to match one of the via group.

NRDB-976

NAME

NRDB-976

SUMMARY

The TRACK STEP %.4f for preferred direction tracks is smaller than the PITCH %.4f for %s %s. This will cause routability problems for NanoRoute.

DESCRIPTION

If track resolution is too fine and results in lots of tracks, it will affect routing runtime. Also, if adjacent tracks cannot satisfy PICTH requirement, spacing violations cannot be prevented naturally, causing more DRC.

The issue is usually caused by a DEF file loaded by defIn. To fix the issue, use generateTracks in Innovus or modify tracks in the DEF file.

NRDB-1007

NAME

NRDB-1007

SUMMARY

Design has advanced design rules which require the Advanced Node license. NanoRoute failed to check out a Advanced Node license.

DESCRIPTION

DRC rules for 32 and below process nodes require the Advanced Node (encan) license. A encan license must be checked out if these rules exist in the library. Every major NanoRoute command will try to check out a encan license, unless a previous command has checked it out already. If fails, NanoRoute will stop.

The failure may happen when no Advanced Node license is installed on site, or all licenses are used up by other people.

NRDB-2005

NAME

NRDB-2005

SUMMARY

%s %s has special wires but no definitions for instance pins or top level pins. This will cause routability problems later.

DESCRIPTION

The router will flag false violations between unconnected pins and the special net wires, please ensure that all pins are connected to their special net wires.

NRDB-2016

NAME

NRDB-2016

SUMMARY

VIA %s will be corrected in routing as it is same as VIA %s.

DESCRIPTION

This warning is issued by the generated routing vias flow either by NanoRoute or dumpOutVias, if an NDR generated via geometry matches an existing via, the NDR will reuse the default rule via. The generated via will be removed as it is same as the default via and a warning is issued to inform the user.

NRDB-2026

NAME

NRDB-2026

SUMMARY

Design has top and bottom routing layers as %s %s, Some nets in the design have top and bottom preferred routing layer as %s %s. Top and bottom preferred routing layers should be within top and bottom routing layer range. Fix this before continuing.

DESCRIPTION

Design has top and bottom routing layers, some nets in the design have top and bottom preferred routing layer and the preferred routing layer effort is medium or high. Top and bottom preferred routing layers of a net should be within top and bottom routing layer range.

For example, if design has top routing layer as M7, then preferred routing layer on a net can be M7 or lower layers but not M8:

setDesignMode -topRoutingLayer 7

setAttribute -net net1 -top_preferred_routing_layer 7 -bottom_preferred_routing_layer 6

NRDB-2040

NAME

NRDB-2040

SUMMARY

Rule %s doesn't specify any vias that satisfy all of the area rules for layer %s

DESCRIPTION

Modern processes require each piece of metal to have a minimum area. This is defined in the LEF LAYER definition using the AREA keyword. For example:

LAYER M2

...

AREA 0.5 ;

...

END M2

It's important you have at least one via definition whose bottom metal layer meets the minimum area rule. Otherwise, NanoRoute cannot meet the minimum area rule when stacking vias. For example:

#The M2 rectangle for the following via is not large enough to meet the minimum area rule. It's area is 0.7 * 0.7 = 0.49 which is less than 0.5.

VIA VIA23 DEFAULT

LAYER M2 ;

RECT -0.35 -0.35 0.35 0.35 ;

LAYER CUT23 ;

RECT -0.25 -0.25 0.25 0.25 ;

LAYER M3 ;

RECT -0.35 -0.35 0.35 0.35 ;

END VIA23

#The M2 rectangle for the following via does meet the minimum area rule. It's area is 0.9 * 0.7 = 0.63 which is greater than 0.5.

VIA VIA23_v DEFAULT

LAYER M2 ;

RECT -0.35 -0.45 0.35 0.45 ;

LAYER CUT23 ;

RECT -0.25 -0.25 0.25 0.25 ;

LAYER M3 ;

RECT -0.45 -0.35 0.45 0.35 ;

END VIA23

Note not all vias need to meet the minimum area rule but you must have at least one or else the NRDB-2040 warning is issued and you will likely have a lot of minimum area violations when NanoRoute completes.

NRDB-2048

NAME

NRDB-2048

SUMMARY

More than one MINSTEP...MAXEDGES 1 NOADJACENTEOL... rules are defined for %s %s. Keep the first one.

DESCRIPTION

{DETAILMESSAGE]

NRDB-2050

NAME

NRDB-2050

SUMMARY

More than one MINSTEP...MAXEDGES 1 NOBETWEENEOL... rules are defined for %s %s. Keep the first one.

DESCRIPTION

{DETAILMESSAGE]

NRDB-2062

NAME

NRDB-2062

SUMMARY

Net %s is fully connected and it has off-grid wires/vias. NanoRoute will set it as skip_routing and ignore it during routing/verifying

DESCRIPTION

This Warning is triggered by inconsistent usage of,

setNanoRouteMode -drouteOnGridOnly {wire layer:layer}

setNanoRouteMode -drouteOnGridOnly {via layer:layer}

NR would mark the input full routed nets as 'skip_routing' true if there are any wires/via off-grid for the option check - setNanoRouteMode -drouteOnGridOnly {wire Mx:My via Vx:Vy}

For example,

If you route the clock nets without on-grid constraint, and then using below setting for data net routing or ECO routing in the flow, you will get this warning message.

setNanoRouteMode -routeSelectedNetOnly true

setNanoRouteMode -drouteOnGridOnly {wire 2:6 via 3:6}

NRDB-2081

NAME

NRDB-2081

SUMMARY

INST %s of CELL %s may not have on-grid via access.

DESCRIPTION

If the metal pins of this instance are off-grid, NanoRoute may not be able to drop on-grid via to access those PINs with "setNanoRouteMode -drouteOnGridOnly true

NRDB-2085

NAME

NRDB-2085

SUMMARY

Pin access impeded near Instance %s and Instance %s. Please inspect the area near the pin for any obstacle.

DESCRIPTION

This pin may be difficult to access and cost extra runtime, impact timing, and fail to route cleanly.

Please inspect the area near the pin for

1) Power routing near pin

2) Obstruction near pin

3) Pins near this pin

4) Overlapping instances and pins

NRDB-2106

NAME

NRDB-2106

SUMMARY

Ignoring layer %s MINIMUMCUT rule with WIDTH (%f) <= the layer's MINWIDTH (%f).

DESCRIPTION

The MINIMUMCUT rule is applied only to wide wires greater than the specified width. To force multi-cut vias globally on narrrow wires, use the following mode setting to restrict the usage of a particular cut via:

\t\tsetNanoRouteMode -dbViaWeight "<via_name_prefix>*" -1

NRDB-2111

NAME

NRDB-2111

SUMMARY

Found overlapping instances %s %s. This may result in unnecessary runtime, added violations, timing issues, and fail sign-off verification. Run checkPlace to display the placement violations and use routeDesign -placementCheck to prevent routing which placement issues.

DESCRIPTION

The design has overlapping cells. This is not always a disaster but can have undetected sub-straight violations as well as overlapping instance pins. The router will work diligently but not be able to resolve violations when routing to overlapping pins. You should not continue with placement violations. Please run checkPlace and inspect the design visually and resolve all placement issues before proceeding to routing.

For example:

routeDesign -placementCheck # fix any placement issues routeDesign -placementCheck

or

checkPlace # fix any placement issues

routeDesign

NRDR-4

NAME

NRDR-4

SUMMARY

Turning off power domain constraint for %s %s in region %s to avoid creating open net. Please check the power domain specification for the given net.

DESCRIPTION

setNanoRouteMode -routeHonorPowerDomain true With this option set, if a net connects to pins belonging to the same power domain, NanoRoute tries to route this net within that power domain. If this is not possible, NanoRoute completes the routing and issues the above warning to alert the user to check the routing of the listed nets.

NRDR-12

NAME

NRDR-12

SUMMARY

The width of LAYER %s in RULE %s is not defined. Define the missing width before proceeding.

DESCRIPTION

In some cases, some NONDEFAULTRULEs may be incomplete, and some layers are missing in the rule. Those non-default rules may be from manually crafted scripts or third-party tools. Make sure all layers are well defined in the non-default rule.

NRDR-13

NAME

NRDR-13

SUMMARY

Some nets are not global routed. Detail routing cannot be run.

DESCRIPTION

The above warnings can be seen during detailRoute for nets which are already routed and verifyConnectivity shows no opens but they have a FIXED segment and a trunk routing net attribute.

NanoRoute does not support trunk routing for nets with FIXED wires. Changing the pre routed segment to ROUTED or removing the nets trunk routing attribute or deleting the pre route will solve the issue.

You may also be limiting the layer rang during an ECO route such that the route can not be completed. Check the range of Bottom, Top limits and -modifyOnlyLayers option.

For example,

selectNet FOOBAR/FECTS_CLONE_N7

verifyConnectivity -selected

Found no problems or warnings.

Solution example :

selectNet FECTS_CLONE_N7

setNanoRouteMode -routeSelectedNetOnly true

editSelect -nets FECTS_CLONE_N7

editSelectVia -nets FECTS_CLONE_N7

editChangeStatus -to ROUTED

NRDR-30

NAME

NRDR-30

SUMMARY

Detail routing is stopped due to too many DRC violations.

DESCRIPTION

This warning occurs when NanoRoute sees an abnormal number of DRC violations during initial routing. It issues this warning and then stops so you can debug the violations to determine their cause. To override this automatic stop you can set the drouteAutoStop option to false

Note: Since this can add significant run time you should only override this setting when you're confident. NanoRoute will be able to resolve the violations and you have investigate the initial violations and are pursuing remedies to the violation.

setNanoRouteMode -drouteAutoStop false

There are several reasons NanoRoute may initial violations and stop:

1) Congestion - Review the global route congestion map to identify hot spots visually and reduce the congestion in this area by reducing the placement density using partial placement blockages or modifying the floorplan.

2) Pin access problems - Are the majority of violations on M1 and M2? If so, this can indicate pin access problems on standard cell pins or a Tracking problem, or a power rail issue. Review the violations at these pins and determine why they are occurring. For example, blockage is too close to the pin, pin is off the routing track or a proper via is not defined which can be dropped to the pin.

3) Pins under power stripes - Are the violations occurring when trying to route to standard cells placed under stripes? If so, use setPrerouteAsObs to treat these stripes as placement blockages. For example, the following treats strips on M1, M2 and M3 as placement blockages:

setPrerouteAsObs {1 2 3}

If you standard cells pin on M2 being placed under M3 stripes you can set the following instead. This will avoid placing M2 pins under M3 stripes but allow M1 standard cell pins to be place under the M3 stripes:

setPlaceMode -checkPinLayerForAccess { 1 2 }

4) Routing layers too limited - Make sure you have not set the max routing layer too low.

5) Other library or design issues - Review warnings at the beginning of the NanoRoute run which may indicate problems

NRDR-123

NAME

NRDR-123

SUMMARY

Some nets are not detail routed. Post-route operations (via_swapping, minimize detour, wire widening, spreading, or matching) cannot be done. If possible, normal detail routing will be done.

DESCRIPTION

Post-route operations cannot be performed unless all the signal nets are completely routed. Disable post-route options and then route the remaining nets using the routeDesign or ecoRoute command. Only use ecoRoute if less than 10% of the signal nets are unrouted. Once all the nets are routed you can then run post-route operations. The unrouted net can also be skipped using the net attribute setting if there is some reason it is to remain incomplete.

NRDR-126

NAME

NRDR-126

SUMMARY

Post-routing optimization is disabled because of too many DRC violations

DESCRIPTION

This warning occurs when NanoRoute sees too many violations in the post routing optimization stage. To avoid this warning and force NanoRoute to continue "setNanoRouteMode -drouteAutoStop false" before routing.

Note: You should only override this setting when you're confident NanoRoute will be able to resolve the violations. Otherwise, review the violations to determine the cause. It can be due to congestion, pin access problems, bad design rules, improper via definitions, track missalignment etc. Ignoring the violations causing the auto stop can lead to long runtime, timing problems, and the routing may not complete.

NRDR-129

NAME

NRDR-129

SUMMARY

Cannot do post-route optimization (minimize detour, wire widening, spreading, or matching) using command '%s', use 'detailRoute' command instead. If possible, normal detail routing will be done.

DESCRIPTION

Generally, you get this warning message when you do incremental globalDetailRoute and don't reset post-route wire optimization options. When post-route wire optimization is being run (i.e. wire widening, spreading) you should set the appropriate "setNanoRouteMode -drouteePostRoute*" options then run detailRoute or routeDesign -wireOpt. If you run globalDetailRoute or just routeDesign this warning will be reported.

NRDR-175

NAME

NRDR-175

SUMMARY

Routing must start from drouteStartIteration 0 when the routing state is unknown or external routing is imported.

DESCRIPTION

Iterations can be separated 0,1,2,3,4, but you are not allowed to use any other command that will change the design routing unless you start from iteration 0 for the next detailRoute command.

For example,

globalRoute

saveDesign groute

setNanoRouteMode -drouteEndIteration 0

detailRoute

savedesign droute_0

setNanoRouteMode -drouteStartIteration 1

setNanorouteMode -drouteEndIteration 1

detailRoute

saveDesign droute_1

If the users modifies teh clock net or introduced other pre routes the iteration must be returned to 0
For large changes starting from globalroute is recommended..

setNanoRouteMode -drouteStartIteration 0

setNanorouteMode -drouteEndIteration default

detailRoute

NRDR-240

NAME

NRDR-240

SUMMARY

Deleting shielding during routing and optimization.

DESCRIPTION

Shielding will be temporarily removed during routing and routing optimization commands, eg. via swapping, wire widening, wire spreading, and then the nets will be re-shielded after the operation.

To keep the shielding users can set the shielded net to be fixed or its attribute to skip routing however the shielding may interfere with the success of the ECO route or optimization requested. In some cases the ECO can fail if the resources are insufficient so it is recommended to allow the

methodology to remove and re add the shielding automatically.

NRDR-328

NAME

NRDR-328

SUMMARY

Some nets are not detail routed. routeFixSignoffDrc command to fix signoff DRC violation cannot be done.

DESCRIPTION

Signoff DRC violation fixing cannot be performed unless all the signal nets are completely routed. Perform detail route first to route all nets using routeDesign command. Once all the nets are routed you can then run routeFixSignoffDrc. The unrouted net can also be skipped using the net attribute setting if there is some reason it is to remain incomplete.

NRDR-334

NAME

NRDR-334

SUMMARY

Unable to run 'ecoRoute -target' command because insufficient eco routing information is available. Regular 'ecoRoute' command will be executed instead.

DESCRIPTION

One possible reason that can cause this is when a fully routed design from DEF file is imported. The design must be loaded from a saved DB (from the original routing step) before 'ecoRoute -

target' command can be executed.

NREX-32

NAME

NREX-32

SUMMARY

The dielectric layer has wrong RANGE values 'RANGE %lf %lf'. It should start from high value of %f.

DESCRIPTION

The range value error may be due to a resolution mismatch between the routing technology file and the dielectric layers in the PCS file.

For example, if the LEF Database unit value is 1000, then all values in the PCS file should be rounded to the nearest 0.001. In the PCS file.

NRFL-215

NAME

NRFL-215

SUMMARY

DATBASE UNIT is not set in the first technology file. Using 1000 DATABASE UNITS per MICRON.

DESCRIPTION

DATBASE UNIT is not set in the first technology file.

The DATBASE UNIT will be set to 1000 DATABASE UNITS per MICRON

This can occur when the manufacturing grid is defined prior to the units in the technology LEF file.

For example:

\tMANUFACTURINGGRID 0.005 ;

\t\tUNITS

\t\tDATABASE MICRONS 2000 ;

\tEND UNITS

To fix the above issue, In the LEF file you must specify the statements in the following order:

\tUNITS

\t\tDATABASE MICRONS 2000 ;

\tEND UNITS

\tMANUFACTURINGGRID 0.005 ;

NRFL-217

NAME

NRFL-217

SUMMARY

Too many table entries (> %d). Please check the table with line %s in file

DESCRIPTION

This message means the table at the specified line has two many values. This can occur for example with AntennaDiffAreaRatio that are defined with Piece-Wise Linear (PWL) functions. In this example the PWL table might contain more than 100 lines which is the limit. To resolve this issue, values must be removed to reduce the number to be less than 100.

NRFL-374

NAME

NRFL-374

SUMMARY

%sSpacing table is not monotonically increasing. Layer %s spacing table entry %f is less than the previous entry %f.

DESCRIPTION

This error can occur when the spacing rules in the technology file are not increasing in order.

Spacing needs to increase like 1,2,3,4,5 not 1,2,4,3,5.

Please check the spacing table values in the technology file.

NRGR-21

NAME

NRGR-21

SUMMARY

Selected nets are already detail routed or no nets are selected.

DESCRIPTION

Routing with setNanoRouteMode -routeSelectedNetOnly true or selecting route selected nets from the GUI will route only the selected nets. If no nets are selected, NanoRoute can not route and will issues this warning message.

This can happen if selected nets were routed and the design was then saved before setting the above mode to false.

see getNanoRouteMode -routeSelectedNetOnly

To route, either select unrouted nets or set setNanoRouteMode -routeSelectedNetOnly false.

NRGR-59

NAME

NRGR-59

SUMMARY

Pin %s of instance %s (cell %s) is not accessible. NanoRoute will continue but the pin is not accessible and will result in an open net. To correct this problem please check the manufacturing grid, placement and pin shape.

DESCRIPTION

The pin was drawn using a different manufacturing grid from the one defined in the LEF technology file.

Please check the pin shape and the technology files database units and manufacturing grid to make sure the pin shape can be describe or that the technology is set to the correct resolution for the foundry.

DATABASE MICRONS 1000 ;

MANUFACTURINGGRID 0.005 ;

NRGR-145

NAME

NRGR-145

SUMMARY

Gcell grid area %s does not cover inst("%s") pin("%s") @ %s.

DESCRIPTION

Tracks and Gcells must cover the design. If data was read in with incomplete Gcell or Track definitions the design will not be routable.

Please fix the imported data or use generateTracks to rebuild the definitions for this design.

For example:

generateTracks

NRGR-164

NAME

NRGR-164

SUMMARY

This design is over congested and will have routability problem. Correct the placement to fix congestion problem.

DESCRIPTION

You can check the globalRoute congestion map to find the congested areas. If the congested areas are all over the design, you may redo the floorplan. If the floorplan cannot be resized, check if the routing track can be optimized on the congested layer from the Congestion Analysis Table shown in log. If the congested areas are located in some small area which we called hotspot, you may optimized the placement.

NRGR-190

NAME

NRGR-190

SUMMARY

Cannot find routing solution for net %s within bus guide. The net will be open. This problem may be caused by discontinuous bus guide path. Bus Guides need to contain a path from pin to pin defined by a group of 3-D guiding rectangles. Check the continuity of the layers and rectangles between the set of pins of the net to be guided.

DESCRIPTION

This message is reported when bus guides are not continuous in guiding the nets path.

\t1. The bus guide should be continuous overlapping layers and rectangular shapes

\t2. The bus guide should overlap driver and receiver pins completely

\t3. The bus guides should follow the preferred routing direction.

\t4. The top and bottom routing layer of "setNanoRouteMode" should cover the specified bus guide layers.

For example:

createBusGuide -netGroup my_grp \

-centerLine 492.365 1174.930 492.365 1276.975 \ -width 1.000 -layer 3:3

setNanoRouteMode -routeTopRoutingLayer 4 setNanoRouteMode -routeBottomRoutingLayer 0

routeDesign

NRGR-228

NAME

NRGR-228

SUMMARY

The net %s has can not be routed. Fixed wire and routePGPinSignalRoute is not sported with eco route.

DESCRIPTION

NanoRoute issues the warning above when user requests eco routing on secondary power/ground pins using routePGPinSignalRoute that have fixed net segments.

For example:

Below commands will change the status of a net and its vias to routed. See the example below:

editSelect -type Signal -nets VDD

editSelectVia -nets VDD

editChangeStatus -to ROUTED

NRGR-261

NAME

NRGR-261

SUMMARY

Internal error with Global Route Setup up. Report to Cadence representative.

DESCRIPTION

This message is reported when the gcell size is larger than the variables which store the hcell x and y index.

\t1.

NRIG-34

NAME

NRIG-34

SUMMARY

Power/Ground pin %s of instance %s is not connected to any power/ground net. Use command globalNetConnect to connect the power/ground pin to a power/ground net.

DESCRIPTION

The instance has pins defined with USE POWER or USE GROUND in the LEF But the pins do not have a net associated for connectivity. Check the power and ground pins for this instance and verify you have specified a globalNetConnect command to connect them.

If you do not want the pins connected, you can ignore this warning.

If the instanceName is PIN this means an IO power pin on the block does not have a net specified.

NRIG-43

NAME

NRIG-43

SUMMARY

Cannot have special via %s at location %s in signal net %s. Removing routing segment for %s %s.

DESCRIPTION

If generateVias was used the vias are stored in the DEF and imported but may not be sufficent without either LEF vias or regenerating a full via set.

To resolve this issues please use: setGenerateViaMode -auto true

Setting the above command before importing the design will save the variable in the .mode file.

If you have a third party DEF, it's recommended that you import the design into innovus, set the above variable and save the DB from innovus and exit. Now again open a new Innovus session and restore the saved innovus DB .

NRIG-74

NAME

NRIG-74

SUMMARY

Found pre-routed non default rules %s and %s in %s %s. Currently only one non default rule is supported. Net will be skipped and may be open. Enable setNanoRouteMode -drouteUseLefPinTaperRule to allow pin taper rules.

DESCRIPTION

When such nets are hand routed with two NDR's and the connecting instance got moved or buffer is added during the course of timing eco at postroute stage, By default nanoRoute does not support more than one NDR, so the Net will be skipped and the net attribute set to avoid routing. Use setAttribute -net %d skip_routing false for NanoRoute to check and route the net next time.

Please change the Net to use a single NDR and then reset the skip attribute on the net and reroute or re-ecoRoute to resolve open nets.

For example, to convert two NDR to an single NDR and reset skip route on such nets and then do ecoRoute

convertNetToSNet $net1

setAttribute -net $net1 -non_default_rule NDR1

convertSNetToNet $net1

setAttribute -net $net1 skip_routing false

setNanoRouteMode -routeWithEco true

ecoRoute

verifyConnectivity -net $net

NRIG-77

NAME

NRIG-77

SUMMARY

Found placement violations. Please investigate and correct before routing. Routing with placement violations can cause long runtime and may be irresolvable. Use routeDesign -placementCheck to stop on violations. Use routeDesign -noPlacementCheck to skip the check.

DESCRIPTION

The message is reported to alert user that the design has placement violations like cell overlaps, pin access issues etc...

Run checkPlace to catch the violations and fix them before routing

NRIG-96

NAME

NRIG-96

SUMMARY

Selected single pass global detail route "-globalDetail". Clock eco and post optimizations will not be run. See "man NRIG-96" for more details.

DESCRIPTION

Use option "-globalDetail" to run multiple iterations of routing with user specified net selections and routing options. The following examples will mimic pre-11.13 behavior.

To run pre-clock eco plus global detail route:

innovus 1> routeDesign

Note that if high effort flow is enabled, post optimizations will be executed. If this is not desired, then disable the high effort flow:

innovus 1> setDesignMode -flowEffort none

innovus 2> routeDesign

To run post route optimizations in non high effort flows:

innovus 1> routeDesign

innovus 2> routeDesign -viaOpt -wireOpt

NRIG-117

NAME

NRIG-117

SUMMARY

Cannot have special via %s at location %s in signal net %s. This routing segment is fixed, so net will be skipped.

DESCRIPTION

If generateVias was used the vias are stored in the DEF and imported but may not be sufficent without either LEF vias or regenerating a full via set.

To resolve this issues please use: setGenerateViaMode -auto true

Setting the above command before importing the design will save the variable in the .mode file.

If you have a third party DEF, it's recommended that you import the design into innovus, set the above variable and save the DB from innovus and exit. Now again open a new Innovus session and restore the saved innovus DB .

NRTM-24

NAME

NRTM-24

SUMMARY

Read error in timing file %s.

DESCRIPTION

This message is reported when .tif file is corrupted or not fully generated.

Possible causes is truncated file due to disk space issue etc.

PRL-0389

NAME

PRL-0389

SUMMARY

Could not create a new process for %s.

DESCRIPTION

fork cannot allocate sufficient memory to copy the parent's page tables and allocate a task structure for the child. Release more memory to rerun it. Or it was not possible to create a new process because the caller's RLIMIT_NPROC resource limit was encountered. Terminate some processes to rerun it.

PRL-0390

NAME

PRL-0390

SUMMARY

Could not create a new process for %s.

DESCRIPTION

fork failed to allocate the necessary kernel structures because memory is tight. Release more memory to rerun it.

PTNASMD-90

NAME

PTNASMD-90

SUMMARY

Pin %s of abutted partition %s could not be assigned. Could not find a feasible slot for the pin. Create more feasible location before for pin assignment by inserting feedthrough buffers using insertPtnFeedthrough command or allowing more layers for assigning pins or using setPinAssignMode -strict_abutment false or using setPinAssignMode -allow_unconnected_in_abutted_edge true for relaxing this check.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1 In abutted designs, pins of following type can not be placed on common edges between two

adjoining partitions.

.in +2

A. Pins of net not connected to adjacent partition (fences of the two partitions being connected are not touching each other in floorplan).

B. Pins of nets having connections to two or more partitions any pin belonging to net of above type will have to route over an unconnected partition and result in illegal routing.

Feedthrough step is required to get rid of pins which connect non-adjacent partitions or multiple partitions, by changing netlist and making all pins connect to only one pin on adjacent partition to make the routing of net feasible/legal

C. Floating pins

.in

#2. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

#3. Use setPinAssignMode -strict_abutment false to relax abutment violations checks for placing multi partition pin of a net, non neighbor pins of a net and floating pins on abutted edges.

#4. Use setPinAssignMode -allow_unconnected_in_abutted_edge true to relax abutment violations checks for placing floating pins on abutted edges.

Example:

---

eg. if pins are not assigned for a net which has more than two partition pins to connect use insertPtnFeedthrough command to change netlist to have new nets added and older net modified in way that, now nets only connect two pins of adjacent partitions only.

PTNASMD-100

NAME

PTNASMD-100

SUMMARY

The net %s is not connected to any terminal. This net will not be considered for feedthrough buffer insertion. Correct the netlist to get this net considered for feedthrough buffer insertion.

DESCRIPTION

An unconnected net will not be considered for feedthrough insertion. The net should be connected to an output port and an input port to be considered for feedthrough insertion.

PTNASMD-233

NAME

PTNASMD-233

SUMMARY

No legal free slots available for %s of partition %s. Create additional slots using definePartition command or by removing blockage before pin assignment.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

PTNASMD-426

NAME

PTNASMD-426

SUMMARY

Adjusting partition %s core to left from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

This is happening because the core spacing values specified (I/O to core distance of partition block) are not multiple of placement grid. Same issue for IMPPTN-427, IMPPTN-428 and IMPPTN-429 based or the side.

Example:

<CMD> definePartition -hinst uCORE/uPKTSS/uPKTSS_PPCS_PMA_SYS -coreSpacing {2.7 2.7 1.9 1.9} -reservedLayer {1 2 3 4 5 6 7 8} -routingHalo 1.9 -routingHaloTopLayer 7 -routingHaloBottomLayer 1 -placementHalo {2.7 2.7 1.9 1.9} -railwidth 0.1 -minPitchLeft 3 -

minPitchRight 3 -minPitchTop 3 -minPitchBottom 3 -pinLayerTop {3 5} -pinLayerBottom {3 5} -pinLayerLeft {4 6} -pinLayerRight {4 6}

Creating partition PKTSS_PPCS_PMA_SYS.

**WARN: (IMPPTN-426): Adjusting partition PKTSS_PPCS_PMA_SYS core to left from 1.900000 to 2.025000.

**WARN: (IMPPTN-427): Adjusting partition PKTSS_PPCS_PMA_SYS core to right from 1.900000 to 2.025000.

**WARN: (IMPPTN-428): Adjusting partition PKTSS_PPCS_PMA_SYS core to top from 2.700000 to 2.850000.

**WARN: (IMPPTN-429): Adjusting partition PKTSS_PPCS_PMA_SYS core to bottom from 2.700000 to 2.850000.

Placement grid is at 0.135 x-direction, 0.095 y-direction.

PTNASMD-427

NAME

PTNASMD-427

SUMMARY

Adjusting partition %s core to right from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

During partitioning, the warnings above are issued. How does Innovus determine these adjustments?

\t Innovus snaps the partition coreBox (area where rows are created and placement can be done) boundary to the placement grid. The remaining difference between coreBox and partition box is adjusted in core to right, core to top values.

Example:

**WARN: (IMPPTN-427): Adjusting partition lbrx_top_0 core to right from 0.000000 to 0.100000.

PTNASMD-428

NAME

PTNASMD-428

SUMMARY

Adjusting partition %s core to top from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

During partitioning, the warnings above are issued. How does Innovus determine these adjustments?

\t Innovus snaps the partition coreBox (area where rows are created and placement can be done) boundary to the placement grid. The remaining difference between coreBox and partition box is adjusted in core to right, core to top values.

Example:

**WARN: (IMPPTN-428): Adjusting partition lbrx_top_0 core to top from 0.000000 to 3.680000.

PTNASMD-429

NAME

PTNASMD-429

SUMMARY

Adjusting partition %s core to bottom from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

This is happening because the core spacing values specified (I/O to core distance of partition block) are not multiple of placement grid. Same issue for IMPPTN-427, IMPPTN-428 and IMPPTN-429 based or the side.

Example:

**WARN: (IMPPTN-429): Adjusting partition PKTSS_PPCS_PMA_SYS core to bottom from 2.700000 to 2.850000.

PTNASMD-555

NAME

PTNASMD-555

SUMMARY

A feasible legal location was not found for %d (out of %d) pins. Consequently, the following pins could not be assigned:

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

2. Insert feedthrough buffers using the insertPtnFeedthrough command.

PTNASMD-624

NAME

PTNASMD-624

SUMMARY

insertPtnFeedthrough could not find a path for net '%s' to reach '%s'. If the -topoFile option is being used, the topology specified for this net is incomplete.

DESCRIPTION

In case automatic feedthrough insertion is being done, it means that a path to some of the terminals could not be found. If the routeBased option is used, the routing may be incomplete. For the case the topology file is used an explanation follows.

Tool issues above warning during insertPtnFeedthrough command step, when topology file provided with -topoFile is used to guide the tool for creating the feedthrough in a specified partition for multi-fanout nets. You will get above warning if the topology file did not define for all the terminals for a multi-fanout net. Always follow the convention from_pin to to_pin for writing the topology file.

Example:

If the net goes to three partition A, B and C and you want to make a part of the net from A to D then to C, then you can use the following approach to write the topology file.

net n123

hinst-hinst A D;

hinst-hinst D C;

hinst-hinst A B;

end net

So, here all the combinations are covered where the net goes, instead of defining the A-D-C.

PTNASMD-646

NAME

PTNASMD-646

SUMMARY

insertPtnFeedthrough is trying to find a feedthrough path for net %s. It could not find a path to partition or terminal [%s]. Partitions connected to this net may not be adjacent to each other.

DESCRIPTION

Automatic feedthrough insertion derives the feedthrough topology using the placement. It assumes a channel-less design. The possibility of routing through channels is considered minimal. In this design a path to a partition or terminal connected to the above mentioned net could not be found without avoiding the channels.

PTNASMD-647

NAME

PTNASMD-647

SUMMARY

insertPtnFeedthrough skipping net [%s] because a path to some of the partitions or terminals could not be found. It might not be necessary to insert feedthrough buffers for this net. If you wish to insert feedthrough buffers for this net, then use the topology file for guided feedthrough buffer insertion or use the -routeBased option after routing the net.

DESCRIPTION

insertPtnFeedthrough assumes the design to be channel-less and partitions to be in the line of sight for feedthrough path to pass from one partition to another. In case of channel based designs where this is not true, the named net is ignored. In case feedthrough insertion is required for the net, either route the design and used insertPtnFeedthrough -routeBased or define the path for the net in a topology file and use insertPtnFeedthrough -topoFile <filename>

Example:

---

earlyGlobalRoute

insertPtnFeedthrough -routeBased

Or

insertPtnFeedthrough -topoFile <filename>

PTNASMD-652

NAME

PTNASMD-652

SUMMARY

The pushdownBuffer command cannot create an instance with name [%s%s]. An instance with this name already exists in the design. Using default prefix and name [%s] for this instance.

DESCRIPTION

This message is issued if the pushdownBuffer uses the prefix provided with the -prefix option and the resulting name has a conflict with an existing instance name. No action needs to be taken as it will make another name with the default prefix.

PTNASMD-716

NAME

PTNASMD-716

SUMMARY

Partition %s constraint missing. Specify a Guide, Region, Fence constraint on the partition or place the blackbox instance.

DESCRIPTION

While committing partitions 1. Blackboxes should be placed inside core 2. Partitions fences must be core

PTNASMD-780

NAME

PTNASMD-780

SUMMARY

Selected pin assignment: could not assign %d (out of %d) pins because feasible legal location was not found for following pins, need legal locations for pin to be assigned.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

2. Insert feedthrough buffers using the insertPtnFeedthrough command.

PTNASMD-882

NAME

PTNASMD-882

SUMMARY

The insertPtnFeedthrough command was invoked with the -routeBased option, but the design has not yet been routed. The insertPtnFeedthrough command will skip the nets that are not routed. Route the design using earlyGlobalRoute for these nets to be considered for feedthrough insertion.

DESCRIPTION

The insertPtnFeedthrough command invoked with the -routeBased option requires routing for the net to find a path based on which it will insert the feedthrough ports.

The net reported is not routed so it gets ignored. Route the design prior to running this command. The earlyGlobalRoute command can be used to route the design.

Otherwise insertPtnFeedthrough should be invoked without using the -routeBased option in which case the command will try to find a path for the net based on the floorplan and placement (placement based feedthrough insertion).

Example:

---

earlyGlobalRoute

insertPtnFeedthrough -routeBased.

PTNASMD-946

NAME

PTNASMD-946

SUMMARY

Pin named [%s] does not exist in cell [%s]. Ignoring the pin. Check and correct the pin name.

DESCRIPTION

Pin name specified for the specified partition does not exist. Check the pin name and partition name and correct accordingly. Problem could be case sensitivity. Command requires exact name which is case sensitive or incorrect manipulation of "alphabet l or numeric 1" "likewise "alphabet o and numeric 0"

Example:

Pin name could be "isCaseSensitive" but pin name supplied could be "iscasesensitive

PTNASMD-1211

NAME

PTNASMD-1211

SUMMARY

Specified layer [%s] is not within the allowed pin layer range [%s] and [%s] of the partition %s. Re-specify a valid pin layer value or change the partition definition to allow this pin layer and rerun the command again.

DESCRIPTION

Specified layer is not within the allowed pin layer range of the specified partition. Use the Partition->Specify Partition GUI to view the current specified allowed layers. Edit the current allowed pin layers of the partition to include this specified pin layer or re-specify pin layer and rerun the

command again.

PTNASMD-1250

NAME

PTNASMD-1250

SUMMARY

Pin placement has been enabled on metal layer 1.

DESCRIPTION

You have this message because you have enabled metal layer 1 for pin placement. However, metal layer 1 is generally reserved for follow pins. Make sure follow pins are already routed, to ensure that the pins do not block follow pins creation.

Example:

---

setDesignMode -bottomRoutingLayer 1 enables pins in M1

PTNASMD-1520

NAME

PTNASMD-1520

SUMMARY

Pin '%s' of %s '%s' cannot be placed at the constrained location [%0.2f %0.2f] due to a blocked pin slot close to the location. Placing the pin at location [%0.2f %0.2f].

DESCRIPTION

Pin slot can be blocked because of the following reasons

\t 1. pin blockages

\t 2. routing blockages

\t 3. Power ground routing

\t 4. availability of layers to put pins

PTNASMD-1521

NAME

PTNASMD-1521

SUMMARY

Unable to get any valid location for the constrained pin [%s] at location [%0.2f %0.2f].

DESCRIPTION

Pin slot can be blocked because of the following reasons

\t 1. pin blockages

\t 2. routing blockages

\t 3. Power ground routing

\t 4. availability of layers to put pins

PTNASMD-1550

NAME

PTNASMD-1550

SUMMARY

Cell [%s] cannot be specified as a black box because the design does not have any instance associated with this cell or instance may create nested blackBox. Ensure the design has an instance referenced to this cell or specify correct name of cell and rerun %s again.

DESCRIPTION

Specified cell cannot be defined as a black box because the design does not have any instance that is referenced to this cell or instance may create nested blackBox. Ensure there is at least one instance that is associated with this cell and rerun the command again.

PTNASMD-1669

NAME

PTNASMD-1669

SUMMARY

Ptn %s does not have any reserved slots for assigning ptn pins. Check the allowed layers for the partition and make sure that layers based on preferred routing tracks are reserved.

DESCRIPTION

This warning message is issued while assigning pins on a partition using the Innovus GUI with Partition => Assign Pin... or when using the assignPtnPin Tcl command.

The floorplan likely contains a problem with routing tracks and/or pin layer definitions. The problem can be debugged graphically using: Partition => Specify Partition

Select the offending partition and review the Partition Pin Layer Used section. Make sure the layers defined for pins are included in the Layers Reserved For Partition. Corrections may be made and applied with this form. Check the min max layer allowed though getDesignMode another reason could be presence of route blockage or PG on partition edge blocking the routing tracks.

Next, confirm there are preferred routing tracks defined for the pin layers using the Layer Control => Track => Pref Track and the Wire&Via layer defined for the pins. If the tracks are incorrect, they may be regenerated using the "generateTracks" Tcl command.

Example:

getPinConstraint -cell c -side all -layer

Constraint on partition c :

Allowed layer on side [top] : 2 4 6

Allowed layer on side [left] : 3 5

Allowed layer on side [bottom] : 2 4 6

Allowed layer on side [right] : 3 5

getDesignMode -bottomRoutingLayer -topRoutingLayer

-bottomRoutingLayer 2 # string, default=""

-topRoutingLayer 15 # string, default=""

{bottomRoutingLayer 2} {topRoutingLayer 15}

Look for the Tracks in a section with: Track:

While corrections can be made to the tmp.fp file and reloaded with the "loadFPlan tmp.fp" Tcl command, it is generally easier to do make changes with the Innovus GUI.

PTNASMD-1671

NAME

PTNASMD-1671

SUMMARY

The option %s cannot be used for updating pin attribute. Correct the command options and run the command again.

DESCRIPTION

Specified option cannot be used for just updating pin attribute. This option is used with other options for assigning pin location. Check the reference manual for the legal specified options. Then correct the command options and rerun the editPin command again.

PTNASMD-1699

NAME

PTNASMD-1699

SUMMARY

Selective-pin-assignment by specifying just partition name(s) to command assignPtnPin is obsolete and will be removed in future releases. The old usage still works in this release, but to avoid this warning and to ensure compatibility with future releases, replace the obsolete usage with "assignPtnPin -ptn -pin ".

DESCRIPTION

To avoid this warning and to ensure compatibility with future releases, replace the obsolete usage with 'assignPtnPin -ptn <ptnName> -pin <pinName>'

Example:

---

* The following command assign pins name starting with "in" of partition "A" and pins name starting with "out" of partition "B"

assignPtnPin -ptn {A} -pin {in*} -ptn {B} -pin {out*}

* The following command accept a file pinLst.txt that contains the list of pins to be placed for partition A and partition B.

assignPtnPin -ptn A -ptn B -pin_file pinLst.txt

PTNASMD-1704

NAME

PTNASMD-1704

SUMMARY

The options [-row] and [-bringBackRow] are obsolete. Rows are brought back automatically, without using any of these options. To avoid this warning and ensure compatibility with future releases, update your script to not use any of these options.

DESCRIPTION

This messages is issued when obsolete options are used.Using these options will have no impact in this case.

Example:

---

eg. use flattenPartition

PTNASMD-1717

NAME

PTNASMD-1717

SUMMARY

The specifyPartition command will be obsolete in the next release. Use the definePartition command to define the partitions.

DESCRIPTION

The message occurs because you are using 'specifyPartition' which is obsoletelease use the 'definePartition' command to define the partitions.

Example:

The following example defines a partition:

definePartition \

-hinst ctr_inst \

-coreSpacing 0.56 0.56 0.0 0.0 \

-railwidth 0.0 \

-minPitchLeft 2 \

-minPitchRight 2 \

-minPitchTop 2 \

-minPitchBottom 2 \

-reservedLayer {1 2 3 4} \

-pinLayerTop {2 4} \

-pinLayerLeft {3} \

-pinLayerBottom {2 4} \

-pinLayerRight {3} \

-placementHalo 1.0 1.0 1.0 1.0 \

-routingHalo 1.0 \

-routingHaloTopLayer 7 \

-routingHaloBottomLayer 1

PTNASMD-1755

NAME

PTNASMD-1755

SUMMARY

Pin [%s] of %s [%s] connected to net [%s] is [%s] at location (%8.3f, %8.3f) on layer %1d %s.

DESCRIPTION

Message reports specific error/violation on a partition pin.

Example of ABUTMENT violation on a pin:

Pin [pin_1] of partition [ptn_1] connected to net [net_1] is [PLACED] at location (210.452, 540.160) on layer 8 has ABUTMENT violation WITH partition chip.

In above example error/violation is being reported for partition “ptn_1” pin's “pin_1” which is connected to net “net_1” and is placed at location “210.452, 540.160” on layer “8” having assignment status as “placed”. Pin has abutment (is placed on adjoining boundary of “ptn_1” and “chip”) violation with partition named “chip”. Ideally the pin pair of two adjoining (abutting) partitions should be placed on same track on edge of partition boundaries, touching each other (abutting).

Abutment violation could be because of following two reasons:

1. Net has multi-partition-pins. Since all other pins of different partitions cannot be placed at same location (no electrical connection through any overlap of physical shape), so it is reported as abutment violation.

2. “pin_1” pin of net “net_1” is not connected to any pin of adjoining (abutted) partition “chip”.

List other violations on pin:

- pin min-width violation

- pin min-depth violation

- pin missing metal shape violation

- pin min-area violation
- pin-color violation
- pin not on routing track (or ndr-rule-routing-track) violation
- pin not on fence violation
- pin spacing (drc and spacing constraints) violation
- pin not on allowed layer violation
- For nested partition it checks for child fence area violation
- pin outside pin-guide or bus-guide violation
- Pin associated pin-group or net-group violation

PTNASMD-1802

NAME

PTNASMD-1802

SUMMARY

Route layer setting through routing modes [setRouteMode %s <value>] or [setNanoRouteMode %s <value>] setting will not be honored. Set the value using setDesignMode command [setDesignMode %s <value>] and run the command again.

DESCRIPTION

This message is reported related to IO pin routing if there are any IO pins falls above maxRouteLayer. Message ENCPTN-1802 is generated to correct the user expectation, when user had set either setRouteMode or setNanoRouteMode for minLayer but has missed to set setDesignMode for minLayer, and user would like to set min/max layer of pin that is different from earlyGlobalRoute. Innovus checks for this issue and generate the message as user may forget to set min/max layer of pin when it differs from earlyGlobalRoute.

Example:

Because of the following reason the ENCPTN-1802 is reported.

Message ENCPTN-1802 is generated to correct the user expectation, when user had set either setRouteMode or setNanoRouteMode for minLayer but has missed to set setDesignMode for minLayer.

Use "setDesignMode -topRoutingLayer <layer>" to placing IO pins, to avoid this problem.

PTNASMD-3207

NAME

PTNASMD-3207

SUMMARY

The hierarchical-PG net %s is connected to an instance term %s inside the partition hinst %s. However, it is not connected to any PG port of the partition hinst. This is erroneous data. As a consequence, instance term %s will become unconnected. To correct this error, ensure that the above net is connected to a partition PG port when connecting to an instance PG term inside the partition, and run the command again.

DESCRIPTION

Reason of such incorrect PG net connection is generally introduced by either incorrect UPF or incorrect GNC rule. To correct this error, ensure that the above net is connected to a partition PG port when connecting to an instance PG term inside partition. Or, if this connection is not needed inside the partition hinst, then ensure that the net does not connect to any of the PG terms inside the partition hinst.

PTNFEED-90

NAME

PTNFEED-90

SUMMARY

Pin %s of abutted partition %s could not be assigned. Could not find a feasible slot for the pin. Create more feasible location before for pin assignment by inserting feedthrough buffers using insertPtnFeedthrough command or allowing more layers for assigning pins or using setPinAssignMode -strict_abutment false or using setPinAssignMode -allow_unconnected_in_abutted_edge true for relaxing this check.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1 In abutted designs, pins of following type can not be placed on common edges between two adjoining partitions.

.in +2

A. Pins of net not connected to adjacent partition (fences of the two partitions being connected are not touching each other in floorplan).

B. Pins of nets having connections to two or more partitions any pin belonging to net of above type will have to route over an unconnected partition and result in illegal routing.

Feedthrough step is required to get rid of pins which connect non-adjacent partitions or multiple partitions, by changing netlist and making all pins connect to only one pin on adjacent partition to make the routing of net feasible/legal

C. Floating pins

.in

#2. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

#3. Use setPinAssignMode -strict_abutment false to relax abutment violations checks for placing multi partition pin of a net, non neighbor pins of a net and floating pins on abutted edges.

#4. Use setPinAssignMode -allow_unconnected_in_abutted_edge true to relax abutment violations checks for placing floating pins on abutted edges.

Example:

---

eg. if pins are not assigned for a net which has more than two partition pins to connect use insertPtnFeedthrough command to change netlist to have new nets added and older net modified in way that, now nets only connect two pins of adjacent partitions only.

PTNFEED-100

NAME

PTNFEED-100

SUMMARY

The net %s is not connected to any terminal. This net will not be considered for feedthrough buffer insertion. Correct the netlist to get this net considered for feedthrough buffer insertion.

DESCRIPTION

An unconnected net will not be considered for feedthrough insertion. The net should be connected to an output port and an input port to be considered for feedthrough insertion.

PTNFEED-233

NAME

PTNFEED-233

SUMMARY

No legal free slots available for %s of partition %s. Create additional slots using definePartition command or by removing blockage before pin assignment.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

PTNFEED-426

NAME

PTNFEED-426

SUMMARY

Adjusting partition %s core to left from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

This is happening because the core spacing values specified (I/O to core distance of partition block) are not multiple of placement grid. Same issue for IMPPTN-427, IMPPTN-428 and IMPPTN-429 based or the side.

Example:

<CMD> definePartition -hinst uCORE/uPKTSS/uPKTSS_PPCS_PMA_SYS -coreSpacing {2.7 2.7 1.9 1.9} -reservedLayer {1 2 3 4 5 6 7 8} -routingHalo 1.9 -routingHaloTopLayer 7 -routingHaloBottomLayer 1 -placementHalo {2.7 2.7 1.9 1.9} -railwidth 0.1 -minPitchLeft 3 -minPitchRight 3 -minPitchTop 3 -minPitchBottom 3 -pinLayerTop {3 5} -pinLayerBottom {3 5} -pinLayerLeft {4 6} -pinLayerRight {4 6}

Creating partition PKTSS_PPCS_PMA_SYS.

**WARN: (IMPPTN-426): Adjusting partition PKTSS_PPCS_PMA_SYS core to left from 1.900000 to 2.025000.

**WARN: (IMPPTN-427): Adjusting partition PKTSS_PPCS_PMA_SYS core to right from 1.900000 to 2.025000.

**WARN: (IMPPTN-428): Adjusting partition PKTSS_PPCS_PMA_SYS core to top from 2.700000 to 2.850000.

**WARN: (IMPPTN-429): Adjusting partition PKTSS_PPCS_PMA_SYS core to bottom from 2.700000 to 2.850000.

Placement grid is at 0.135 x-direction, 0.095 y-direction.

PTNFEED-427

NAME

PTNFEED-427

SUMMARY

Adjusting partition %s core to right from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

During partitioning, the warnings above are issued. How does Innovus determine these adjustments?

\t Innovus snaps the partition coreBox (area where rows are created and placement can be done) boundary to the placement grid. The remaining difference between coreBox and partition box is adjusted in core to right, core to top values.

Example:

**WARN: (IMPPTN-427): Adjusting partition lbrx_top_0 core to right from 0.000000 to 0.100000.

PTNFEED-428

NAME

PTNFEED-428

SUMMARY

Adjusting partition %s core to top from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

During partitioning, the warnings above are issued. How does Innovus determine these adjustments?

\t Innovus snaps the partition coreBox (area where rows are created and placement can be done) boundary to the placement grid. The remaining difference between coreBox and partition box is adjusted in core to right, core to top values.

Example:

**WARN: (IMPPTN-428): Adjusting partition lbrx_top_0 core to top from 0.000000 to 3.680000.

PTNFEED-429

NAME

PTNFEED-429

SUMMARY

Adjusting partition %s core to bottom from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

This is happening because the core spacing values specified (I/O to core distance of partition block) are not multiple of placement grid. Same issue for IMPPTN-427, IMPPTN-428 and IMPPTN-429 based or the side.

Example:

**WARN: (IMPPTN-429): Adjusting partition PKTSS_PPCS_PMA_SYS core to bottom from 2.700000 to 2.850000.

PTNFEED-555

NAME

PTNFEED-555

SUMMARY

A feasible legal location was not found for %d (out of %d) pins. Consequently, the following pins could not be assigned:

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

2. Insert feedthrough buffers using the insertPtnFeedthrough command.

PTNFEED-624

NAME

PTNFEED-624

SUMMARY

insertPtnFeedthrough could not find a path for net '%s' to reach '%s'. If the -topoFile option is being used, the topology specified for this net is incomplete.

DESCRIPTION

In case automatic feedthrough insertion is being done, it means that a path to some of the terminals could not be found. If the routeBased option is used, the routing may be incomplete. For the case the topology file is used an explanation follows.

Tool issues above warning during insertPtnFeedthrough command step, when topology file provided with -topoFile is used to guide the tool for creating the feedthrough in a specified partition for multi-fanout nets. You will get above warning if the topology file did not define for all the terminals for a multi-fanout net. Always follow the convention from_pin to to_pin for writing the topology file.

Example:

If the net goes to three partition A, B and C and you want to make a part of the net from A to D then to C, then you can use the following approach to write the topology file.

net n123

hinst-hinst A D;

hinst-hinst D C;

hinst-hinst A B;

end net

So, here all the combinations are covered where the net goes, instead of defining the A-D-C.

PTNFEED-646

NAME

PTNFEED-646

SUMMARY

insertPtnFeedthrough is trying to find a feedthrough path for net %s. It could not find a path to partition or terminal [%s]. Partitions connected to this net may not be adjacent to each other.

DESCRIPTION

Automatic feedthrough insertion derives the feedthrough topology using the placement. It assumes a channel-less design. The possibility of routing through channels is considered minimal. In this design a path to a partition or terminal connected to the above mentioned net could not be found without avoiding the channels.

PTNFEED-647

NAME

PTNFEED-647

SUMMARY

insertPtnFeedthrough skipping net [%s] because a path to some of the partitions or terminals could not be found. It might not be necessary to insert feedthrough buffers for this net. If you wish to insert feedthrough buffers for this net, then use the topology file for guided feedthrough buffer insertion or use the -routeBased option after routing the net.

DESCRIPTION

insertPtnFeedthrough assumes the design to be channel-less and partitions to be in the line of sight for feedthrough path to pass from one partition to another. In case of channel based designs where

this is not true, the named net is ignored. In case feedthrough insertion is required for the net, either route the design and used insertPtnFeedthrough -routeBased or define the path for the net in a topology file and use insertPtnFeedthrough -topoFile <filename>

Example:

---

earlyGlobalRoute

insertPtnFeedthrough -routeBased

Or

insertPtnFeedthrough -topoFile <filename>

PTNFEED-652

NAME

PTNFEED-652

SUMMARY

The pushdownBuffer command cannot create an instance with name [%s%s]. An instance with this name already exists in the design. Using default prefix and name [%s] for this instance.

DESCRIPTION

This message is issued if the pushdownBuffer uses the prefix provided with the -prefix option and the resulting name has a conflict with an existing instance name. No action needs to be taken as it will make another name with the default prefix.

PTNFEED-716

NAME

PTNFEED-716

SUMMARY

Partition %s constraint missing. Specify a Guide, Region, Fence constraint on the partition or place the blackbox instance.

DESCRIPTION

While committing partitions 1. Blackboxes should be placed inside core 2. Partitions fences must be core

PTNFEED-780

NAME

PTNFEED-780

SUMMARY

Selected pin assignment: could not assign %d (out of %d) pins because feasible legal location was not found for following pins, need legal locations for pin to be assigned.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

2. Insert feedthrough buffers using the insertPtnFeedthrough command.

PTNFEED-882

NAME

PTNFEED-882

SUMMARY

The insertPtnFeedthrough command was invoked with the -routeBased option, but the design has not yet been routed. The insertPtnFeedthrough command will skip the nets that are not routed. Route the design using earlyGlobalRoute for these nets to be considered for feedthrough insertion.

DESCRIPTION

The insertPtnFeedthrough command invoked with the -routeBased option requires routing for the net to find a path based on which it will insert the feedthrough ports.

The net reported is not routed so it gets ignored. Route the design prior to running this command. The earlyGlobalRoute command can be used to route the design.

Otherwise insertPtnFeedthrough should be invoked without using the -routeBased option in which case the command will try to find a path for the net based on the floorplan and placement (placement based feedthrough insertion).

Example:

---

earlyGlobalRoute

insertPtnFeedthrough -routeBased.

PTNFEED-946

NAME

PTNFEED-946

SUMMARY

Pin named [%s] does not exist in cell [%s]. Ignoring the pin. Check and correct the pin name.

DESCRIPTION

Pin name specified for the specified partition does not exist. Check the pin name and partition name and correct accordingly. Problem could be case sensitivity. Command requires exact name which is case sensitive or incorrect manipulation of "alphabet l or numeric 1" "likewise "alphabet o and numeric 0"

Example:

Pin name could be "isCaseSensitive" but pin name supplied could be "iscasesensitive

PTNFEED-1211

NAME

PTNFEED-1211

SUMMARY

Specified layer [%s] is not within the allowed pin layer range [%s] and [%s] of the partition %s. Re-specify a valid pin layer value or change the partition definition to allow this pin layer and rerun the command again.

DESCRIPTION

Specified layer is not within the allowed pin layer range of the specified partition. Use the Partition->Specify Partition GUI to view the current specified allowed layers. Edit the current allowed pin layers of the partition to include this specified pin layer or re-specify pin layer and rerun the

command again.

PTNFEED-1250

NAME

PTNFEED-1250

SUMMARY

Pin placement has been enabled on metal layer 1.

DESCRIPTION

You have this message because you have enabled metal layer 1 for pin placement. However, metal layer 1 is generally reserved for follow pins. Make sure follow pins are already routed, to ensure that the pins do not block follow pins creation.

Example:

---

setDesignMode -bottomRoutingLayer 1 enables pins in M1

PTNFEED-1520

NAME

PTNFEED-1520

SUMMARY

Pin '%s' of %s '%s' cannot be placed at the constrained location [%0.2f %0.2f] due to a blocked pin slot close to the location. Placing the pin at location [%0.2f %0.2f].

DESCRIPTION

Pin slot can be blocked because of the following reasons

\t 1. pin blockages

\t 2. routing blockages

\t 3. Power ground routing

\t 4. availability of layers to put pins

PTNFEED-1521

NAME

PTNFEED-1521

SUMMARY

Unable to get any valid location for the constrained pin [%s] at location [%0.2f %0.2f].

DESCRIPTION

Pin slot can be blocked because of the following reasons

\t 1. pin blockages

\t 2. routing blockages

\t 3. Power ground routing

\t 4. availability of layers to put pins

PTNFEED-1550

NAME

PTNFEED-1550

SUMMARY

Cell [%s] cannot be specified as a black box because the design does not have any instance associated with this cell or instance may create nested blackBox. Ensure the design has an instance referenced to this cell or specify correct name of cell and rerun %s again.

DESCRIPTION

Specified cell cannot be defined as a black box because the design does not have any instance that is referenced to this cell or instance may create nested blackBox. Ensure there is at least one instance that is associated with this cell and rerun the command again.

PTNFEED-1669

NAME

PTNFEED-1669

SUMMARY

Ptn %s does not have any reserved slots for assigning ptn pins. Check the allowed layers for the partition and make sure that layers based on preferred routing tracks are reserved.

DESCRIPTION

This warning message is issued while assigning pins on a partition using the Innovus GUI with Partition => Assign Pin... or when using the assignPtnPin Tcl command.

The floorplan likely contains a problem with routing tracks and/or pin layer definitions. The problem can be debugged graphically using: Partition => Specify Partition

Select the offending partition and review the Partition Pin Layer Used section. Make sure the layers defined for pins are included in the Layers Reserved For Partition. Corrections may be made and applied with this form. Check the min max layer allowed though getDesignMode another reason could be presence of route blockage or PG on partition edge blocking the routing tracks.

Next, confirm there are preferred routing tracks defined for the pin layers using the Layer Control =>

Track => Pref Track and the Wire&Via layer defined for the pins. If the tracks are incorrect, they may be regenerated using the "generateTracks" Tcl command.

Example:

getPinConstraint -cell c -side all -layer

Constraint on partition c :

Allowed layer on side [top] : 2 4 6

Allowed layer on side [left] : 3 5

Allowed layer on side [bottom] : 2 4 6

Allowed layer on side [right] : 3 5

getDesignMode -bottomRoutingLayer -topRoutingLayer

-bottomRoutingLayer 2 # string, default=""

-topRoutingLayer 15 # string, default=""

{bottomRoutingLayer 2} {topRoutingLayer 15}

Look for the Tracks in a section with: Track:

While corrections can be made to the tmp.fp file and reloaded with the "loadFPlan tmp.fp" Tcl command, it is generally easier to do make changes with the Innovus GUI.

PTNFEED-1671

NAME

PTNFEED-1671

SUMMARY

The option %s cannot be used for updating pin attribute. Correct the command options and run the command again.

DESCRIPTION

Specified option cannot be used for just updating pin attribute. This option is used with other options for assigning pin location. Check the reference manual for the legal specified options. Then

correct the command options and rerun the editPin command again.

PTNFEED-1699

NAME

PTNFEED-1699

SUMMARY

Selective-pin-assignment by specifying just partition name(s) to command assignPtnPin is obsolete and will be removed in future releases. The old usage still works in this release, but to avoid this warning and to ensure compatibility with future releases, replace the obsolete usage with "assignPtnPin -ptn -pin ".

DESCRIPTION

To avoid this warning and to ensure compatibility with future releases, replace the obsolete usage with 'assignPtnPin -ptn <ptnName> -pin <pinName>'

Example:

---

* The following command assign pins name starting with "in" of partition "A" and pins name starting with "out" of partition "B"

assignPtnPin -ptn {A} -pin {in*} -ptn {B} -pin {out*}

* The following command accept a file pinLst.txt that contains the list of pins to be placed for partition A and partition B.

assignPtnPin -ptn A -ptn B -pin_file pinLst.txt

PTNFEED-1704

NAME

PTNFEED-1704

SUMMARY

The options [-row] and [-bringBackRow] are obsolete. Rows are brought back automatically, without using any of these options. To avoid this warning and ensure compatibility with future releases, update your script to not use any of these options.

DESCRIPTION

This messages is issued when obsolete options are used.Using these options will have no impact in this case.

Example:

---

eg. use flattenPartition

PTNFEED-1717

NAME

PTNFEED-1717

SUMMARY

The specifyPartition command will be obsolete in the next release. Use the definePartition command to define the partitions.

DESCRIPTION

The message occurs because you are using 'specifyPartition' which is obsoletelease use the 'definePartition' command to define the partitions.

Example:

The following example defines a partition:

definePartition \

-hinst ctr_inst \

```
-coreSpacing 0.56 0.56 0.0 0.0 \
-railwidth 0.0 \
-minPitchLeft 2 \
-minPitchRight 2 \
-minPitchTop 2 \
-minPitchBottom 2 \
-reservedLayer {1 2 3 4} \
-pinLayerTop {2 4} \
-pinLayerLeft {3} \
-pinLayerBottom {2 4} \
-pinLayerRight {3} \
-placementHalo 1.0 1.0 1.0 1.0 \
-routingHalo 1.0 \
-routingHaloTopLayer 7 \
-routingHaloBottomLayer 1
```

PTNFEED-1755

NAME

PTNFEED-1755

SUMMARY

Pin [%s] of %s [%s] connected to net [%s] is [%s] at location (%8.3f, %8.3f) on layer %1d %s.

DESCRIPTION

Message reports specific error/violation on a partition pin.

Example of ABUTMENT violation on a pin:

Pin [pin_1] of partition [ptn_1] connected to net [net_1] is [PLACED] at location (210.452, 540.160) on layer 8 has ABUTMENT violation WITH partition chip.

In above example error/violation is being reported for partition “ptn_1” pin's “pin_1” which is connected to net “net_1” and is placed at location “210.452, 540.160” on layer “8” having assignment status as “placed”. Pin has abutment (is placed on adjoining boundary of “ptn_1” and “chip”) violation with partition named “chip”. Ideally the pin pair of two adjoining (abutting) partitions should be placed on same track on edge of partition boundaries, touching each other (abutting).

Abutment violation could be because of following two reasons:

1. Net has multi-partition-pins. Since all other pins of different partitions cannot be placed at same location (no electrical connection through any overlap of physical shape), so it is reported as abutment violation.

2. “pin_1” pin of net “net_1” is not connected to any pin of adjoining (abutted) partition “chip”.

List other violations on pin:

- pin min-width violation
- pin min-depth violation
- pin missing metal shape violation
- pin min-area violation
- pin-color violation
- pin not on routing track (or ndr-rule-routing-track) violation
- pin not on fence violation
- pin spacing (drc and spacing constraints) violation
- pin not on allowed layer violation
- For nested partition it checks for child fence area violation
- pin outside pin-guide or bus-guide violation
- Pin associated pin-group or net-group violation

PTNFEED-1802

NAME

PTNFEED-1802

SUMMARY

Route layer setting through routing modes [setRouteMode %s <value>] or [setNanoRouteMode %s <value>] setting will not be honored. Set the value using setDesignMode command [setDesignMode %s <value>] and run the command again.

DESCRIPTION

This message is reported related to IO pin routing if there are any IO pins falls above maxRouteLayer. Message ENCPTN-1802 is generated to correct the user expectation, when user had set either setRouteMode or setNanoRouteMode for minLayer but has missed to set setDesignMode for minLayer, and user would like to set min/max layer of pin that is different from earlyGlobalRoute. Innovus checks for this issue and generate the message as user may forget to set min/max layer of pin when it differs from earlyGlobalRoute.

Example:

Because of the following reason the ENCPTN-1802 is reported.

Message ENCPTN-1802 is generated to correct the user expectation, when user had set either setRouteMode or setNanoRouteMode for minLayer but has missed to set setDesignMode for minLayer.

Use "setDesignMode -topRoutingLayer <layer>" to placing IO pins, to avoid this problem.

PTNFEED-3207

NAME

PTNFEED-3207

SUMMARY

The hierarchical-PG net %s is connected to an instance term %s inside the partition hinst %s. However, it is not connected to any PG port of the partition hinst. This is erroneous data. As a consequence, instance term %s will become unconnected. To correct this error, ensure that the above net is connected to a partition PG port when connecting to an instance PG term inside the partition, and run the command again.

DESCRIPTION

Reason of such incorrect PG net connection is generally introduced by either incorrect UPF or incorrect GNC rule. To correct this error, ensure that the above net is connected to a partition PG port when connecting to an instance PG term inside partition. Or, if this connection is not needed inside the partition hinst, then ensure that the net does not connect to any of the PG terms inside the partition hinst.

PTNPART-90

NAME

PTNPART-90

SUMMARY

Pin %s of abutted partition %s could not be assigned. Could not find a feasible slot for the pin. Create more feasible location before for pin assignment by inserting feedthrough buffers using insertPtnFeedthrough command or allowing more layers for assigning pins or using setPinAssignMode -strict_abutment false or using setPinAssignMode -allow_unconnected_in_abutted_edge true for relaxing this check.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1 In abutted designs, pins of following type can not be placed on common edges between two adjoining partitions.

.in +2

A. Pins of net not connected to adjacent partition (fences of the two partitions being connected are not touching each other in floorplan).

B. Pins of nets having connections to two or more partitions any pin belonging to net of above type will have to route over an unconnected partition and result in illegal routing.

Feedthrough step is required to get rid of pins which connect non-adjacent partitions or multiple partitions, by changing netlist and making all pins connect to only one pin on adjacent partition to make the routing of net feasible/legal

C. Floating pins

.in

#2. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

#3. Use setPinAssignMode -strict_abutment false to relax abutment violations checks for placing multi partition pin of a net, non neighbor pins of a net and floating pins on abutted edges.

#4. Use setPinAssignMode -allow_unconnected_in_abutted_edge true to relax abutment violations checks for placing floating pins on abutted edges.

Example:

---

eg. if pins are not assigned for a net which has more than two partition pins to connect use insertPtnFeedthrough command to change netlist to have new nets added and older net modified in way that, now nets only connect two pins of adjacent partitions only.

PTNPART-100

NAME

PTNPART-100

SUMMARY

The net %s is not connected to any terminal. This net will not be considered for feedthrough buffer insertion. Correct the netlist to get this net considered for feedthrough buffer insertion.

DESCRIPTION

An unconnected net will not be considered for feedthrough insertion. The net should be connected to an output port and an input port to be considered for feedthrough insertion.

PTNPART-233

NAME

PTNPART-233

SUMMARY

No legal free slots available for %s of partition %s. Create additional slots using definePartition command or by removing blockage before pin assignment.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

PTNPART-426

NAME

PTNPART-426

SUMMARY

Adjusting partition %s core to left from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

This is happening because the core spacing values specified (I/O to core distance of partition block) are not multiple of placement grid. Same issue for IMPPTN-427, IMPPTN-428 and IMPPTN-429 based or the side.

Example:

<CMD> definePartition -hinst uCORE/uPKTSS/uPKTSS_PPCS_PMA_SYS -coreSpacing {2.7 2.7 1.9 1.9} -reservedLayer {1 2 3 4 5 6 7 8} -routingHalo 1.9 -routingHaloTopLayer 7 -routingHaloBottomLayer 1 -placementHalo {2.7 2.7 1.9 1.9} -railwidth 0.1 -minPitchLeft 3 -minPitchRight 3 -minPitchTop 3 -minPitchBottom 3 -pinLayerTop {3 5} -pinLayerBottom {3 5} -pinLayerLeft {4 6} -pinLayerRight {4 6}

Creating partition PKTSS_PPCS_PMA_SYS.

**WARN: (IMPPTN-426): Adjusting partition PKTSS_PPCS_PMA_SYS core to left from 1.900000 to 2.025000.

**WARN: (IMPPTN-427): Adjusting partition PKTSS_PPCS_PMA_SYS core to right from 1.900000 to 2.025000.

**WARN: (IMPPTN-428): Adjusting partition PKTSS_PPCS_PMA_SYS core to top from 2.700000 to 2.850000.

**WARN: (IMPPTN-429): Adjusting partition PKTSS_PPCS_PMA_SYS core to bottom from 2.700000 to 2.850000.

Placement grid is at 0.135 x-direction, 0.095 y-direction.

PTNPART-427

NAME

PTNPART-427

SUMMARY

Adjusting partition %s core to right from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

During partitioning, the warnings above are issued. How does Innovus determine these adjustments?

\t Innovus snaps the partition coreBox (area where rows are created and placement can be done) boundary to the placement grid. The remaining difference between coreBox and partition box is adjusted in core to right, core to top values.

Example:

**WARN: (IMPPTN-427): Adjusting partition lbrx_top_0 core to right from 0.000000 to 0.100000.

PTNPART-428

NAME

PTNPART-428

SUMMARY

Adjusting partition %s core to top from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

During partitioning, the warnings above are issued. How does Innovus determine these adjustments?

\t Innovus snaps the partition coreBox (area where rows are created and placement can be done) boundary to the placement grid. The remaining difference between coreBox and partition box is adjusted in core to right, core to top values.

Example:

**WARN: (IMPPTN-428): Adjusting partition lbrx_top_0 core to top from 0.000000 to 3.680000.

PTNPART-429

NAME

PTNPART-429

SUMMARY

Adjusting partition %s core to bottom from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

This is happening because the core spacing values specified (I/O to core distance of partition block) are not multiple of placement grid. Same issue for IMPPTN-427, IMPPTN-428 and IMPPTN-429 based or the side.

Example:

**WARN: (IMPPTN-429): Adjusting partition PKTSS_PPCS_PMA_SYS core to bottom from 2.700000 to 2.850000.

PTNPART-555

NAME

PTNPART-555

SUMMARY

A feasible legal location was not found for %d (out of %d) pins. Consequently, the following pins could not be assigned:

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

2. Insert feedthrough buffers using the insertPtnFeedthrough command.

PTNPART-624

NAME

PTNPART-624

SUMMARY

insertPtnFeedthrough could not find a path for net '%s' to reach '%s'. If the -topoFile option is being used, the topology specified for this net is incomplete.

DESCRIPTION

In case automatic feedthrough insertion is being done, it means that a path to some of the terminals could not be found. If the routeBased option is used, the routing may be incomplete. For the case the topology file is used an explanation follows.

Tool issues above warning during insertPtnFeedthrough command step, when topology file provided with -topoFile is used to guide the tool for creating the feedthrough in a specified partition for multi-fanout nets. You will get above warning if the topology file did not define for all the terminals for a multi-fanout net. Always follow the convention from_pin to to_pin for writing the topology file.

Example:

If the net goes to three partition A, B and C and you want to make a part of the net from A to D then to C, then you can use the following approach to write the topology file.

net n123

hinst-hinst A D;

hinst-hinst D C;

hinst-hinst A B;

end net

So, here all the combinations are covered where the net goes, instead of defining the A-D-C.

PTNPART-646

NAME

PTNPART-646

SUMMARY

insertPtnFeedthrough is trying to find a feedthrough path for net %s. It could not find a path to partition or terminal [%s]. Partitions connected to this net may not be adjacent to each other.

DESCRIPTION

Automatic feedthrough insertion derives the feedthrough topology using the placement. It assumes a channel-less design. The possibility of routing through channels is considered minimal. In this design a path to a partition or terminal connected to the above mentioned net could not be found without avoiding the channels.

PTNPART-647

NAME

PTNPART-647

SUMMARY

insertPtnFeedthrough skipping net [%s] because a path to some of the partitions or terminals could not be found. It might not be necessary to insert feedthrough buffers for this net. If you wish to insert feedthrough buffers for this net, then use the topology file for guided feedthrough buffer insertion or use the -routeBased option after routing the net.

DESCRIPTION

insertPtnFeedthrough assumes the design to be channel-less and partitions to be in the line of sight for feedthrough path to pass from one partition to another. In case of channel based designs where this is not true, the named net is ignored. In case feedthrough insertion is required for the net, either route the design and used insertPtnFeedthrough -routeBased or define the path for the net in a topology file and use insertPtnFeedthrough -topoFile <filename>

Example:

---

earlyGlobalRoute

insertPtnFeedthrough -routeBased

Or

insertPtnFeedthrough -topoFile <filename>

PTNPART-652

NAME

PTNPART-652

SUMMARY

The pushdownBuffer command cannot create an instance with name [%s%s]. An instance with this name already exists in the design. Using default prefix and name [%s] for this instance.

DESCRIPTION

This message is issued if the pushdownBuffer uses the prefix provided with the -prefix option and the resulting name has a conflict with an existing instance name. No action needs to be taken as it will make another name with the default prefix.

PTNPART-716

NAME

PTNPART-716

SUMMARY

Partition %s constraint missing. Specify a Guide, Region, Fence constraint on the partition or place the blackbox instance.

DESCRIPTION

While committing partitions 1. Blackboxes should be placed inside core 2. Partitions fences must be core

PTNPART-780

NAME

PTNPART-780

SUMMARY

Selected pin assignment: could not assign %d (out of %d) pins because feasible legal location was not found for following pins, need legal locations for pin to be assigned.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

2. Insert feedthrough buffers using the insertPtnFeedthrough command.

PTNPART-882

NAME

PTNPART-882

SUMMARY

The insertPtnFeedthrough command was invoked with the -routeBased option, but the design has not yet been routed. The insertPtnFeedthrough command will skip the nets that are not routed. Route the design using earlyGlobalRoute for these nets to be considered for feedthrough insertion.

DESCRIPTION

The insertPtnFeedthrough command invoked with the -routeBased option requires routing for the net to find a path based on which it will insert the feedthrough ports.

The net reported is not routed so it gets ignored. Route the design prior to running this command. The earlyGlobalRoute command can be used to route the design.

Otherwise insertPtnFeedthrough should be invoked without using the -routeBased option in which case the command will try to find a path for the net based on the floorplan and placement (placement based feedthrough insertion).

Example:

---

earlyGlobalRoute

insertPtnFeedthrough -routeBased.

PTNPART-946

NAME

PTNPART-946

SUMMARY

Pin named [%s] does not exist in cell [%s]. Ignoring the pin. Check and correct the pin name.

DESCRIPTION

Pin name specified for the specified partition does not exist. Check the pin name and partition name and correct accordingly. Problem could be case sensitivity. Command requires exact name which is case sensitive or incorrect manipulation of "alphabet l or numeric 1" "likewise "alphabet o and numeric 0"

Example:

Pin name could be "isCaseSensitive" but pin name supplied could be "iscasesensitive

PTNPART-1211

NAME

PTNPART-1211

SUMMARY

Specified layer [%s] is not within the allowed pin layer range [%s] and [%s] of the partition %s. Re-specify a valid pin layer value or change the partition definition to allow this pin layer and rerun the command again.

DESCRIPTION

Specified layer is not within the allowed pin layer range of the specified partition. Use the Partition->Specify Partition GUI to view the current specified allowed layers. Edit the current allowed pin layers of the partition to include this specified pin layer or re-specify pin layer and rerun the

command again.

PTNPART-1250

NAME

PTNPART-1250

SUMMARY

Pin placement has been enabled on metal layer 1.

DESCRIPTION

You have this message because you have enabled metal layer 1 for pin placement. However, metal layer 1 is generally reserved for follow pins. Make sure follow pins are already routed, to ensure that the pins do not block follow pins creation.

Example:

---

setDesignMode -bottomRoutingLayer 1 enables pins in M1

PTNPART-1520

NAME

PTNPART-1520

SUMMARY

Pin '%s' of %s '%s' cannot be placed at the constrained location [%0.2f %0.2f] due to a blocked pin slot close to the location. Placing the pin at location [%0.2f %0.2f].

DESCRIPTION

Pin slot can be blocked because of the following reasons

\t 1. pin blockages

\t 2. routing blockages

\t 3. Power ground routing

\t 4. availability of layers to put pins

PTNPART-1521

NAME

PTNPART-1521

SUMMARY

Unable to get any valid location for the constrained pin [%s] at location [%0.2f %0.2f].

DESCRIPTION

Pin slot can be blocked because of the following reasons

\t 1. pin blockages

\t 2. routing blockages

\t 3. Power ground routing

\t 4. availability of layers to put pins

PTNPART-1550

NAME

PTNPART-1550

SUMMARY

Cell [%s] cannot be specified as a black box because the design does not have any instance associated with this cell or instance may create nested blackBox. Ensure the design has an instance referenced to this cell or specify correct name of cell and rerun %s again.

DESCRIPTION

Specified cell cannot be defined as a black box because the design does not have any instance that is referenced to this cell or instance may create nested blackBox. Ensure there is at least one instance that is associated with this cell and rerun the command again.

PTNPART-1669

NAME

PTNPART-1669

SUMMARY

Ptn %s does not have any reserved slots for assigning ptn pins. Check the allowed layers for the partition and make sure that layers based on preferred routing tracks are reserved.

DESCRIPTION

This warning message is issued while assigning pins on a partition using the Innovus GUI with Partition => Assign Pin... or when using the assignPtnPin Tcl command.

The floorplan likely contains a problem with routing tracks and/or pin layer definitions. The problem can be debugged graphically using: Partition => Specify Partition

Select the offending partition and review the Partition Pin Layer Used section. Make sure the layers defined for pins are included in the Layers Reserved For Partition. Corrections may be made and applied with this form. Check the min max layer allowed though getDesignMode another reason could be presence of route blockage or PG on partition edge blocking the routing tracks.

Next, confirm there are preferred routing tracks defined for the pin layers using the Layer Control => Track => Pref Track and the Wire&Via layer defined for the pins. If the tracks are incorrect, they may be regenerated using the "generateTracks" Tcl command.

Example:

getPinConstraint -cell c -side all -layer

Constraint on partition c :

Allowed layer on side [top] : 2 4 6

Allowed layer on side [left] : 3 5

Allowed layer on side [bottom] : 2 4 6

Allowed layer on side [right] : 3 5

getDesignMode -bottomRoutingLayer -topRoutingLayer

-bottomRoutingLayer 2 # string, default=""

-topRoutingLayer 15 # string, default=""

{bottomRoutingLayer 2} {topRoutingLayer 15}

Look for the Tracks in a section with: Track:

While corrections can be made to the tmp.fp file and reloaded with the "loadFPlan tmp.fp" Tcl command, it is generally easier to do make changes with the Innovus GUI.

PTNPART-1671

NAME

PTNPART-1671

SUMMARY

The option %s cannot be used for updating pin attribute. Correct the command options and run the command again.

DESCRIPTION

Specified option cannot be used for just updating pin attribute. This option is used with other options for assigning pin location. Check the reference manual for the legal specified options. Then correct the command options and rerun the editPin command again.

PTNPART-1699

NAME

PTNPART-1699

SUMMARY

Selective-pin-assignment by specifying just partition name(s) to command assignPtnPin is obsolete and will be removed in future releases. The old usage still works in this release, but to avoid this warning and to ensure compatibility with future releases, replace the obsolete usage with "assignPtnPin -ptn -pin ".

DESCRIPTION

To avoid this warning and to ensure compatibility with future releases, replace the obsolete usage with 'assignPtnPin -ptn <ptnName> -pin <pinName>'

Example:

---

* The following command assign pins name starting with "in" of partition "A" and pins name starting with "out" of partition "B"

assignPtnPin -ptn {A} -pin {in*} -ptn {B} -pin {out*}

* The following command accept a file pinLst.txt that contains the list of pins to be placed for partition A and partition B.

assignPtnPin -ptn A -ptn B -pin_file pinLst.txt

PTNPART-1704

NAME

PTNPART-1704

SUMMARY

The options [-row] and [-bringBackRow] are obsolete. Rows are brought back automatically, without using any of these options. To avoid this warning and ensure compatibility with future releases, update your script to not use any of these options.

DESCRIPTION

This messages is issued when obsolete options are used.Using these options will have no impact in this case.

Example:

---

eg. use flattenPartition

PTNPART-1717

NAME

PTNPART-1717

SUMMARY

The specifyPartition command will be obsolete in the next release. Use the definePartition command to define the partitions.

DESCRIPTION

The message occurs because you are using 'specifyPartition' which is obsoletelease use the 'definePartition' command to define the partitions.

Example:

The following example defines a partition:

definePartition \

-hinst ctr_inst \

-coreSpacing 0.56 0.56 0.0 0.0 \

-railwidth 0.0 \

-minPitchLeft 2 \

-minPitchRight 2 \

-minPitchTop 2 \

-minPitchBottom 2 \

-reservedLayer {1 2 3 4} \

-pinLayerTop {2 4} \

-pinLayerLeft {3} \

-pinLayerBottom {2 4} \

-pinLayerRight {3} \

-placementHalo 1.0 1.0 1.0 1.0 \

-routingHalo 1.0 \

-routingHaloTopLayer 7 \

-routingHaloBottomLayer 1

PTNPART-1755

NAME

PTNPART-1755

SUMMARY

Pin [%s] of %s [%s] connected to net [%s] is [%s] at location (%8.3f, %8.3f) on layer %1d %s.

DESCRIPTION

Message reports specific error/violation on a partition pin.

Example of ABUTMENT violation on a pin:

Pin [pin_1] of partition [ptn_1] connected to net [net_1] is [PLACED] at location (210.452, 540.160) on layer 8 has ABUTMENT violation WITH partition chip.

In above example error/violation is being reported for partition “ptn_1” pin's “pin_1” which is connected to net “net_1” and is placed at location “210.452, 540.160” on layer “8” having assignment status as “placed”. Pin has abutment (is placed on adjoining boundary of “ptn_1” and “chip”) violation with partition named “chip”. Ideally the pin pair of two adjoining (abutting) partitions should be placed on same track on edge of partition boundaries, touching each other (abutting).

Abutment violation could be because of following two reasons:

1. Net has multi-partition-pins. Since all other pins of different partitions cannot be placed at same location (no electrical connection through any overlap of physical shape), so it is reported as abutment violation.

2. “pin_1” pin of net “net_1” is not connected to any pin of adjoining (abutted) partition “chip”.

List other violations on pin:

- pin min-width violation

- pin min-depth violation

- pin missing metal shape violation

- pin min-area violation
- pin-color violation
- pin not on routing track (or ndr-rule-routing-track) violation
- pin not on fence violation
- pin spacing (drc and spacing constraints) violation
- pin not on allowed layer violation
- For nested partition it checks for child fence area violation
- pin outside pin-guide or bus-guide violation
- Pin associated pin-group or net-group violation

PTNPART-1802

NAME

PTNPART-1802

SUMMARY

Route layer setting through routing modes [setRouteMode %s <value>] or [setNanoRouteMode %s <value>] setting will not be honored. Set the value using setDesignMode command [setDesignMode %s <value>] and run the command again.

DESCRIPTION

This message is reported related to IO pin routing if there are any IO pins falls above maxRouteLayer. Message ENCPTN-1802 is generated to correct the user expectation, when user had set either setRouteMode or setNanoRouteMode for minLayer but has missed to set setDesignMode for minLayer, and user would like to set min/max layer of pin that is different from earlyGlobalRoute. Innovus checks for this issue and generate the message as user may forget to set min/max layer of pin when it differs from earlyGlobalRoute.

Example:

Because of the following reason the ENCPTN-1802 is reported.

Message ENCPTN-1802 is generated to correct the user expectation, when user had set either setRouteMode or setNanoRouteMode for minLayer but has missed to set setDesignMode for minLayer.

Use "setDesignMode -topRoutingLayer <layer>" to placing IO pins, to avoid this problem.

PTNPART-3207

NAME

PTNPART-3207

SUMMARY

The hierarchical-PG net %s is connected to an instance term %s inside the partition hinst %s. However, it is not connected to any PG port of the partition hinst. This is erroneous data. As a consequence, instance term %s will become unconnected. To correct this error, ensure that the above net is connected to a partition PG port when connecting to an instance PG term inside the partition, and run the command again.

DESCRIPTION

Reason of such incorrect PG net connection is generally introduced by either incorrect UPF or incorrect GNC rule. To correct this error, ensure that the above net is connected to a partition PG port when connecting to an instance PG term inside partition. Or, if this connection is not needed inside the partition hinst, then ensure that the net does not connect to any of the PG terms inside the partition hinst.

PTNPIN-90

NAME

PTNPIN-90

SUMMARY

Pin %s of abutted partition %s could not be assigned. Could not find a feasible slot for the pin. Create more feasible location before for pin assignment by inserting feedthrough buffers using insertPtnFeedthrough command or allowing more layers for assigning pins or using setPinAssignMode -strict_abutment false or using setPinAssignMode -allow_unconnected_in_abutted_edge true for relaxing this check.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1 In abutted designs, pins of following type can not be placed on common edges between two adjoining partitions.

.in +2

A. Pins of net not connected to adjacent partition (fences of the two partitions being connected are not touching each other in floorplan).

B. Pins of nets having connections to two or more partitions any pin belonging to net of above type will have to route over an unconnected partition and result in illegal routing.

Feedthrough step is required to get rid of pins which connect non-adjacent partitions or multiple partitions, by changing netlist and making all pins connect to only one pin on adjacent partition to make the routing of net feasible/legal

C. Floating pins

.in

#2. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

#3. Use setPinAssignMode -strict_abutment false to relax abutment violations checks for placing multi partition pin of a net, non neighbor pins of a net and floating pins on abutted edges.

#4. Use setPinAssignMode -allow_unconnected_in_abutted_edge true to relax abutment violations checks for placing floating pins on abutted edges.

Example:

---

eg. if pins are not assigned for a net which has more than two partition pins to connect use insertPtnFeedthrough command to change netlist to have new nets added and older net modified in way that, now nets only connect two pins of adjacent partitions only.

PTNPIN-100

NAME

PTNPIN-100

SUMMARY

The net %s is not connected to any terminal. This net will not be considered for feedthrough buffer insertion. Correct the netlist to get this net considered for feedthrough buffer insertion.

DESCRIPTION

An unconnected net will not be considered for feedthrough insertion. The net should be connected to an output port and an input port to be considered for feedthrough insertion.

PTNPIN-233

NAME

PTNPIN-233

SUMMARY

No legal free slots available for %s of partition %s. Create additional slots using definePartition command or by removing blockage before pin assignment.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

PTNPIN-426

NAME

PTNPIN-426

SUMMARY

Adjusting partition %s core to left from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

This is happening because the core spacing values specified (I/O to core distance of partition block) are not multiple of placement grid. Same issue for IMPPTN-427, IMPPTN-428 and IMPPTN-429 based or the side.

Example:

<CMD> definePartition -hinst uCORE/uPKTSS/uPKTSS_PPCS_PMA_SYS -coreSpacing {2.7 2.7 1.9 1.9} -reservedLayer {1 2 3 4 5 6 7 8} -routingHalo 1.9 -routingHaloTopLayer 7 -routingHaloBottomLayer 1 -placementHalo {2.7 2.7 1.9 1.9} -railwidth 0.1 -minPitchLeft 3 -minPitchRight 3 -minPitchTop 3 -minPitchBottom 3 -pinLayerTop {3 5} -pinLayerBottom {3 5} -pinLayerLeft {4 6} -pinLayerRight {4 6}

Creating partition PKTSS_PPCS_PMA_SYS.

**WARN: (IMPPTN-426): Adjusting partition PKTSS_PPCS_PMA_SYS core to left from 1.900000 to 2.025000.

**WARN: (IMPPTN-427): Adjusting partition PKTSS_PPCS_PMA_SYS core to right from 1.900000 to 2.025000.

**WARN: (IMPPTN-428): Adjusting partition PKTSS_PPCS_PMA_SYS core to top from 2.700000 to 2.850000.

**WARN: (IMPPTN-429): Adjusting partition PKTSS_PPCS_PMA_SYS core to bottom from 2.700000 to 2.850000.

Placement grid is at 0.135 x-direction, 0.095 y-direction.

PTNPIN-427

NAME

PTNPIN-427

SUMMARY

Adjusting partition %s core to right from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

During partitioning, the warnings above are issued. How does Innovus determine these adjustments?

\t Innovus snaps the partition coreBox (area where rows are created and placement can be done) boundary to the placement grid. The remaining difference between coreBox and partition box is adjusted in core to right, core to top values.

Example:

**WARN: (IMPPTN-427): Adjusting partition lbrx_top_0 core to right from 0.000000 to 0.100000.

PTNPIN-428

NAME

PTNPIN-428

SUMMARY

Adjusting partition %s core to top from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

During partitioning, the warnings above are issued. How does Innovus determine these adjustments?

\t Innovus snaps the partition coreBox (area where rows are created and placement can be done) boundary to the placement grid. The remaining difference between coreBox and partition box is adjusted in core to right, core to top values.

Example:

**WARN: (IMPPTN-428): Adjusting partition lbrx_top_0 core to top from 0.000000 to 3.680000.

PTNPIN-429

NAME

PTNPIN-429

SUMMARY

Adjusting partition %s core to bottom from %f to %f because specified core spacing value is not multiple of placement grid.

DESCRIPTION

This is happening because the core spacing values specified (I/O to core distance of partition block) are not multiple of placement grid. Same issue for IMPPTN-427, IMPPTN-428 and IMPPTN-429 based or the side.

Example:

**WARN: (IMPPTN-429): Adjusting partition PKTSS_PPCS_PMA_SYS core to bottom from 2.700000 to 2.850000.

PTNPIN-555

NAME

PTNPIN-555

SUMMARY

A feasible legal location was not found for %d (out of %d) pins. Consequently, the following pins could not be assigned:

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

2. Insert feedthrough buffers using the insertPtnFeedthrough command.

PTNPIN-624

NAME

PTNPIN-624

SUMMARY

insertPtnFeedthrough could not find a path for net '%s' to reach '%s'. If the -topoFile option is being used, the topology specified for this net is incomplete.

DESCRIPTION

In case automatic feedthrough insertion is being done, it means that a path to some of the terminals could not be found. If the routeBased option is used, the routing may be incomplete. For the case the topology file is used an explanation follows.

Tool issues above warning during insertPtnFeedthrough command step, when topology file provided with -topoFile is used to guide the tool for creating the feedthrough in a specified partition for multi-fanout nets. You will get above warning if the topology file did not define for all the terminals for a multi-fanout net. Always follow the convention from_pin to to_pin for writing the topology file.

Example:

If the net goes to three partition A, B and C and you want to make a part of the net from A to D then to C, then you can use the following approach to write the topology file.

net n123

hinst-hinst A D;

hinst-hinst D C;

hinst-hinst A B;

end net

So, here all the combinations are covered where the net goes, instead of defining the A-D-C.

PTNPIN-646

NAME

PTNPIN-646

SUMMARY

insertPtnFeedthrough is trying to find a feedthrough path for net %s. It could not find a path to partition or terminal [%s]. Partitions connected to this net may not be adjacent to each other.

DESCRIPTION

Automatic feedthrough insertion derives the feedthrough topology using the placement. It assumes a channel-less design. The possibility of routing through channels is considered minimal. In this design a path to a partition or terminal connected to the above mentioned net could not be found without avoiding the channels.

PTNPIN-647

NAME

PTNPIN-647

SUMMARY

insertPtnFeedthrough skipping net [%s] because a path to some of the partitions or terminals could not be found. It might not be necessary to insert feedthrough buffers for this net. If you wish to insert feedthrough buffers for this net, then use the topology file for guided feedthrough buffer insertion or use the -routeBased option after routing the net.

DESCRIPTION

insertPtnFeedthrough assumes the design to be channel-less and partitions to be in the line of sight for feedthrough path to pass from one partition to another. In case of channel based designs where

this is not true, the named net is ignored. In case feedthrough insertion is required for the net, either route the design and used insertPtnFeedthrough -routeBased or define the path for the net in a topology file and use insertPtnFeedthrough -topoFile <filename>

Example:

---

earlyGlobalRoute

insertPtnFeedthrough -routeBased

Or

insertPtnFeedthrough -topoFile <filename>

PTNPIN-652

NAME

PTNPIN-652

SUMMARY

The pushdownBuffer command cannot create an instance with name [%s%s]. An instance with this name already exists in the design. Using default prefix and name [%s] for this instance.

DESCRIPTION

This message is issued if the pushdownBuffer uses the prefix provided with the -prefix option and the resulting name has a conflict with an existing instance name. No action needs to be taken as it will make another name with the default prefix.

PTNPIN-716

NAME

PTNPIN-716

SUMMARY

Partition %s constraint missing. Specify a Guide, Region, Fence constraint on the partition or place the blackbox instance.

DESCRIPTION

While committing partitions 1. Blackboxes should be placed inside core 2. Partitions fences must be core

PTNPIN-780

NAME

PTNPIN-780

SUMMARY

Selected pin assignment: could not assign %d (out of %d) pins because feasible legal location was not found for following pins, need legal locations for pin to be assigned.

DESCRIPTION

In order to resolve this issue, do the following before pin assignment:

#1. Create additional location for pins

.in +2

A. By removing blockages

B. By removing PG stripes

C. Allow more layers for pin assignment

.in

.in +4

i. By using the definePartition command to allow more layers

ii. By choosing higher layer for setDesignMode -topRoutingLayer

iii. By removing constraints on the pin using unsetPinConstraint command

.in

2. Insert feedthrough buffers using the insertPtnFeedthrough command.

PTNPIN-882

NAME

PTNPIN-882

SUMMARY

The insertPtnFeedthrough command was invoked with the -routeBased option, but the design has not yet been routed. The insertPtnFeedthrough command will skip the nets that are not routed. Route the design using earlyGlobalRoute for these nets to be considered for feedthrough insertion.

DESCRIPTION

The insertPtnFeedthrough command invoked with the -routeBased option requires routing for the net to find a path based on which it will insert the feedthrough ports.

The net reported is not routed so it gets ignored. Route the design prior to running this command. The earlyGlobalRoute command can be used to route the design.

Otherwise insertPtnFeedthrough should be invoked without using the -routeBased option in which case the command will try to find a path for the net based on the floorplan and placement (placement based feedthrough insertion).

Example:

---

earlyGlobalRoute

insertPtnFeedthrough -routeBased.

PTNPIN-946

NAME

PTNPIN-946

SUMMARY

Pin named [%s] does not exist in cell [%s]. Ignoring the pin. Check and correct the pin name.

DESCRIPTION

Pin name specified for the specified partition does not exist. Check the pin name and partition name and correct accordingly. Problem could be case sensitivity. Command requires exact name which is case sensitive or incorrect manipulation of "alphabet l or numeric 1" "likewise "alphabet o and numeric 0"

Example:

Pin name could be "isCaseSensitive" but pin name supplied could be "iscasesensitive

PTNPIN-1211

NAME

PTNPIN-1211

SUMMARY

Specified layer [%s] is not within the allowed pin layer range [%s] and [%s] of the partition %s. Re-specify a valid pin layer value or change the partition definition to allow this pin layer and rerun the command again.

DESCRIPTION

Specified layer is not within the allowed pin layer range of the specified partition. Use the Partition->Specify Partition GUI to view the current specified allowed layers. Edit the current allowed pin layers of the partition to include this specified pin layer or re-specify pin layer and rerun the

command again.

PTNPIN-1250

NAME

PTNPIN-1250

SUMMARY

Pin placement has been enabled on metal layer 1.

DESCRIPTION

You have this message because you have enabled metal layer 1 for pin placement. However, metal layer 1 is generally reserved for follow pins. Make sure follow pins are already routed, to ensure that the pins do not block follow pins creation.

Example:

---

setDesignMode -bottomRoutingLayer 1 enables pins in M1

PTNPIN-1520

NAME

PTNPIN-1520

SUMMARY

Pin '%s' of %s '%s' cannot be placed at the constrained location [%0.2f %0.2f] due to a blocked pin slot close to the location. Placing the pin at location [%0.2f %0.2f].

DESCRIPTION

Pin slot can be blocked because of the following reasons

\t 1. pin blockages

\t 2. routing blockages

\t 3. Power ground routing

\t 4. availability of layers to put pins

PTNPIN-1521

NAME

PTNPIN-1521

SUMMARY

Unable to get any valid location for the constrained pin [%s] at location [%0.2f %0.2f].

DESCRIPTION

Pin slot can be blocked because of the following reasons

\t 1. pin blockages

\t 2. routing blockages

\t 3. Power ground routing

\t 4. availability of layers to put pins

PTNPIN-1550

NAME

PTNPIN-1550

SUMMARY

Cell [%s] cannot be specified as a black box because the design does not have any instance associated with this cell or instance may create nested blackBox. Ensure the design has an instance referenced to this cell or specify correct name of cell and rerun %s again.

DESCRIPTION

Specified cell cannot be defined as a black box because the design does not have any instance that is referenced to this cell or instance may create nested blackBox. Ensure there is at least one instance that is associated with this cell and rerun the command again.

PTNPIN-1669

NAME

PTNPIN-1669

SUMMARY

Ptn %s does not have any reserved slots for assigning ptn pins. Check the allowed layers for the partition and make sure that layers based on preferred routing tracks are reserved.

DESCRIPTION

This warning message is issued while assigning pins on a partition using the Innovus GUI with Partition => Assign Pin... or when using the assignPtnPin Tcl command.

The floorplan likely contains a problem with routing tracks and/or pin layer definitions. The problem can be debugged graphically using: Partition => Specify Partition

Select the offending partition and review the Partition Pin Layer Used section. Make sure the layers defined for pins are included in the Layers Reserved For Partition. Corrections may be made and applied with this form. Check the min max layer allowed though getDesignMode another reason could be presence of route blockage or PG on partition edge blocking the routing tracks.

Next, confirm there are preferred routing tracks defined for the pin layers using the Layer Control =>

Track => Pref Track and the Wire&Via layer defined for the pins. If the tracks are incorrect, they may be regenerated using the "generateTracks" Tcl command.

Example:

getPinConstraint -cell c -side all -layer

Constraint on partition c :

Allowed layer on side [top] : 2 4 6

Allowed layer on side [left] : 3 5

Allowed layer on side [bottom] : 2 4 6

Allowed layer on side [right] : 3 5

getDesignMode -bottomRoutingLayer -topRoutingLayer

-bottomRoutingLayer 2 # string, default=""

-topRoutingLayer 15 # string, default=""

{bottomRoutingLayer 2} {topRoutingLayer 15}

Look for the Tracks in a section with: Track:

While corrections can be made to the tmp.fp file and reloaded with the "loadFPlan tmp.fp" Tcl command, it is generally easier to do make changes with the Innovus GUI.

PTNPIN-1671

NAME

PTNPIN-1671

SUMMARY

The option %s cannot be used for updating pin attribute. Correct the command options and run the command again.

DESCRIPTION

Specified option cannot be used for just updating pin attribute. This option is used with other options for assigning pin location. Check the reference manual for the legal specified options. Then

correct the command options and rerun the editPin command again.

PTNPIN-1699

NAME

PTNPIN-1699

SUMMARY

Selective-pin-assignment by specifying just partition name(s) to command assignPtnPin is obsolete and will be removed in future releases. The old usage still works in this release, but to avoid this warning and to ensure compatibility with future releases, replace the obsolete usage with "assignPtnPin -ptn -pin ".

DESCRIPTION

To avoid this warning and to ensure compatibility with future releases, replace the obsolete usage with 'assignPtnPin -ptn <ptnName> -pin <pinName>'

Example:

---

* The following command assign pins name starting with "in" of partition "A" and pins name starting with "out" of partition "B"

assignPtnPin -ptn {A} -pin {in*} -ptn {B} -pin {out*}

* The following command accept a file pinLst.txt that contains the list of pins to be placed for partition A and partition B.

assignPtnPin -ptn A -ptn B -pin_file pinLst.txt

PTNPIN-1704

NAME

PTNPIN-1704

SUMMARY

The options [-row] and [-bringBackRow] are obsolete. Rows are brought back automatically, without using any of these options. To avoid this warning and ensure compatibility with future releases, update your script to not use any of these options.

DESCRIPTION

This messages is issued when obsolete options are used.Using these options will have no impact in this case.

Example:

---

eg. use flattenPartition

PTNPIN-1717

NAME

PTNPIN-1717

SUMMARY

The specifyPartition command will be obsolete in the next release. Use the definePartition command to define the partitions.

DESCRIPTION

The message occurs because you are using 'specifyPartition' which is obsoletelease use the 'definePartition' command to define the partitions.

Example:

The following example defines a partition:

definePartition \

-hinst ctr_inst \

-coreSpacing 0.56 0.56 0.0 0.0 \

-railwidth 0.0 \

-minPitchLeft 2 \

-minPitchRight 2 \

-minPitchTop 2 \

-minPitchBottom 2 \

-reservedLayer {1 2 3 4} \

-pinLayerTop {2 4} \

-pinLayerLeft {3} \

-pinLayerBottom {2 4} \

-pinLayerRight {3} \

-placementHalo 1.0 1.0 1.0 1.0 \

-routingHalo 1.0 \

-routingHaloTopLayer 7 \

-routingHaloBottomLayer 1

PTNPIN-1755

NAME

PTNPIN-1755

SUMMARY

Pin [%s] of %s [%s] connected to net [%s] is [%s] at location (%8.3f, %8.3f) on layer %1d %s.

DESCRIPTION

Message reports specific error/violation on a partition pin.

Example of ABUTMENT violation on a pin:

Pin [pin_1] of partition [ptn_1] connected to net [net_1] is [PLACED] at location (210.452, 540.160) on layer 8 has ABUTMENT violation WITH partition chip.

In above example error/violation is being reported for partition “ptn_1” pin's “pin_1” which is connected to net “net_1” and is placed at location “210.452, 540.160” on layer “8” having assignment status as “placed”. Pin has abutment (is placed on adjoining boundary of “ptn_1” and “chip”) violation with partition named “chip”. Ideally the pin pair of two adjoining (abutting) partitions should be placed on same track on edge of partition boundaries, touching each other (abutting).

Abutment violation could be because of following two reasons:

1. Net has multi-partition-pins. Since all other pins of different partitions cannot be placed at same location (no electrical connection through any overlap of physical shape), so it is reported as abutment violation.

2. “pin_1” pin of net “net_1” is not connected to any pin of adjoining (abutted) partition “chip”.

List other violations on pin:

- pin min-width violation
- pin min-depth violation
- pin missing metal shape violation
- pin min-area violation
- pin-color violation
- pin not on routing track (or ndr-rule-routing-track) violation
- pin not on fence violation
- pin spacing (drc and spacing constraints) violation
- pin not on allowed layer violation
- For nested partition it checks for child fence area violation
- pin outside pin-guide or bus-guide violation
- Pin associated pin-group or net-group violation

PTNPIN-1802

NAME

PTNPIN-1802

SUMMARY

Route layer setting through routing modes [setRouteMode %s <value>] or [setNanoRouteMode %s <value>] setting will not be honored. Set the value using setDesignMode command [setDesignMode %s <value>] and run the command again.

DESCRIPTION

This message is reported related to IO pin routing if there are any IO pins falls above maxRouteLayer. Message ENCPTN-1802 is generated to correct the user expectation, when user had set either setRouteMode or setNanoRouteMode for minLayer but has missed to set setDesignMode for minLayer, and user would like to set min/max layer of pin that is different from earlyGlobalRoute. Innovus checks for this issue and generate the message as user may forget to set min/max layer of pin when it differs from earlyGlobalRoute.

Example:

Because of the following reason the ENCPTN-1802 is reported.

Message ENCPTN-1802 is generated to correct the user expectation, when user had set either setRouteMode or setNanoRouteMode for minLayer but has missed to set setDesignMode for minLayer.

Use "setDesignMode -topRoutingLayer <layer>" to placing IO pins, to avoid this problem.

PTNPIN-3207

NAME

PTNPIN-3207

SUMMARY

The hierarchical-PG net %s is connected to an instance term %s inside the partition hinst %s. However, it is not connected to any PG port of the partition hinst. This is erroneous data. As a consequence, instance term %s will become unconnected. To correct this error, ensure that the above net is connected to a partition PG port when connecting to an instance PG term inside the partition, and run the command again.

DESCRIPTION

Reason of such incorrect PG net connection is generally introduced by either incorrect UPF or incorrect GNC rule. To correct this error, ensure that the above net is connected to a partition PG port when connecting to an instance PG term inside partition. Or, if this connection is not needed inside the partition hinst, then ensure that the net does not connect to any of the PG terms inside the partition hinst.

SPEF-1123

NAME

SPEF-1123

SUMMARY

Invalid capacitor node (%s) does not belong to net found in D_NET (%s) that starts on line %u.

DESCRIPTION

This message is issued when one of the capacitor nodes defined in D_NET section does not belong to the same spef file. For Example, Design consisting two spef files i.e. spef1 and spef2 and one of the capacitor nodes specified in D_NET section in spef1 belongs to D_NET section of spef2.

SPEF-1124

NAME

SPEF-1124

SUMMARY

Invalid capacitor node (%s) found in D_NET (%s) that starts on line %u. %s. Check the SPEF file is valid, correct as needed and read it again.

DESCRIPTION

This message is issued when the capacitor nodes defined in D_NET section are invalid. This could be due to either the capacitor node doesn't have corresponding pin or port in the netlist or the net in spef doesn't have corresponding net in the netlist or the node name is not present in the netlist.

SPEF-1125

NAME

SPEF-1125

SUMMARY

Capacitor nodes (%s) do not belong to net found in D_NET (%s) that starts on line %u.

DESCRIPTION

This message is issued when both the capacitor nodes defined in D_NET section do not belong to the same spef file. For Example, Design consisting two spef files i.e. spef1 and spef2 and both the capacitor nodes specified in D_NET section of spef1 belong to D_NET section of spef2.

SPEF-1127

NAME

SPEF-1127

SUMMARY

Invalid CONN connection found (%s) for D_NET (%s) that starts on line %u.

DESCRIPTION

This message is issued when the connection defined in "CONN" section for a D_NET of spef file does not exist in design netlist.

SPEF-1132

NAME

SPEF-1132

SUMMARY

An invalid or ignored D_NET reference (%s) is detected in D_NET. %s. This D_NET starts on line %u. Check the SPEF file is valid, correct as needed and read it again.

DESCRIPTION

This message is issued when the net name specified with D_NET is invalid. For example spef file consisting D_NET n1 does not exist in netlist even though it is being referenced in "NAME_MAP" section of the spef file.

SPEF-1134

NAME

SPEF-1134

SUMMARY

Invalid resistor node (%s) does not belong to net found in D_NET (%s) that starts on line %u.

DESCRIPTION

This message is issued when both the resistor nodes defined in D_NET section do not belong to the same spef file. For Example, Design consisting two spef files i.e. spef1 and spef2 and both the resistor nodes specified in D_NET section in spef1 belong to D_NET section of spef2.

SPEF-1135

NAME

SPEF-1135

SUMMARY

Invalid resistor node (%s) found in D_NET (%s) that starts on line %u. %s. Check the SPEF file is valid, correct as needed and read it again.

DESCRIPTION

This message is issued when the resistor node defined in D_NET section is invalid. This could be due to either the resistor node doesn't have corresponding pin or port in the netlist or the net in spef doesn't have corresponding net in the netlist or the node name is not present in the netlist.

SPEF-1149

NAME

SPEF-1149

SUMMARY

Net (%s) referenced in SPEF but has no D_NET data.

DESCRIPTION

This message is issued when the D_NET section has a net but corresponding connection, capacitance and resistance information is missing.

SPEF-1152

NAME

SPEF-1152

SUMMARY

Net '%s' is not fully specified as per its connectivity in design netlist. Missing ports have been added to the net using low RC values. The timing accuracy is not reliable for such nets.

DESCRIPTION

This message is issued when there is mismatch in the connectivity of net specified in the SPEF file and design netlist. Missing ports will be added to the net in SPEF file with low RC values to match the netlist connectivity. The timing accuracy is not reliable for such nets. Refer the file with extension .incomplete_res.net in working directory for list of such design nets.

SPEF-1155

NAME

SPEF-1155

SUMMARY

Detected resistor attached on both ends to the same node (%s) in the SPEF file for D_NET (%s) starting on or around line %u.

DESCRIPTION

This message is issued when resistor is connected to the same nodes (i.e., input and output nodes are same). SPEF parser expects a resistor between two different nodes in *RES section of a D_NET and issues the message (SPEF-1155), whenever this is violated.

Example:

*D_NET *2468 0.000936122

*RES

9 *2468:4 *2468 2.20892

10 *2468 *2468 12.1356 ===== Here, both the nodes of the resistor are the same.

TAMODEL-101

NAME

TAMODEL-101

SUMMARY

%d registers and latches have data signals at the control input pins. One example of such a control input pin is '%s'. This arises because clocks are not defined properly or because control input pins are fed by register/latch output pins. To model this data/clock conflict, the model extractor preserves register/latch clock pins and the register/latch output pins along with associated check arcs and delay arcs. Model extraction is terminating because this may lead to a very long runtime, a large memory consumption and a large TLF size. Please use '-force' option to continue.

DESCRIPTION

To remedy this problem, please 1) define clocks, or 2) remove '-keep_trigger_arcs' option to ignore the data/clock conflicts or 3) use '-force' option to continue with the preservation of clock trigger arcs

TAMODEL-112

NAME

TAMODEL-112

SUMMARY

Output file '%s' specified with -outFile option of compare_model_timing command cannot be created. Please specify a valid file path with write permission.

DESCRIPTION

Output file specified with -outFile option of compare_model_timing command cannot be created. Please specify a valid file path with write permission.

TAMODEL-113

NAME

TAMODEL-113

SUMMARY

Input file '%s' specified with %s option of %s command does not exist or cannot be read. Please specify valid file name with read permission.

DESCRIPTION

Input file specified does not exist or cannot be read. Please specify valid file name with read permission.

TAMODEL-114

NAME

TAMODEL-114

SUMMARY

pg_pin '%s'is not connected to any power net. Attribute power_down_function cannot be written for output pin '%s'.

DESCRIPTION

This message is issued when rail net is not defined for power pg_pin or non-zero ground pg_pins. Attribute 'power_down_function' cannot be written for such output pins.

TAMODEL-115

NAME

TAMODEL-115

SUMMARY

Attribute power_down_function '%s' consists floating ground rail with operator other than + and *.

Attribute power_down_function cannot be written for pin '%s'.

DESCRIPTION

This message is issued when power_down_function is encountered with complex operators.

TAMODEL-116

NAME

TAMODEL-116

SUMMARY

The attribute '%s' defined on pin '%s' of cell '%s' and '%s' defined on pin '%s' of cell '%s' have different voltage range. The attribute '%s' cannot be written for pin '%s' in ETM.

DESCRIPTION

This message is issued when non-overlapping voltage range is found for multi driver and multi receiver cases.

TAMODEL-117

NAME

TAMODEL-117

SUMMARY

The internal_power could not be calculated for the block as there is no switching activity at any interface pin

DESCRIPTION

This message is issues when there's no pin found with non zero switching activity to write internal power on.

TAMODEL-301

NAME

TAMODEL-301

SUMMARY

This design contains assertions at internal or hierarchical pins that will be ignored in the black box model

DESCRIPTION

Black box models do not support assertions at internal or hierarchical pins unless they are of the type set_disable_timing or set_case_analysis. Such assertions are being ignored. The resulting model may not reflect the original timing behavior.

TAMODEL-303

NAME

TAMODEL-303

SUMMARY

TLF does not recognize a time unit of %f ns, 1 ns assumed

DESCRIPTION

Possible time units in TLF are 1ns, 10ns, 1ps, 10ps and 100ps. Please use set_time_unit command to change the time unit to one of the legal values prior to extracting timing models.

TAMODEL-307

NAME

TAMODEL-307

SUMMARY

Three-dimensional model for delay arc from '%s' to '%s' has been reduced to two-dimensional model. The model will lose accuracy if loading at secondary output '%s' changes from the current value of %.4f\n

DESCRIPTION

Three-dimensional models are reduced to two-dimensional model by fixing the secondary loading at the value used in the present context. Avoid using '-blackbox_2d' option unless the model is to be used within a tool that does not understand three-dimensional models.

TAMODEL-308

NAME

TAMODEL-308

SUMMARY

The number of slew values (%d) for delay arc from '%s' to '%s' exceeds the maximum permissible value of %d. Only the first %d slew values are considered for delay characterization.

DESCRIPTION

The large number of slew values usually arises from output-to-output paths due to secondary loading effect. To account for the secondary loading, the number of slews is multiplied by the number of primary load values and this product can become very large. To avoid this warning, specify a higher tolerance value using -tolerance option.

TAMODEL-309

NAME

TAMODEL-309

SUMMARY

The '%s' to '%s' transition of arc from '%s' to '%s' have early delays greater than the late delays. This may cause issue in timing analysis with the extracted model.

DESCRIPTION

The early delays becomes greater than the late delays in special scenarios like cycle / latency / uncertainty adjustment, or greater early derated, or greater delays in early input libraries. As the extracted model have two parallel arcs; one for early analysis and other for late analysis, In such cases the early arcs being worst delay arc will be used for late analysis and vice-versa.

TAMODEL-310

NAME

TAMODEL-310

SUMMARY

The extracted model will be context dependent on clock frequencies, as multicycle path exception for '%s' arc from '%s' to '%s' can not be pushed out.

DESCRIPTION

When multicycle paths exception on arcs between two pins can not pushed out, the cycle adjustment is adjusted in the arcs delay itself. This cause the extracted model to be context clock frequencies dependent. For such designs the model needs to be re-extracted whenever the clock

frequencies change.

TAMODEL-311

NAME

TAMODEL-311

SUMMARY

Found a feedback loop on transparent latch pin %s while traversing path to output port : %s for %s transition.

DESCRIPTION

If the worst path to an output port is coming from a transparent latch then tools traces backward the latch to find the actual start point of data and stop at non-borrowing latch, flop or input port. In case while tracing backward if there is a feedback loop in the latches, then no actual path is found. Such paths will be skipped.

TAMODEL-312

NAME

TAMODEL-312

SUMMARY

Pin : %s is duplicated to combinational and sequential part, as both combinational and trigger present on this pin.

DESCRIPTION

When two pins have both combinational and sequential arc between then, and one arc is valid for setup analysis and other arc is valid for hold analysis only. In such cases pin is duplicated to

<pinName>_COMB_pin and <pinName>_SEQ_pin, and the sequential and combinational arcs are bind to the duplicated pins.

TAMODEL-313

NAME

TAMODEL-313

SUMMARY

The testcase is running in MMMC configuration. Specify -view option.

DESCRIPTION

In MMMC configuration user need to specify the view for which model need to be extracted. The view specified should be active for both setup and hold analysis. Use -view option to specify the required view.

TAMODEL-314

NAME

TAMODEL-314

SUMMARY

View : %s is not active for %s analysis mode. Use set_analysis_view command to make the view active for both setup and hold analysis.

DESCRIPTION

Extracted model contain both setup and hold arc information. So the view, for which you want to extract the model should be active for both setup and hold analysis. You can make view active by using the set_analysis_view command.

TAMODEL-315

NAME

TAMODEL-315

SUMMARY

Path from '%s' of '%s' and captured by clock '%s' have pin-based clock uncertainties. These constraints will not be a part of the generated ETM model as the global variable 'timing_extract_model_include_latency_and_uncertainty' has been set to false. Ensure that these pin based uncertainty constraints are re-applied after stitching the ETM at the top level.

DESCRIPTION

Setting the global variable 'timing_extract_model_include_latency_and_uncertainty' to false means that clock latency and uncertainty will not be a part of the generated ETM model. Both of these constraints are expected to come from the clock waveforms of the top level when a design is stitched together for timing analysis. However, the internal pin-based clock latency and certainty will not come from the top level. So, if required, during timing analysis, you will need to reapply these constraints when the design is stitched together using ETM models.

TAMODEL-316

NAME

TAMODEL-316

SUMMARY

The software has encountered a problem subdividing the maximum capacitance range for port '%s' into '%d' unique indices due its small value and the current precision setting. The capacitance range for this port will be extended to the default value of %f to allow the calculation of intermediate load points.

DESCRIPTION

In case the precision of the capacitance range is very low, for instance, in femtofarad and as a result the range is too low to be expressed in the unit specified by the user, for instance, picofarad. In such cases, it is not feasible to divide the already small capacitance interval into unique index points. In such cases, extending the capacitance range to the default value makes sense in order to calculate the index points for the load.

TAMODEL-317

NAME

TAMODEL-317

SUMMARY

The software has encountered a problem subdividing the maximum slew range for port '%s' into '%d' unique indices due its small value and the current precision setting. The slew range for this port will be extended to the default value of %f to allow the calculation of intermediate slew points.

DESCRIPTION

In case the precision of the slew range is very low, and as a result the range is too low to be expressed in the unit specified by the user. In such cases, it is not feasible to divide the already small slew interval into unique index points. In such cases, extending the slew range to the default value makes sense in order to calculate the index points for the slew.

TAMODEL-319

NAME

TAMODEL-319

SUMMARY

CPPR aware model extraction is not supported in BcWc mode. The value of the global

timing_extract_model_enable_cppr will be ignored by model extractor.

DESCRIPTION

The tool does not support generation of ETM that is CPPR aware in the BcWc mode. The current setting of the global timing_extract_model_enable_cppr is true, which will be ignored by the command model extractor.

TAMODEL-320

NAME

TAMODEL-320

SUMMARY

The multicycle path exception for '%s' arc from '%s' to '%s' can not be pushed out. No context-dependent cycle adjustment was made, since the global variable 'timing_extract_model_disable_cycle_adjustment' has been set to true.

DESCRIPTION

When multicycle paths exception on arcs between two pins can not pushed out, the resulting model may not reflect the original timing behavior. In such cases, when the ETM is instantiated at the top, recoding the multicycle path that is applied at the block will remove the inconsistency.

TAMODEL-321

NAME

TAMODEL-321

SUMMARY

Waveform Propagation is currently not supported in ETM in worst-case slew propagation mode.

Extracting ETM in path-based slew propagation mode.

DESCRIPTION

Waveform Propagation is currently not supported in ETM in worst-case slew propagation mode. Extracting ETM in path-based slew propagation mode.

TAMODEL-322

NAME

TAMODEL-322

SUMMARY

Model extractor will characterize all the feed through paths for a default load range, which has 64pf/ff as highest load characterization point. This may lead to interpolation error when timing models are read. For better accuracy user should set the highest load characterization point using global timing_extract_model_max_feedthrough_characterization_load before extracting the timing models.

DESCRIPTION

Model extractor will characterize all the feed through paths for a default load range, which has 64pf/ff as highest load characterization point. This may lead to interpolation error when timing models are read. For better accuracy user should set the highest load characterization point using global 'timing_extract_model_max_feedthrough_characterization_load' before extracting the timing models.

TAMODEL-323

NAME

TAMODEL-323

SUMMARY

Compare_model_timing cannot compare '%s' with '%s' as they have been generated with different 'write_model_timing -type' arguments. Please generate both the files with the same argument of 'write_model_timing -type' and compare.

DESCRIPTION

Compare_model_timing cannot compare the pre and post write_model_timing's reports as they have been generated with different 'write_model_timing -type' arguments. Please generate both the files with the same argument of 'write_model_timing -type' and compare.

TAMODEL-324

NAME

TAMODEL-324

SUMMARY

do_extract_model encountered path delay exception that may prevent a timing arc from being extracted from port '%s'. You may want to remove the path exception before extracting the model.

DESCRIPTION

do_extract_model encountered path delay exception that may prevent a timing arc from being extracted from port '%s'. You may want to remove the path exception before extracting the model.

TAMODEL-325

NAME

TAMODEL-325

SUMMARY

Both analog and digital receivers found for port '%s'. Tool will model this as analog pin and write 'is_analog : true' on '%s' pin.

DESCRIPTION

Both analog and digital receivers found for port '%s'. Tool will model this as analog pin and write 'is_analog : true' on '%s' pin.

TAMODEL-326

NAME

TAMODEL-326

SUMMARY

Both analog and digital drivers found for port '%s'. Tool will model this as analog pin and write 'is_analog : true' on '%s' pin.

DESCRIPTION

Both analog and digital drivers found for port '%s'. Tool will model this as analog pin and write 'is_analog : true' on '%s' pin.

TCLCMD-ERR_COMCMD86

NAME

TCLCMD-ERR_COMCMD86

SUMMARY

More than one objects to be renamed are specified

DESCRIPTION

Only one object to be renamed can be specified at a time

TCLCMD-ERR_INVALID_DATA_REQUESTED2

NAME

TCLCMD-ERR_INVALID_DATA_REQUESTED2

SUMMARY

'%s' checks can only be reported in '%s' analysis mode, or simultaneous setup/hold analysis mode. Use either '%s' or simultaneous setup/hold analysis mode, and re-run the command.

DESCRIPTION

The software maintains different analysis modes which at a given time can provide either Setup check related data, Hold check related data, or the combined data for both Setup and Hold style checks. The default and normal operation in Innovus is to have either the Setup or Hold data active at any given time. In Tempus, the normal operation is to have both Setup and Hold active at the same time. The general recommendation is for users to run both of the tools in their respective default modes. As such, users are more likely to see this error message while running Innovus rather than Tempus.\n); detail (\n); detail (The type of analysis being performed by the timer is controlled by:\n); detail (\n); detail (> setAnalysisMode -checkType setup | hold (Innovus Legacy UI)\n); detail (> set_analysis_mode -checkType setup| hold (Tempus Legacy UI)\n); detail (> set_db timing_analysis_mode setup | hold (Stylus UI)\n); detail (\n); detail (When Setup and Hold analysis data are not simultaneously present in the timer, some types of reporting queries will generate an error - indicating the timer is not in the correct analysis mode to provide the requested data.\n); detail (\n); detail (Example:\n); detail (\n); detail (innovus> setAnalysisMode -checkType hold\n); detail (innovus> report_timing -check_type setup\n); detail (\n); detail (**ERROR: (TCLCMD-1045): 'setup' checks can only be reported in 'setup' analysis mode, or simultaneous setup/hold analysis mode. Use either 'setup' or simultaneous setup/hold analysis mode, and re-run the command.\n); detail (\n); detail (In Innovus, you could resolve this issue by switching the analysis type back to 'setup'.\n); detail (\n); detail (innovus> setAnalysisMode -checkType setup\n); detail (\n); detail (You should be aware that switching the check type back-and-forth between 'setup' and 'hold' will cause

timing reset's to occur. You will need to wait for delay calculation and timing analysis to be regenerated.\n); detail (\n); detail (Tempus is almost always run in a mode where both Setup and Hold data are present at the same time - so this type of error condition is rarely encountered.\n

TCLCMD-ERR_MODCMD2

NAME

TCLCMD-ERR_MODCMD2

SUMMARY

No module selected

DESCRIPTION

You must set a current module

TCLCMD-ERR_TACMD6

NAME

TCLCMD-ERR_TACMD6

SUMMARY

The current module is not unique with respect to the top timing module.

DESCRIPTION

You must set a top timing module and set a unique current module or set a current instance (using set_current_instance) before performing any timing commands.

TCLCMD-ERR_VIEWCMD1

NAME

TCLCMD-ERR_VIEWCMD1

SUMMARY

No view selected

DESCRIPTION

You must set a current view by setting a current module

TCLCMD-WARN_COMCMD8

NAME

TCLCMD-WARN_COMCMD8

SUMMARY

The software could not find a matching object of the specified type for the pattern '%s'

DESCRIPTION

The get_* commands are used for retrieving object and collection references from the timing system. If no objects could be returned that match the specified pattern, possible causes include: \n.P\n - The object truly does not exist in the design.\n.sp .5 \n - You have specified an incorrect wildcard matching pattern - refer to the documentation for more information on proper wildcarding syntax.

TCLCMD-WARN_VERBOSE_PBA_EXHAUSTIVE_LIMIT_1

NAME

TCLCMD-WARN_VERBOSE_PBA_EXHAUSTIVE_LIMIT_1

SUMMARY

There are some endpoints which are not able to converge in EPBA Bounded Mode. Refer to verbose log file of current session for more details.

DESCRIPTION

Exhaustive PBA nworst limit set by timing_pba_exhaustive_path_nworst_limit is exhausted for some end-points due to which not all paths terminating to these endpoints are exercised for PBA. To avoid this message, increase the limit by using the global 'set timing_pba_exhaustive_path_nworst_limit <value>'.

TCLCMD-WARN_WRGCF1

NAME

TCLCMD-WARN_WRGCF1

SUMMARY

Constraint of clock required time on pin '%s' will not be converted in GCF

DESCRIPTION

The command set_clock_required_time should be replaced by the command set_external_delay -ref in order to specify required times for output ports on the clock network. set_clock_required_time should only generated internally by timing analysis during time budgeting and is an obsolete

command.

TCLCMD-WARN_WRGCF3

NAME

TCLCMD-WARN_WRGCF3

SUMMARY

Required time on pin '%s' with respect to clock '%s' cannot be converted to GCF

DESCRIPTION

Currently there is no corresponding construct defined in GCF which can represent set_required_time constraint

TCLCMD-WARN_WRGCF4

NAME

TCLCMD-WARN_WRGCF4

SUMMARY

Edge identifier and/or timing check type at target pin '%s' doesn't match the type at source pin '%s' in false path assertion

DESCRIPTION

Due to the mismatch, the path may be over-constrained when converted to GCF

TCLCMD-WARN_WRGCF5

NAME

TCLCMD-WARN_WRGCF5

SUMMARY

Edge identifier and/or timing check type at target pin '%s' doesn't match the type at source pin '%s' in multi-cycle path assertion

DESCRIPTION

Due to the mismatch, the path may be over-constrained when converted to GCF

TCLCMD-WARN_WRGCF12

NAME

TCLCMD-WARN_WRGCF12

SUMMARY

Path exception with '-through' pin to target pin '%s' is not supported by back-end tool

DESCRIPTION

The generated GCF output may contain unsupported GCF v1.3 construct(s)

TCLCMD-WARN_WRGCF13

NAME

TCLCMD-WARN_WRGCF13

SUMMARY

Path exception with %s pin asserted on %s port '%s' is not supported by back-end tool

DESCRIPTION

The generated GCF output may contain unsupported GCF v1.3 construct(s)

TCLCMD-WARN_WRGCF14

NAME

TCLCMD-WARN_WRGCF14

SUMMARY

Path exception asserted on hierarchical pin '%s' is not supported by back-end tool

DESCRIPTION

The generated GCF output may contain unsupported GCF v1.3 construct(s)

TCLCMD-WARN_WRGCF15

NAME

TCLCMD-WARN_WRGCF15

SUMMARY

Path exception with TO pin '%s' asserted on instance output is not supported by back-end tool

DESCRIPTION

The generated GCF output may contain unsupported GCF v1.3 construct(s)

TCLCMD-WARN_WRGCF16

NAME

TCLCMD-WARN_WRGCF16

SUMMARY

Path exception with FROM pin '%s' asserted on instance output other than register data output is not supported by back-end tool

DESCRIPTION

The generated GCF output may contain unsupported GCF v1.3 construct(s)

TCLCMD-WARN_WRGCF19

NAME

TCLCMD-WARN_WRGCF19

SUMMARY

Path exception asserted on bi-directional pin '%s' is not supported by back-end tool

DESCRIPTION

The generated GCF output may contain unsupported GCF v1.3 construct(s)

TCLCMD-WARN_WRGCF20

NAME

TCLCMD-WARN_WRGCF20

SUMMARY

Path exception with FROM pin '%s' asserted on instance input other than register clock input is not supported by back-end tool

DESCRIPTION

The generated GCF output may contain unsupported GCF v1.3 construct(s)

TCLCMD-WARN_WRGCF21

NAME

TCLCMD-WARN_WRGCF21

SUMMARY

Path exception with TO pin '%s' asserted on instance input other than register clock or data input is not supported by back-end tool

DESCRIPTION

The generated GCF output may contain unsupported GCF v1.3 construct(s)

TCLCMD-WARN_WRGCF30

NAME

TCLCMD-WARN_WRGCF30

SUMMARY

Default pin based clock uncertainty (without '-to' option) can not be converted to GCF, treating it as a '-to' unceratinty.

DESCRIPTION

In PKS by default, an uncertainty specification on pin X is honored only at those registers or latches where there is a path from pin X to both the data pin and the clock pin of the register or latch. However, the -to option lifts this restriction and makes it applicable to all registers and latches whose clock pin is in the transitive fanout of pin X. Since the default uncertainty can not be converted to GCF, it treats default uncertainty in the same way as '-to' uncertainty.

TECHLIB-103

NAME

TECHLIB-103

SUMMARY

Unknown timing sense '%s' on pin '%s', cell '%s'

DESCRIPTION

This message is issued when the invalid timing_sense is defined on pin of the cell. The valid timing_sense is negative_unate, positive_unate and non_unate. To fix the issue, re-characterize the library with appropriate settings, such that the valid timing_sense is defined.

TECHLIB-104

NAME

TECHLIB-104

SUMMARY

Incorrect latch/ff/bank combination, cell '%s'

DESCRIPTION

This message is issued when the ff/latch bank is specified with negative bit or ff/latch is defined with bit. To fix the issue, re-characterize the library with appropriate settings, such that the correct combination is used.

TECHLIB-106

NAME

TECHLIB-106

SUMMARY

Could not find any cells in library '%s'

DESCRIPTION

This message is issued when library does not have any cell defined in it.

TECHLIB-107

NAME

TECHLIB-107

SUMMARY

Could not find pin '%s' on cell '%s'

DESCRIPTION

This message is issued when the undefined related_pin is used in the power arcs/EM arcs/timing arcs of cell. To fix the issue, re-characterize the library with appropriate settings, such that the related_pin specified is defined in cell.

TECHLIB-122

NAME

TECHLIB-122

SUMMARY

Wireload model %s in selection table not found

DESCRIPTION

This message is issued when the wire_load group is not defined in library but referred in wire_load_table group. To fix the issue, re-characterize the library with appropriate settings, such that the wire_load group used in wire_load_table group is defined.

TECHLIB-123

NAME

TECHLIB-123

SUMMARY

Undefined template '%s' referred in cell '%s'

DESCRIPTION

This message is issued when a template is referred in cell but is not defined at library level. To fix the issue, re-characterize the library with appropriate settings, such that the template used is defined in library.

TECHLIB-152

NAME

TECHLIB-152

SUMMARY

Linear timing property '%s' found on pin '%s' of cell '%s' in the non-linear library '%s'

DESCRIPTION

This error happens when your non-linear library contains a linear model cell or you update a linear model cell to a non-linear library

TECHLIB-169

NAME

TECHLIB-169

SUMMARY

Couldn't find pin '%s' specified in the function of cell '%s'

DESCRIPTION

This message is issued when a pin is used in function statement but is not defined in the cell. Function statement will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the undefined pins are not used in function statement.

TECHLIB-180

NAME

TECHLIB-180

SUMMARY

Unknown model for PVT multiplier '%s'

DESCRIPTION

Currently only constant and linear models are supported for PVT multiplier

TECHLIB-183

NAME

TECHLIB-183

SUMMARY

The index '%d' of bus '%s' is out of bus range

DESCRIPTION

This message is issued when the scaler bit is specified which is out of range as per the bus bit definition. To fix the issue, re-characterize the library with appropriate settings, such that the correct range is defined.

TECHLIB-184

NAME

TECHLIB-184

SUMMARY

Attempt to create BDD for '%s' string '%s' on timing arc of pin '%s' in cell '%s' failed. This is an internal error.

DESCRIPTION

When the tool is unable to create a BDD against the when/when_start/when_end expression it reports an ERROR. The reason can be multiple. One of the reason can be incorrect logic in the expression.

TECHLIB-190

NAME

TECHLIB-190

SUMMARY

Unrecognized value '%s' of library attribute '%s'

DESCRIPTION

This message is issued when the value of the attributes default operating condition/default wire load selection/default wireload is undefined in library. To fix the issue, re-characterize the library with appropriate settings, such that no undefined value of these attributes are used in the library.

TECHLIB-191

NAME

TECHLIB-191

SUMMARY

The value '%f' on cell '%s', pin '%s', '%s' should be non-negative

DESCRIPTION

This message is issued when either the constraint attribute in minimum_period group or the constraint_high/constraint_low attributes in minimum_pulse_width group are defined with negative value. Negative values are not allowed in these attributes. To fix the issue, re-characterize the library with appropriate settings, such that constraints are defined with positive value.

TECHLIB-246

NAME

TECHLIB-246

SUMMARY

Error encountered while reading cell '%s' in library '%s'

DESCRIPTION

This message is issued when the error is already issued while reading a cell in library. Refer the log file for the failure reason.

TECHLIB-248

NAME

TECHLIB-248

SUMMARY

Thresholds cannot have negative values

DESCRIPTION

This message is issued when the slew threshold values are specified as negative. Slew thresholds cannot have negative values. To fix the issue, re-characterize the library with appropriate settings, such that positive slew threshold is defined.

TECHLIB-249

NAME

TECHLIB-249

SUMMARY

'%s': '%f' should be less than '%s': '%f'

DESCRIPTION

This message is issued when the value of attribute slew_upper_threshold/slew_measured_upper_threshold is less than slew_lower_threshold/slew_measured_lower_threshold. Value of upper threshold should be greater than the lower threshold value. To fix the issue, re-characterize the library with appropriate settings, such that slew threshold values are defined correctly.

TECHLIB-257

NAME

TECHLIB-257

SUMMARY

%s '%s' has identical lower and upper measured slew thresholds for %s transition

DESCRIPTION

This message is issued when the value of attribute slew_measured_lower_threshold and slew_measured_upper_threshold is defined as same for rise_transition or fall_transition in a library. Value of the upper threshold should be greater than the lower threshold value. To fix the issue, re-characterize the library with appropriate settings, such that slew threshold values are defined correctly.

TECHLIB-258

NAME

TECHLIB-258

SUMMARY

%s '%s' has identical lower and upper slew thresholds for %s transition

DESCRIPTION

This message is issued when the value of attribute slew_lower_threshold and slew_upper_threshold is defined as same for rise_transition or fall_transition in a library. Value of the upper threshold should be greater than the lower threshold value. To fix the issue, re-characterize the library with appropriate settings, such that slew threshold values are defined correctly.

TECHLIB-263

NAME

TECHLIB-263

SUMMARY

Pin %s property %s/%s is negative: %f. Check arc is not created

DESCRIPTION

Setup and hold time can be negative. However other check arcs such as: pulse_width, period, nochange, skew, . These can not be negative values.

TECHLIB-264

NAME

TECHLIB-264

SUMMARY

Pin %s property %s/%s -> %s(related_pin) is negative: %f. Check arc is not created

DESCRIPTION

Setup and hold time can be negative. However other check arcs such as: pulse_width, period, nochange, skew, . These can not be negative values.

TECHLIB-265

NAME

TECHLIB-265

SUMMARY

Pin %s property (%s %s %s %s) %s/%s is negative: %f. Check arc is not created

DESCRIPTION

Setup and hold time can be negative. However other check arcs such as: pulse_width, period, nochange, skew, . These can not be negative values.

TECHLIB-266

NAME

TECHLIB-266

SUMMARY

Attribute '%s' on pin '%s' of cell '%s' is not defined in the library

DESCRIPTION

This message is issued when the attributes fanout_load/max_fanout/min_fanout/max_transition/min_transition/max_capacitance/min_capacitance are not defined on pin of cell in the library. To fix the issue, re-characterize the library with appropriate settings, such that the attributes are defined in the cell pin.

TECHLIB-269

NAME

TECHLIB-269

SUMMARY

Wrong usage of template '%s', used in cell '%s' pin '%s'

DESCRIPTION

Libcompile will exit when this error occurs. This error happens when a template is wrongly used. For example, in 2-dimensional table lookup, The 'cell_rise' table expects template that contains The 'input_net_transition' and The 'total_output_net_capacitance' indices. If these two template index types can not be found at the compile time of 'cell_rise' table, BuildGates will flag an error and exit.

TECHLIB-270

NAME

TECHLIB-270

SUMMARY

Wrong usage of template '%s', used in cell '%s'

DESCRIPTION

Libcompile will exit when this error occurs. This error happens when a template is wrongly used by non-pin related arcs, such as either in 'rise/fall_transition_degradation' or in 'rise/fall_net_delay' For an example, in 2-dimensional table lookup, The 'rise_net_delay' table expects template that contains The 'output_pin_transition' and The 'connect_delay' indices. If these two template index types can not be found at the compile time of 'rise_net_delay' table, BuildGates will flag an error and exit.

TECHLIB-271

NAME

TECHLIB-271

SUMMARY

%s threshold specifications are incomplete

DESCRIPTION

This message is to inform users that only partial slew/delay threshold points are specified. For example, only rise threshold points are specified while the fall threshold points are not

TECHLIB-272

NAME

TECHLIB-272

SUMMARY

Syntax error in '%s' specification. Expecting a '%s'

DESCRIPTION

This message is issued when the attribute input_threshold_fall/input_threshold_rise is specified with invalid value, for example 'string'. These attributes can accept 'float' values only. To fix the issue, re-characterize the library with appropriate settings, such that valid value is defined for threshold.

TECHLIB-274

NAME

TECHLIB-274

SUMMARY

Can not resolve the when expressions found in the two libraries

DESCRIPTION

There are various possibilities this error may occur as follows: 1. The when condition of pin power construct specified in multiple libraries are overlapping 2. The sum of subsets when-functions is not equal to the superset when-function 3. The when condition of pin power construct specified in from library do not cover all specified in to library, or vice-versa

TECHLIB-275

NAME

TECHLIB-275

SUMMARY

Multiple pin power are specified but no when condition specified on each pin power table

DESCRIPTION

BuildGates requires that each pin power table of a specific cell pin to have when condition expression that is mutually exclusive from other when expressions. This message though is limited to detect a case where multiple pin power are specified but do not have when condition expression. When this error message occurs, it means that the library is bad and BuildGates will error out

TECHLIB-276

NAME

TECHLIB-276

SUMMARY

Library defines an invalid %s threshold for %s transition of %.0f%%. Use -force option to continue with default values

DESCRIPTION

Delay and slew thresholds of 0 or 100% is physically impossible. Rising exponential waveform will never reach 100%. Falling exponential waveform will never reach 0%

TECHLIB-277

NAME

TECHLIB-277

SUMMARY

Only one default power table can be specified. BuildGates can not merge libraries.

DESCRIPTION

A default power table is a power table that does not have the WHEN condition specified. Following this message, pin and cell names are displayed, which tell you where the multiple default power tables are found. If you have the min and max library source files, you can compare the power tables to find the source of the error.

TECHLIB-278

NAME

TECHLIB-278

SUMMARY

Library '%s' %s does not have correct FE ASIC license

DESCRIPTION

When using FE ASIC license, you should only use the library that is provided by specific ASIC vendor. Contact your ASIC vendor to provide you with the library that contains proper FE ASIC license string

TECHLIB-279

NAME

TECHLIB-279

SUMMARY

The number of input pins for cell '%s' differ between two libraries. First library has %d input pins, whereas second has %d. Aborting update.

DESCRIPTION

To load the library successfully, make sure the information for the cell in both libraries is consistent.

TECHLIB-280

NAME

TECHLIB-280

SUMMARY

Invalid slew threshold range %.2f-%.2f%%. The slew threshold range must be greater than one percent.

DESCRIPTION

This message is issued when the difference between the attributes slew_lower_threshold and slew_upper_threshold is less than 1%. To fix the issue, re-characterize the library with appropriate settings, such that the slew threshold range greater than 1% is defined.

TECHLIB-281

NAME

TECHLIB-281

SUMMARY

Attempt to read .lib library '%s' failed

DESCRIPTION

This message is issued when the error is already issued while reading a library. Refer the log file for the failure reason.

TECHLIB-282

NAME

TECHLIB-282

SUMMARY

Table values less than expected in user defined group '%s'%s''. Table index points being truncated

DESCRIPTION

This message is issued when the number of table values specified in user defined group are less than product of dimensions of index values. To fix the issue, re-characterize the library with appropriate settings, such that the table values are specified correctly.

TECHLIB-302

NAME

TECHLIB-302

SUMMARY

No function defined for cell '%s'. The cell will only be used for analysis.

DESCRIPTION

This message is issued when the function of the cell is not defined. This cell will not be used for optimization. To fix the issue, re-characterize the library with appropriate settings, such that the function should be specified.

TECHLIB-305

NAME

TECHLIB-305

SUMMARY

Library '%s' is already loaded. You need to use read_library_update command to update a library.

DESCRIPTION

You can not use subsequent read_alf to read in two different libraries with different names. You will have to use read_library_update to update the library which share the same name. read_library_update only updates cells, operating conditions, and wireload model. It assumes that other properties such as templates and units are already defined in the first library and BG will not update these properties.

TECHLIB-311

NAME

TECHLIB-311

SUMMARY

Can't derive the asynchronous type of input pin '%s' from the function of output pin '%s' in sequential cell '%s'

DESCRIPTION

The asynchronous timing type (preset or clear) of an input-to-output timing arc in a sequential cell is derived by checking if the input is in the support set of the corresponding asynchronous function of that output. If the asynchronous function of the output is not specified, the asynchronous type cannot be determined and therefore the timing type of that timing arc will be set to combinational by default

TECHLIB-313

NAME

TECHLIB-313

SUMMARY

Property '%s' can not be set on pin '%s' of cell '%s'

DESCRIPTION

Some attributes are specific to certain pin types (input/output/inout). The reported property may not be applicable to the given pin based on its pin type.

TECHLIB-318

NAME

TECHLIB-318

SUMMARY

Derating table '%s' already defined, ignored

DESCRIPTION

Currently the old derating table is not overridden by the new one

TECHLIB-319

NAME

TECHLIB-319

SUMMARY

Template '%s' already defined, ignored

DESCRIPTION

Currently the old template is not overridden by the new one

TECHLIB-324

NAME

TECHLIB-324

SUMMARY

Scaling_factors table '%s' was referenced at cell level but not defined in the library. The scaling_factors table will be ignored.

DESCRIPTION

All cell scaling_factors references must have the scaling_factor defined in the library level in the same file. read_library_update may not be used to merge scaling_factors defined in one file with scaling_factors references defined in another file

TECHLIB-327

NAME

TECHLIB-327

SUMMARY

Cell '%s' has more than %d input pins. The cell will only be used for analysis.

DESCRIPTION

This message is issued when a cell has more than 24 input pins. Such cells are not used during optimization and are used only for analysis.

TECHLIB-336

NAME

TECHLIB-336

SUMMARY

The minimum clock %s constraint in cell '%s' is not a constant, ignored

DESCRIPTION

Only constant TLF model is supported now

TECHLIB-338

NAME

TECHLIB-338

SUMMARY

Linear timing property '%s' found on pin '%s' of cell '%s' in the non-linear library '%s'

DESCRIPTION

This message is issued when the non-linear library contains a linear model cell or update a linear model cell to a non-linear library.

TECHLIB-342

NAME

TECHLIB-342

SUMMARY

Attempt to create mode '%s' belonging to mode group '%s' failed

DESCRIPTION

The BDD for the conditional expression associated with this mode could not be built

TECHLIB-357

NAME

TECHLIB-357

SUMMARY

Test cell '%s' uses '%s' as state variable whereas scan cell uses '%s' in library '%s'; '%s' is used as state variable in test cell

DESCRIPTION

This message is issued when the state variables defined in the library are not same in the test cell and scan cell. To fix the issue, re-characterize the library with appropriate settings, such that the state variables are defined correctly.

TECHLIB-368

NAME

TECHLIB-368

SUMMARY

Unable to find the ff/latch '%s' functionality pin for cell '%s'

DESCRIPTION

This message is issued when the ff/latch functionality pin (IQ/IQn) for cell is undefined. To fix the issue, re-characterize the library with appropriate settings, such that the function of a cell is defined.

TECHLIB-369

NAME

TECHLIB-369

SUMMARY

Unable to extract the '%s' function for sequential cell '%s'

DESCRIPTION

This message is issued when the values defined for statetable for the attributes next_state/clocked_on/preset/clear/clear_preset_var1/clear_preset_var2 cannot be converted into ff/latch.

TECHLIB-377

NAME

TECHLIB-377

SUMMARY

%s '%s' not equivalent to %s '%s'.

DESCRIPTION

This message is issued when there is discrepancy between the scaled cell and regular cell. Cells are not equivalent. To fix the issue, re-characterize the library with appropriate settings, such that the cells are matched.

TECHLIB-381

NAME

TECHLIB-381

SUMMARY

Values for '%s' different between the scaled and regular %s '%s'.

DESCRIPTION

This message is issued when there is discrepancy between the scaled cell and regular cell in values for direction/number of timing arcs/timing arc/number of related pins for power arc/number of equal or opposite pins for power arc/when string for power arc/period/pulse_width/fanout_load/output_function/three_state_function for I/O pins. To fix the issue, re-characterize the library with appropriate settings, such that the values for these attributes between cells are matched.

TECHLIB-382

NAME

TECHLIB-382

SUMMARY

No pin '%s' found in scaled cell but present in regular cell.

DESCRIPTION

This message is issued when there is discrepancy in pins between the scaled cell and regular cell. To fix the issue, re-characterize the library with appropriate settings, such that the pins are consistent between the cells

TECHLIB-383

NAME

TECHLIB-383

SUMMARY

Attempt to create three-state function for %s pin '%s' in cell '%s' failed

DESCRIPTION

Check if three-state function is incorrectly defined in terms of output pin itself. Check if the pins defined in the three-state function are defined for the cell. Cell will not be mapped to but if instantiated manually, will be correctly timed.

TECHLIB-385

NAME

TECHLIB-385

SUMMARY

Pin %s property %s/%s is zero or negligible: %f. BG will still create the check arc

DESCRIPTION

BuildGates will still create any check arcs that are zero.

TECHLIB-386

NAME

TECHLIB-386

SUMMARY

Pin %s property %s/%s -> %s(related_pin) is zero or negligible: %f. BG will still create the check arc

DESCRIPTION

BuildGates will still create any check arcs that are zero.

TECHLIB-387

NAME

TECHLIB-387

SUMMARY

Pin %s property (%s %s %s %s) %s/%s is zero or negligible: %f. BG will still create the check arc

DESCRIPTION

BuildGates will still create any check arcs that are zero.

TECHLIB-389

NAME

TECHLIB-389

SUMMARY

Unable to find cell '%s' in library to update spice pin order

DESCRIPTION

'read_library_update -spice' is to update spice pin order This warning message occurs if the spice subckt file contains cells that can not be found in the timing library In which case, BuildGates will ignore such subckt

TECHLIB-390

NAME

TECHLIB-390

SUMMARY

No delay threshold points for %s transition specified in library '%s', assuming delay thresholds %.0f%%-%.0f%%

DESCRIPTION

This warning is encountered if the following constructs are missing from the library. input_threshold_pct_fall input_threshold_pct_rise output_threshold_pct_fall output_threshold_pct_rise These constructs in the timing library define how the delay of the characterized cells has been deduced. For example a input_threshold_pct_rise of 30 and output_threshold_pct_rise of 60 means theat the delay value in the tables are the time difference between the input rising to 30% of its values and output rising to 70% of its value. If these are missing, then they are assumed to be 50% for both input and output and rise and fall. To avoid this warning make sure that the timing labraries have the correct values of input and output rise/fall thresholds specified.

TECHLIB-391

NAME

TECHLIB-391

SUMMARY

No slew threshold points for %s transition specified in library '%s', assuming slew thresholds %.0f%%-%.0f%% (measured) %.0f%%-%.0f%% (reported).

DESCRIPTION

This warning is encountered if the following constructs are missing from the library. slew_lower_threshold_pct_fall slew_upper_threshold_pct_fall slew_lower_threshold_pct_rise slew_upper_threshold_pct_rise These constructs in the timing libraries are the slew thresholds which define how slew values are calculated. For example a slew_lower_threshold_pct_rise of 20 and slew_upper_threshold_pct_rise of 80 means that the time values present in the library were written as if 'measured' at 20% of the signal and 80% of the signal, and the slew is represented as their difference. If these are missing, they are assumed to be 40% -60% (measured) 10%-90% (reported). The measured thresholds are the ones at which timing is actually measured from spice. These can be then stretched to reported thresholds linearly, to generate the data in the timing library. To avoid this warning make sure that the timing libraries have the correct slew threshold values specified.

TECHLIB-392

NAME

TECHLIB-392

SUMMARY

Ignoring pin power table on pin '%s' of cell '%s' because of bad type: %d

DESCRIPTION

This message tells the user that specific INTERNAL_ENERGY statement is ignored because of invalid TLF data type. BuildGates only accepts the following data types for internal energy: - INTERNAL_ENERGY(model [COND(cond)]) - INTERNAL_ENERGY(RISE(model) FALL(model) [COND(cond)])

TECHLIB-393

NAME

TECHLIB-393

SUMMARY

Pin '%s' of cell '%s' has power arcs with incomplete when conditions

DESCRIPTION

This message occurs if pin power arcs has incomplete when conditions Incomplete means that the when conditions for a specific power arcs do not add to 1.

TECHLIB-395

NAME

TECHLIB-395

SUMMARY

Library defines an invalid %s threshold for %s transition of %.0f%%. Default value of %.0f%% is used instead.

DESCRIPTION

Delay and slew thresholds of 0 or 100% is physically impossible. Rising exponential waveform will never reach 100%. Falling exponential waveform will never reach 0%

TECHLIB-397

NAME

TECHLIB-397

SUMMARY

BG computes reported slew threshold that is beyond the 0%%-100%% range. For rising transition: %.0f%%-%.0f%% For falling transition: %.0f%%-%.0f%%

DESCRIPTION

The reported slew threshold is computed using the library defined slew threshold and the library defined slew_derate value Such case may happen for example if the library defines a slew threshold of 20-80 and a slew_derate value of 0.5

TECHLIB-398

NAME

TECHLIB-398

SUMMARY

%s threshold specifications are incomplete. You can override the threshold specifications using set_tech_info command

DESCRIPTION

Only partial slew/delay threshold points are specified. For example, delay threshold for rising transition is specified while delay threshold for falling transition is not.

TECHLIB-399

NAME

TECHLIB-399

SUMMARY

No %s threshold for %s transition specified, assuming default value of %.0f%%

DESCRIPTION

The mentioned threshold value is missing from the library and the default value is used to compensate for the missing information. This message occurs only if partial threshold information is specified. For example, delay threshold for rising transition is specified while delay threshold for falling transition is not.

TECHLIB-400

NAME

TECHLIB-400

SUMMARY

State table for cell '%s' is ignored because it contains multiple references to input map. The input_map attribute can be defined more than once for multi-bit sequential cells only.

DESCRIPTION

Examples of multiple instances of a sequential device in a single cell include master-slave devices, shift registers or counters. Only simple register/latch banks with explicit bundle specification are supported

TECHLIB-401

NAME

TECHLIB-401

SUMMARY

There are multiple power pin defined with the same related_pin and the same when condition on pin %s of cell %s. Only the last data is used.

DESCRIPTION

Multiple power pin with the same related_pin, same equal_or_opposite_pins, same when conditions, and same transition edges will be merged. i.e. the last data will override the earlier one.

TECHLIB-402

NAME

TECHLIB-402

SUMMARY

Support for libcompile is being phased out. Use read_dotlib to read in .lib natively or syn2tlf and read_tlf to compile into TLF. Some constructs such as generated clocks and interface_timing are supported only in read_dotlib and syn2tlf/read_tlf

DESCRIPTION

Refer to the Timing Analysis Using BuildGates Synthesis and Cadence PKS for more details on constructs that are not supported by libcompile

TECHLIB-403

NAME

TECHLIB-403

SUMMARY

Invalid specification of %s in the output/internal pin %s of cell %s. These specifications are only allowed in input/bidir pins; therefor, these specifications will be ignored when library loading.

DESCRIPTION

According to the Liberty format, hyperbolic noise can only be specified on input pins of a cell. All hyperbolic noise specifications on internal and output pins will be ignored.

TECHLIB-404

NAME

TECHLIB-404

SUMMARY

The coefficient value is less than 0 for the hyperbolic %s coefficient for %s in pin %s of Cell %s. Therefore the entire group will be ignored.

DESCRIPTION

Hyperbolic coefficients for area, width and height can not be negative. Even if one of them is specified as negative, the entire hyperbolic noise group is ignored.

TECHLIB-405

NAME

TECHLIB-405

SUMMARY

Template %s should be of size 2D, specified as a function of noise width (input_noise_width) and output load (total_output_net_capacitance). Ignoring this template.

DESCRIPTION

The Noise Immunity templates must have exactly two axies. The input_noise_width axis specifies the noise width and the output load is specified by the total_output_net_capacitance axis

TECHLIB-406

NAME

TECHLIB-406

SUMMARY

Ignoring the specified 'steady_state_current_tristate' table in the non three_state pin/bus/bundle %s of cell %s. The above specification applies only to three_state pins.

DESCRIPTION

The steady_state_current_tristate can only be specified for three state pins, buses or bundles. If it is specified for a non three-state pin, its value is ignored.

TECHLIB-407

NAME

TECHLIB-407

SUMMARY

The specified value is less than 0 for %s steady_state_resistance in pin %s of cell %s. Values must be positive float numbers.

DESCRIPTION

The steady_state_resistance can not take negative values. All such negative values are neglected.

TECHLIB-408

NAME

TECHLIB-408

SUMMARY

The template definition for %s, referenced in pin %s of cell %s is missing in the library. Therefore, the table would be ignored while loading the library.

DESCRIPTION

Specify the missing template at the library level.

TECHLIB-409

NAME

TECHLIB-409

SUMMARY

Invalid axis specified for 'iv_lut_template' %s. It must be function of output voltage (iv_output_voltage). Ignoring this template.

DESCRIPTION

The iv_lut_template must be a single dimensional table. The only axis is the output voltage axis, specified by iv_output_voltage

TECHLIB-410

NAME

TECHLIB-410

SUMMARY

Invalid combination of axis specified for 'propagation_lut_template' %s. It must be a function of noise width (input_noise_width), noise height (input_noise_height) and output load (total_output_net_capacitance). Ignoring this template.

DESCRIPTION

The propagation_lut_template must be a 3D table. The axes which need to specified are - noise width (input_noise_width), noise height (input_noise_height) and output load (total_output_net_capacitance)

TECHLIB-411

NAME

TECHLIB-411

SUMMARY

The lookup table template %s specified in the library is a Scalar lookup template. All of the axis in the template contain only single co-ordinate points, which would not be useful during table lookup.

DESCRIPTION

A scalar lookup template is one which has only one axis point in each of its axis. Such a lookup template is useless for table lookup.

TECHLIB-412

NAME

TECHLIB-412

SUMMARY

A single data point found in the axis point redefinition of template %s in pin %s of cell %s. This axis point will not be useful during table lookup.

DESCRIPTION

Single point axis is not useful for lookups. Any redefinition of such single points will not effect the lookup in any way

TECHLIB-413

NAME

TECHLIB-413

SUMMARY

Negative data found in table for %s noise immunity in pin %s of cell %s. The data values must be positive.

DESCRIPTION

Noise immunity data can not specified as negative.

TECHLIB-414

NAME

TECHLIB-414

SUMMARY

Missing %s %s noise propagation specification in pin %s of cell %s in the library. Height and width tables for a particular region (low, high, below_low, above_high) must be specified in pairs.

DESCRIPTION

Height and Width specifications for a particular noise region should always come in a pair. Need to specify both the parameters for propagation.

TECHLIB-415

NAME

TECHLIB-415

SUMMARY

Template definition for %s, referenced in pin %s of cell %s missing in the library. Table would be ignored while library loading.

DESCRIPTION

The template used must be defined at the library level.

TECHLIB-416

NAME

TECHLIB-416

SUMMARY

Single Data point found in the axis point redefinition of template %s in pin %s of cell %s. Axis point would not be useful during lookup.

DESCRIPTION

Single point axis are not useful for lookups. Any redefinition of such single points will not effect the lookup in any way

TECHLIB-417

NAME

TECHLIB-417

SUMMARY

Multiple definitions of template %s found in the library. Preserving the latest definition.

DESCRIPTION

If a template is defined multiple number of times at the library level, only the latest definition is preserved.

TECHLIB-418

NAME

TECHLIB-418

SUMMARY

Number of data points in the table %s in pin %s in cell %s does not match the number of axis points specified in the template.

DESCRIPTION

The number of data points should preferably match the number of axis points in a template. If this is not the case, table lookups might not be accurate.

TECHLIB-419

NAME

TECHLIB-419

SUMMARY

Number of index point in axis redefinition of template %s in pin %s in cell %s is not equal to that in the original template.

DESCRIPTION

The number of points in axis redefinition should be exactly equal to the number of axis points in the template.

TECHLIB-420

NAME

TECHLIB-420

SUMMARY

Number of ecsm_waveforms in the '%s' table on pin %s of cell %s does not match the number of transition table axis points specified in the template '%s'. Ignoring waveform data.

DESCRIPTION

The number of ecsm_waveforms must match the number of data points in the transition table for correct waveform lookup. If this is not the case, waveform data for the transition group is ignored.

TECHLIB-421

NAME

TECHLIB-421

SUMMARY

Invalid ecsm_waveform group name %s specified in pin %s of cell %s. Ignoring waveform data.

DESCRIPTION

Waveform group name must be a digit and the value of the digit must not be greater than or equal to the total number of entries in the output transition table. All the waveforms must start from 0.

TECHLIB-422

NAME

TECHLIB-422

SUMMARY

The output transition table '%s' for pin '%s' of cell '%s' is not a function of capacitive load. No ECSM data is available for this transition group. Capacitive load indices are required for generating the ECSM data.

DESCRIPTION

This message is issued when the output transition table is not a function of capacitive load. Such ECSM data will not be available. To fix the issue, re-characterize the library with appropriate settings, such that the capacitive load indices are defined.

TECHLIB-423

NAME

TECHLIB-423

SUMMARY

Unable to infer polarity for pin %s of cell %s. Positive polarity assumed.

DESCRIPTION

Couldn't find two different delay values in the table for pair of input slew and output load.

TECHLIB-424

NAME

TECHLIB-424

SUMMARY

Invalid ECSM_Current/PGDC waveform group name %s specified in pin %s of cell %s. Ignoring waveform data.

DESCRIPTION

Waveform group name must be a digit and the value of the digit must not be greater than or equal to the total number of entries in the output transition table. All the waveforms must start from 0.

TECHLIB-425

NAME

TECHLIB-425

SUMMARY

Invalid rail connection name %s specified in ECSM_Power/PGDC group for pin %s of cell %s. Ignoring waveform data.

DESCRIPTION

Waveform rail connection name is optional. If provided it must be valid one

TECHLIB-426

NAME

TECHLIB-426

SUMMARY

Incompatible ecsm_power_version/pgdc_version %f in library %s

DESCRIPTION

The ecsm_power_version/pgdc_version defined in a library must be equal to 1.0

TECHLIB-427

NAME

TECHLIB-427

SUMMARY

Empty ECSM_Current/PGDC waveform group found in cell %s, of library %s

DESCRIPTION

If ECSM_Current/PGDC groups are defined, they must contain waveform groups also. They can not be empty

TECHLIB-428

NAME

TECHLIB-428

SUMMARY

Number of index_1 points does not match with the number of values points for the %s waveform group %s specified in pin %s of cell %s Ignoring waveform data.

DESCRIPTION

This message is issued when the total number of index_1 points are not equal to the total number of values specified in pin of cell for ECSM power/PGDC group. To fix the issue, re-characterize the library with appropriate settings, such that the index_1 is correctly defined.

TECHLIB-429

NAME

TECHLIB-429

SUMMARY

Waveform group count does not match with the template %s in pin %s of cell %s

DESCRIPTION

The total number of waveform groups must be equal to the total number of values described by the corresponding template

TECHLIB-430

NAME

TECHLIB-430

SUMMARY

Values of the %s waveform group %s should monotonically increase in pin %s of cell %s

DESCRIPTION

This warning is encountered if the ECSM waveform in the timing library is not monotonically increasing or monotonically decreasing. ECSM waveform models the v-t relationship for a signal. The voltage should monotonically increase (for rise waveforms) and monotonically fall(for fall waveforms). If there is glitch in the waveform the above message is issued. To avoid this warning, fix the ECSM waveform data in the library so that there are no glitches in the waveform.

TECHLIB-431

NAME

TECHLIB-431

SUMMARY

Mismatch in the number values redefined for Index_%d of template %s in pin %s of cell %s

DESCRIPTION

Index redefinitions should contain exactly the same number of values as defined in the original template

TECHLIB-432

NAME

TECHLIB-432

SUMMARY

Unknown ecsm_capacitance type defined in pin %s of cell %s. Ignoring ecsm_capacitance defined in the pin.

DESCRIPTION

The ecsm_capacitance type should be either rise or fall. If a value other than rise or fall is encountered, the ecsm_capacitance information will be ignored

TECHLIB-433

NAME

TECHLIB-433

SUMMARY

Cell %s is not an isolation cell, pin %s on line %d is specified isolation %s pin. Ignoring 'isolation_cell_%s_pin' attribute of this pin.

DESCRIPTION

'isolation_cell_enable_pin' attribute specifies the enable pin of an isolation cell and 'isolation_cell_data_pin' attribute specifies the data pin of an isolation cell. The parent cell of this pin is not an isolation cell. To mark the cell as an isolation cell, mention 'is_isolation_cell : true' at the cell level.

TECHLIB-434

NAME

TECHLIB-434

SUMMARY

Cell %s is not a level shifter cell, pin %s is specified level shifter %s pin. No data is ignored.

DESCRIPTION

'level_shifter_enable_pin' and 'level_shifter_data_pin' attribute specifies the enable pin and data pin of a level shifter cell respectively. The parent cell of this pin is not a level shifter cell. To mark the cell as a level shifter cell mention 'is_level_shifter : true' at the cell level.

TECHLIB-435

NAME

TECHLIB-435

SUMMARY

Nominal Voltage for library %s is specified to be 0. This may cause problems with delay calculation

DESCRIPTION

Nominal voltage of a library defines the voltage at which the library was characterized. A zero value is unrealistic for this attribute.

TECHLIB-436

NAME

TECHLIB-436

SUMMARY

Attribute 'fanout_load' on '%s' %s of cell '%s' is not defined in the library.

DESCRIPTION

When a library is loaded, software checks for the presence of fanout_load attribute on input pins of all cells in library automatically. This message is issued when any of the mentioned attribute is missing.

TECHLIB-437

NAME

TECHLIB-437

SUMMARY

The ecsm_waveform_set group in pin '%s' cell '%s' is redefined with different axis points

DESCRIPTION

Number of index and value points defined in the ecsm_waveform_set group should be same. If the index points are redefined, the number of redefined index points should be same as the number of index points defined in the original template

TECHLIB-452

NAME

TECHLIB-452

SUMMARY

The %s capacitances %s table group %s%s%s for %s transition in pin '%s' of cell '%s' are not in the range of min cap value

DESCRIPTION

For correct calculation of delay value the capacitances value should be more than or equal to min cap value.

TECHLIB-453

NAME

TECHLIB-453

SUMMARY

The %s capacitances %s table value %s%s%s for %s transition in pin '%s' of cell '%s' are not in the range of pin's capacitances value

DESCRIPTION

For correct calculation of delay value the capacitances value should be less than or equal to pin's capacitances value.

TECHLIB-458

NAME

TECHLIB-458

SUMMARY

The %s index of ECSM capacitances table %s %s in pin '%s' of cell '%s' is greater than pin's capacitances value

DESCRIPTION

For correct calculation of delay value the capacitances value should be less than or equal to pin's cap value.

TECHLIB-459

NAME

TECHLIB-459

SUMMARY

Appending library '%s' to the previously read library of the same name and nominal PVT. Cell definitions from the previously read library will not be overridden.

DESCRIPTION

This warning is encountered if two library files with the same library name and nominal pvts are specified in the same group (conf file ui_timelib* variables) or in the same libset. Two library files with same name and nominal pvts when specified in the same group or in the same libset are considered as two parts of the same library. Any new cells in the subsequent libraries are append to the library already present in the memory. Any cells in the second library file, which are already present in the first library are ignored. To avoid this warning, unify the cells in both the libraries into a single library file.

TECHLIB-460

NAME

TECHLIB-460

SUMMARY

The internal power arcs on the output/inout pin '%s' of cell '%s' does not have the related pin construct. This can cause problem for some application to generate the ecsm_power tables.

DESCRIPTION

For correct calculation of ecsm power tables related pin information should be provided in the

internal power tables.

TECHLIB-461

NAME

TECHLIB-461

SUMMARY

The %s %s on output/inout pin '%s' of cell '%s' is single dimensional. The power arc should be atleast two dimensional for correct generation of ecsm power tables i.e load and slew index point should be defined.

DESCRIPTION

For correct calculation of ecsm power the power arc should have atleast two dimensional template defined.

TECHLIB-604

NAME

TECHLIB-604

SUMMARY

Operating condition library '%s' not found in library set '%s'. Operating condition library must be part of library set. Check the library provided is internal library name and not the file name. Ignoring operating condition '%s'.

DESCRIPTION

This warning is encountered if the operating condition specified for a delay corner is not present in the timing library set specified for that delay corner. The user can specify the operating condition

with delay corner information like this - create_delay_corner -name xxxx -opcond OpCondName -opcond_library <OPCONDLIB>. This means that the operating condition for the delay corner needs to be picked up from the specified library. This library needs to be specified in the library set for the delay corner. To avoid this warning make sure to include the library containing the operating condition defined for a delay corner in the library set for that delay corner.

TECHLIB-606

NAME

TECHLIB-606

SUMMARY

An inconsistency was found during interpolated library checking of library set '%s'. Cell '%s' found in library '%s', but missing in library '%s'. This can potentially cause issues during delay calculation.

DESCRIPTION

This message is issued when inconsistency found due to the cell mismatch between the libraries during interpolation of library set. For example interpolated libarary set has two libraries and cell_1 is present in library_1 but missing in library_2. To fix the issue, re-characterize the library with appropriate settings, such that cell is present in library.

TECHLIB-608

NAME

TECHLIB-608

SUMMARY

An inconsistency was found during interpolated library checking of library set '%s'. The timing arc with related pin '%s', timing_type '%s', timing_sense '%s' %s of pin '%s' of cell '%s' is present in library '%s' but missing in library '%s'. This can potentially cause issues during delay calculation.

DESCRIPTION

This message is issued when inconsistency found due to the timing arc mismatch between the libraries during interpolation of library set. For example interpolated library set has two libararies and timing arc_1 defined for cell_1 is present in library_1 but missing for cell_1 in library_2. To fix the issue, re-characterize the library with appropriate settings, such that timing arc is present in library.

TECHLIB-609

NAME

TECHLIB-609

SUMMARY

Operating condition '%s' not found in library set '%s'. Ignoring operating condition '%s'.

DESCRIPTION

This message is issued when the operating condition name specified with commands 'update_delay_corner -opcond' and/or 'create_delay_corner -opcond' is not present in library set. To fix the issue, specify valid opcond name.

TECHLIB-620

NAME

TECHLIB-620

SUMMARY

Can not open %s for writing. Check the write permissions and path.

DESCRIPTION

This message is issued when software cannot open a file for writing. It could be the unix write permission issue.

TECHLIB-622

NAME

TECHLIB-622

SUMMARY

Could not read %s. Check the file path and read permissions.

DESCRIPTION

This message is issued when software cannot open a file to read. It could be the unix read permission issue.

TECHLIB-700

NAME

TECHLIB-700

SUMMARY

Cell %s is not a power switch cell, pin %s is specified switch pin. Ignoring 'switch_pin' attribute of this pin.

DESCRIPTION

'switch_pin' attribute specifies the enable pin of a power switch cell. The parent cell of this pin is not a power switch cell. To mark the cell as a power switch define 'switch_cell_type : ' at the cell level.

TECHLIB-701

NAME

TECHLIB-701

SUMMARY

Invalid axis specified for 'lut_template' %s. This axis type should be input_voltage/output_voltage. Ignoring this template.

DESCRIPTION

This message is issued when the axis type specified for the lut_template for dc_current group is invalid. The valid axes are input_voltage/output_voltage. Such template will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the valid axis type is defined.

TECHLIB-702

NAME

TECHLIB-702

SUMMARY

No pg_pin with name '%s' has been read in the cell '%s'. The attribute '%s' specified for the %s '%s' is being ignored.

DESCRIPTION

This message is issued when the pg_pin specified with related_power_pin/related_ground_pin/related_bias_pin does not exist at cell level. These attributes will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the undefined pg_pin is not used.

TECHLIB-703

NAME

TECHLIB-703

SUMMARY

Setting '%s' as the default value for the attribute '%s' for the pin '%s' for cell '%s'

DESCRIPTION

This message is issued when the pg_pin is not defined for the attributes related_power_pin or related_ground_pin of cell. In such cases the first pg_pin group having pg_type primary_power/primary_ground will be considered. To fix the issue, re-characterize the library with appropriate settings, such that the pg_pin is defined.

TECHLIB-704

NAME

TECHLIB-704

SUMMARY

The voltage_map attribute with name '%s' referenced by the pg_pin '%s' in the cell '%s', is absent in the library. The required voltage_map group needs to be added. This pg_pin is ignored. Related low power constructs referencing this pg_pin may not be read correctly.

DESCRIPTION

This message is issued when the attribute voltage_map with voltage_name referenced by pg_pin in the cell is not defined in the library. Such pg_pin will be ignored and any low power constructs referencing this pg_pin may not work as expected. To fix the issue, re-characterize the library with appropriate settings, such that the attribute volatge_map referenced by pg_pin is defined at library

level.

TECHLIB-705

NAME

TECHLIB-705

SUMMARY

The voltage_name attribute is missing in the pg_pin '%s' in the cell '%s'. This is a mandatory attribute for the pg_pin group. This pg_pin is ignored. Related low power constructs referencing this pg_pin may not be read correctly.

DESCRIPTION

This message is issued when the attribute voltage_name is not defined in the pg_pin group in the cell. The attribute voltage_name is mandatory attribute. Such pg_pin will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the volatge_map in pg_pin is specified.

TECHLIB-707

NAME

TECHLIB-707

SUMMARY

The attribute '%s' is missing in the dc_current group '%s' in cell '%s'. This may result in incorrect behavior later.

DESCRIPTION

This message is issued when the attributes related_switch_pin, related_pg_pin and

related_internal_pg_pin are not defined for dc_current group. To fix the issue, re-characterize the library with appropriate settings, such that the attributes should be specified for dc_current group.

TECHLIB-708

NAME

TECHLIB-708

SUMMARY

No pg_pin with name '%s' has been read in the cell '%s'. The attribute '%s' for the dc_current group '%s' is referencing this pg_pin. Ignoring this attribute value.

DESCRIPTION

This message is issued when the pg_pin specified with related_pg_pin/related_internal_pg_pin does not exist at cell level for dc_current group. Such attribute will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the pg_pin is defined.

TECHLIB-709

NAME

TECHLIB-709

SUMMARY

No lu_table_template with name '%s' has been read in the library '%s'. The dc_current group is ignored for cell '%s'.

DESCRIPTION

This message is issued when lu_table_template is specified in cell but not defined at library level. Such dc_current group will be ignored. To fix the issue, re-characterize the library with appropriate

settings, such that the lu_table_template is defined.

TECHLIB-710

NAME

TECHLIB-710

SUMMARY

EM group for cell: '%s' and pin: '%s' has negative values in the EM toggle rate group. This group will be ignored.

DESCRIPTION

This message is issued when the attribute values specified in the em_max_toggle_rate group is defined with negative value. Such EM group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the defined value is positive.

TECHLIB-711

NAME

TECHLIB-711

SUMMARY

EM group for cell: '%s' and pin: '%s' should have related_pin/related_bus_pin attribute defined for a two dimension EM toggle rate table. This group will be ignored.

DESCRIPTION

This message is issued when the attributes related_pin and related_bus_pin are not defined for an electromigration group specified with two-dimensional tables. For two-dimensional tables, related_pin and related_bus_pin are mandatory attributes in electromigration group. To fix the

issue, re-characterize the library with appropriate settings, such that the related_pin and related_bus_pin are defined.

TECHLIB-712

NAME

TECHLIB-712

SUMMARY

For the cell '%s', the lowerbound value '%f' is greater than upperbound value '%f' for the attribute '%s'. This is not permitted. The attribute is being ignored.

DESCRIPTION

This message is issued when the lowerbound value of attributes input_voltage_range/output_voltage_range is greater than the upperbound value of these attributes at cell level. To fix the issue, re-characterize the library with appropriate settings, such that the lowerbound/upperbound values are specified correctly.

TECHLIB-713

NAME

TECHLIB-713

SUMMARY

For the pin '%s' of cell '%s', the lowerbound value '%f' is greater than upperbound value '%f' for the attribute '%s'. The attribute is being ignored

DESCRIPTION

This message is issued when the lowerbound value of input_voltage_range and

output_voltage_range is greater than upperbound value for the pin of cell. To fix the issue, re-characterize the library with appropriate settings, such that the lowerbound value should be specified lower than the upperbound value.

TECHLIB-715

NAME

TECHLIB-715

SUMMARY

Power_rail '%s' specified in rail_connection '%s' of cell '%s' is not present in power_supply group. This rail_connection will be ignored.

DESCRIPTION

This message is issued when the attribute power_rail is specified in rail_connection of the cell but not specified in the power_supply group. For example, Power_rail 'VDD3' is specified in rail_connection 'PV3' of cell but is not present in power_supply group. Such rail_connection will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the power_rail should be specified in both i.e. rail_connection as well as power_supply_group.

TECHLIB-716

NAME

TECHLIB-716

SUMMARY

Number of primary outputs specified as the bundle members do not match with the number of bits in the sequential bank for cell '%s'. The bundle definition needs to be checked.

DESCRIPTION

This message is issued when there is a mismatch in bundle width and number of bits in the sequential bank. To fix the issue, re-characterize the library with appropriate settings, such that the number of bits should match with bundle width.

TECHLIB-800

NAME

TECHLIB-800

SUMMARY

For the timing arc of pin '%s' of cell '%s', the value '%s' specified for the user defined attribute domino_arc_typeis invalid. This attribute is being ignored.

DESCRIPTION

This message is issued when the value defined for domino_arc_type for the timing arc of pin of cell for user defined group is invalid. The valid values of domino_arc_type are clock_precharge, clock_eval and data_eval. The attribute will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the valid value is defined.

TECHLIB-802

NAME

TECHLIB-802

SUMMARY

The vector template '%s' for the vector group number '%d' specified in '%s' group of the timing arc in pin '%s' of cell '%s' is not defined. The CCS data for this current_rise/fall group is ignored

DESCRIPTION

This message is issued when an undefined template is used in vector groups output_current_fall and output_current_rise. Such output_current group would be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the template used is defined in output_current group.

TECHLIB-804

NAME

TECHLIB-804

SUMMARY

Invalid specification for input_net_transition axis for the vector group number '%d' specified in '%s' group of the timing arc in pin '%s' of cell '%s'. Only a single slew value is expected. The CCS data for this output current rise/fall group is ignored.

DESCRIPTION

This message is issued when the input_net_transition axis for the vector group specified in output_current_fall and output_current_rise has more than one value. The axis can have only single value. The CCS data for output_current_fall and output_current_rise group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that input_net_transition for output_current group should have only single value.

TECHLIB-805

NAME

TECHLIB-805

SUMMARY

Invalid specification for total_output_net_capacitance axis for the vector group number '%d' specified in '%s' group of the timing arc in pin '%s' of cell '%s'. Only a single cap value is expected. The CCS data for this output current rise/fall group is ignored

DESCRIPTION

This message is issued when the total_output_net_capacitance axis for the vector group specified in output_current_fall and output_current_rise has more than one value. The axis can have only single value. The CCS data for output_current_fall and output_current_rise group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that total_output_net_capacitance for output_current group should have only single value.

TECHLIB-806

NAME

TECHLIB-806

SUMMARY

Invalid axis specified for the vector group number '%d' specified in '%s' group of the timing arc in pin '%s' of cell '%s'. The CCS data for this output current rise/fall group is ignored

DESCRIPTION

This message is issued when the axes specified for the vector group output_current_fall and output_current_rise are invalid. The valid axes are input_net_transition and total_output_net_capacitance. Therefore CCS data will be ignored for this group. To fix the issue, re-characterize the library with appropriate settings, such that the defined axes should be valid.

TECHLIB-807

NAME

TECHLIB-807

SUMMARY

The axis '%s' is missing for the vector group number '%d' specified in '%s' group of the timing arc in pin '%s' of cell '%s'. The CCS data for this output current rise/fall group is ignored

DESCRIPTION

This message is issued when the axis input_net_transition or total_output_net_capacitance is missing for the vector group output_current_fall and output_current_rise of the timing arc in pin of the cell. The CCS data for this group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the axes should be specified for output_current_fall and output_current_rise.

TECHLIB-808

NAME

TECHLIB-808

SUMMARY

The number of current values is not equal to the number of time index points for the vector group number '%d' specified in '%s' group of the timing arc in pin '%s' of cell '%s'. The CCS data for this output current rise/fall group is ignored

DESCRIPTION

This message is issued when the number of current values is not equal to the time index points specified in the output_current_fall and output_current_rise of the timing arc in pin of cell. The CCS data for this group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the number of time index points should match with the current values for output_current_fall and output_current_rise.

TECHLIB-809

NAME

TECHLIB-809

SUMMARY

Time values of the vector group number '%d' specified in '%s' group of the timing arc in pin '%s' of cell '%s', should monotonically increase.

DESCRIPTION

This message is issued when the time values specified in the vector groups output_current_fall and output_current_rise of the timing arc in pin of cell do not monotonically increase. To fix the issue, re-characterize the library with appropriate settings, such that the time values for output_current_fall and output_current_rise groups vector are monotonic.

TECHLIB-810

NAME

TECHLIB-810

SUMMARY

Both the '%s' groups must be specified for the timing arc in pin '%s' of cell '%s'. The receiver capacitance data for this timing arc is ignored

DESCRIPTION

This message is issued when any of the receiver_capacitance1_rise, receiver_capacitance1_fall, receiver_capacitance2_rise, receiver_capacitance2_fall is missing for the timing arc in pin of the cell of receiver_capacitance group. All of them must be defined if any one of them is defined. Such receiver_capacitance data for this timing arc will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the receiver_capacitance group is defined correctly.

TECHLIB-811

NAME

TECHLIB-811

SUMMARY

Undefined template '%s' for the '%s' group specified for the timing arc in pin '%s' of cell '%s'. The receiver capacitance data for this timing arc is ignored.

DESCRIPTION

This message is issued when an undefined template is used in receiver_capacitance_rise and receiver_capacitance_fall groups. Such receiver_capacitance data for this timing arc would be ignored.To fix the issue, re-characterize the library with appropriate settings, such that the template used is defined in library.

TECHLIB-812

NAME

TECHLIB-812

SUMMARY

The number of cap values in the '%s' group specified in the timing arc in pin '%s' of cell '%s' is not equal to the number of index points specified. The receiver capacitance data for this timing arc is ignored.

DESCRIPTION

This message is issued when the number of cap values in the receiver_capacitance_rise1/receiver_capacitance_rise2/receiver_capacitance_fall1/receiver_capacitance_fall2 specified in the timing arc in pin of cell is not equal to the number of index points. Such

receiver_capacitance data for this timing arc will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the number of cap values and index points match.

TECHLIB-814

NAME

TECHLIB-814

SUMMARY

Number of vector groups(%d) specified in '%s' group of timing arc in pin '%s' of cell '%s' do not match unique slew/load(%dx%d) pair value. This output current group will be ignored.

DESCRIPTION

This message is issued when there is mismatch in the number of vector groups and unique slew/load pair. For this output current group, conversion of the CCS vector groups to ECSM waveform groups is ignored for timing analysis. This may impact delay calculation accuracy. Re-characterize the library such that output current group is specified correctly.

TECHLIB-816

NAME

TECHLIB-816

SUMMARY

The receiver_capacitance group specified over the output pin '%s' of cell '%s' is ignored.

DESCRIPTION

This message is issued when the receiver_capacitance group is specified on the output pin of cell. The receiver_capacitance group can be defined on input pin or inout pin at pin level. The

receiver_capacitance group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the receiver_capacitance group is not specified on output pin of the cell.

TECHLIB-817

NAME

TECHLIB-817

SUMMARY

The receiver capacitance %s groups are missing in the receiver capacitance group %s specified for %s of cell '%s'.

DESCRIPTION

This message is issued when either of the rise group (receiver_capacitance1_rise/receiver_capacitance2_rise) or fall group (receiver_capacitance1_fall/receiver_capacitance2_fall) is missing for pin in the receiver_capacitance group for a 'when' condition. If there are duplicate 'when' conditions, this data must be present for at least one of the 'when' condition. In such case, other receiver_capacitance group with same 'when' condition need not have all 4 groups. They can just have either rise or fall groups. To fix the issue, re-characterize the library with appropriate settings, such that the receiver_capacitance group is defined correctly.

TECHLIB-818

NAME

TECHLIB-818

SUMMARY

Only input_net_transition axis is expected for '%s' group defined within receiver_capacitance group specified on the pin '%s' of cell '%s'. This receiver_capacitance group is ignored.

DESCRIPTION

This message is issued when the invalid axis is defined for receiver_capacitance1_rise/receiver_capacitance2_rise/receiver_capacitance1_fall/receiver_capacitance2_fall on the pin of the cell for receiver_capacitance group. The valid axis is only input_net_transition. Such receiver_capacitance group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the input_net_transition axis should be specified for receiver_capacitance group.

TECHLIB-819

NAME

TECHLIB-819

SUMMARY

The number of cap values is not equal to the number of time index points for the '%s' group specified in pin '%s' of cell '%s'. This receiver_capacitance group is ignored.

DESCRIPTION

This message is issued when the number of capacitance value is specified for receiver_capacitance_rise1/receiver_capacitance_rise2/receiver_capacitance_fall1/receiver_capacitance_fall2 are not equal to the number of time index points. Such receiver_capacitance group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the number of cap value should be equal to the number of time index points.

TECHLIB-820

NAME

TECHLIB-820

SUMMARY

Undefined template '%s' for the '%s' group specified for the pin '%s' of cell '%s'. The receiver capacitance data for this pin is ignored.

DESCRIPTION

This message is issued when an undefined template is used in receiver_capacitance1_rise/receiver_capacitance2_rise/ receiver_capacitance1_fall/receiver_capacitance2_fall groups. Such receiver_capacitance data for this pin would be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the template used is defined in library.

TECHLIB-827

NAME

TECHLIB-827

SUMMARY

The support to threshold construct in ecsm capacitance group has be provided post ECSM VERSION 1.2. The library ECSM VERSION is %s, therefore the threshold construct will be ignored for the ecsm capacitance group in pin '%s' and cell '%s'.

DESCRIPTION

This message is issued when threshold_pct construct in ecsm_capacitance group is specified in library but the ECSM VERSION<1.2. Threshold construct will be ignored for the ecsm capacitance group.

TECHLIB-828

NAME

TECHLIB-828

SUMMARY

The 'pulse_generator' and 'pulse_generator_polarity' attributes are obsolete, as specified over the pin '%s' of the cell '%s'. The 'pulse_clock' attribute should be used instead.

DESCRIPTION

This message is issued when the attributes pulse_generator and pulse_generator_polarity are specified on the pins of the cell. The pulse_clock attribute should be defined instead of pulse_generator and pulse_generator_polarity, as they are discontinued now. To fix the issue, re-characterize the library with appropriate settings, such that the pulse_clock should be defined.

TECHLIB-904

NAME

TECHLIB-904

SUMMARY

Cell '%s' has both edge and combinational arcs between pins '%s' and '%s'. Such arcs can cause problems in the timing analysis flow.

DESCRIPTION

For correct timing analysis both combinational and edge arcs should not be present between two pins.

TECHLIB-905

NAME

TECHLIB-905

SUMMARY

Found a function attribute specified on pin '%s' with 'interface_timing' attribute set to true on cell '%s'. As per the liberty standard, a function attribute should not be specified for a cell which has interface_timing attribute set to true. This function attribute will be ignored.

DESCRIPTION

When 'interface_timing: true', the cell is regarded as a complex black box cell instead of a regular standard cell and 'function' attribute should not be specified for a black box cell. Re-characterize the library such that the correct attribute is set on the cell.

TECHLIB-906

NAME

TECHLIB-906

SUMMARY

Input Timing Library '%s' already loaded in the session. write_ldb command will not work for this library.

DESCRIPTION

For correct ldb generation write_ldb command should be invoked in a separate session.

TECHLIB-908

NAME

TECHLIB-908

SUMMARY

The ccsn_last_stage group is present on the timing arc, but the ccsn_first_stage is not present on %s and cell '%s'. The ccsn_last_stage group can be present on a timing arc only when cssn_first_stage group is present. The ccsn_last_stage group will be ignored.

DESCRIPTION

The timing group can contain a ccsn_last_group only when ccsn_first_stage group is present. Otherwise it can cause problems during noise analysis.

TECHLIB-914

NAME

TECHLIB-914

SUMMARY

The vector template '%s' for the vector group number '%d' specified in '%s' group on pin '%s' of cell '%s' is not defined. The CCS Noise data for this %s group is ignored

DESCRIPTION

This message is issued when the vector template of vector group output_voltage_fall and output_voltage_rise is not defined. Therefore CCS noise data for this group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the vector template used for output_voltage_fall and output_voltage_rise groups is defined in library.

TECHLIB-915

NAME

TECHLIB-915

SUMMARY

Invalid axis '%s' specified for the vector group number '%d' specified in '%s' group on pin '%s' of cell '%s'. The CCS Noise data for this %s group is ignored

DESCRIPTION

This message is issued when the axis type specified for the vector group output_voltage_rise/output_voltage_fall is invalid. The valid axes are input_net_transition and total_output_net_capacitance. Such ccs noise data will be ignored for this group. To fix the issue, re-characterize the library with appropriate settings, such that the valid axis type is defined.

TECHLIB-916

NAME

TECHLIB-916

SUMMARY

The number of time index points does not match with the voltage values of vector group number '%d' specified in '%s' group on pin '%s' of cell '%s'. The CCS Noise data for this %s group is ignored

DESCRIPTION

This message is issued when the voltage value of vector groups propagated_noise_high and propagated_noise_low of a cell do not match with the number of time index points. Therefore CCS noise data for this group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the number of time index points should match with the voltage values of vector

group propagated_noise_high and propagated_noise_low.

TECHLIB-919

NAME

TECHLIB-919

SUMMARY

The pin level %s group(s) found on %s %s of cell '%s'. The pin level %s group(s) are expected only on %s or inout pins, therefore the %s group(s) will be ignored.

DESCRIPTION

This message is issued when the ccsn_first_stage group is defined at pin level on output pin or the ccsn_last_stage is defined on input pin of a cell. The ccsn_first_stage group can be defined only on an input pin or inout pin and the ccsn_last_stage can be defined only on an output pin or inout pin. If ccsn group is not defined at proper pin then they will be ignored. To fix the issue, re-characterize the library with appropriate settings.

TECHLIB-921

NAME

TECHLIB-921

SUMMARY

Invalid number of index_%d points specified for the vector group number '%d', in '%s' group on pin '%s' of cell '%s'. Only single value is expected for this index. The CCS Noise data for this %s group is ignored.

DESCRIPTION

This message is issued when the vector group output_voltage_fall and output_voltage_rise of a cell are not specified with correct number of index points. The axes input_net_transition/total_output_net_capacitance i.e. index_1 and index_2 can have only single value for the vector group output_voltage_fall and output_voltage_rise. To fix the issue, re-characterize the library with appropriate settings, such that the number of index points should be specified correctly for output_voltage_fall and output_voltage_rise groups.

TECHLIB-922

NAME

TECHLIB-922

SUMMARY

The stage_type of ccsn_*_stage group does not match with the pin's driver type '%s' of cell '%s'. The stage_type of CCSN group must match with the pin's driver type. This ccsn_*_stage group will therefore be ignored.

DESCRIPTION

This message is issued when the ccsn_first_stage and ccsn_last_stage groups are not defined with correct driver type. The valid values are pull_up and pull_down. Therefore ccsn_stage group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the correct driver type should be defined.

TECHLIB-924

NAME

TECHLIB-924

SUMMARY

Unable to read the LDB file because it has been compiled with a newer version '%s' of the software than you are currently using. Either recompile it with a compatible version '%s' of the software, or

use the equivalent Liberty (.lib) format.

DESCRIPTION

Cadence supports backward compatibility between newer versions of the software and LDB timing libraries compiled using older releases, but the reverse is not possible. The reason is that whenever a new syntax is added or adopted from the Liberty library specification, the binary representation of that data in the form of the LDB file will change, and older versions of the software will not be able to interpret the new library syntax properly. To use this library data, you must either recompile the library with a compatible version of the software, or use the uncompiled (.lib) version of the Liberty library.

TECHLIB-925

NAME

TECHLIB-925

SUMMARY

Input library file '%s' contains more than one library definition. This is not supported for LDB conversion. Separate the library definitions to individual files for converting to individual LDBs. Output LDB '%s' not written.

DESCRIPTION

This message is issued when a single file contains more than one library definition. LDB conversion is not possible for such libraries because tool will read only first library and rest will be ignored.

TECHLIB-935

NAME

TECHLIB-935

SUMMARY

No indices specified for the ecsm capacitance in pin %s of cell %s. Ignoring ecsm_capacitance defined in the pin.

DESCRIPTION

The index_1 attribute needs to be defined for ecsm_capacitance. If it is not defined, the ecsm_capacitance information will be ignored

TECHLIB-1001

NAME

TECHLIB-1001

SUMMARY

Multiple normalized driver waveform groups without a driver_waveform_name were found. The latest definition would overwrite the earlier ones.

DESCRIPTION

This message is issued when the normalized driver waveform group is defined multiple times but driver_waveform_name is absent. The latest definition will be retained and rest will be ignored.

TECHLIB-1002

NAME

TECHLIB-1002

SUMMARY

Mismatch found in the number of index points for '%s' in the normalized_driver_waveform and its template. The normalized_driver_waveform data at the group level will be used.

DESCRIPTION

This message is issued when the number of index points are different in the normalized_driver_waveform group and its template at the library level. Data specified in the template will be ignored and data specified in the normalized_driver_waveform group will be used.

TECHLIB-1003

NAME

TECHLIB-1003

SUMMARY

The number of values in the normalized_driver_waveform group does not match the number of index points. This could cause delay calculation issues and should be corrected

DESCRIPTION

This message is issued when there is discrepancy between the number of values (M x N) in the normalized_driver_waveform group and number of index points M and N. This may result in a loss of accuracy during analysis.

TECHLIB-1004

NAME

TECHLIB-1004

SUMMARY

The normalized_driver_waveform group is specified with only one axis. This may result in accuracy

loss during analysis.

DESCRIPTION

This message is issued when the normalized_driver_waveform is specified with only one axis i.e. either input_net_transition or normalized_voltage only is specified as axis. This may cause inaccuracy in timing analysis. To fix the issue, re-characterize the library with appropriate settings, such that the normalized_driver_waveform should be specified with both axes.

TECHLIB-1005

NAME

TECHLIB-1005

SUMMARY

The normalized_driver_waveform '%s' specified as '%s' for cell '%s' was not found in the library

DESCRIPTION

This message is issued when the normalized_driver_waveform is specified as driver_waveform/driver_waveform_rise/driver_waveform_fall for a cell but is not defined in library. To fix the issue, re-characterize the library with appropriate settings, such that the library does not use undefined normailzed_driver_waveform.

TECHLIB-1006

NAME

TECHLIB-1006

SUMMARY

The normalized_driver_waveform '%s' specified as '%s' for pin '%s' in cell '%s' was not found in the

library

DESCRIPTION

This message is issued when the normalized_driver_waveform is specified as driver_waveform/driver_waveform_rise/driver_waveform_fall for a pin in a cell but is not found in library. To fix the issue, re-characterize the library with appropriate settings, such that the library does not use undefined normailzed_driver_waveform.

TECHLIB-1007

NAME

TECHLIB-1007

SUMMARY

Incorrect axis type specified in the template '%s' for driver waveform. The template and all normalized_driver_waveform groups using this template would be ignored.

DESCRIPTION

This message is issued when the axis type is specified in the normalized_driver_waveform group template is not correct. The valid axes are input_net_transition and normalized_voltage. The template and all normalized_driver_waveform groups using this template would be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the template should be specified with correct axis type.

TECHLIB-1010

NAME

TECHLIB-1010

SUMMARY

Template of the name '%s' was not found in the library. The driver waveform group at (line no: %d) would be ignored.

DESCRIPTION

This message is issued when an undefined template is used in driver waveform group. Such driver waveform group would be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the template used is defined in library.

TECHLIB-1051

NAME

TECHLIB-1051

SUMMARY

Library reading has failed due to an error that occurred in one of the libraries to be merged. Refer to the previous messages issued to find the details of the issue in the library.

DESCRIPTION

This message is issued when library reading is failed due to some error in library. Refer to the previous messages issued to find the details of the issue. For example: if there is some syntax error then library reading will be failed.

TECHLIB-1056

NAME

TECHLIB-1056

SUMMARY

Missing cell:%s in 'library:%s ' but present in 'library:%s'. The libraries cannot be used for merging.

DESCRIPTION

This message is issued when there is discrepancy between the nominal PVT of two timing libraries having same library name in library header. To fix the issue, re-characterize the library with appropriate settings, such that the library should be specified with different name.

TECHLIB-1064

NAME

TECHLIB-1064

SUMMARY

Missing internal pin '%s' in cell '%s' of library '%s ' but present in library '%s'.

DESCRIPTION

This message is issued when the internal pin is missing in a cell of one library but specified in other library.

TECHLIB-1068

NAME

TECHLIB-1068

SUMMARY

Identified number of pins mismatch for cell '%s' between library '%s' and '%s'

DESCRIPTION

This message is issued when there is mismatch in number of pins for cell between the libraries. To fix the issue, re-characterize the library with appropriate settings, such that the number of pins should match for cell between libraries.

TECHLIB-1069

NAME

TECHLIB-1069

SUMMARY

The number of cells are more than one in library '%s'. The ETM libraries should have only one cell. The libraries cannot be used for merging.

DESCRIPTION

This message is issued when the ETM libraries is having more than one cell. Multiple cells are not allowed in ETM libraries. Such libraries cannot be merged.

TECHLIB-1070

NAME

TECHLIB-1070

SUMMARY

No AOCV libraries have been read.

DESCRIPTION

This message is issued when AOCV libraries have not been loaded in the session. Use

create_library_set -aocv command to load AOCV libraries.

TECHLIB-1071

NAME

TECHLIB-1071

SUMMARY

Identified pin capacitance mismatch '%f' and '%f' in pin '%s', for cell '%s', between libraries '%s' and '%s'. The libraries cannot be used for merging.

DESCRIPTION

This message is issued when there is discrepancy between the pin capacitance of a cell pin in two libraries. This may not permit the merging of these two libraries. To fix the issue, re-characterize the library with appropriate settings, such that there is no discrepency in pin capacitance across two libraries.

TECHLIB-1073

NAME

TECHLIB-1073

SUMMARY

Identified mismatch in %s definition in pin '%s', for cell '%s', between libraries '%s and '%s'. The %s definition will be ignored in merged library.

DESCRIPTION

This message is issued when there is discrepancy between the definition of function and three_state function in a pin of a cell of two libraries. To fix the issue, re-characterize the library with

appropriate settings, such that the library should be specified with different name.

TECHLIB-1076

NAME

TECHLIB-1076

SUMMARY

The vector template '%s' for the vector group number '%d' of cell '%s' is not defined in pg_current group. The CCS power data in this group is ignored

DESCRIPTION

This message is issued when the vector template for the vector group of cell is not defined in pg_current group. The CCS power data in this group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the template name should be defined for pg_current group.

TECHLIB-1077

NAME

TECHLIB-1077

SUMMARY

Invalid specification for input_net_transition/total_output_net_capacitance axis for the vector group '%s' specified in pg_current group. Only a single slew/cap value is expected. The CCS Power data for this pg_current group is ignored.

DESCRIPTION

This message is issued when the input_net_transition/total_output_net_capacitance indices for the

vector group specified in pg_current group have more than one value. These attributes can have only single value. The CCS Power data for such pg_current group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that input_net_transition/total_output_net_capacitance in pg_current group have only single value.

TECHLIB-1078

NAME

TECHLIB-1078

SUMMARY

The number of current values is not equal to the number of time index points for the vector group number '%d' specified in pg_current. The CCS Power data for this pg_current group is ignored

DESCRIPTION

This message is issued when the number of current values in CCS power data for pg_current group is not matched with the number of time index points. CCS power data for such pg_current group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the number of current values is equal to the number of time index points.

TECHLIB-1103

NAME

TECHLIB-1103

SUMMARY

The number of pins in input_map for the pin '%s' of cell '%s' doesn't match the number of inputs given in the state table. This may cause issues in function inference from state table.

DESCRIPTION

This message is issued when there is a discrepancy between the number of inputs given in the state table and number of pins in input_map for the pin of the cell. This may cause issues in function inference from state table. To fix the issue, re-characterize the library with appropriate settings, such that the number of inputs in the state table is equal to the number of pins in input_map.

TECHLIB-1104

NAME

TECHLIB-1104

SUMMARY

Time values of the %s specified in '%s' group of cell '%s', should monotonically increase.

DESCRIPTION

This message is issued when the time values specified in the ccs_power vector group of a cell do not monotonically increase. To fix the issue, re-characterize the library with appropriate settings, such that the time value for the ccs_power vector group are monotonic.

TECHLIB-1105

NAME

TECHLIB-1105

SUMMARY

Vector groups specified in '%s' group of cell '%s' are not defined for every slew and load pair value. This may lead to undesirable analysis results.

DESCRIPTION

This message is issued when vector group is not defined for each load and slew pair. The vector

group should be defined for each slew and load pair and number of vector group should match with slew * cap value pair. To fix the issue, re-characterize the library with appropriate settings such that corresponding vector groups are defined for each slew and load pair.

TECHLIB-1106

NAME

TECHLIB-1106

SUMMARY

The operating condition '%s' with PVT ('%.4f', '%.4f', '%.4f') already exists in the library '%s'. The new operating condition PVT ('%.4f', '%.4f', '%.4f') will be ignored.

DESCRIPTION

This message is issued when an operating conditions with pvt values is specified but a previous operating condition with same PVT definition already exists in the library. The new operating conditions with PVT values will be ignored.To fix the issue, re-characterize the library with appropriate settings, such that same PVT conditions are not specified in two different oprerating conditions.

TECHLIB-1107

NAME

TECHLIB-1107

SUMMARY

The phase %d is not supported for retention pin for cell %s, pin %s. The retention pin would be ignored.

DESCRIPTION

Unrecognized phase/retention_disable_value for state retention power gating pin/retention pin. The cell cannot be used for SRPG synthesis

TECHLIB-1108

NAME

TECHLIB-1108

SUMMARY

No normalized driver waveform found in this library. This can cause accuracy issues during delay calculation.

DESCRIPTION

The normalized driver waveform is required for higher precision during delay calculation.

TECHLIB-1109

NAME

TECHLIB-1109

SUMMARY

Nominal Condition '%s' is not defined in timing library. Assuming default value %.3f. Setting this attribute is recommended as it can impact timing and SI results.

DESCRIPTION

This message is issued when the nominal condition PVT is not defined in the timing library and thus it assumes the default values. The default value of Process is 1, default value of voltage is 5 and default value of temperature is 25. The nominal condition attributes should be set appropriately.

TECHLIB-1114

NAME

TECHLIB-1114

SUMMARY

There is mismatch between '%s' tables for '%s' arc defined on pin '%s' of cell '%s' for mode '%s' specified with command merge_model_timing.

DESCRIPTION

This message is issued when there is mismatch in rise_constarint/fall_constraint tables defined for minimum_pulse_width/minimum_period arc while merging the libraries using command 'merge_model_timing' for a specified mode. To fix the issue, specified the libraries with consistent tables.

TECHLIB-1115

NAME

TECHLIB-1115

SUMMARY

Multiple definitions of the power_rail '%s' for the power_supply group at line %d. The last definition would be retained

DESCRIPTION

This message is issued when power_rail for power_supply group is defined more than once. The same attribute cannot have multiple definition. Last definition will be retained and rest will be ignored.

TECHLIB-1116

NAME

TECHLIB-1116

SUMMARY

Multiple definitions of the voltage '%s' for the voltage_map at line %d. The first definition would be retained

DESCRIPTION

This message is issued when a supply voltage is defined more than once with different values in voltage_map. The same voltage cannot have multiple definition. First definition will be retained and rest will be ignored.

TECHLIB-1117

NAME

TECHLIB-1117

SUMMARY

Power supply group at line %d has no default_power_rail attribute defined.

DESCRIPTION

This message is issued when the attribute default_power_rail is not present for power supply group. To fix the issue, re-characterize the library with appropriate settings, such that this attribute is specified for power supply group.

TECHLIB-1118

NAME

TECHLIB-1118

SUMMARY

Cell %s is an Isolation cell, pin %s is specified level shifter %s pin. Ignoring '%s' attribute of this pin.

DESCRIPTION

'level_shifter_enable_pin' and level_shifter_data_pin attribute specifies the enable pin and data pin of a level shifter cell respectively. The parent cell of this pin is not a level shifter cell. To mark the cell as a level shifter cell mention 'is_level_shifter : true' at the cell level.

TECHLIB-1119

NAME

TECHLIB-1119

SUMMARY

Conflicting definition of user defined %s attribute %s. It is defined as %s in present library and as %s in previous library '%s'.

DESCRIPTION

This message is issued when there is conflict between the attributes defined by the user in the present library and defined in the previous library. To fix the issue, re-characterize the library with appropriate settings, such that there should not be mismatch between the attributes across libraries.

TECHLIB-1120

NAME

TECHLIB-1120

SUMMARY

Input map for bus/bundle %s for cell %s is not defined on all pins.

DESCRIPTION

This message is issued when the input map for bus/bundle is not defined on all pins of a bus/bundle. To fix the issue, re-characterize the library with appropriate settings, such that the input map for bus/bundle should be defined on all pins at cell level.

TECHLIB-1123

NAME

TECHLIB-1123

SUMMARY

Identified multiple definitions of the related_pin for the '%s' group defined on pin '%s' of cell '%s'. The first definition would be retained and rest will be ignored.

DESCRIPTION

This message is issued when related_pin is specified more than once for max_trans and max_cap groups defined at pin level. The first definition would be retained and rest will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the related_pin is defined correctly.

TECHLIB-1131

NAME

TECHLIB-1131

SUMMARY

The normalized driver waveform '%s' will be extrapolated to span the voltage range 0 to 1.

DESCRIPTION

This message is issued when the voltage range of normalized_driver_waveform is specified within the range of 0 to 1 but does not span fully from 0 to 1. In such cases, tool will extrapolate to span the voltage from 0 to 1. To fix the issue, re-characterize the library with appropriate settings, such that the normalized_driver_waveform should be defined with appropriate voltage range.

TECHLIB-1135

NAME

TECHLIB-1135

SUMMARY

Identified multiple spatial table for %s '%s'. The first table would be retained.

DESCRIPTION

This message is issued when the multiple spatial tables are defined at cell level. The first definition will be considered and rest will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the spatial tables are defined correctly.

TECHLIB-1141

NAME

TECHLIB-1141

SUMMARY

Cell '%s' redefined in library. The first cell definition will be retained, rest will be ignored.

DESCRIPTION

Cell re-definitions in a library is not allowed. In case of multiple definitions for the same cell name, only the first definition is retained and rest are ignored. In order to retain all cell definitions, the cell names must be unique. Modify the cell definition in library by changing name of cells such that all the cells are distinct

TECHLIB-1142

NAME

TECHLIB-1142

SUMMARY

No 'values' attribute found for normalized driver waveform group at line number %d. This is a mandatory attribute for normalized waveform group. This group will be ignored.

DESCRIPTION

The normalized driver waveform group should have mandatory attribute 'values'. If this attribute is not present the characterized library is incorrect and the library should be re-characterized.

TECHLIB-1143

NAME

TECHLIB-1143

SUMMARY

The pin '%s' in the statetable/input_map is not defined in the cell '%s'. The statetable will be ignored. Fix incorrect pin names or any special characters in the statetable to rectify the error.

DESCRIPTION

The pin names defined in the input_map or statetable should be the same as defined in the library cell definition. Also, per liberty statetable syntax, pin names are identified based on white space delimiter. Any special characters, if any in the statetable, separated by white spaces could be also be identified as pins. To rectify the Error, correct the incorrect pin names or remove special characters from the statetable, if any.

TECHLIB-1144

NAME

TECHLIB-1144

SUMMARY

The pg pin '%s' has also been defined as pin in cell '%s'. The pin will be retained, but the pg_pin will be ignored. Correct the pin names in library cell definition to fix the error.

DESCRIPTION

This error is displayed when both pg_pin and pin of a cell defined in the library, have the same name. The cell definition in the library must have unique pin names for pin and pg_pin for a cell. Due to this error, the software will retain the pin and ignore the pg_pin in the cell definition. The pin

name with pg_pin attribute will be ignored. This may lead to issues during design load and analysis, especially if the design includes pg information.

TECHLIB-1145

NAME

TECHLIB-1145

SUMMARY

Message with id '%d' not found.

DESCRIPTION

This message is issued when valid message id is not specified.

TECHLIB-1146

NAME

TECHLIB-1146

SUMMARY

Mismatch between values of library global(s) set during LDB reading versus those set during LDB compilation. For a detailed list of library global settings, you can use the 'check_ldb_version' command. To avoid this warning, recompile LDBs with the same library global values

DESCRIPTION

This warning is issued when the library global settings, set during LDB compilation, do not have the same values as those set while reading LDBs. To rectify this issue, you need to recompile the LDBs with the same library global setting(s). The recommended settings for LDB compilation are the software default settings.

TECHLIB-1147

NAME

TECHLIB-1147

SUMMARY

Equivalent waveform model and/or waveform propagation mode is enabled for delay calculation during analysis. This requires normalized driver waveform (NDW) information in timing libraries. The timing libraries used in the design are missing NDW information. The software will auto-generate the NDW information to be used for analysis.

DESCRIPTION

The software auto-generates the NDW waveform by weighted mean of linear and exponential waveform. The default value of weighted mean is 0.5 and it can be controlled using the 'timing_normalized_driver_waveform_weight_factor' global variable.

TECHLIB-1148

NAME

TECHLIB-1148

SUMMARY

Found redefined indices in the ecsm_capacitance group of timing arc section of cell '%s'. Indices cannot be redefined in the ecsm_capacitance group of timing arc section as this group would use the indices of transition table. This can cause issues during delay calculation.

DESCRIPTION

In timing arc section, the ECSM Capacitance group defined is 2 dimensional and would use the

indices of transition table. The ECSM capacitance are not expected to have index_1 or index_2 defined in this group of timing arc section.

TECHLIB-1150

NAME

TECHLIB-1150

SUMMARY

The template '%s' for dc_current group on pin '%s' of cell '%s' is not defined. The 'dc_current' group will be ignored.

DESCRIPTION

The dc_current group should have a template defined at library level otherwise group will be ignored. To rectify the problem define the template at library level.

TECHLIB-1151

NAME

TECHLIB-1151

SUMMARY

Invalid axis '%s' specified for '%s' group referred by template name '%s' on pin '%s' of cell '%s'. This group is ignored.

DESCRIPTION

The valid index name needs to be specified for group template. To rectify the problem change the variable_1 or variable_2 or variable_3 to these valid values in the template group.

TECHLIB-1152

NAME

TECHLIB-1152

SUMMARY

Identified path_depth axis for the ocv derate group '%s' referred by '%s' attribute. This path_depth axis is not allowed for ocv derate distance group. This attribute will be ignored.

DESCRIPTION

When the ocv derate group is referred by ocv_derate_distance_group or default_ocv_derate_distance_group should have template with distance as axis name. If any template has path_depth as axis then this ocv group will not be applied for specified cell or library level group.

TECHLIB-1153

NAME

TECHLIB-1153

SUMMARY

The ocv derate group name '%s' referred by '%s' attribute is not defined at %s level. This attribute is ignored.

DESCRIPTION

The default_ocv_derate_group/default_ocv_derate_distance_group/ocv_derate_group/ocv_derate_distance_group name referred should be defined at library level otherwise it will be ignored. The cell specific ocv derate group can be defined at cell level as well. The issue can be rectified by

specifying the ocv derate group at library level or cell specific derate at cell level.

TECHLIB-1154

NAME

TECHLIB-1154

SUMMARY

Identified more than one leakage_power groups with same condition in cell '%s', Last definition will be retained.

DESCRIPTION

Identified more than one leakage_power groups with same condition in cell <cellName>. The last definition will be retained.

TECHLIB-1156

NAME

TECHLIB-1156

SUMMARY

The nominal PVT (%.2f, %.2f, %.2f) of timing library '%s' does not match with previously read timing library of the same name with nominal PVT (%.2f, %.2f, %.2f). To read this library you must change the library name.

DESCRIPTION

This message is issued when there is discrepancy between the nominal PVT of two timing libraries having same library name in library header. To fix the issue, re-characterize the library with appropriate settings, such that the library should be specified with different name.

TECHLIB-1157

NAME

TECHLIB-1157

SUMMARY

Identified non monotonic time value during CCS to ECSM conversion.

DESCRIPTION

This is a debug message which would be flagged only when the global timing_library_debug_mode_on is set.

TECHLIB-1161

NAME

TECHLIB-1161

SUMMARY

The library level attribute %s on line %d is defined after at least one cell definition. The attribute will be ignored.

DESCRIPTION

This message is issued when any library level simple or complex attribute is defined after the cell definition in library file. Since such attributes are applicable for all cells in design, they must be specified before the cell definition.

TECHLIB-1170

NAME

TECHLIB-1170

SUMMARY

Name of '%s' group is missing on line %d. To fix this issue, define the missing group name in the library.

DESCRIPTION

The message is issued when a group such as cell, pin etc., is defined in the library without any name. For example, the group pin is defined as: pin. To rectify the issue, correct the library to define the missing name of the group in the library.

TECHLIB-1171

NAME

TECHLIB-1171

SUMMARY

The attribute '%s' of group '%s' has one or more values which are %s. This may lead to unexpected analysis results.

DESCRIPTION

The message is issued when attribute values defined are beyond the value/range. Beyond the range could include, less than, less than equal to, greater than or greater than equal to. Valid values could be integers, 0,1 or n and float values. This may lead to unexpected results in analysis. To fix the issue, re-characterize the library with appropriate settings to have requisite values per the standard for the attributes for which this message is issued.

TECHLIB-1172

NAME

TECHLIB-1172

SUMMARY

The '%s' attribute has been defined more than once for group '%s' on line %d. The attribute should be defined only once.

DESCRIPTION

The message is issued when multiple values has been defined within a group. For example, index_1 in lu_table_template group is defined more than once. Each attribute should be defined only once per group. To fix the issue, re-characterize the library with appropriate settings.

TECHLIB-1173

NAME

TECHLIB-1173

SUMMARY

The '%s' attribute has not been defined for %s '%s' on line %d. This may lead to undesirable analysis results. To fix this issue, define the missing attribute in library.

DESCRIPTION

The message is issued when an expected attribute is not defined for a group. For example, directionattribute expected for the pingroup is not defined in the library. To fix the issue, define the missing attribute in the library or re-characterize the library with appropriate settings.

TECHLIB-1174

NAME

TECHLIB-1174

SUMMARY

The attribute '%s' defined in group '%s' on line %d is not monotonically %s for values '%f' to '%f'. This may lead to undesirable analysis results.

DESCRIPTION

The message is issued when an attribute range does not increase or decrease monotonically as per the Liberty standard or convention. For example, instead of the expected range of monotonically increasing index_1: (1, 2, 3, 4, 5), the range defined in library is index_1: (1, 2, 3, 2, 3). To fix the issue, re-characterize the library with appropriate settings.

TECHLIB-1175

NAME

TECHLIB-1175

SUMMARY

Template name '%s' used in group '%s' on line %d is not defined in the library. To fix this issue, define the missing template in the library.

DESCRIPTION

The message is issued when a template name which has not been defined in the library, has been specified in a table group. For example, the group 'cell_rise(abc)' given, but the template name 'abc' has not been defined in the library. To rectify the issue, correct the library to define the missing template definition.

TECHLIB-1176

NAME

TECHLIB-1176

SUMMARY

The table size (%d) of the lookup table group '%s' on line %d is not as per the indices definition '%s'. This may lead to unexpected analysis results.

DESCRIPTION

The message is issued when the table size of the lookup table in the library is different from the expected size. The expected size is (size of index_1) x (size of index_2). For example, index_1: (1, 2); index_2: (3, 4); values (1, 2,3 ,4, 5, 6,7). The size of look up table here is 7, whereas the expected size of table in this case is (2x2). To fix the issue, re-characterize the library with appropriate settings.

TECHLIB-1177

NAME

TECHLIB-1177

SUMMARY

'index_%d' defined in '%s' group should have at least '%d' float values. This may lead to undesirable analysis results.

DESCRIPTION

The message is issued when any index specified in the library has less than the minimum number of float values expected To fix this issue, re-characterize the library such that all indices match the

expected number of float values.

TECHLIB-1179

NAME

TECHLIB-1179

SUMMARY

The 'index_%d' is defined for '%s' group on line %d but its corresponding 'variable_%d' is not defined for template '%s' '%s' on line %d. This may lead to undesirable analysis results.

DESCRIPTION

This message is issued when an index is defined in the group but its corresponding variable name is not defined in the template. For index definition to be complete, its variable must be defined in the template. To fix the issue, re-characterize the library with appropriate settings such that all indices have defined variables in the template.

TECHLIB-1180

NAME

TECHLIB-1180

SUMMARY

The 'index_%d' is not defined for '%s' group on line %d, but is required as per definition of template '%s' %s on line %d. This may lead to undesirable analysis results.

DESCRIPTION

This message is issued when an index is not defined for a group but is required as per the template definition. To fix the issue, re-characterize the library with appropriate settings such that all indices

are defined in the group as per the template definition.

TECHLIB-1181

NAME

TECHLIB-1181

SUMMARY

The 'variable_%d' is defined but 'index_%d' is not defined for %s '%s' on line %d.

DESCRIPTION

This message is issued when a variable is defined in the template but its corresponding index is not defined. All variables should have defined indices in the template. To fix the issue, re-characterize the library with appropriate settings such that all indices exist corresponding to the variables in the template definition.

TECHLIB-1182

NAME

TECHLIB-1182

SUMMARY

The higher level variable_%d is defined but variable_%d is not defined for template group '%s' '%s'. This template group will be ignored.

DESCRIPTION

This message is issued when a higher level variable is defined without the lower level variable definition. For example, variable_2 is defined but variable_1 definition is missing. To fix the issue, re-characterize the library with appropriate settings such that higher level variables are not defined

without the lower level variable definitions.

TECHLIB-1183

NAME

TECHLIB-1183

SUMMARY

The variable_%d and variable_%d have the same value %s for template group '%s' '%s' on line %d.

DESCRIPTION

This message is issued when two variables in a template have same value. Each variable should have unique value in the template. To fix the issue, re-characterize the library with appropriate settings such that all variables in a template have unique values.

TECHLIB-1184

NAME

TECHLIB-1184

SUMMARY

The attribute '%s' is defined but the attribute '%s' is not defined in '%s' group on line %d.

DESCRIPTION

This message is issued when defining one attribute alone is not sufficient, but another attribute which is also mandatorily needed to be defined with that attribute, is missing. Not only either one but both attributes are necessary for analysis. For example, in one case where attribute 'sdf_cond' is defined, but 'when' attribute is missing from library or vice-versa. Another case, where the library does not specify the 'default_wire_load_selection' when wire load models are present. In both the

cases, both attributes are required to be defined in the library. To fix the issue, re-characterize the library with appropriate settings, such that all mandatory dependent attributes are defined in the library.

TECHLIB-1185

NAME

TECHLIB-1185

SUMMARY

The '%s' '%s' is defined in '%s' cell group but not defined in '%s' group.

DESCRIPTION

This message is issued when a cell object such as bus, bundle, pin etc., is inconsistent between the main and test cell defined in the library. To fix the issue, re-characterize the library with appropriate settings, such that cell objects are consistent between main cell and test cell definition

TECHLIB-1186

NAME

TECHLIB-1186

SUMMARY

The '%s' table found for timing group with timing_type %s.

DESCRIPTION

This message is issued when attributes cell_rise/cell_fall/rise_transition/fall_transition are found for timing group with sequential timing arcs. To fix the issue, re-characterize the library with appropriate settings, such that the correct attributes are specified for sequential timing arcs.

TECHLIB-1187

NAME

TECHLIB-1187

SUMMARY

The cell '%s' on line %d has both pad cell and auxiliary pad cell attributes defined.

DESCRIPTION

This message is issued when both pad_cell and auxiliary_pad_cell attributes are defined for a cell. The cell can be classified either as a pad cell or an auxiliary pad cell, but not both. To fix the issue, re-characterize the library with appropriate settings, such that the cell is defined with the correct attribute.

TECHLIB-1188

NAME

TECHLIB-1188

SUMMARY

The cell '%s' on line %d has attribute pad_type defined, but it is not a pad cell.

DESCRIPTION

This message is issued when the attribute pad_type has been defined for a cell which is not a pad cell. Only pad cells are expected to have the attribute pad_type defined on them. To fix the issue, re-characterize the library with appropriate settings, such that the correct attributes are defined on the cell.

TECHLIB-1189

NAME

TECHLIB-1189

SUMMARY

The cell '%s' on line %d has pad_cell attribute but has no 'is_pad' attribute set to true on any pin/pg_pin.

DESCRIPTION

This message is issued when the attribute is_pad is missing for all the pins or pg_pins of the cell which is defined as a pad cell. To fix the issue, re-characterize the library with appropriate settings, such that the correct attributes are defined on the pin and cell.

TECHLIB-1190

NAME

TECHLIB-1190

SUMMARY

The cell '%s' is not a pad cell but has '%s' attribute specified for %s '%s'.

DESCRIPTION

This message is issued when pad attributes such as hysteresis, drive_current etc., have been defined for a pin of cell which is not a pad cell. Only pad pins are expected to have pad attributes defined on them. To fix the issue, re-characterize the library with appropriate settings, such that the correct attributes are defined on the pin/cell.

TECHLIB-1191

NAME

TECHLIB-1191

SUMMARY

The attribute 'power_down_function' has been defined for %s '%s' of test_cell on line %d.

DESCRIPTION

This message is issued when attribute power_down_function is defined on any pin of test_cell. The test_cell pins cannot have power_down_function attribute. To fix the issue, re-characterize the library with appropriate settings, such that the correct attributes are defined on test_cell pins.

TECHLIB-1192

NAME

TECHLIB-1192

SUMMARY

The attribute '%s' has been defined for %s %s '%s' on line %d.

DESCRIPTION

This message is issued when the attributes function/state_function/Clock_gate_out_pin are defined incorrectly on pins with certain direction i.e. function attribute cannot be defined for input pins, state_function cannot be defined for input and internal pins and clock_gate_out_pin cannot be set true for input and internal pins. To fix the issue, re-characterize the library with appropriate settings, such that the attributes function/state_function/Clock_gate_out_pin should be defined on correct pins.

TECHLIB-1193

NAME

TECHLIB-1193

SUMMARY

The %s '%s' on line %d is undefined in the library.

DESCRIPTION

This message is issued when any attribute is used but it is not defined in the library. To fix the issue, re-characterize the library with appropriate settings, such that there is no undefined attribute getting used in library.

TECHLIB-1194

NAME

TECHLIB-1194

SUMMARY

The attribute 'bit_width' %d on line %d does not match with the bit range specified using attributes 'bit_from' %d and 'bit_to' %d.

DESCRIPTION

This message is issued when specified bit_width attribute does not match with the bus_width calculated from bit_from and bit_to attributes. To fix the issue, re-characterize the library with appropriate settings, such that there is no such conflict.

TECHLIB-1195

NAME

TECHLIB-1195

SUMMARY

The bus pin '%s' on line %d, is out of range as per bus bit definition %d to %d.

DESCRIPTION

This message is issued when a bus pin is specified with width which is out of range as per the bus bit definition. For example, the pin X is specified with bus bit range 2 i.e. (0 to 1) but the bus pin is specified like X[3]. To fix the issue, re-characterize the library with appropriate settings, such that the correct range is defined.

TECHLIB-1196

NAME

TECHLIB-1196

SUMMARY

The group '%s' with name '%s' on line %d is already defined on line %d. The first definition will be retained, rest will be ignored.

DESCRIPTION

This message is issued when an attribute is defined more than once. The same attribute cannot have multiple definition. First definition will be retained and rest will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the attributes are defined correctly.

TECHLIB-1197

NAME

TECHLIB-1197

SUMMARY

The cell '%s' on line %d is neither a pad cell nor an auxiliary pad cell but has 'is_pad' attribute set to true on %s at line %d.

DESCRIPTION

This message is issued when the attribute pad_cell/auxiliary_pad_cell is missing at cell level but has pin(s)/pg_pin(s) with is_pad attribute. Pins should have is_pad attribute only if cell is a pad cell. To fix the issue, re-characterize the library with appropriate settings, such that the correct attributes are defined on pin/cell.

TECHLIB-1198

NAME

TECHLIB-1198

SUMMARY

The 'index_%d' is defined but its corresponding 'variable_%d' is not defined for template '%s' '%s'. This may lead to undesirable analysis results.

DESCRIPTION

This message is issued when an index is defined but its corresponding variable name is not defined in the template. For index definition to be complete, its variable must be defined in the template. To fix the issue, re-characterize the library with appropriate settings such that all indices have defined variables in the template.

TECHLIB-1199

NAME

TECHLIB-1199

SUMMARY

The delay_model attribute specified on line %d should be the first attribute in the library.

DESCRIPTION

This message is issued when delay_model attribute is specified in library but it is not the first attribute in library. As per Liberty standards, delay_model attribute must be first attribute if technology attribute is not specified in library.

TECHLIB-1200

NAME

TECHLIB-1200

SUMMARY

The attribute '%s' defined on line %d is not supported for '%s' group. It should be defined at '%s' level.

DESCRIPTION

The message is issued when an attribute defined for a group is not supported by that group and needs to be defined at a different parent level in the library. For example, if a library level attribute (such as time_unit) is defined at the cell or pin level definition. To fix the issue, re-characterize the library with appropriate settings, such that only attributes supported by a group definition are specified in that group.

TECHLIB-1201

NAME

TECHLIB-1201

SUMMARY

The attribute '%s' defined on line %d is not supported for the '%s' group.

DESCRIPTION

The message is issued when an attribute defined for a group is not supported by that group and needs to be defined at a different parent level in the library. For example, if a library level attribute (such as time_unit) is defined at the cell or pin level definition. To fix the issue, re-characterize the library with appropriate settings, such that only attributes supported by a group definition are specified in that group.

TECHLIB-1202

NAME

TECHLIB-1202

SUMMARY

The %s statement for '%s' on line %d is first defined on line %d. The first definition will be retained.

DESCRIPTION

The message is issued when more than one definitions of the define_group attribute are defined in the library. To fix the issue, re-characterize the library with appropriate settings, such that only one definition per define_group is present in the library.

TECHLIB-1203

NAME

TECHLIB-1203

SUMMARY

The name of cell defined on line %d is missing. The definition will be ignored.

DESCRIPTION

The message is issued when the cell definition is missing the name string. In such cases, the cell definition will be completely ignored. To fix the issue, re-characterize the library with appropriate settings, such that the name of the cell definition is defined such that it can be referenced correctly.

TECHLIB-1204

NAME

TECHLIB-1204

SUMMARY

Illegal value '%s' defined for attribute '%s'. The attribute will be ignored.

DESCRIPTION

The message is issued when non-legal and unacceptable values are specified for attributes. For example, per liberty guidelines, the acceptable values for attributes such as dont_touch and dont_use are only true/false. If the library has other values such as enum or integers specified, the attribute will not be honored. To fix the issue, re-characterize the library with appropriate settings, such that the attribute has legal value specified and can be honored.

TECHLIB-1205

NAME

TECHLIB-1205

SUMMARY

Boolean value '%s' defined for attribute %s on line %d. The acceptable value is true/false. However, the value and the attribute will be honored.

DESCRIPTION

The message is issued when boolean values are specified for attributes. For example, per liberty guidelines the acceptable values for attributes such as dont_touch and dont_use are only true/false. However, if the library has boolean values specified, the tool honors the valu and the attribute, along with this message. To fix the issue, re-characterize the library with appropriate settings, such that the attribute has values specified per the required syntax.

TECHLIB-1206

NAME

TECHLIB-1206

SUMMARY

The attribute '%s' defined on line %d has invalid syntax for floating number. It will be ignored.

DESCRIPTION

The message is issued when a library attribute having inconvertible floating point numbers such as single float is expected but multiple values are provided or unusable values are provided like nan/inf in float value or float array. For example, the attributes rise_capacitance and fall_capacitance are expected to have a single float value defined. To fix the issue, re-characterize

the library with appropriate settings, such that the attribute takes a scalar float value.

TECHLIB-1207

NAME

TECHLIB-1207

SUMMARY

The attribute wire_load_from_area defined on line %d of wire_load_selection group has max area value %f specified less than min area value %f.

DESCRIPTION

The message is issued when the min area value defined in the wire_load_from_area attribute of the wire_load_selection group, is less than that defined as the max area value. Min area should be lesser than the max area value. To fix the issue, re-characterize the library with appropriate settings, such that the area range is defined correctly.

TECHLIB-1208

NAME

TECHLIB-1208

SUMMARY

The attribute '%s' of '%s' group '%s' has value '%f' which is '%s'.

DESCRIPTION

The message is issued when the attribute in a group has a value which is different (less than, less than equal to, greater than, greater than equal to defined values which could be integers or float values) than the expected value/range per the Liberty standard. For example, if max_area value

defined in the wire_load_from_area attribute of the wire_load_selection group, is less than or equal to 0. Or min_area value is less than 0. To fix the issue, re-characterize the library with appropriate settings, such that the attribute values are defined per Liberty standard.

TECHLIB-1209

NAME

TECHLIB-1209

SUMMARY

The area range %f-%f specified for wire_load_from_area attribute defined on line %d of wire_load_selection group '%s' overlaps with the range %f-%f of the wire_load_from_area attribute defined on line %d.

DESCRIPTION

The message is issued when area range defined in one wire_load_from_area attribute of the wire_load_selection group, overlaps the area range defined in the another wire_load_from_area attribute. The range of area defined should be mutually exclusive. To fix the issue, re-characterize the library with appropriate settings, such that the area range is defined correctly.

TECHLIB-1210

NAME

TECHLIB-1210

SUMMARY

The %s attribute(s) is not defined for %s group on line %d, even though %s attributes(s) are defined.

DESCRIPTION

The message is issued when the ff/ff_bank attributes such as preset, clear, clear_preset_var1 and clear_preset_var2 are not all defined in the library when either of the attributes are defined. For example, in case one, if preset and clear are not defined when clear_preset_var1 or clear_preset_var2 are defined or in case two, if when both clear and preset are defined, but clear_preset_var1 and/or clear_preset_var2 are not defined. To fix the issue, re-characterize the library with appropriate settings, such that the attributes are defined per the requirement.

TECHLIB-1211

NAME

TECHLIB-1211

SUMMARY

The %s '%s' is not a pad pin but has '%s' attribute specified on line %d.

DESCRIPTION

The message is issued when pad attributes such as hysteresis, drive_current etc., have been defined for a pin which is not a pad pin. Only pad pins are expected to have pad attributes defined on them. To fix the issue, re-characterize the library with appropriate settings, such that the correct attributes are defined on the pad pin

TECHLIB-1212

NAME

TECHLIB-1212

SUMMARY

The pad attribute '%s' is defined on %s '%s' on line %d. It should be defined on '%s'.

DESCRIPTION

The message is issued when pad attributes such as hysteresis, drive_current are defined on incorrect pin based on direction. Per Liberty standard, the hysteresis attribute is valid only for input pad pins, whereas drive_current can only be defined for output pad pins. In cases where the library specifies it the differently, the message is issued. To fix the issue, re-characterize the library with appropriate settings, such that the correct attributes are defined with respect to the pad pin directions.

TECHLIB-1213

NAME

TECHLIB-1213

SUMMARY

For '%s' timing group defined on line %d, related_pin %s is not same as the pin %s.

DESCRIPTION

This message is issued when the attribute related_pin name is not same as the parent pin name for 'min_pulse_width' and 'minimum_period' timing groups. To fix the issue, re-characterize the library with appropriate settings, such that the correct related_pin value is set.

TECHLIB-1214

NAME

TECHLIB-1214

SUMMARY

For '%s' timing group defined on line %d, related_pin is same as the parent pin '%s'.

DESCRIPTION

This message is issued when the attribute related_pin name is defined same as parent pin for timing arcs other than min_pulse_width and minimum_period. To fix the issue, re-characterize the library with appropriate settings, such that the correct related_pin value is set.

TECHLIB-1215

NAME

TECHLIB-1215

SUMMARY

For cell '%s', pin name %s defined on line %d conflicts with sequential variable for '%s' group defined on line %d

DESCRIPTION

This message is issued when the pin name is defined same as the variable(s) specified for 'ff' and 'latch' group. To fix the issue, re-characterize the library with appropriate settings, such that the correct pin name is specified.

TECHLIB-1216

NAME

TECHLIB-1216

SUMMARY

The reference time values '%f' and '%f' defined for vector groups on line '%d' and '%d' respectively are different, even though their input_transition_time index is same.

DESCRIPTION

This message is issued when values of the reference_time and input_net_transition attributes are

inconsistent inside the output_current_rise or output_current_fall group. To fix the issue, re-characterize the library with appropriate settings, such that there is no such inconsistency.

TECHLIB-1217

NAME

TECHLIB-1217

SUMMARY

For the cell '%s', the always-on %s has related_power_pin '%s' which is not of pg_type 'backup_power'.

DESCRIPTION

This message is issued for an always-on cell, when the cell pin has related_power_pin which is not the pg_type 'backup_power'. To fix the issue, re-characterize the library with appropriate settings, such that the correct pg_type pin is specified.

TECHLIB-1218

NAME

TECHLIB-1218

SUMMARY

For the cell '%s', the always-on %s has related_ground_pin '%s' which is not of pg_type 'backup_ground'.

DESCRIPTION

This message is issued for an always-on cell, when the cell pin has related_ground_pin which is not the 'backup_ground' pg_type. To fix the issue, re-characterize the library with appropriate

settings, such that the correct pg_type pin is specified.

TECHLIB-1220

NAME

TECHLIB-1220

SUMMARY

The '%s' attribute is not defined for the cell %s. This may lead to undesirable analysis results. To fix this issue, define the missing attribute in library.

DESCRIPTION

This message is issued when the attributes such as ecsm_vtp and ecsm_vtn are not defined for the cell in library with ecsm version >= 1.2. To fix the issue, re-characterize the library with appropriate settings, such that these attributes are defined on the cell.

TECHLIB-1221

NAME

TECHLIB-1221

SUMMARY

The attribute pg_type of the pg_pin '%s' on line %d is not defined as 'primary_power' even though the attribute 'std_cell_main_rail' is true

DESCRIPTION

The message is issued when even though the attribute 'std_cell_main_rail' is defined as true on a pg_pin, but the attribute 'pg_type' is not defined as 'primary_power'. When 'std_cell_main_rail' is set as true, it is mandated to have the 'pg_type' defined as 'primary_power'. To fix the issue, re-

characterize the library with appropriate settings, such that attributes are correctly defined.

TECHLIB-1222

NAME

TECHLIB-1222

SUMMARY

The 'index_%d' of type '%s' defined in '%s' group on line %d should have single float value. The group will be ignored.

DESCRIPTION

The message is issued when any index specified in the library is expected to have single float value but has more than one float value. To fix this issue, re-characterize the library such that all indices match the expected number of float values.

TECHLIB-1223

NAME

TECHLIB-1223

SUMMARY

The attribute '%s' has value '%g' which is not '%s'.

DESCRIPTION

This message is issued when the attribute has float values beyond the defined range as per the Liberty standard.

TECHLIB-1224

NAME

TECHLIB-1224

SUMMARY

The internal_power group is defined multiple times for cell '%s', %s '%s' on lines %d and %d. First definition will be used for analysis

DESCRIPTION

This message is issued for multiple definitions of internal_power groups for a pin with the same related_pg_pin and same 'when' condition attributes. First definition is used for analysis.

TECHLIB-1225

NAME

TECHLIB-1225

SUMMARY

For clock gating integrated cell '%s', output %s '%s', the function attribute has both '%s' and '%s' at line %d. This may lead to unexpected analysis results.

DESCRIPTION

This message is issued when pin function attribute is defined with both IQ and IQN pins for clock gating integrated cells. To fix the issue, re-characterize the library with appropriate settings.

TECHLIB-1226

NAME

TECHLIB-1226

SUMMARY

For the cell '%s', inout %s '%s' on line %d has missing three_state function.

DESCRIPTION

This message is issued when the three_state function is not specified for the inout pin of the cell. To fix the issue, re-characterize the library with appropriate settings, such that the three_state function should be specified.

TECHLIB-1227

NAME

TECHLIB-1227

SUMMARY

For cell %s, %s pg pin %s on line %d has related bias pin %s which is not of type %s.

DESCRIPTION

This message is issued when the attribute related_bias_pin has invalid value. For power pins, it can only be nwell/deepnwell and for ground pins, it can only be pwell/deeppwell. To fix the issue, re-characterize the library with appropriate settings, such that the correct related_bias_pin values are set.

TECHLIB-1228

NAME

TECHLIB-1228

SUMMARY

The pin name '%s' defined on line %d is part of the list of reserved words for sequential cells. However, the pin name is honored.

DESCRIPTION

This message is issued when a sequential cell has pin names that are part of the reserved words for sequential cells. List of the reserved words is following: clocked_on_also, data_in, enable, enable_also, preset, clear, force_00, force_01, force_10, force_11. To fix the issue, re-characterize the library with appropriate settings, such that the correct pin name is specified.

TECHLIB-1229

NAME

TECHLIB-1229

SUMMARY

The first value %f for '%s' group defined on line %d is the '%s' value.

DESCRIPTION

This message is issued when the first value of the current waveform in CCS library is not correctly specified. The first value in the 'values' attribute of the group 'output_current_rise' cannot be the maximum value and the first value in the 'values' attribute of the group 'output_current_fall' cannot be the minimum value. To fix the issue, re-characterize the library with appropriate settings, such that the correct values are specified.

TECHLIB-1230

NAME

TECHLIB-1230

SUMMARY

Failed to parse '%s' expression for %s group on line number %d. %s

DESCRIPTION

This message is issued when software encounters an error in parsing the boolean expressions like next_state/function/when/when_start/when_end/sdf_cond etc.. To rectify the issue, fix the error issued by correcting the Boolean expression definition.

TECHLIB-1231

NAME

TECHLIB-1231

SUMMARY

The attribute fanout_length for wire_load group '%s' defined on line %d has %d arguments. It must have 2 or 5 arguments.

DESCRIPTION

This message is issued when the attribute fanout_length for wire_load group has incorrect number of arguments. It must have either 2 or 5 arguments. To fix the issue, re-characterize the library with appropriate settings, such that the correct value is set for the attribute.

TECHLIB-1232

NAME

TECHLIB-1232

SUMMARY

The input_transition_time index values '%f' and '%f' defined for vector groups on line '%d' and '%d' respectively are different, even though their respective reference time is same.

DESCRIPTION

This message is issued when values of the reference_time and input_net_transition attributes are inconsistent inside the output_current_rise or output_current_fall group. To fix the issue, re-characterize the library with appropriate settings, such that there is no such inconsistency.

TECHLIB-1233

NAME

TECHLIB-1233

SUMMARY

Number of values in ecsm_waveform_set in the transition table %s on line %d in pin %s of cell %s does not match the number of transition table axis points specified in the template. Ignoring waveform data.

DESCRIPTION

The number of values in ecsm_waveform_set must match the number of data points in the transition table for correct waveform lookup. If this is not the case, waveform data for the transition group is ignored.

TECHLIB-1234

NAME

TECHLIB-1234

SUMMARY

The %s is not present for the %s '%s' on line '%d' for cell '%s'. This may cause incorrect voltage to be used during timing analysis

DESCRIPTION

This message is issued when the attribute related_power_pin or related_ground_pin is absent. For special cells (macro/level shifter/always on/retention/isolation/pad etc.), it is mandatory to specify the related_power_pin/related_ground_pin attribute for every pin definition. Absence of this attribute may cause incorrect voltage to be used during timing analysis. To fix the issue, re-characterize the library with appropriate settings, such that this information is correctly specified for every pin.

TECHLIB-1235

NAME

TECHLIB-1235

SUMMARY

The pg_pin with the name %s specified for %s attribute for %s on line '%d' is not defined for cell '%s'.

DESCRIPTION

This message is issued when the pin name specified for related_pg_pin attribute is not defined at the cell level. To fix the issue, re-characterize the library with appropriate settings, such that the correct pins are specified.

TECHLIB-1236

NAME

TECHLIB-1236

SUMMARY

The ecsm_waveform_set group on line %d in the transition table %s in pin %s of cell %s does not have valid index_1 attribute specified. Ignoring waveform data.

DESCRIPTION

Attribute index_1 is mandatory attribute in ecsm_waveform_set group which represents the normalized output voltage sample points which are shared by all voltage waveforms represented by the ecsm_waveform_set group. It can be specified at the group level or at the template level. If it is not specified, waveform data for the transition group is ignored.

TECHLIB-1237

NAME

TECHLIB-1237

SUMMARY

The related_pin '%s' specified for %s group on line '%d' is not defined for cell '%s'.

DESCRIPTION

This message is issued when an undefined pin is specified as related_pin. To fix the issue, re-characterize the library such that valid pin is used for related_pin.

TECHLIB-1238

NAME

TECHLIB-1238

SUMMARY

The %s group on line %d can have only %d parameters. The extra parameters will be ignored.

DESCRIPTION

This message is issued when the extra parameters are defined for the ff/latch and ff_bank/latch_bank. For ff/latch parameter limit is 2 and ff_bank/latch_bank parameter limit is 3, rest will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the parameter should be defined within the limit.

TECHLIB-1239

NAME

TECHLIB-1239

SUMMARY

The software could not locate the master timing library specified in the side-file library '%s'. You are required to have timing libraries that match your side-file libraries. The variation data will not be loaded.

DESCRIPTION

The software could not locate the master timing library specified in the side-file library. You are required to have timing libraries that match your side-file libraries. The variation data will not be loaded.

TECHLIB-1240

NAME

TECHLIB-1240

SUMMARY

The software could not locate the timing library cell '%s' specified in the side-file library '%s'. You are required to have timing library cells to match the cells in your side-file libraries. The variation data will not be loaded.

DESCRIPTION

The software could not locate the timing library cell specified in the side-file library. You are required to have timing library cells to match the cells in your side-file libraries. The variation data will not be loaded.

TECHLIB-1241

NAME

TECHLIB-1241

SUMMARY

The software could not locate the timing library arc in library '%s' for cell '%s' between pin '%s' and pin '%s' for condition '%s'. You are required to have timing library cells that the match arc topology of the cells in your side-file libraries. The variation data will not be loaded.

DESCRIPTION

The software could not locate the timing library arc in library. You are required to have timing library cells that the match arc topology of the cells in your side-file libraries. The variation data will not be loaded.

TECHLIB-1242

NAME

TECHLIB-1242

SUMMARY

The library format in the file '%s' is not supported by software. Check the format.

DESCRIPTION

The software is not able to recognize the library format of file. Liberty timing libraries or side-file files must be in either text-readable format or Cadence compiled .ldb format.

TECHLIB-1244

NAME

TECHLIB-1244

SUMMARY

The LDB file cannot be read because it has been compiled with a newer software version '%s' than the currently used software version. Recompile the LDB file with a compatible software version '%s' or use the equivalent non-compiled library.

DESCRIPTION

This message is issued when the LDB file is compiled with a later software version than the version being used to read the LDB file. This is not allowed because the LDB file may have some data which is not supported in the backward software version you are using to read the LDB file. To fix this issue, re-compile the LDB file with a compatible software version.

TECHLIB-1245

NAME

TECHLIB-1245

SUMMARY

The LDB file cannot be read because LDB file size is not as per expected file size. LDB file may be corrupted. Recompile the LDB file.

DESCRIPTION

This message is issued when the on-disk file size of the LDB file does not match the file size stored in the header of LDB file. This indicates some data corruption issues. To fix this issue, re-compile the LDB file.

TECHLIB-1246

NAME

TECHLIB-1246

SUMMARY

The LDB file cannot be read because the LDB is compiled on a CPU whose endianness is different from the endianness of the current machine CPU architecture. Re-compile the LDB file on the same CPU architecture that you are using to read the LDB file.

DESCRIPTION

This message is issued when the CPU architecture reading the LDB file and CPU architecture which was used to generate the LDB file are not compatible in terms of endianness. Use machines with same endianness to fix this issue.

TECHLIB-1247

NAME

TECHLIB-1247

SUMMARY

The report_aocv_derate command is disabled because encrypted AOCV libraries have been loaded in the session.

DESCRIPTION

Since this command reports the AOCV derating tables from AOCV libraries in AOCV library format, it is disabled when any of the AOCV library is loaded in encrypted format

TECHLIB-1248

NAME

TECHLIB-1248

SUMMARY

Generated LDB '%s' can be read only within %s flows.

DESCRIPTION

LDB files generated by Innovus is not interoperable across Cadence tools and can be used only in Innovus and Conformal.

TECHLIB-1249

NAME

TECHLIB-1249

SUMMARY

The LDB is generated by %s tool and is not interoperable with current tool.

DESCRIPTION

LDB files generated by Innovus is not interoperable across Cadence tools and can be used only in Innovus and conformal. LDB files generated from Tempus can be used as input by all tools (Innovus, Tempus, Genus and Voltus). To fix this issue, recompile the LDB file with Tempus.

TECHLIB-1250

NAME

TECHLIB-1250

SUMMARY

The input library file can not be in LDB format. Specify the text library file.

DESCRIPTION

This message is issued when LDB file is specified as input library file to -library option. Input library file must be in text format. To fix this issue, specify text library file.

TECHLIB-1251

NAME

TECHLIB-1251

SUMMARY

For cell '%s', arc '%s', 'CCS '%s' waveform has more than one peak '%s' at line %d. Review the multiple peaks and ensure that these are as per the expectations.

DESCRIPTION

This message is issued when CCS output current waveform (rise/fall) has distortions and has more than one peak. Review the multiple peaks and ensure that these are as per the expectations. The default threshold value for maximum peak violation is 0.95. To change the default value in valus, use the command line option 'set_valus_mode -ccs_current_peak_tolerance'

TECHLIB-1252

NAME

TECHLIB-1252

SUMMARY

The '%s' attribute is defined for '%s %s %s' of cell '%s'. This attribute will be ignored.

DESCRIPTION

The input_voltage attribute can be defined only for input or inout pins, bus or bundle and output_voltage attribute can be defined only for output or inout pins, bus or bundle. Incorrectly applied attributes will be ignored during timing analysis. To fix this issue, re-characterize the library with appropriate settings.

TECHLIB-1253

NAME

TECHLIB-1253

SUMMARY

'%s' group '%s' is undefined in library. This attribute will be ignored.

DESCRIPTION

This message is issued when input_voltage and/or output_voltage group(s) referred by these attributes at the pin level are not defined in the library. Attribute referring to undefined group will be ignored. To fix this issue, re-characterize the library with appropriate settings.

TECHLIB-1254

NAME

TECHLIB-1254

SUMMARY

The '%s - %s' table of the '%s' group on the '%s' %s '%s' does not have a template that uses '%s' as a variable. Ensure that the templates used are in accordance with the direction of the pin.

DESCRIPTION

This message is issued when the input_net_transition and total_output_net_capacitance tables defined with incorrect direction of the pin for the power/rise_power/fall_power groups. For 1-d tables input pin should have input_net_transition. For 2-d tables input and output pins should be defined with both input_net_transition and total_output_net_capacitance tables and inout pins can be defined with any of the attribute. To fix the issue, re-characterize the library with appropriate settings, such that the templates used are defined in accordance with the direction of pin.

TECHLIB-1255

NAME

TECHLIB-1255

SUMMARY

The '%s' table on the timing arc has %s as '%s' on pin '%s' for cell '%s' but it has no 'ecsm_capacitance %s' tables. Ensure that the corresponding ecsm_capacitance/ecsm_capacitance_set tables are present.

DESCRIPTION

This message is issued when complete ECSM data is not present for a timing arc. For example, in timing arc, if ecsm waveform data is present but corresponding ecsm capacitance data is missing then software issues this message. This incomplete data can lead to inaccuracy in timing analysis. To fix this issue, re-characterize the library such that ECSM data is complete for the mentioned timing arc.

TECHLIB-1256

NAME

TECHLIB-1256

SUMMARY

The %s is being ignored due to errors in this group. This group will be excluded for any further library checks. Refer to the previous messages issued for %s to find the details of the issues in this group.

DESCRIPTION

This message is issued in scenarios when any liberty group has problem. For example, if the template at library level and cell level do not match for number of indices or number of values in indices. It can also occur if indices are expected to have single value for some attributes per Liberty format but library has more than one value for that index. Another case can be when timing type is not specified/invalid and timing arc has sequential timing arcs. In such scenarios, the corresponding table data is ignored.

TECHLIB-1257

NAME

TECHLIB-1257

SUMMARY

Found %s '%s' in the library. This is not a mandatory %s for merged library and may result in increased library size.

DESCRIPTION

For a merged library only the following constructs are mandatory:\n ecsm_version and 4 ECSM-Timing Constructs - ecsm_waveform_set, ecsm_capacitance_set, ecsm_vtp, ecsm_vtn and 2 CCS-Noise Constructs - ccsn_first_stage, ccsn_last_stage \n If any other construct is present, it may cause an increase in size, beyond the expected value for a merge library.

TECHLIB-1258

NAME

TECHLIB-1258

SUMMARY

Necessary %s '%s' is missing from the '%s' table on the timing arc of pin '%s' for cell '%s' of the merged library. This is a mandatory %s for merged library and may lead to inaccuracy in timing analysis.

DESCRIPTION

For a merged library only the following constructs are mandatory:\n ecsm_version and 4 ECSM-Timing Constructs - ecsm_waveform_set, ecsm_capacitance_set, ecsm_vtp, ecsm_vtn and 2 CCS-Noise Constructs - ccsn_first_stage, ccsn_last_stage\n If these constructs are not present, it may cause inaccuracy in timing analysis.

TECHLIB-1259

NAME

TECHLIB-1259

SUMMARY

Necessary %s '%s' is %s for the merged library. This is a mandatory %s for merged library and may lead to inaccuracy in timing analysis.

DESCRIPTION

For a merged libray only the following constructs are mandatory:\n ecsm_version and 4 ECSM-Timing Constructs - ecsm_waveform_set, ecsm_capacitance_set, ecsm_vtp, ecsm_vtn and 2 CCS-Noise Constructs - ccsn_first_stage, ccsn_last_stage\n If these constructs are not present, it may casue inaccuracy in timing analysis. Furthermore ecsm_vtp and ecsm_vtn are checked only if the ecsm_version is greater than 1.2/2.1 as the support for these attributes was added in the aforementioned version.

TECHLIB-1260

NAME

TECHLIB-1260

SUMMARY

Cell '%s' does not have electromigration/max_cap group on any pin

DESCRIPTION

This message is issued when the cell is not specified with any electromigration/max_cap table on any pin. To fix the issue, re-characterize the library with appropriate settings, such that the electromigration/max_cap table is defined on pin at cell level.

TECHLIB-1261

NAME

TECHLIB-1261

SUMMARY

Found invalid/missing attribute value. The attribute will be ignored.

DESCRIPTION

This message is issued in scenarios when attribute value is invalid/missing. For example related_pin attribute is specified but its value is empty string or integer value is specified where string value is expected, the attribute will not be honored. To fix the issue, re-characterize the library with appropriate settings, such that the attribute has legal value specified and can be honored.

TECHLIB-1262

NAME

TECHLIB-1262

SUMMARY

%s

DESCRIPTION

This message is issued in scenarios when there is error in command line arguments.

TECHLIB-1263

NAME

TECHLIB-1263

SUMMARY

Unknown capacitance type '%s' defined for %s in cell %s.

DESCRIPTION

The ecsm_capacitance/ecsm_capacitance_set type should be either rise or fall. If a value other than rise or fall is encountered, the ecsm_capacitance information will be ignored

TECHLIB-1264

NAME

TECHLIB-1264

SUMMARY

Pin index range [%d:%d] is out of range of bus %s in cell '%s'

DESCRIPTION

This message is issued when the specified pin index range is out of range as per the bus definition in cell. To fix the issue, re-characterize the library with appropriate settings, such that the correct range is defined.

TECHLIB-1265

NAME

TECHLIB-1265

SUMMARY

scalar pin %s specified as bus with index range [%d:%d] in boolean expression in cell %s. The boolean expression is ignored.

DESCRIPTION

This message is issued when the scalar pin is defined as bus bit in boolean expressions like function, when expression etc. To fix the issue, re-characterize the library with appropriate settings, such that the index range is specified for scaler pin.

TECHLIB-1266

NAME

TECHLIB-1266

SUMMARY

Error while translating binary string '%s'

DESCRIPTION

This message is issued when binary string cannot be translated into required format.

TECHLIB-1267

NAME

TECHLIB-1267

SUMMARY

Pin '%s' does not exist in cell '%s' or it is the part of the function string mapped to a latch/ff element, which has been ignored due to the cell having 'interface_timing' set to true.

DESCRIPTION

The message is issued when the cell is a black box cell but it contains function attribute or ff group.

TECHLIB-1269

NAME

TECHLIB-1269

SUMMARY

Pin '%s' does not exist in cell '%s'. The functions expression will be ignored.

DESCRIPTION

This message is issued when the pin is not defined in the cell and referred in the function. Function statement will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the pin is defined in the cell.

TECHLIB-1270

NAME

TECHLIB-1270

SUMMARY

The '%s' attribute/group has been defined more than once. Only the %s occurrence of the attribute will be retained.

DESCRIPTION

The message is issued when there are multiple definitions for an attribute/group. Each attribute/group should be defined only once. To fix this issue, re-characterize the library with the appropriate settings.

TECHLIB-1271

NAME

TECHLIB-1271

SUMMARY

No ocv_derate_factors group specified for ocv_derate group %s of cell %s.

DESCRIPTION

At least one ocv_derate_factors group must be specified within an ocv_derate group.

TECHLIB-1272

NAME

TECHLIB-1272

SUMMARY

The '%s' %s has been defined more than once on %s. Only the %s occurrence of the %s will be retained.

DESCRIPTION

The message is issued when there are multiple definitions for an attribute/group. Each attribute/group should be defined only once. To fix this issue, re-characterize the library with the appropriate settings.

TECHLIB-1273

NAME

TECHLIB-1273

SUMMARY

'%s' should not be defined in lu_table_template '%s' used in group %s on line %d, in pin '%s' of cell '%s'.)

DESCRIPTION

The ocv_sigma_cell_rise, ocv_sigma_cell_fall, ocv_sigma_rise_transition, ocv_sigma_fall_transition, ocv_sigma_rise_constraint and ocv_sigma_fall_constraint groups can be 1D, 2D, 3D or scalar only.

TECHLIB-1274

NAME

TECHLIB-1274

SUMMARY

The valid value of %s is %s in the lu_table_template '%s' used in group '%s' on line %d, in pin %s of cell %s.

DESCRIPTION

For the ocv_sigma_cell_rise, ocv_sigma_cell_fall, ocv_sigma_rise_transition, and ocv_sigma_fall_transition groups, the valid values of variable_1, variable_2, and variable_3 are input_net_transition, total_output_net_capacitance, and related_out_total_output_net_capacitance. For the ocv_sigma_rise_constraint and ocv_sigma_fall_constraint groups, the values of variable_1 and variable_2 are related_pin_transition and constrained_pin_transition respectively. The values of variable_3 can be related_out_total_output_net_capacitance, related_out_output_net_length, related_out_net_wire_cap, or related_out_output_net_pin_cap.

TECHLIB-1276

NAME

TECHLIB-1276

SUMMARY

Cannot find timing library file '%s' specified with '%s'. Check unix permissions.

DESCRIPTION

This message is issued when the specified library is not found

TECHLIB-1277

NAME

TECHLIB-1277

SUMMARY

The %s '%s' has been defined for %s %s '%s'. '%s' cannot be defined at this level and is being ignored.

DESCRIPTION

This message is issued when any attribute/group is specified at incorrect level/context. Such attributes/groups are ignored. To fix the issue, recharacterize the library such that attributes/groups are specified correctly.

TECHLIB-1278

NAME

TECHLIB-1278

SUMMARY

The mandatory %s '%s' is missing for %s %s '%s'.

DESCRIPTION

This message is issued when any mandatory attribute/groups is missing in library. This can cause issues later in tool applications.

TECHLIB-1279

NAME

TECHLIB-1279

SUMMARY

For cell '%s', in group '%s', voltage swing on pin/bus/bundle '%s' with load '%f' and slew '%f' is '%.1f%', should be within five percent of '%s'.

DESCRIPTION

Using current waveform for the cell pin in the library, tool converts it to calculate the charging voltage. If the calculated voltage does not reach a particular threshold (within 5% of VDD voltage) then this message is issued. To fix the issue, re-characterize the library with appropriate settings, such that the full voltage swing is reached.

TECHLIB-1280

NAME

TECHLIB-1280

SUMMARY

The group '%s' has not been specified corresponding to the group '%s', but '%s' data has been specified corresponding to other groups on the same arc, on %s for cell '%s'.

DESCRIPTION

This message is issued when the CCS timing/ECSM/LVF/FIT data is defined for one or more slew tables but missing on other slew tables within the same arc. The valid slew groups are rise_transition, fall_transition, retain_rise_slew, retain_fall_slew, ocv_sigma_rise_transition, ocv_sigma_fall_transition, ocv_sigma_cell_rise, ocv_sigma_cell_fall, ocv_sigma_rise_constraint

and ocv_sigma_fall_constraint. To fix the issue, re-characterize the library with appropriate settings, such that the CCS timing/ECSM waveform/LVF/FIT data is defined corresponding to all group within the same arc.

TECHLIB-1281

NAME

TECHLIB-1281

SUMMARY

The timing arc on %s for %s '%s' has CCS timing driver information, but CCS timing receiver information is missing.

DESCRIPTION

This message is issued when the CCS timing driver information is specified but CCS timing receiver information is missing for the timing arc on pin of the cell. The CCS receiver data on arc is a mandatory if CCS driver model information is present. The valid CCS receiver model pairs are receiver_capacitance1_rise, receiver_capacitance2_rise and receiver_capacitance1_fall, receiver_capacitance2_fall. To fix the issue, re-characterize the library with appropriate settings, such that timing arc should be specified with both driver and receiver information.

TECHLIB-1282

NAME

TECHLIB-1282

SUMMARY

%s data has been defined on one or more %s for %s '%s' but is missing for the %s on %s of the cell.

DESCRIPTION

This message is issued when the CCS timing/ECSM waveform/LVF/FIT data is specified on one or more timing arc on pin of the cell and missing for another timing arc on pin of the cell. Only those timing arcs will be considered which have slew tables present on them. The valid slew groups are rise_transition, fall_transition, retain_rise_slew, retain_fall_slew, ocv_sigma_rise_transition, ocv_sigma_fall_transition, ocv_sigma_cell_rise, ocv_sigma_cell_fall, ocv_sigma_rise_constraint and ocv_sigma_fall_constraint. To fix the issue, re-characterize the library with appropriate settings, such that CCS timing/ECSM waveform/LVF/FIT data is defined for all timing arcs of all pins of the cell.

TECHLIB-1283

NAME

TECHLIB-1283

SUMMARY

The '%s' timing group is defined, but its corresponding '%s' timing group is missing for %s in cell '%s'.

DESCRIPTION

The message is issued when the setup_rising/setup_falling timing_type is defined but its corresponding timing_type hold_rising/hold_falling is not defined in the timing group. To fix the issue, re-characterize the library with appropriate settings, such that setup and hold timing arcs are present in pair for fall/rise transitions.

TECHLIB-1284

NAME

TECHLIB-1284

SUMMARY

The '%s' table indices do not match in %s timing group on line %d and %s timing group for %s in

cell '%s'

DESCRIPTION

This message is issued when there is discrepancy in number of indices of rise_constraint/fall_constraint table for setup_rising and hold_rising timing group. To fix the issue, re-characterize the library with appropriate settings, such that the indices match in constraint tables.

TECHLIB-1285

NAME

TECHLIB-1285

SUMMARY

The sum of values in '%s' table of %s timing group on line %d and corresponding %s timing group, is below %fps for %s in cell '%s'

DESCRIPTION

This message is issued when the sum of values of rise_constraint/fall_constraint table for setup_rising/setup_falling and corresponding hold_rising/hold_falling timing group is less than the minimum value. This sum can only be zero or any positive value specified using min_value. To fix the issue, re-characterize the library with appropriate settings, such that the sum of values matches the specified value. Default value of min_value is zero.

TECHLIB-1286

NAME

TECHLIB-1286

SUMMARY

%s data has been defined on one or more cells in the library, but is missing for cell '%s'.

DESCRIPTION

This message is issued when the data for CCS timing/ECSM/LVF/FIT data is defined for one or more cell but missing on other cell in the same library. The valid slew groups are rise_transition, fall_transition, retain_rise_slew, retain_fall_slew, ocv_sigma_rise_transition, ocv_sigma_fall_transition, ocv_sigma_cell_rise, ocv_sigma_cell_fall, ocv_sigma_rise_constraint and ocv_sigma_fall_constraint. To fix the issue, re-characterize the library with appropriate settings, such that the CCS timing/ECSM waveform/LVF/FIT data is defined corresponding to all cell within the same library.

TECHLIB-1287

NAME

TECHLIB-1287

SUMMARY

For point '%d' in index_%d (%s) in '%s' table on %s of cell '%s', values %f to %f are not monotonically %s across the index_%d (%s)

DESCRIPTION

This message is issued when em_max_toggle_rate table values (M x N), for a fixed point of index_1/index_2 of table indices do not monotonically increase/decrease across the index_2/index_1 axis. For example, in the em_max_toggle_rate table, for a fixed value of slew index, the table values are not monotonically decreasing across the load axis or for fixed value of load index, the table values are not monotonically increasing across the slew axis. To fix the issue, re-characterize the library with appropriate settings, such that table values are monotonic as per liberty standard.

TECHLIB-1288

NAME

TECHLIB-1288

SUMMARY

Incorrect value '%s' specified for variable_1 in 1-D %s '%s' in electomigration group defined on line %d defined in %s and direction '%s'.

DESCRIPTION

For one dimensional template, variable_1 can have only a specific value. For example, in 1-D electromigration template (em_lut_template) variable_1 can only be 'input_transition_time'.

TECHLIB-1290

NAME

TECHLIB-1290

SUMMARY

The cell '%s' is a phase-locked loop cell but '%s' attribute is not defined on any pin of this cell.

DESCRIPTION

This message is issued when attributes is_pll_reference_pin/is_pll_feedback_pin/is_pll_output_pin, are not defined for a pin of cell which is a phase-locked loop cell. These attributes are mandatory for phase-locked loop cell. To fix the issue, re-characterize the library with appropriate settings, such that the correct attributes are defined on the pin/cell.

TECHLIB-1291

NAME

TECHLIB-1291

SUMMARY

The '%s' attribute has been defined on more than one pin for cell '%s'. First definition at line %d would be retained and rest will be ignored.

DESCRIPTION

This message is issued when the attributes is_pll_reference_pin/is_pll_feedback_pin are defined on more than one pin for a phase-locked loop cell. The same attribute cannot have multiple definition. First definition will be retained and rest will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the attributes are defined correctly.

TECHLIB-1292

NAME

TECHLIB-1292

SUMMARY

The cell '%s' is not a phase-locked loop cell but has '%s' attribute specified for %s.

DESCRIPTION

This message is issued when attributes is_pll_reference_pin/is_pll_feedback_pin/is_pll_output_pin , have been defined for a pin of cell which is not a phase-locked loop (PLL) cell. Only phase-locked loop pins are expected to have phase-locked loop attributes defined on them. To fix the issue, re-characterize the library with appropriate settings, such that the correct attributes are defined on the pin/cell.

TECHLIB-1293

NAME

TECHLIB-1293

SUMMARY

For group '%s', number of vector groups defined is less than four.

DESCRIPTION

There should be a minimum of four vector groups defined within an output_current_rise or output_current_fall group.

TECHLIB-1294

NAME

TECHLIB-1294

SUMMARY

For group '%s', less than two vector groups are defined having unique values of '%s'.

DESCRIPTION

There should be a minimum of four vector groups defined within an output_current_rise or output_current_fall group. Current information should be specified for at least two different values of input slew and two different values of output load.

TECHLIB-1295

NAME

TECHLIB-1295

SUMMARY

Voltage (%0.3f) specified in nom_voltage attribute does not match the voltage (%0.3f) specified in default_operating_conditions (%s) group.

DESCRIPTION

The nominal voltage and the voltage specified in the default operating condition of the library must be identical.

TECHLIB-1296

NAME

TECHLIB-1296

SUMMARY

CCS checks will not be thorough as library contains both CCS and ECSM data.

DESCRIPTION

In case both CCS and ECSM data is present, ECSM data is given priority for timing and power.

TECHLIB-1297

NAME

TECHLIB-1297

SUMMARY

LDB generation could not complete. Refer to previously issued error messages in the session.

DESCRIPTION

This message is issued when library has some serious errors which prevent LDB file generation. To fix the issue, re-characterize the library to fix the error messages issued in the session.

TECHLIB-1298

NAME

TECHLIB-1298

SUMMARY

Number of '%s' specified is %d in generated_clock group in cell '%s'. It must be odd number.

DESCRIPTION

This message is issued when the number of edges/shifts are specified as even number in generated_clock group. Number of edges/shifts must be an odd number. To fix the issue, re-characterize the library with appropriate settings, such that the generated clock is correctly defined.

TECHLIB-1299

NAME

TECHLIB-1299

SUMMARY

Number of specified 'edges' (%d) is not equal to number of specified 'shifts' (%d) in generated_clock group in cell '%s'.

DESCRIPTION

This message is issued when there is a mismatch in the number of edges and shifts in generated_clock group. Number of edges must be equal to the number of shifts. To fix the issue, re-characterize the library with appropriate settings, such that the generated clock is correctly defined.

TECHLIB-1300

NAME

TECHLIB-1300

SUMMARY

Invalid frequency %s factor '%d' specified in '%s' attribute in generated_clock group in cell '%s'. It must be a power of 2.

DESCRIPTION

This message is issued when the invalid frequency multiplication factor or division factor is specified for the attribute multiplied_by/divided_by in generated_clock group. The factor must be a power of two. To fix the issue, re-characterize the library with appropriate settings, such that the generated clock is correctly defined.

TECHLIB-1301

NAME

TECHLIB-1301

SUMMARY

Invalid generated_clock definition in cell '%s'. Attribute(s) '%s' are not allowed together.

DESCRIPTION

This message is issued when the generated_clock group is defined incorrectly. The attribute divide_by can not be combined with any of these 'multiply_by', 'edges', 'shift' and the attribute 'multiply_by' can not be combined with any of these 'divide_by', 'edges', 'shift'. To fix the issue, re-characterize the library with appropriate settings, such that the generated clock is correctly defined.

TECHLIB-1302

NAME

TECHLIB-1302

SUMMARY

First edge specified in '%s' is %d in generated_clock group in cell '%s'. It must be greater than equal to 1.

DESCRIPTION

This message is issued when the first edge is specified as less than 1 in generated_clock group. The first edge must be greater than or equal to 1. To fix the issue, re-characterize the library with appropriate settings, such that the correct value of first edge is specified.

TECHLIB-1303

NAME

TECHLIB-1303

SUMMARY

Number of '%s' specified is %d in generated_clock group in cell '%s'. It must be greater than or equal to 3

DESCRIPTION

This message is issued when the number of edges specified is less than three in generated_clock group. The number of edges must be greater than or equal to 3. To fix the issue, re-characterize the library with appropriate settings, such that the correct value of number of edges is defined.

TECHLIB-1304

NAME

TECHLIB-1304

SUMMARY

Invalid generated_clock definition in cell '%s'. Attribute 'shifts' is specified without attribute 'edges'.

DESCRIPTION

This message is issued when the shifts are specified but edges are not specified in generated_clock group. Both are required as the shifts are added to the edges specified in the edge list to generate the clock. To fix the issue, re-characterize the library with appropriate settings, such that the edges should be defined if shifts are specified.

TECHLIB-1305

NAME

TECHLIB-1305

SUMMARY

The edges specified must be monotonically increasing in generated_clock group in cell '%s'.

DESCRIPTION

This message is issued when the edges specified in generated_clock group of cell do not monotonically increase. To fix the issue, re-characterize the library with appropriate settings, such that the edges defined are monotonic.

TECHLIB-1306

NAME

TECHLIB-1306

SUMMARY

The group %s with name '%s' already defined for %s of cell %s. This will be ignored

DESCRIPTION

The ecsm_waveform group with same name already exists. First will be retained and rest will be ignored

TECHLIB-1307

NAME

TECHLIB-1307

SUMMARY

The %s group contains values which are not monotonically %s from %f to %f for %s %f and %s %f in group %s.

DESCRIPTION

This message is issued when ecsm_waveform_set table values (PxQxR), for a fixed point of two of table indices do not monotonically increase/decrease across the third axis. For example, in the ecsm_waveform_set table, for a fixed value of slew index and load index, the table values are not monotonically increasing across the values axis. To fix the issue, re-characterize the library with appropriate settings, such that table values are monotonic as per Liberty standard.

TECHLIB-1308

NAME

TECHLIB-1308

SUMMARY

The user defined group '%s' defined on parent group '%s' has missing 'define_group' statement at library level. However, group data will be honored.

DESCRIPTION

This message is issued when certain user defined groups are used but not defined at library level using define_group statements. In such cases, Cadence tools will accept the data but other tools may not do so. It is recommended that library is re-characterized such that undefined user-defined

groups are not used.

TECHLIB-1309

NAME

TECHLIB-1309

SUMMARY

For point '%d' in index_%d (%s) in '%s' table on %s of cell '%s', values %f to %f are not monotonically %s across the index_%d (%s)

DESCRIPTION

This message is issued when delay table values (M x N), for a fixed point of index_1/index_2 of table indices do not monotonically increase/decrease across the index_2/index_1 axis. For example, in the cell_rise table, for a fixed value of slew index, the table values are not monotonically decreasing across the load axis or for fixed value of load index, the table values are not monotonically increasing across the slew axis. To fix the issue, re-characterize the library with appropriate settings, such that table values are monotonic as per Liberty standard.

TECHLIB-1310

NAME

TECHLIB-1310

SUMMARY

The %s group contains values which are not monotonically %s from %f to %f for %s %f and %s %f in group %s.

DESCRIPTION

This message is issued when delay table values (PxQxR), for fixed point of two of table indices do not monotonically increase/decrease across the third axis. For example, in the cell_rise table, for a fixed value of load index and load index1, the table values are not monotonically increasing across the slew axis. To fix the issue, re-characterize the library with appropriate settings, such that table values are monotonic as per Liberty standard.

TECHLIB-1311

NAME

TECHLIB-1311

SUMMARY

For point '%d' in index_%d (%s) in '%s' table on %s of cell '%s', values %f to %f are not monotonically %s across the index_%d (%s)

DESCRIPTION

This message is issued when transition table values (M x N), for a fixed point of index_1/index_2 of table indices do not monotonically increase/decrease across the index_2/index_1 axis. For example, in the rise_transition table, for a fixed value of slew index, the table values are not monotonically decreasing across the load axis or for fixed value of load index, the table values are not monotonically increasing across the slew axis. To fix the issue, re-characterize the library with appropriate settings, such that table values are monotonic as per Liberty standard.

TECHLIB-1312

NAME

TECHLIB-1312

SUMMARY

The %s group contains values which are not monotonically %s from %f to %f for %s %f and %s %f in group %s.

DESCRIPTION

This message is issued when transition table values (PxQxR), for fixed point of two of table indices do not monotonically increase/decrease across the third axis. For example, in the rise_transition table, for a fixed value of load index and load index1, the table values are not monotonically increasing across the slew axis. To fix the issue, re-characterize the library with appropriate settings, such that table values are monotonic as per Liberty standard.

TECHLIB-1313

NAME

TECHLIB-1313

SUMMARY

For cell '%s', in group '%s', voltage swing on pin/bus/bundle '%s' with load '%f' and slew '%f' is '%.1f%', should at least reach second slew threshold.

DESCRIPTION

This message is issued when the voltage swing defined for cell on pin/bus/bundle in output_current_rise /output_current_fall vector group with specified load and slew is not reaching the second slew threshold. To fix the issue, re-characterize the library with appropriate settings, such that the full voltage swing is reached.

TECHLIB-1314

NAME

TECHLIB-1314

SUMMARY

For cell '%s', in group '%s', voltage swing on pin/bus/bundle '%s' with load '%f' and slew '%f' is '%.1f%', should at least reach second slew threshold.

DESCRIPTION

This message is issued when the voltage swing defined for cell on pin/bus/bundle in output_current_rise /output_current_fall vector group with specified load and slew is not reaching the second slew threshold.

TECHLIB-1315

NAME

TECHLIB-1315

SUMMARY

For cell '%s', pg_pin groups %s share the same voltage_name '%s'. These PG pins cannot have same voltage_name. These PG pins definitions will be ignored.

DESCRIPTION

This message is issued when the same voltage_name is specified on the pins among opposite(power/ground) category of pg_type. The power category includes pins with pg_type as primary_power/backup_power/internal_power/nwell/deepnwell and ground category includes pins with pg_type as primary_ground/backup_ground/internal_ground/pwell/deeppwell for the cell for pg_pin group. Such pins will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the pg_pin(s) of opposite type are not defined with same voltage.

TECHLIB-1316

NAME

TECHLIB-1316

SUMMARY

For MSV cell '%s', pg_pin groups %s share the same voltage_name '%s'. These PG pins cannot have same voltage_name. This library will be ignored.

DESCRIPTION

This message is issued when the same voltage_name is specified on the pins among opposite(power/ground) category of pg_type. The power category includes pins with pg_type as primary_power/backup_power/internal_power/nwell/deepnwell and ground category includes pins with pg_type as primary_ground/backup_ground/internal_ground/pwell/deeppwell for MSV cell for pg_pin group. Such library will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the pg_pin(s) are not defined with same voltage.

TECHLIB-1317

NAME

TECHLIB-1317

SUMMARY

Timing library contains '%s' attribute/group, these will be ignored. To enable loading these data, specify 'set timing_library_enable_advanced_capacitance_support 1' before loading the libraries in flow.

DESCRIPTION

Support for advanced capacitance data in libraries is enabled under global variable timing_library_enable_advanced_capacitance_support. This global variable must be set before read_lib or read_view_definition command in the flow.

TECHLIB-1318

NAME

TECHLIB-1318

SUMMARY

All the table values in the '%s' group on %s of cell '%s' are within '%f' of each other.

DESCRIPTION

This message is issued when all the values defined in any of the cell_rise/cell_fall/ rise_transition/fall_transition table are within default threshold (0.00001). To fix the issue, re-characterize the library with appropriate settings, such that the table values defined are reasonable.

TECHLIB-1319

NAME

TECHLIB-1319

SUMMARY

The user-defined attribute '%s' is defined for group '%s' with type '%s'. This is an invalid definition.

DESCRIPTION

This message is issued when the define statement for user-defined attributes (related_spice_node/load_cap_rise/load_cap_fall) is not specified with appropriate group or type. The related_spice_node should be specified for ccsn_first_stage/ccsn_last_stage groups with type string and load_cap_rise/load_cap_fall should be specified for ccsn_first_stage group with type float. To fix the issue, re-characterize the library with appropriate settings, such that the required user-defined attributes are defined properly.

TECHLIB-1320

NAME

TECHLIB-1320

SUMMARY

The user-defined attribute '%s' is not present in any of the '%s' group. This attribute is required for Tempus if SPICE correlation of ROP glitch needs to be performed. The missing attribute does not affect SI delay or glitch analysis.

DESCRIPTION

This message is issued when the user-defined attribute related_spice_node attribute is not present in library. To fix the issue, re-characterize the library with appropriate settings, such that the required user-defined attributes are defined and used properly.

TECHLIB-1321

NAME

TECHLIB-1321

SUMMARY

The %sattribute '%s' is not specified in the group '%s' on %s of cell '%s'.

DESCRIPTION

This message is issued when the related_spice_node/load_cap_rise/load_cap_fall attribute is defined in library but is not specified on corresponding group ccsn_first_stage/ccsn_last_stage, or, in cases where related_ccb_node is missing on an input_ccb group. To fix the issue, re-characterize the library with appropriate settings, such that the required user-defined attributes are specified properly.

TECHLIB-1322

NAME

TECHLIB-1322

SUMMARY

In cell '%s', on %s, the user-defined attribute '%s' with value '%f' is not in the reasonable range of [%f, %f].

DESCRIPTION

The attribute load_cap_rise/load_cap_fall doesn't have proper load_cap_rise/fall value. It should be within range(min, max) valus of rise/fall pin capacitance. Attributes capacitance/rise_capacitance/fall_capacitance/rise_capacitance_range/fall_capacitance_range are considered for calculating min/max value to find reasonable range. Min value is defined as 0.001 times of lowest NLDM Pin cap value and max value is defined as 5 times of highest NLDM Pin cap value defined on the cell.

TECHLIB-1323

NAME

TECHLIB-1323

SUMMARY

The define statement of user-defined %s is not valid. The definition contains %d parameters instead of %d parameters.

DESCRIPTION

The define statement should follow the syntax as: 'define(attr_name, group_name, attr_value_type);'. To fix the issue, re-characterize the library with appropriate settings, such that the required user-defined attributes are defined properly.

TECHLIB-1324

NAME

TECHLIB-1324

SUMMARY

The specified type '%s' of user-defined attribute '%s' is invalid. It will be taken as string as default.

DESCRIPTION

The type of user-defined attribute should one of these: integer, boolean, string and float. To fix the issue, re-characterize the library with appropriate settings, such that the required user-defined attributes are defined properly.

TECHLIB-1325

NAME

TECHLIB-1325

SUMMARY

The specified parent group '%s' of user-defined %s '%s' is invalid. This definition will be ignored.

DESCRIPTION

The parent group of user-defined attribute or group should be either a standard group as per liberty or it should be a user-defined group which is defined using define_group statement. To fix the issue, re-characterize the library with appropriate settings, such that the required user-defined attributes are defined properly.

TECHLIB-1327

NAME

TECHLIB-1327

SUMMARY

The 'retention_pin' attribute on the pin '%s' in cell '%s' is honored, even though the 'retention_cell' attribute is missing at cell level.

DESCRIPTION

It is advisable to have the retention_cell attribute set on a cell having a retention pin. The retention_cell simple attribute identifies a retention cell.

TECHLIB-1329

NAME

TECHLIB-1329

SUMMARY

The attribute '%s' on the %s in cell '%s' is missing, even though the cell has multiple supply voltages.

DESCRIPTION

This message is issued when the attributes related_power_pin or related_ground_pin is not specified on the pin in cell and cell is marked as MSV cell. These are mandatory attributes for MSV cell. To fix the issue, re-characterize the library with appropriate settings, such that the related_power_pin or related_ground_pin is specified on the pin in cell.

TECHLIB-1330

NAME

TECHLIB-1330

SUMMARY

The attribute '%s' on the %s in cell '%s' is missing, it will be considered as standard cell.

DESCRIPTION

This message is issued when the attributes related_power_pin or related_ground_pin is not specified on the pin in cell and cell has multiple pg pins but only one pg pin is used as

related_power_pin. Such cell will be considered as standard cell. To fix the issue, re-characterize the library with appropriate settings, such that the related_power_pin or related_ground_pin is specified on the pin in cell

TECHLIB-1331

NAME

TECHLIB-1331

SUMMARY

The pg_pin '%s' with pg_type '%s' cannot be used in '%s' attribute for pin '%s' of the cell '%s'. This attribute is being ignored which may impact analysis accuracy.

DESCRIPTION

This message is issued when the pg_pin specified with related_power_pin/related_ground_pin does not match with the corresponding pg_type e.g. pg_pin VDD with pg_type as primary_power is used in related_ground_pin. These attributes will be ignored which may impact analysis accuracy. To fix the issue, re-characterize the library with appropriate settings, such that the incompatible pg_pin is not used.

TECHLIB-1332

NAME

TECHLIB-1332

SUMMARY

The ecsm waveform associated with '%s' group of pin '%s' in cell '%s' will be ignored due to incorrect voltage values.

DESCRIPTION

This message is issued when the voltage values specified in ecsm_waveform/ecsm_waveform_set is either outside of range [0.02, 0.098] or are too close (less than 0.01 difference between two consecutive values), then that point will be ignored and if after applying this criteria, there are less than 2 values left in voltage grid then the complete group in the rise_transition and fall_transition group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the correct voltage values is specified

TECHLIB-1333

NAME

TECHLIB-1333

SUMMARY

The %s value defined in index_%d (%s) of group '%s' on %s of cell '%s' is '%f' which is %s '%f'.

DESCRIPTION

This message is issued when the first/last value defined in input_voltage or output_voltage indices on pin of cell is above VSS/below VDD of dc_current group. The first value of input_voltage/output_voltage indices must be less than or equal to VSS and last value of input_voltage/output_voltage indices must be greater than or equal to VDD. To fix the issue, re-characterize the library with appropriate settings, such that the input_voltage/output_voltage indices of dc_current group are correctly defined.

TECHLIB-1334

NAME

TECHLIB-1334

SUMMARY

Identified one or more of the required attributes/groups missing from '%s' group defined %s of cell '%s'. When the stage_type is '%s', the required attributes/groups are %s. This may impact analysis

accuracy.

DESCRIPTION

This message is issued when the required attributes/groups are missing from ccsn_*_stage. The required attributes/groups are when stage_type is both : miller_cap_rise, miller_cap_fall, dc_current, output_voltage_rise, output_voltage_fall, when stage_type is pull_up : miller_cap_rise, dc_current, output_voltage_rise, when stage_type is pull_down : miller_cap_fall, dc_current, output_voltage_fall. This may impact analysis accuracy. To fix the issue, re-characterize the library with appropriate settings, such that the CCSN groups are correctly defined.

TECHLIB-1335

NAME

TECHLIB-1335

SUMMARY

The timing sense and sense of the group '%s' specified on timing arc on %s of cell '%s' is '%s' are inconsistent.

DESCRIPTION

This message is issued when the timing sense is inconsistent with the sense of the ccsn_*_stage group on the arc. The arc sense must match the combination i.e. chaining of the ccsn_*_stage senses; for example, an inverting arc must contain only a single inverting ccsn_first_stage group or an inverting ccsn_first_stage group, and a non-inverting ccsn_last_stage group, or a non-inverting ccsn_first_stage group and an inverting ccsn_last_stage group. To fix the issue, re-characterize the library with appropriate settings, such that the timing sense of the arc should be consistent with sense of the ccsn_*_stage group.

TECHLIB-1336

NAME

TECHLIB-1336

SUMMARY

The first or last value in %s attribute is not equal %d or %d respectively. The attribute will be ignored.

DESCRIPTION

This message is issued when the first/last value of the attribute receiver_capacitance_rise_threshold_pct/receiver_capacitance_fall_threshold_pct is incorrectly defined. The valid value of first and last point for receiver_capacitance_rise_threshold_pct attribute is [0.0, and 100] and for receiver_capacitance_fall_threshold_pct attribute is [100, and 0.0]. Such attribute will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the threshold values are correctly defined at library level.

TECHLIB-1337

NAME

TECHLIB-1337

SUMMARY

The library has '%s' groups defined but the '%s' definition is missing from library group. All '%s' groups will be ignored.

DESCRIPTION

This message is issued when the attribute receiver_capacitance_rise_threshold_pct/receiver_capacitance_fall_threshold_pct is missing at

library level but receiver_capacitance_rise/receiver_capacitance_fall groups are defined. Complete set of receiver_capacitance groups will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the threshold values are not undefined.

TECHLIB-1338

NAME

TECHLIB-1338

SUMMARY

The segment value for '%s' group for %s and cell '%s' has value %d which is not in the expected range [1, %d]. The group will be ignored.

DESCRIPTION

This message is issued when the attribute segment defined for receiver_capacitance_rise/receiver_capacitance_fall group is out of range as per segment definition. The valid range of segment attribute is 1 to N where N is the number of {threshold points -1} defined in the attribute receiver_capacitance_rise_threshold_pct/receiver_capacitance_fall_threshold_pct. For example if seven threshold points are defined then valid range of segment attribute would be {threshold points -1} that is six. Complete set of receiver_capacitance groups will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the segment values are defined correctly.

TECHLIB-1339

NAME

TECHLIB-1339

SUMMARY

The '%s' groups for all segments in the range [1, %d] for %s and cell '%s' are not defined. The

segment '%d' is missing. The '%s' groups will be ignored.

DESCRIPTION

This message is issued when the receiver_capacitance_rise/receiver_capacitance_fall group for all the segments is not defined. The valid range of segment attribute is 1 to N where N is the number of {threshold points -1} defined in the attribute receiver_capacitance_rise_threshold_pct/receiver_capacitance_fall_threshold_pct. Complete set of receiver_capacitance groups will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the receiver_capacitance groups are defined for all segment values.

TECHLIB-1340

NAME

TECHLIB-1340

SUMMARY

The value %s specified for variable_%d for '%s' group '%s' is invalid. This template group is used in '%s' (line %d). For this group valid variable values are %s only. The group '%s' will be ignored.

DESCRIPTION

This message is issued when invalid variable is defined in the template used for specifc groups. For example variable time specified for the receiver_capacitance_rise/receiver_capacitance_fall group is invalid, the valid values are input_net_transition and total_output_net_capacitance. These groups with invalid template will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the defined variable should be valid.

TECHLIB-1341

NAME

TECHLIB-1341

SUMMARY

The %s index values for '%s' group (line %d) for %s and cell '%s' do not match among all segments. These '%s' groups will be ignored.

DESCRIPTION

This message is issued when there is mismatch in the index values of input_net_transition/total_output_net_capacitance defined for receiver_capacitance_rise/receiver_capacitance_fall group at pin or timing level. Complete set of receiver_capaciatnce groups will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the index values should be same.

TECHLIB-1342

NAME

TECHLIB-1342

SUMMARY

The %s group with segment value '%d' is redefined at line %d for %s and cell '%s'. The last definition will be considered.

DESCRIPTION

This message is issued when the receiver_capacitance_rise/receiver_capacitance_fall group with the same segment value is defined more than once at pin or timing level. The multiple definition of same segment value is not allowed. Last definition will be considered and rest will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the segment value is correctly defined.

TECHLIB-1343

NAME

TECHLIB-1343

SUMMARY

The %s group can have only one or two dimensional tables. All %s groups for %s and cell '%s' will be ignored.

DESCRIPTION

This message is issued when the dimensions of receiver_capacitance_rise/receiver_capacitance_fall table is more than two. The receiver_capacitance group can have only one or two dimensional tables. Complete set of receiver_capaciatnce groups will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the table dimension should be correct.

TECHLIB-1344

NAME

TECHLIB-1344

SUMMARY

The size of %s tables for %s and cell '%s' do not match among all segments. All '%s' groups will be ignored.

DESCRIPTION

This message is issued when there is mismatch in the size of receiver_capacitance_rise/receiver_capacitance_fall tables among all the segments defined at pin or timing level. Complete set of receiver_capacitance groups will be ignored. To fix the issue, re-

characterize the library with appropriate settings, such that the receiver_capacitance tables should be matched.

TECHLIB-1345

NAME

TECHLIB-1345

SUMMARY

This library contains both multi-segmented CCS receiver capacitance models and the older two piece receiver capacitance models. The multi-segmented CCS receiver capacitance models will be used in analysis.

DESCRIPTION

This message is issued when the library contains both multi-segmented CCS receiver capacitance model and the two piece receiver capacitance model. The multi-segmented CCS receiver capacitance models will be used for analysis.

TECHLIB-1346

NAME

TECHLIB-1346

SUMMARY

The attribute '%s' defined in group '%s' on line %d is not monotonically %s for values '%f' to '%f'. This may lead to undesirable analysis results. The attribute will be ignored.

DESCRIPTION

The message is issued when an attribute range does not increase or decrease monotonically as

per the Liberty standard or convention. For example, instead of the expected range of monotonically increasing index_1: (1, 2, 3, 4, 5), the range defined in library is index_1: (1, 2, 3, 2, 3). To fix the issue, re-characterize the library with appropriate settings.

TECHLIB-1347

NAME

TECHLIB-1347

SUMMARY

Identified mismatch in the number of pins specified in the attributes pin_names and pin_name_map for the cell '%s' for sensitization group '%s'. The sensitization group for that cell will be ignored.

DESCRIPTION

This message is issued when there is mismatch in the number of pins specified in pin_names attribute at library level and pin_name_map attribute at cell/timing level for the sensitization group. The sensitization group for that cell will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the pins are correctly defined.

TECHLIB-1348

NAME

TECHLIB-1348

SUMMARY

Referred sensitization group '%s' in cell '%s' is not defined at library level. The sensitization group for that cell will be ignored.

DESCRIPTION

This message is issued when the sensitization group name specified in sensitization_master attribute at cell/timing level is not defined at library level. The sensitization group for that cell will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the undefined sensitization group is not referred.

TECHLIB-1349

NAME

TECHLIB-1349

SUMMARY

The attributes '%s' defined with value ('%d') for cell '%s' is invalid, the value should not be 0.

DESCRIPTION

This message is issued when the attributes wave_rise_sampling_index and wave_fall_sampling_index are defined with '0' value in sensitization group. Such attribute will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the attributes are defined correctly.

TECHLIB-1350

NAME

TECHLIB-1350

SUMMARY

The attribute '%s' defined with value '%d' for cell '%s' is invalid, the value should not be greater than the number of entries in {wave_rise/wave_fall} -1 ('%d').

DESCRIPTION

This message is issued when the attributes wave_rise_sampling_index and wave_fall_sampling_index are defined with the value which is greater than the number of entries in {wave_rise/wave_fall} -1. Such attribute will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the attributes are defined correctly.

TECHLIB-1351

NAME

TECHLIB-1351

SUMMARY

The number of entries ('%d') in the attribute '%s' defined for cell '%s' is greater than the number of entries in {wave_rise/wave_fall}-1 ('%d'). The attribute will be ignored.

DESCRIPTION

This message is issued when the number of entries defined in the attributes wave_rise_time_interval and wave_fall_time_interval are greater than the number of entries in {wave_rise/wave_fall} -1. Such attribute will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the attributes are defined correctly.

TECHLIB-1352

NAME

TECHLIB-1352

SUMMARY

The attribute '%s' has undefined vector ID (%d) for the sensitization group (%s) specified for cell '%s'. The attribute is ignored.

DESCRIPTION

This message is issued when the attributes wave_rise and wave_fall are defined with incorrect vector ID in the sensitization group. Such attribute will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the attributes are defined correctly.

TECHLIB-1353

NAME

TECHLIB-1353

SUMMARY

The vector ID ('%d') defined is already present in sensitization group '%s'. Last definition of the vector ID will be considered. Vector ID should be unique.

DESCRIPTION

This message is issued when the sensitization group has two or more vectors with the same vector ID. If duplicate vector IDs are present then tool will use the last vector with that ID. To fix the issue, re-characterize the library with appropriate settings, such that the vector ID defined should be unique.

TECHLIB-1354

NAME

TECHLIB-1354

SUMMARY

The sensitization_master attribute is not present in cell '%s' but cell contains sensitization information. Sensitization group information for that cell will be ignored.

DESCRIPTION

This message is issued when the sensitization_master attribute is not defined at cell level but cell contains sensitization information. sensitization_master attribute is required attribute if cell contains sensitization information. Sensitization group information for that cell will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the attribute is completely specified.

TECHLIB-1355

NAME

TECHLIB-1355

SUMMARY

Pin '%s' specified in pin_name_map attribute at cell/timing level is either not present or refers to bus/bundle in cell '%s'. The sensitization group for that cell will be ignored.

DESCRIPTION

This message is issued when the pin specified for the sensitization in the pin_name_map attribute at cell or timing level either does not exist or refers to bus/bundle in cell. The sensitization group for that cell will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the pins are correctly specified.

TECHLIB-1356

NAME

TECHLIB-1356

SUMMARY

The number of pins in pin_names ('%d') do not match with the number of pins specified ('%d') in the vector attribute of sensitization group '%s'.

DESCRIPTION

This message is issued when the size of the attribute pin_names does not match with the number of columns of the second argument of vector attribute in the sensitization group. All the attributes defined for the sensitization group for that cell/timing will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the size of pin_names attribute is defined correctly.

TECHLIB-1357

NAME

TECHLIB-1357

SUMMARY

The attribute vector defined with vector ID ('%d') in sensitization group '%s' is negative. Vector ID should not be negative.

DESCRIPTION

This message is issued when the attribute vector is specified with negative vector ID in the sensitization group. Such vector attribute will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the vector ID is defined correctly.

TECHLIB-1358

NAME

TECHLIB-1358

SUMMARY

One or more vector values defined in the vector with ID '(%d)' in sensitization group '%s' are invalid. This vector attribute will be ignored

DESCRIPTION

This message is issued when the attribute vector is specified with invalid value in the sensitization group. The valid values are {0,1,X,Z} . The attribute vector will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the vector values are defined correctly.

TECHLIB-1359

NAME

TECHLIB-1359

SUMMARY

Timing library contains both 2-piece and multi-piece receiver capacitance data. Multi-piece receiver capacitance data will be ignored. To use multi-piece receiver capacitance data for timing analysis, specify 'set timing_library_enable_advanced_capacitance_support 1' before loading the libraries in flow.

DESCRIPTION

Support for advanced capacitance data in libraries is enabled under global variable timing_library_enable_advanced_capacitance_support. If library contains both 2-piece and N-piece receiver capacitance data, tool will load 2-piece capacitance data by default. To enable loading of N-piece receiver capacitance data, this global variable must be set before read_lib or read_view_definition command in the flow.

TECHLIB-1360

NAME

TECHLIB-1360

SUMMARY

The voltage values for %s group in '%s' is not %s at point close to %f (%s at '%f'). The value should

%s in the tolerance range of %f.

DESCRIPTION

The voltage waveform for rise/fall transition should start at point close to 0/1 and end at close to 1/0.

TECHLIB-1361

NAME

TECHLIB-1361

SUMMARY

The number of index/values points found is '%d'. The number of sample points(index/values) should be 10 or more than 10 for accurate delay calculation.

DESCRIPTION

The number of sample time and voltage points should be more than 10 for accurate delay calculation.

TECHLIB-1362

NAME

TECHLIB-1362

SUMMARY

The sample points for ECSM waveform number %d in %s transition are not near the %s threshold.

DESCRIPTION

The number of sample time and voltage points should be more than 10 for accurate delay calculation.

TECHLIB-1363

NAME

TECHLIB-1363

SUMMARY

The slew value %f for ECSM waveform number %d in %s transition for %s of cell '%s' does not match the corresponding NLDM slew value %f.

DESCRIPTION

This message is issued when the slew value calculated from ECSM waveform (e.g slew = time values at (upper slew threshold-lower slew threshold)) for rise/fall transition does not match with corresponding NLDM slew value. This can cause delay calculation discrepancies.

TECHLIB-1364

NAME

TECHLIB-1364

SUMMARY

The attribute '%s' is defined but the attribute '%s' is not defined in '%s' group. The attribute '%s' will be ignored.

DESCRIPTION

This message is issued when defining one attribute alone is not sufficient, but another attribute which is also mandatorily needed to be defined with that attribute, is missing.

TECHLIB-1365

NAME

TECHLIB-1365

SUMMARY

The %s vector group for %s has a duplicate definition (line '%d') on %s and cell '%s'. The duplicate definition will be ignored.

DESCRIPTION

This message is issued when the vector group specified in output_voltage_rise/output_voltage_fall group for ccsn_first_stage/ccsn_last_stage group or output_current_rise/output_current_fall for timing group is defined more than once with the same value of 'total_output_net_capacitance' and 'input_net_transition'. Multiple definition of vector group with same values of 'total_output_net_capacitance' and 'input_net_transition' is not allowed. To fix the issue, re-characterize the library with appropriate settings, such that the vector group defined is unique.

TECHLIB-1366

NAME

TECHLIB-1366

SUMMARY

All combinations of %s in vector groups(s) of %s are not defined. The definition for %s vector group(s) is missing on %s and cell %s. The group will be ignored.

DESCRIPTION

This message is issued when any of the combination of input_net_transition and

total_output_net_capacitance defined in vector group for the output_voltage_rise/output_voltage_fall group in ccsn_first_stage/ccsn_last_stage group or output_current_rise/output_current_fall for timing group is missing. To fix the issue, re-characterize the library with appropriate settings, such that the vector groups are defined for all combination of input_net_transition and total_output_net_capacitance.

TECHLIB-1367

NAME

TECHLIB-1367

SUMMARY

The delay value '%f' calculated for CCS waveform for '%s' vector group on %s of cell '%s' does not match with the corresponding NLDM delay value '%f' at line '%d' and has '%.2g%%' error

DESCRIPTION

This message is issued when there is mismatch in delay value calculated for CCS timing waveform and its corresponding NLDM delay value. The percentage error is calculated with reference to NLDM delay value.

TECHLIB-1368

NAME

TECHLIB-1368

SUMMARY

The slew value '%f' calculated for CCS waveform for '%s' vector group on %s of cell '%s' does not match with the corresponding NLDM slew value '%f' at line '%d' and has '%.2g%%' error

DESCRIPTION

This message is issued when there is mismatch in slew value calculated for CCS timing waveform and its corresponding NLDM slew value. The percentage error is calculated with reference to NLDM slew value.

TECHLIB-1369

NAME

TECHLIB-1369

SUMMARY

Design loading is aborted as the input ldb '%s' is not compatible with the current tool settings which enable support for advanced pin capacitance in library. It is recommended to either re-compile the ldb using write_ldb command with current tool version or turn off the global 'timing_library_enable_advanced_capacitance_support' to proceed.

DESCRIPTION

This message is issued when global 'timing_library_enable_advanced_capacitance_support' is on to enable support of libraries with multi-piece CCS capacitance or ecsm_capacitance_set library constructs but input ldb provided is generated with version prior to Tempus 15.2 or Innovus 16.1 release. Such ldb files are incompatible with advanced pin capacitance feature support. User must either re-compile the ldb file with current tool version (or at least version newer than Tempus 15.2 or Innovus 16.1) if advanced capacitance feature is to be used or else turn off the global to disable the feature.

TECHLIB-1370

NAME

TECHLIB-1370

SUMMARY

Identified inconsistency between function and timing sense for timing arc on pin '%s' of cell '%s'

DESCRIPTION

This message is issued when the timing sense defined for timing arc is not consistent with the function of pin. For example, in case of inverter, which has function '!A' then arc should have a negative_unate timing sense. To fix the issue, re-characterize the library with appropriate settings, such that the timing_sense and function are consistent.

TECHLIB-1371

NAME

TECHLIB-1371

SUMMARY

The '%s' pin '%s' defined for cell '%s' in library '%s' is either not defined or defined with different direction in the cell '%s' in library '%s'. The design loading will be aborted.

DESCRIPTION

This message is issued when either the pin is defined for cell in one library and not defined for the same cell in other library or pins are defined with different direction. For example: Pin(A) defined as input pin for cell in one library and is not defined or defined as output pin in other library. Design loading will be aborted. To fix the issue, re-characterize the libraries with appropriate settings, such that the pins of same cell across libraries are consistent

TECHLIB-1372

NAME

TECHLIB-1372

SUMMARY

Scalar table specified for '%s' group defined on %s of cell '%s' is not supported. This group will be ignored.

DESCRIPTION

This message is issued when the scalar table is specified for ecsm_capacitance group. Such ecsm_capacitance group will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the tables are specified with correct dimension.

TECHLIB-1374

NAME

TECHLIB-1374

SUMMARY

The normalized_driver_waveform %s is already defined on line %d. The first definition will be retained, rest will be ignored.

DESCRIPTION

This message is issued when the normalized_driver_waveform group is defined multiple times either with same driver_waveform_name or without driver_waveform_name at library level. The first definition will be retained and rest will be ignored. To fix the issue, re-characterize the library with appropriate settings, such that the normalized_driver_waveform groups defined at library level are unique.

TECHLIB-1377

NAME

TECHLIB-1377

SUMMARY

Invalid data_type '%s' is specified with command option -liberty_incremental. Valid values of data_type is ccs_power.

DESCRIPTION

This message is issued when data_type specified with command option -liberty_incremental is invalid. Valid values of data_type is ccs_power. To fix the issue, specify the correct data_type.

TECHLIB-1378

NAME

TECHLIB-1378

SUMMARY

Attribute driver_waveform_name '%s' specified with '%s' in set_normalized_driver_waveform command is not defined in reference library '%s'. The command will be ignored.

DESCRIPTION

This message is issued when the driver_waveform_name specified with command option 'set_normalized_driver_waveform_lib -rise_waveform/fall_waveform' is not defined in reference library. To fix the issue, specify the correct driver_waveform_name.

TECHLIB-1379

NAME

TECHLIB-1379

SUMMARY

An inconsistency was found due to power arc defined on pin '%s' of cell '%s' between first library '%s' and second library. The power arc with attribute(s) '%s' is not defined in '%s' library.

DESCRIPTION

This message is issued when inconsistency found due to the power arc between the libraries. For example power_arc_1 defined for cell_1 is present in library_1 but missing for cell_1 in library_2.

TECHLIB-1380

NAME

TECHLIB-1380

SUMMARY

An inconsistency was found due to '%s(%f,%f)' value defined at library level between first library '%s' and second library. The PVT condition must be same between two libraries.

DESCRIPTION

This message is issued when there is a mismatch in the PVT condition between two libraries. Library header name and PVT condition must be same.

TECHLIB-1381

NAME

TECHLIB-1381

SUMMARY

The library merging has failed due to the inconsistency between reference library '%s' and incremental library. To fix the issue, refer the previous messages.

DESCRIPTION

This message is issued when library merging has failed due to the inconsistency between reference library and incremental library. Fix TECHLIB-1380 and TECHLIB-1382 errors issued related to library merging.

TECHLIB-1382

NAME

TECHLIB-1382

SUMMARY

No matching library is present with library header name '%s' corresponding to incremental library.

DESCRIPTION

This message is issued when incremental library set does not have any library which has the same header name as the reference library. For library merging, header name must be same.

TECHLIB-1383

NAME

TECHLIB-1383

SUMMARY

Invalid pin '%s' is specified with the attribute related_output_pin for timing group on %s of cell '%s'. The pin specified with related_output_pin must be an output or inout pin.

DESCRIPTION

This message is issued when the pin specified with attribute related_output_pin is invalid. The direction of pin specified with related_output_pin must be either output or inout. To fix the issue, re-characterize the library with appropriate settings, such that the related_output_pin is correctly defined.

TECHLIB-1384

NAME

TECHLIB-1384

SUMMARY

The absolute mean shift value for '%s' group on %s of cell '%s' has value %f which is greater than the value %f. This may impact the delay calculation accuracy.

DESCRIPTION

This message is issued when the absolute mean shift value is beyond the range. The value should be less than the value calculated as {0.5*std_dev} for accurate delay calculation. To fix the issue, re-characterize the library with appropriate settings, such that the absolute mean shift is within the defined range.

TECHLIB-1385

NAME

TECHLIB-1385

SUMMARY

The standard deviation value for '%s' group on %s of cell '%s' has value %f which is greater than the value %f. This may impact the delay calculation accuracy.

DESCRIPTION

This message is issued when the standard deviation value is beyond the range. The value should be less than the value calculated as {0.3*input slew} for accurate delay calculation. To fix the issue, re-characterize the library with appropriate settings, such that the standard deviation is within the defined range.

TECHLIB-1386

NAME

TECHLIB-1386

SUMMARY

The cell '%s' has %u sigma tables out of %u(%g%%) which have beyond the range(1/%g and %g) ratios of attribute sigma_type late to early value. This can result in inaccurate analysis. Cadence recommends libraries with LVF moments for such high sigma variation cells.

DESCRIPTION

This message is issued when the ratio of late and early sigma values is not within the range of (1/x and x). The default value of x is 3. Cadence recommends libraries with LVF moments for such high sigma variation cells.

TECHLIB-1388

NAME

TECHLIB-1388

SUMMARY

The cell '%s' is %s in library '%s' but %s in other library.

DESCRIPTION

This message is issued when the cell is defined in one library but not defined in other library. For example: cell (AND) is defined is defined in one library and is not defined in other library. To fix the issue, re-characterize the libraries with appropriate settings, such that the cells across libraries are consistent.

TECHLIB-1389

NAME

TECHLIB-1389

SUMMARY

The %s '%s' is '%s' for cell '%s' in library '%s' but '%s' in the cell '%s' in other library.

DESCRIPTION

This message is issued when the pin is defined for cell in one library and not defined for the same cell in other library. For example: Pin(A) defined is defined for cell in one library and is not defined in other library. To fix the issue, re-characterize the libraries with appropriate settings, such that the pins for the same cell across libraries are consistent.

TECHLIB-1391

NAME

TECHLIB-1391

SUMMARY

The test_cell group is defined for cell '%s' but its corresponding sequential group information is missing. The test_cell group will be ignored.

DESCRIPTION

This message is issued when the cell has test_cell group but its corresponding sequential group information is not defined. The behavior defined in test_cell group, must be already described by an ff, ff_bank, latch, latch_bank or statetable at cell level. To fix the issue, re-characterize the library with appropriate settings, such that the cell having test_cell group must have corresponding

sequential group information.

TECHLIB-1392

NAME

TECHLIB-1392

SUMMARY

The voltage_name '%s' specified in pg_pin '%s' of pg_type '%s' of cell '%s' is mapped to voltage %gV. The nom_voltage %gV will be used for this pg_pin.

DESCRIPTION

This message is issued when pg_pin of pg_type primary_power/backup_power is mapped with the voltage having 0V or less than 0V. In such case, nominal voltage will be used for power pg_pin. To fix the issue, re-characterize the libraries with appropriate settings

TECHLIB-1393

NAME

TECHLIB-1393

SUMMARY

The %s table is not supported for %s '%s'. This table will be ignored.

DESCRIPTION

This message is issued when a particular attribute is not supported in SOCV side file. For example, RC variation multipler table cannot have object_type attribute as 'library'. To fix the issue, re-characterize the libraries with appropriate settings.

TECHLIB-1394

NAME

TECHLIB-1394

SUMMARY

Missing %s delay value for the path from pin %s to pin %s in the cell %s. Path is not generated. The data in the timing library is incomplete. This can result in a loss of accuracy during delay calculation.

DESCRIPTION

This message is issued when delay/retain values are not specified for the path. Path is not generated if either delay or slew value is missing. To fix the issue, re-characterize the libraries such that delay/retain values are specified correctly

TECHLIB-1395

NAME

TECHLIB-1395

SUMMARY

The library level attribute(s) receiver_capacitance_rise_threshold_pct or(and) receiver_capacitance_fall_threshold_pct are defined in library but the library has no 'receiver_capacitance_rise' and 'receiver_capacitance_fall' groups.

DESCRIPTION

The library level attribute(s) receiver_capacitance_rise_threshold_pct or(and) receiver_capacitance_fall_threshold_pct are defined in library but the library has no 'receiver_capacitance_rise' and 'receiver_capacitance_fall' groups.

TECHLIB-1396

NAME

TECHLIB-1396

SUMMARY

The cell '%s' with ff/latch group has pin reference names but there is no pin with reference_input attribute. The ff/latch group will be ignored.

DESCRIPTION

This message is issued when the ff/latch group is defined with format that expects reference pin as reference_input in any pin but its not present. The ff groups will be ignored in such cases. To fix the issue, re-characterize the library with appropriate settings, such that the correct combination is used.

TECHLIB-1397

NAME

TECHLIB-1397

SUMMARY

The cell '%s' doesn't have ff/latch group with pin reference names but there is pin with reference_input attribute.

DESCRIPTION

This message is issued when the cell has pin with reference_input attribute but it doesn't have any ff/latch group with reference pin names. To fix the issue, re-characterize the library with appropriate settings, such that the correct combination is used.

TECHLIB-1398

NAME

TECHLIB-1398

SUMMARY

The '%s' waveform specified in cell '%s' has very long tail with time value reaching '%f'. The last '%d' points in waveform will be ignored and tool will complete the waveform using extrapolation for timing analysis.

DESCRIPTION

This message is issued when there are points in CCS timing waveform (output_curent_rise/output_current_fall) which results in very long tail in waveform. These long tails in waveform if used as such may cause issues in delay calculations. The waveform has very big values in time index. Tool ignores such bad points and completes the waveform using extrapolation for timing analysis. Such waveform indicate issue in characterization and should be reviewed.

TECHLIB-1399

NAME

TECHLIB-1399

SUMMARY

Attributes tied_off and related_pin present in timing group for pin '%s' of cell '%s'. Attribute related_pin cannot be specified on a tied_off output pin.

DESCRIPTION

This message is issued when tied_off output pin consists related_pin attribute in the timing group.

To fix the issue, re-characterize the library with appropriate settings, such that the related_pin is not specified for tied_off output pin.

TECHLIB-1400

NAME

TECHLIB-1400

SUMMARY

Invalid group names '%s' specified with 'timing_library_ignore_groups'.

DESCRIPTION

This message is issued when invalid group names are specified with 'timing_library_ignore_groups', to be ignored.

TECHLIB-1401

NAME

TECHLIB-1401

SUMMARY

The timing arc defined on pin '%s' of cell '%s' with timing_sense '%s' and related_pin '%s' has invalid when attribute '%s'. The when condition is not compatible with the pin function '%s'.

DESCRIPTION

This message is issued when timing_arc is defined with invalid when condition for specified timing_sense and related_pin attributes. For example: in case of two input Mux (S0 I0 + !S0 I1) for related pin I0, the valid timing arcs are ((S0 I1) and (S0 !I1)) or (S0), which implies that output will toggle on toggling I0 only if S0=0. If when condition is defined as (!S0 I1), which is an invalid when

condition as there would be no transition in this condition at the output. To fix the issue, re-characterize the library with appropriate settings, such that the timing arc is defined with correct when condition.

TECHLIB-1402

NAME

TECHLIB-1402

SUMMARY

The timing arc defined on pin '%s' of cell '%s' with timing_sense '%s' and related_pin '%s' is not defined for all possible 'when' conditions but default arc is present in library. As per the pin function '%s', the timing arc(s) with when condition '%s' are not defined.

DESCRIPTION

This message is issued when timing arc(s) are missing for reported when condition expression for specified pin function but default arc is present. For example, in case of two input Mux (S0 I0 + !S0 I1) for related pin I0, the valid timing arcs are ((S0 I1) and (S0 !I1)) or (S0), which implies that output will toggle on toggling I0 only if S0=0. If any of the arc ((S0 I1) and (S0 !I1)) is missing, it will be an invalid condition. To fix the issue, re-characterize the library with appropriate settings, such that the timing arc for all valid combinations are specified.

TECHLIB-1403

NAME

TECHLIB-1403

SUMMARY

The timing arc defined on pin '%s' of cell '%s' with timing_sense '%s' and related_pin '%s' is not defined for all possible 'when' conditions. As per the pin function '%s', the timing arc(s) with when condition '%s' are not defined.

DESCRIPTION

This message is issued when timing arc(s) are missing for reported when condition expression for specified pin function and default arc is also not specified. For example, in case of two input Mux (S0 I0 + !S0 I1) for related pin I0, the valid timing arcs are ((S0 I1) and (S0 !I1)) or (S0), which implies that output will toggle on toggling I0 only if S0=0. If any of the arc ((S0 I1) and (S0 !I1)) is missing, it will be an invalid condition. To fix the issue, re-characterize the library with appropriate settings, such that the timing arc for all valid combinations are specified.

TECHLIB-1404

NAME

TECHLIB-1404

SUMMARY

The timing arc defined on pin '%s' of cell '%s' with related_pin '%s' has incorrect timing sense '%s'. As per the when condition '%s' and pin function '%s', the timing sense should be '%s'.

DESCRIPTION

This message is issued when timing_sense is invalid as per the 'when' condition defined for timing arc. For example, in case of two input Mux (S0 I0 + !S0 I1) for related pin I0, the valid timing arcs are ((S0 I1) and (S0 !I1)) or (S0), which implies that output will toggle on toggling I0 only if S0=0. This implies positive unate relationship between I0 and output. Attribute timing_sense with 'negative_unate' for this condition would be incorrect. To fix the issue, re-characterize the library with appropriate settings, such that the timing arc is specified with correct timing_sense

TECHLIB-1405

NAME

TECHLIB-1405

SUMMARY

The timing arc defined on pin '%s' of cell '%s' with related_pin '%s' has incorrect timing sense '%s'. As per the pin function '%s', the timing sense should be '%s'.

DESCRIPTION

This message is issued when the timing sense defined for timing arc is not consistent with the function of pin. For example, in case of inverter, which has function (!A) then arc should have a negative_unate timing sense. To fix the issue, re-characterize the library with appropriate settings, such that the timing_sense and function are consistent.

TECHLIB-1406

NAME

TECHLIB-1406

SUMMARY

The timing arc defined on pin '%s' of cell '%s' has related_pin '%s'. As per the pin function '%s', the timing arc is not valid.

DESCRIPTION

This message is issued when timing_arc defined for specified 'related_pin' attribute is invalid as per the pin function. To fix the issue, re-characterize the library with appropriate settings, such that the timing arc is correctly defined.

TECHLIB-1407

NAME

TECHLIB-1407

SUMMARY

There is no combinational timing arc defined on pin '%s' of cell '%s' with related pin '%s'. As per the pin function '%s', there should be at least one timing arc defined.

DESCRIPTION

This message is issued when timing_arc is not defined for specified 'related_pin' attribute as per the pin function. To fix the issue, re-characterize the library with appropriate settings, such that the timing arc is defined for all possible valid condition.

TECHLIB-1408

NAME

TECHLIB-1408

SUMMARY

The ratio of attribute '%s' of group '%s' to the corresponding '%s' group specified on %s of cell '%s' has one or more values(%f) which are not in range [%g <= and >= %g]. This may lead to unexpected analysis results.

DESCRIPTION

This message is issued when ratio of skewness and its corresponding std_dev is not in the pre-defined range. This may lead to unexpected results in analysis. To fix the issue, re-characterize the library with appropriate settings to have requisite values per the standard for the attributes for which this message is issued.

TECHLIB-1409

NAME

TECHLIB-1409

SUMMARY

Attribute related_pin is missing for '%s' group specified on pin '%s' of cell '%s'. Attribute is mandatory if '%s' is specified on output pin.

DESCRIPTION

This message is issued when attribute related_pin is missing for max_trans/cap group. To fix the issue, re-characterize the library with appropriate settings, such that the max_trans/cap group is correctly defined.

TECHLIB-1410

NAME

TECHLIB-1410

SUMMARY

For group '%s', 2-Dimensional table is specified on input %s of cell '%s'. 2-Dimensional table is not supported on input pin.

DESCRIPTION

This message is issued when 2-Dimensional table for group max_trans/cap is specified on input pin. To fix the issue, re-characterize the library with appropriate settings, such that the max_trans/cap tables are correctly defined.

TECHLIB-1411

NAME

TECHLIB-1411

SUMMARY

The libraries being merged have different timing_model_types. The libraries '%s' and '%s' cannot be merged.

DESCRIPTION

This message is issued when libraries with different timing_model_type(s) are attempted to be merged with 'merge_model_timing' command. Libraries need to be merged must have the same timing_model_type.

TECHLIB-1412

NAME

TECHLIB-1412

SUMMARY

The '%s' group '%s' referenced in '%s' attribute of '%s' group of %s is not defined in %s of cell '%s'.

DESCRIPTION

This message is issued when input_ccb/output_ccb groups mentioned in attribute, are not defined on pin. To fix the issue, re-characterize the library with appropriate settings, such that the input_ccb/output_ccb groups should be defined.

TECHLIB-1413

NAME

TECHLIB-1413

SUMMARY

The attribute '%s' of '%s' group of %s of cell '%s' does not support timing arcs with three or more inverting stages.

DESCRIPTION

This message is issued when attribute propagating_ccb mentions timing_arcs with three or more inverting stages. To fix the issue, re-characterize the library with appropriate settings.

TECHLIB-1414

NAME

TECHLIB-1414

SUMMARY

In cell '%s', the '%s' vector groups specified on %s are defined for more than one 'total_output_net_capacitance' index value. This group is defined in '%s' group '%s' that does not directly drive an output pin, referenced in '%s' attribute of 'timing' group defined in %s.

DESCRIPTION

This message is issued when output_voltage_rise/fall vector groups are defined for more than one load index value. To fix the issue, re-characterize the library with appropriate settings, such that vector groups should be specified for only one load index value as CCB group does not directly drives an output pin.

TECHLIB-1415

NAME

TECHLIB-1415

SUMMARY

In cell '%s', the '%s' vector groups specified on %s are defined for only one 'total_output_net_capacitance' index value. This group is defined in '%s' group '%s' that directly drives an output pin, referenced in '%s' attribute of 'timing' group defined in %s.

DESCRIPTION

This message is issued when output_voltage_rise/fall vector groups are defined for only one load index value. To fix the issue, re-characterize the library with appropriate settings, such that vector groups should be specified for more than one load index value as CCB group directly drives an output pin.

TECHLIB-1416

NAME

TECHLIB-1416

SUMMARY

The receiver capacitance %s groups are missing in the timing group%s specified for %s of cell '%s'.

DESCRIPTION

This message is issued when either the rise group (receiver_capacitance1_rise/receiver_capacitance2_rise or receiver_capacitance_rise) or the fall group (receiver_capacitance1_fall/receiver_capacitance2_fall or receiver_capacitance_fall) is missing in the timing arc. Moreover, there is no corresponding pin level receiver_capacitance group with the default or same when condition having the missing information. To fix the issue, re-characterize the library with appropriate settings, such that the receiver_capacitance group is defined correctly

TECHLIB-1417

NAME

TECHLIB-1417

SUMMARY

The SOCV side file library doesn't support voltage attribute with multiple values. It will be ignored.

DESCRIPTION

This message is issued when the voltage attribute in SOCV side file contains more than one voltage entry. To fix the issue, re-characterize the SOCV side file with appropriate settings.

TECHLIB-1418

NAME

TECHLIB-1418

SUMMARY

The command '%s' is recommended to be run in a separate Tempus session. No other commands must be run either before or after this command. Design sanity may not be maintained when this command is run.

DESCRIPTION

This message is issued when commands such as merge_model_timing or write_ldb are executed, to warn the user that such commands are stand-alone and it is recommended to run them in a separate Tempus session. No other commands must be run either before or after this command. Design sanity may not be maintained when this command is run.

TECHLIB-1419

NAME

TECHLIB-1419

SUMMARY

The expression '%s' specified for attribute %s for %s is invalid. %s. The attribute will be ignored.

DESCRIPTION

This message is issued when software encounters an error in parsing the boolean expressions like power_down_function etc.. To rectify the issue, fix the error issued by correcting the Boolean expression definition.

TECHLIB-1420

NAME

TECHLIB-1420

SUMMARY

The receiver capacitance group specified for '%s' input transition is invalid for '%s' timing arc defined for %s in cell '%s'.

DESCRIPTION

This message is issued when a timing arc had receiver capacitance group specified which is not invalid. The validity check is done on the basis of valid input pin transitions for the given timing group.

TECHLIB-1421

NAME

TECHLIB-1421

SUMMARY

Attribute 'max_capacitance' on '%s' %s of cell '%s' is not defined in the library.

DESCRIPTION

This message is issued when the attribute max_capacitance is not defined on output/inout pin of cell in the library. To fix the issue, re-characterize the library with appropriate settings, such that the attributes are defined in the cell pin.

TECHLIB-1422

NAME

TECHLIB-1422

SUMMARY

Attribute 'max_transition' on '%s' %s of cell '%s' is not defined in the library.

DESCRIPTION

This message is issued when the attribute max_transition is not defined on any pin of cell in the library. To fix the issue, re-characterize the library with appropriate settings, such that the attributes are defined in the cell pin.

TECHLIB-1423

NAME

TECHLIB-1423

SUMMARY

Attribute 'max_fanout' on '%s' %s of cell '%s' is not defined in the library.

DESCRIPTION

This message is issued when the attribute max_fanout is not defined on output/inout pin of cell in the library. To fix the issue, re-characterize the library with appropriate settings, such that the attributes are defined in the cell pin.

TECHLIB-1424

NAME

TECHLIB-1424

SUMMARY

The number of values in spatial derate table do not match with number of values in distance array in the SOCV side file library. The spatial derate table will be ignored.

DESCRIPTION

This message is issued when there is a mismatch between number of values in spatial derate table and distance array size. To fix the issue, re-characterize the SOCV side file with appropriate settings.

TECHLIB-1425

NAME

TECHLIB-1425

SUMMARY

There is invalid float value specified for '%s' in the SOCV side file library. It will be ignored.

DESCRIPTION

This message is issued when a float value can not be converted into valid value. To fix the issue, re-characterize the SOCV side file with appropriate settings.

TECHLIB-1426

NAME

TECHLIB-1426

SUMMARY

Specify valid value for the option '%s', while using the command 'report_lib_arcs'.

DESCRIPTION

This message is issued when an invalid collection is specified with the option '-arc' or if no arcs are found in the collection specified. The command 'report_lib_arcs -arc' takes the output of the command 'get_lib_arcs', as input. To fix the issue, specify a valid collection.

TECHLIB-1427

NAME

TECHLIB-1427

SUMMARY

There is a mismatch in dimensions of the table '%s' and the axes value specified, for the arc from pin '%s' to '%s' of cell '%s' and library '%s', while using the command 'report_lib_arcs'. The dimension of the table is '%d' and the axes values specified with command options are '%d'.

DESCRIPTION

This message is issued when there is a mismatch between the options specified with command 'report_lib_arcs' and the dimensions of the table. To fix the issue for delay arcs, specify both options 'input_net_transition' and 'total_output_net_capacitance' for 2-D tables, and either one of them for 1-D tables. For constraint arcs, specify both options 'related_pin_transition' and 'constrained_pin_transition' for 2-D tables, and either one of them for 1-D tables.

TECHLIB-1428

NAME

TECHLIB-1428

SUMMARY

The '%s' variable name '%s' is also used for pin '%s' defined on line %d in cell '%s'. The variable name must be unique name.

DESCRIPTION

This message is issued when variable name specified in ff/latch/ff_bank/latch_bank conflicts with pin/bus/bundle name. To fix the issue, please specify unique variable names.

TECHLIB-1429

NAME

TECHLIB-1429

SUMMARY

The '%s' table has negative value(%g) in the SOCV side file library. It will be ignored

DESCRIPTION

This message is issued when a negative float value is present in derate or distance tables. To fix the issue, re-characterize the SOCV side file with appropriate settings.

TECHLIB-1430

NAME

TECHLIB-1430

SUMMARY

The cell '%s' is being ignored due to errors in its definition. This library cell will not be loaded in this session. Refer to the previous messages issued for this cell to find the details of the issue.

DESCRIPTION

This message is issued when cell is defined incorrectly in library. Such cells will be ignored. Refer to previous messages issued for the cell. To fix the issue, re-characterize the library with appropriate settings, such that the cell is correctly defined in the library.

TECHLIB-1431

NAME

TECHLIB-1431

SUMMARY

Valid command options for a collection of '%s' arc(s) is '%s' and/or '%s'.

DESCRIPTION

This message is issued when there is a mismatch between the axes specified with the command 'report_lib_arcs' and the type of arc(s) in the collection i.e. if input_net_transition or total_output_net_capacitance are specified for a constraint arc collection or if related_pin_transition or constrained_pin_transition are specified for a delay arc collection.

TECHLIB-1433

NAME

TECHLIB-1433

SUMMARY

The pin '%s' defined for bundle '%s' in cell '%s' is not listed in 'members' attribute of bundle.

DESCRIPTION

This message is issued when pin defined as bundle pin but not specified in member attribute. To fix the issue, re-characterize the library with appropriate settings, such that the pins are defined correctly for bundle group.

TECHLIB-1434

NAME

TECHLIB-1434

SUMMARY

The attribute '%s' defined in group '%s' has one or more values which are %s. This may lead to undesirable analysis results. The attribute will be ignored.

DESCRIPTION

The message is issued when attribute values defined are less than zero as per the Liberty standard or convention. For example, slew or cap index ranges cannot have negative values. To fix the issue, re-characterize the library with appropriate settings.

TECHLIB-1435

NAME

TECHLIB-1435

SUMMARY

For dc_current table defined in cell '%s' and pin '%s', the current values are not monotonically decreasing in the range '%.4g' to '%.4g' for '%s' '%f'.

DESCRIPTION

This message is issued when current values specified in dc_current table defined in CCSN/CCB group are not monotonically decreasing from VSS to VDD. This may impact delay calculation accuracy.

TECHLIB-1436

NAME

TECHLIB-1436

SUMMARY

Identified mismatch '%f' and '%f' in '%s' of the hyperbolic noise %s in pin '%s', for cell '%s', between libraries '%s' and '%s'. The value '%f' would be used.

DESCRIPTION

This message is issued when there is discrepancy between the height/width/area of the hyperblic noise of a cell pin in two libraries. In this case, the value from the first library would be retained.

TECHLIB-1437

NAME

TECHLIB-1437

SUMMARY

Identified mismatch in '%s' voltage ranges '%f to %f' and '%f to %f' in pin '%s', for cell '%s', between libraries '%s' and '%s'. The libraries cannot be used for merging.

DESCRIPTION

This message is issued when there is discrepancy between the power_down_function/always_on atribute of a cell pin in two libraries. This may not permit the merging of these two libraries. To fix the issue, re-characterize the library with appropriate settings, such that there is no discrepency in pin the specified attribute across two libraries.

TECHLIB-1438

NAME

TECHLIB-1438

SUMMARY

Identified mismatch in %s definition in pin '%s', for cell '%s', between libraries '%s and '%s'. The libraries cannot be used for merging.

DESCRIPTION

This message is issued when there is discrepancy between the definition of power_down_function/always_on in a pin of a cell of two libraries. To fix the issue, re-characterize the library with appropriate settings, such that such that there is no discrepency in pin the specified attribute across two libraries.

TECHLIB-1439

NAME

TECHLIB-1439

SUMMARY

Identified mismatch in 'leakage_power' definition, for cell '%s', between libraries '%s' and '%s'. The libraries cannot be used for merging.

DESCRIPTION

This message is issued when there is discrepancy between the definition of leakage_power on a cell of two libraries. To fix the issue, re-characterize the library with appropriate settings, such that such that there is no discrepency in pin the specified attribute across two libraries.

TECHLIB-1440

NAME

TECHLIB-1440

SUMMARY

An inconsistency was found due to CCS and ECSM data present in the libraries specified to be merged. The libraries cannot be used for merging.

DESCRIPTION

This message is issued when timing waveform data in the ETM libraries specified for merging does not have same library format. The libraries consists of the mix of CCS timing and ECSM timing data. Such libraries cannot be merged. To fix the issue, re-characterize the library with appropriate settings, such that there is no discrepancy in timing waveform data representation across libraries.

TECHLIB-1441

NAME

TECHLIB-1441

SUMMARY

The group '%s' in timing arc for %s on cell '%s', is missing for sigma_type '%s'. The table for sigma_type '%s' will be used for both sigma_types 'early' and 'late'.

DESCRIPTION

This message is issued when an ocv_sigma group is not present in a pair on a timing arc. For example 'ocv_sigma_cell_rise' group is present for sigma_type early and missing for sigma_type late. In such cases the same tables would be used for both early and late sigma. To fix the issue, re-characterize the library with appropriate settings, to ensure completeness of ocv_sigma data.

TECHLIB-1442

NAME

TECHLIB-1442

SUMMARY

The timing arc defined for cell '%s' and for pin '%s', with related_pin '%s' and timing_type '%s' in library '%s' is not defined in the cell '%s' in library '%s'.

DESCRIPTION

This message is issued when a timing arc is defined for cell in one library and not defined for the same cell in other library. To fix the issue, re-characterize the libraries with appropriate settings, such that the timing arcs of same cell across libraries are consistent.

TECHLIB-1443

NAME

TECHLIB-1443

SUMMARY

The collection of timing arcs specified with option '%s', should either consist of only delay arcs or only constraint arcs.

DESCRIPTION

This message is issued when the collection of timing arcs specified with option '-arc' in the command 'report_lib_arcs', consists of both delay and constraint arcs. To fix the issue, specify a collection of only delay arcs or only constraint arcs.

TECHLIB-1444

NAME

TECHLIB-1444

SUMMARY

The attribute 'clock' defined on pin '%s' of cell '%s' is inconsistent in all the libraries to be merged. The merged library would have the 'clock' attribute, specified as true on this pin.

DESCRIPTION

This message is issued when there is discrepancy in definition of 'clock' attribute on a pin of the cell, in all libraries to be merged. The merged library would have the 'clock' attribute, specified as true on this pin. To fix the issue, consistency in clock pins should be maintained across libraries.

TECHLIB-1445

NAME

TECHLIB-1445

SUMMARY

Attribute 'function' on output %s of cell '%s' is not defined in the library.

DESCRIPTION

This message is issued when the attribute function is not defined on an output pin of cell in the library. To fix the issue, re-characterize the library with appropriate settings, such that the attribute is defined in the cell pin.

TECHLIB-9001

NAME

TECHLIB-9001

SUMMARY

Cell '%s' has timing arcs/checks from %s '%s' to %s '%s'. Such paths are currently not used by some of the backend tools

DESCRIPTION

Cell <cellName> has timing arc/checks from <pintype> <srcPinName> to <pintype> <DstPinName>. Such paths are not supported by some of the backend tools and may possibly create problems with such tools. It is advised that such timing arcs may be removed from the input technology library OR from the generated TLF file before using it with any backend tools.

TECHLIB-9002

NAME

TECHLIB-9002

SUMMARY

%s

DESCRIPTION

It is internal error message. No description is available.

TECHLIB-9004

NAME

TECHLIB-9004

SUMMARY

Command Line Error.

DESCRIPTION

Command Line Error. \n\nCommand line error occurs when either the input file name is not specified or more than one input files are specified.

TECHLIB-9007

NAME

TECHLIB-9007

SUMMARY

Ignoring Command Line Option. (-sunit option is no longer supported.\nTLF3.1/TLF4.1/TLF4.2 are generated in TLF units\nTLF4.3 is generated in input technology library units.).

DESCRIPTION

This command line option is no longer supported.

TECHLIB-9008

NAME

TECHLIB-9008

SUMMARY

The slew measurement points are incompletely specified. Specify all the slew measurement points

DESCRIPTION

While specifying slew measurement points on the command line it is required that all the slew measured points (slew_measure_lower_rise, slew_measure_lower_fall, slew_measure_upper_rise, slew_measure_upper_fall) are completely defined. The slew measured threshold values should correspond to those used during Spice characterization of the library timing/power data.

TECHLIB-9009

NAME

TECHLIB-9009

SUMMARY

Slew measured command line options are not supported for TLF3.1/TLF4.1. .

DESCRIPTION

Slew measured command line options are supported in TLF4.2 and higher version's of TLF

TECHLIB-9010

NAME

TECHLIB-9010

SUMMARY

Incompletely specified threshold values in input technology library. .

DESCRIPTION

Incompletely specified threshold values in input technology library. . \n\nSpecify the delay characterization threshold values completely either in the input technology library or on the command line. The input technology library has one or more, but not all, of the following defined in the input technology library.\n1. input_threshold_pct_fall\n2. input_threshold_pct_rise\n3. output_threshold_pct_fall\n4. output_threshold_pct_rise\n5. slew_lower_threshold_pct_fall\n6. slew_lower_threshold_pct_rise\n7. slew_upper_threshold_pct_fall\n8.slew_upper_threshold_pct_rise.\nSpecify all the threshold points in the input technology library or use the following command line options\nFor TLF3.1/TLF4.1 use -i,-d,-s,-t and\nFor TLF4.2/TLF4.3 use -ir,-if,-dr,-df,-sr,-sf,-tr,-tf.\n.The threshold points are crucial for timing analysis and should be specified correctly.

TECHLIB-9011

NAME

TECHLIB-9011

SUMMARY

%s. .

DESCRIPTION

While generating TLF3.1/TLF4.1 use -i,-d,-s,-t command line options for specifying the threshold points. While generating TLF4.2/TLF4.3 use -ir,-if,-dr,-df,-sr,-sf,-tr,-tf command line options for specifying the threshold points.

TECHLIB-9012

NAME

TECHLIB-9012

SUMMARY

%s. .

DESCRIPTION

Specify the complete set of threshold points using the command line options '-i,-d,-s,-t' OR '-ir,-if,-dr,-df,-sr,-sf,-tr,-tf'. Complete set of threshold points is crucial for correct timing analysis.

TECHLIB-9016

NAME

TECHLIB-9016

SUMMARY

File '%s' could not be opened for writing.

DESCRIPTION

Either the file specified already exists and there is no permission to overwrite or there is no write permission to the user in the run directory. Check the permissions.

TECHLIB-9017

NAME

TECHLIB-9017

SUMMARY

Nominal Condition '%s' not defined.

DESCRIPTION

Nominal Condition (<NomCondName>) not defined\n\nOne or more of the nominal conditions (nom_process, nom_voltage & nom_temperature) are unspecified in the input technology library.

TECHLIB-9018

NAME

TECHLIB-9018

SUMMARY

Nominal Condition '%s' is not defined in timing library. Assuming default value '%f'. Setting this attribute is recommended as it can impact timing and SI results.

DESCRIPTION

This message is issued when the attribute '<NomCondName>' is not defined in timing library. This attribute is a must requirement in case the user uses the set_op_cond/setOpCond or -opcond command with delay corners in MMMC. This value would be used to derate the library values to the operating conditions of the design. \n\n To avoid this warning, make sure that '<NomCondName>' is specified in the timing library.

TECHLIB-9019

NAME

TECHLIB-9019

SUMMARY

Nominal condition '%s' not defined in input technology library.

DESCRIPTION

The input technology library has derating factors k_process_XXX/k_volt_XXX/k_temp_XXX but does not have nom_process/nom_voltage/nom_temperature defined in the library. Tool needs this/these nominal value(s) to translate the derating factors (k_factors) into TLF linear models. Specify the nominal condition(s) in the input technology library.

TECHLIB-9023

NAME

TECHLIB-9023

SUMMARY

Pin/bus/bundle '%s' definition not found in cell '%s'.

DESCRIPTION

Pin/bus/bundle (<PinName>) definition not found in cell (<CellName>). The indicated cell <CellName> does not have description for the pin/bus/bundle <PinName>. Check if <PinName> has been used correctly. If yes, add the necessary description, otherwise modify the cell by deleting the reference(s) to <PinName>.

TECHLIB-9024

NAME

TECHLIB-9024

SUMMARY

Pin '%s' is invalid for bus '%s' in cell '%s'.

DESCRIPTION

This message is issued when there is a mismatch in pin name and bus name or pin index is out of range as per bus index range defined in a cell. To fix the issue, re-characterize the library with appropriate settings, such that the pin name is matched with bus name.

TECHLIB-9025

NAME

TECHLIB-9025

SUMMARY

Pin name '%s' in bus '%s' of cell '%s' does not match library bus_naming_style '%s'.

DESCRIPTION

Pin name (<PinName>) in bus (<PinBusName>) of cell (<CellName>) does not match library bus_naming_style (<bus_naming_style>). Bus pin name must match the bus naming style of library.

TECHLIB-9026

NAME

TECHLIB-9026

SUMMARY

Look-up table template '%s' definition not found.

DESCRIPTION

Look-up table template (<TemplateName>) definition not found. Undefined look-up table template is referred in the timing description. Check the correctness of <TemplateName>. In case it has been used correctly, add definition for it at the library level, otherwise delete reference(s) to this template.

TECHLIB-9027

NAME

TECHLIB-9027

SUMMARY

Clock pin absent in sequential cell(s) '%s'

DESCRIPTION

Clock pin absent in sequential cell(s) (<CellName>)\n\nThe indicated sequential cell(s) <CellName> does not have any pin with Pintype 'clock'. As per the requirement of delay calculation tools, at least one pin in a sequential cell must be a clock pin. Verify the description of the specified cell(s) in the input technology library.

TECHLIB-9028

NAME

TECHLIB-9028

SUMMARY

Sequential block (ff/ff_bank/latch/latch_bank) missing in cell(s) '%s'. This may cause potential problems with results of downstream tools

DESCRIPTION

Sequential block (ff/ff_bank/latch/latch_bank) missing in cell(s) (<CellName>). This may cause potential problems with results of downstream tools\n\nThe indicated sequential cell(s) <CellName> does not have any sequential block (ff/ff_bank/latch/latch_bank) in the input technology library. This means that for TLF 3.0 translations, the corresponding Register/Latch TLF clauses will not be generated. Besides, this leads to imprecise Pintype determination. Also, if the timing groups of such cells do not have timing_sense attributes, then corresponding path polarities are assumed to be either (i.e. paths with both input transitions 01/10 will be generated for every output transition). Provide the sequential block (ff/ff_bank/latch/latch_bank) information in the input technology library or verify the generated pintypes and polarities.

TECHLIB-9030

NAME

TECHLIB-9030

SUMMARY

Could not find pin direction for pin '%s' in cell '%s' .

DESCRIPTION

\n\nDirection attribute absent in pin/busPin/bundlePin (<PinName>), cell (<CellName>). Default direction is not assigned.

TECHLIB-9031

NAME

TECHLIB-9031

SUMMARY

'%s' absent in pin/bundle/bus '%s' of cell '%s'.

DESCRIPTION

(<AttributeName>) absent in pin/bundle/bus (<PinBusBundleName>) of cell (<CellName>). The specified attribute <AttributeName> is absent in the indicated pin/bus/bundle <PinBusBundleName> of the cell <CellName>. This attribute is essential for translation. Rectify the library by specifying the missing information.

TECHLIB-9032

NAME

TECHLIB-9032

SUMMARY

Definition of type group for bus_type '%s' is absent for cell '%s' in library. Library reading will be aborted.

DESCRIPTION

This message is issued when the type group definition is missing at library level for specified bus_type. Library reading will be aborted. To fix the issue, re-characterize the library with

appropriate settings, such that the type is defined for bus_type.

TECHLIB-9034

NAME

TECHLIB-9034

SUMMARY

Conflicting value for direction found in pin '%s' of bundle/bus '%s' in cell '%s'.

DESCRIPTION

This message is issued when the direction of a pin is not matched with the direction specified in its parent bus/bundle. To fix the issue, re-characterize the library with appropriate settings, such that the correct direction is defined.

TECHLIB-9035

NAME

TECHLIB-9035

SUMMARY

Scaling_factors group '%s' referred in cell '%s', is either empty or not defined in the Library.

DESCRIPTION

The scaling factors group <scaling_factors group name> is either empty or not defined in the Library. Define the scaling factors group at library level OR do not refer to it in the cell group.

TECHLIB-9036

NAME

TECHLIB-9036

SUMMARY

The default_wire_load_selection_group '%s' not found in the library.

DESCRIPTION

The default_wire_load_selection(<Group Name>) not found in the library. \n\nVerify that the indicated default_wire_load_selection group has previously been defined using wire_load_selection group.

TECHLIB-9037

NAME

TECHLIB-9037

SUMMARY

Could not translate default wireload '%s' construct. The model has been referred in the library but not defined

DESCRIPTION

Could not translate wireload <WireloadModelName> construct. The model has been referred in the library but no defined. \n\nChange the default wireload name to some defined wireload in the library or define a new wireload for the the indicated name of wireload.

TECHLIB-9038

NAME

TECHLIB-9038

SUMMARY

The default_wire_load_selection_group not found in the library.

DESCRIPTION

The default_wire_load_selection construct not found in the library. \n\nInput library has more than one wire_load_selection groups specified. Therefore, it is must to specify one default_wire_load_selection.

TECHLIB-9039

NAME

TECHLIB-9039

SUMMARY

Missing timing check between constrained pin'%s' and related pin '%s' in cell '%s'. Ignoring timing check corresponding to this arc.

DESCRIPTION

Either of intrinsic_rise/rise_constraint or intrinsic_fall/fall_constraint is missing for the specified timing arc in the library. \n\n Ignoring timing check corresponding to the missing timing arc.

TECHLIB-9040

NAME

TECHLIB-9040

SUMMARY

Improper definition of related pin '%s'.

DESCRIPTION

To resolve the problem, check the definition of related pin.

TECHLIB-9041

NAME

TECHLIB-9041

SUMMARY

Unspecified/zero capacitance value for input/inout pin/bus/bundle in cell(s) '%s'. This may cause potential problems with delay calculation results

DESCRIPTION

Unspecified/zero capacitance value for input/inout pin/bus/bundle in cell(s) (<CellName>). This may cause potential problems with delay calculation results\n\nOne or more input/inout pin/bus/bundle in the indicated cell(s) <CellName> have unspecified or zero capacitance value (considering the default input/inout capacitance values also). As per delay calculation tools' requirement, the input/inout capacitance value should be non-zero. Check the input technology library and provide appropriate capacitance value.

TECHLIB-9042

NAME

TECHLIB-9042

SUMMARY

Both rise/fall_propagation and cell_rise/fall encountered.

DESCRIPTION

Both rise/fall_propagation and cell_rise/fall encountered. The input technology library has both rise/fall_propagation and cell_rise/fall tables. This effectively means that two sets of characterization points are used in the library. This is not supported in TLF. A workaround is to replace rise/fall_propagation with cell_rise/fall (or vice-versa) depending on whether cell_rise/fall or rise/fall_propagation derating factors are used. Check that the rise/fall_transitions are zero in such cases. If not, then the above-mentioned workaround can not be used.

TECHLIB-9044

NAME

TECHLIB-9044

SUMMARY

Multiple references of wire_load group '%s' encountered in wire_load_selection group(s)

DESCRIPTION

Multiple references of wire_load group (<WireLoadName>) encountered in wire_load_selection group(s)\n\nThe indicated wire_load group name <wireLoadName> appears multiple times either in the same wire_load_selection group or in different wire_load_selection groups. A wire_load_group name should appear only once in any wire_load_selection group.

TECHLIB-9045

NAME

TECHLIB-9045

SUMMARY

Single axis point encountered for %s axis in table '%s'. Ignoring axis else TLFC may not compile this library successfully

DESCRIPTION

Single axis point encountered for (<AxisName>) in table (<TableName>). Ignoring axis else TLFC may not compile this library successfully\n\nThe indicated axis <AxisName> of the two-dimensional table <TableName> in the input technology library has only one coordinate point. Hence the values in the table are independent of this axis. Therefore, one-dimensional table in TLF file corresponding to this input technology library table is generated. This does not result in any loss of data.

TECHLIB-9048

NAME

TECHLIB-9048

SUMMARY

Inconsistency in the expression '%s' in cell '%s'; %s.

DESCRIPTION

Inconsistency in the expression '<Expr>' in cell (<CellName>); Extra parenthesis. There is a mismatch in parenthesis in the expression <Expr> in cell <CellName>. Correct the expression.

TECHLIB-9053

NAME

TECHLIB-9053

SUMMARY

Three-state expression for pin '%s' in cell '%s' is missing or does not contain '%s', whereas, tri-state paths exist from '%s' to '%s'.

DESCRIPTION

Three-state expression for pin (<outputPin>) in cell (<cellName>) is missing or does not contain (<relatedPin>), whereas, tri-state paths exist from (<relatedPin>) to (<outputPin>).\n\nThe 'three_state' attribute for pin <outputPin> in cell <cellName> is either missing or does not contain pin <relatedPin> in the three-state expression. But the timing group(s) inside pin <outputPin> with <relatedPin> as input pin have timing_type as 'three_state_disable'. Hence tri-state paths generated in such cases are (Z->0, Z->1, 1->Z and 0->Z transitions at output). But the active level of the control pin <relatedPin> is not determined as the three-state expression does not contain this pin. So the paths are generated for both the rise and fall transitions at control pin and it's pintype is specified without active level. Verify whether the <relatedPin> is a Control High or Control Low pin.

TECHLIB-9056

NAME

TECHLIB-9056

SUMMARY

'%s' not found in the library. Assuming '%s'

DESCRIPTION

This message is issued when the attribute leakage_power_unit is not defined in the library. It defaults to 1nW. To fix the issue, re-characterize the library with appropriate settings, such that the leakage_power_unit is defined.

TECHLIB-9057

NAME

TECHLIB-9057

SUMMARY

'%s' unit not found in the library. Assuming '%s'

DESCRIPTION

Unit is found missing in the library. Verify the data values in the output.

TECHLIB-9058

NAME

TECHLIB-9058

SUMMARY

Incorrect '%s' unit specified in the library. Assuming '%s'

DESCRIPTION

This message is issued when incorrect unit is specified in the library. To fix the issue, re-characterize the library with appropriate settings, such that the correct unit is specified.

TECHLIB-9059

NAME

TECHLIB-9059

SUMMARY

Both force_00 and force_11 found in state group. Only force_00 will be used and force_11 will be ignored

DESCRIPTION

It is message in string format. No description is available.

TECHLIB-9060

NAME

TECHLIB-9060

SUMMARY

Two dimensional table referred in timing group containing related_output_pin

DESCRIPTION

Two dimensional table referred in timing group containing related_output_pin.

TECHLIB-9061

NAME

TECHLIB-9061

SUMMARY

Could not translate the expression for the function string '%s'.

DESCRIPTION

Could not translate the expression correctly. Verify the output. One of the resons for this, could be the presence of interface_timing set to true at cell level, which leads to sequential elements being ignored.

TECHLIB-9062

NAME

TECHLIB-9062

SUMMARY

Functionality is missing at pin '%s' for the cell '%s'.

DESCRIPTION

Function is missing for the cell

TECHLIB-9063

NAME

TECHLIB-9063

SUMMARY

Invalid delay model specified for the library '%s'. Delay model other than table_lookup/cmos2/generic_cmos is not supported.

DESCRIPTION

This message is issued when invalid delay model is specified. To fix the issue, re-characterize the library with appropriate settings, such that the correct delay model is specified.

TECHLIB-9064

NAME

TECHLIB-9064

SUMMARY

Missing delay_model statement in the library '%s'. %s delay model is assumed.

DESCRIPTION

The delay_model statement is missing in the library. Assuming default model

TECHLIB-9065

NAME

TECHLIB-9065

SUMMARY

Invalid polarity/input transition

DESCRIPTION

Invalid polarity/input transition. Verify the output.

TECHLIB-9066

NAME

TECHLIB-9066

SUMMARY

Invalid values in leakage_power group for the cell '%s'

DESCRIPTION

Either the values attribute of leakage_power group in cell <CellName> is not specified or specified incorrectly. verify the output.

TECHLIB-9067

NAME

TECHLIB-9067

SUMMARY

Missing %s delay value for the path from pin %s to pin %s in the cell %s. Path is not generated. The data in the timing library is incomplete. This can result in a loss of accuracy during delay calculation.

DESCRIPTION

This message is issued when delay and retain values are not specified for the path. Path is not generated if either delay or slew value is missing. To fix the issue, re-characterize the libraries such that delay and retain values are specified correctly.

TECHLIB-9068

NAME

TECHLIB-9068

SUMMARY

Missing %s slew value for the path from pin %s to pin %s in the cell %s. %s. The data in the timing library is incomplete. This can result in a loss of accuracy during delay calculation.

DESCRIPTION

This warning is encountered if the delay tables (cell_rise/cell_fall) are specified between a pin pair in the cells and output slew(rise_transition/fall_transition) tables are missing.\n\nIt is imperative to have both the delay and slew tables to accurately model the slew propagation and hence delay for the cell driven by the cell in question. If the output slew table is missing, the output slew is set to 0

for this cell which would definitely cause wrong delay calculation for the cell driven by the cell in question.\n\nTo avoid this warning make sure that the timing libraries have complete delay and slew data.

TECHLIB-9069

NAME

TECHLIB-9069

SUMMARY

Missing disable timing arc for the path from related pin(s) '%s' to source pin(s) '%s' in the cell '%s'.

DESCRIPTION

Disable arc path are not specified for the given path. Verify the output.

TECHLIB-9070

NAME

TECHLIB-9070

SUMMARY

Missing '%s' parameter in operating condition block '%s' in the library. Assuming zero value for the missing parameter.

DESCRIPTION

Process/voltage/temperature is not specified within operating_conditions group. Zero value for the missing parameters are assumed.

TECHLIB-9071

NAME

TECHLIB-9071

SUMMARY

Missing parameter '%s' in voltage block '%s' in the library. Assuming zero value for the missing parameter.

DESCRIPTION

Some of the parameters are not specified within %_voltage group. Zero value for the missing parameters are assumed.

TECHLIB-9072

NAME

TECHLIB-9072

SUMMARY

Missing '%s' parameter in routing_track block '%s' . Assuming zero value for the missing parameter.

DESCRIPTION

The attribute tracks/total_track_area is not specified within routing_track group. Zero value for the missing parameters are assumed.

TECHLIB-9073

NAME

TECHLIB-9073

SUMMARY

The number of member pins in the bundles '%s' and '%s' is not the same.

DESCRIPTION

The number of member pins in the bundles (<ReferencedBundleName>) and (<OriginalBundleName>) is not the same. Since one of the bundles is defined as a function to the other, the number of member pins in both should be the same.

TECHLIB-9074

NAME

TECHLIB-9074

SUMMARY

Voltage Group '%s' definition not found in library.

DESCRIPTION

This message is issued when the undefined voltage group is used in the library. To fix the issue, re-characterize the library with appropriate settings, such that the voltage group is defined.

TECHLIB-9081

NAME

TECHLIB-9081

SUMMARY

Attribute '%s' found in Library/Cell/Pin '%s' is not supported and would not be translated

DESCRIPTION

The specified attribute has no correspondence in TLF and hence will not be translated

TECHLIB-9082

NAME

TECHLIB-9082

SUMMARY

Define attribute '%s' clashes with a TLF reserved keyword of the same name and would not be translated

DESCRIPTION

The specified define attribute clashes with a TLF reserved keyword of the same name and hence is not being translated. An alternative would be to change the name of the define attribute, so that it does not clash with any of the TLF keywords.

TECHLIB-9084

NAME

TECHLIB-9084

SUMMARY

Missing one of rise/fall capacitance in input/inout pin of cell '%s' and would be ignored.

DESCRIPTION

Missing one of rise/fall capacitance in input/inout pin of cell (<CellName>) and would be ignored. \n\nRise capacitance and Fall capacitance must be specified together at cell or pin level. If for a pin rise_capacitance attribute is set, then fall_capacitance must be set for the same and vice versa.

TECHLIB-9085

NAME

TECHLIB-9085

SUMMARY

Scaled cell's enclosing cell handle '%s' not specified in the library, hence, would not be translated

DESCRIPTION

Scaled cell's enclosing cell handle <CellName> not specified in the library, hence, would not be translated. \n\nLibrary does not have a normal cell defintion with name <cellName> for the scaled cell with the same name. Specify a normal cell with name <CellName> to rectify the problem.

TECHLIB-9086

NAME

TECHLIB-9086

SUMMARY

Scaled cell's operating conditions '%s' not specified in the library, hence, would not be translated

DESCRIPTION

Scaled cell's operating condtions <Operating Condition Name> not specified in the library, hence, would not be translated. \n\nEvery scaled cell is associated with an operating condition and library must have the definition for the operating condition with which the scaled cell is associted. Specify the operating condition with name <Operating Condition Name> in the library to rectify the problem.

TECHLIB-9087

NAME

TECHLIB-9087

SUMMARY

Driver type inside pin '%s' of cell '%s' are not specified with the correct pin/bus/bundle type, hence, would be ignored

DESCRIPTION

Driver type inside pin <PinName> of cell <CellName> are not specified with the correct pin/bus/bundle type, hence, would be ignored. \n\nDriver types must be specified with the correct pin/bus/bundle direction. Every driver type has applicable pin/bus/bundle types with which they can be associted. Specfy the correct pin/bus/bundle type to rectify the problem. resistive, resistive_0, resistive_1, open_source and open_drain driver_type can be specifed with output pin/bus/bundle

only. bus_hold can only be specified with inout pin/bus/bundle and pull_up, pull_down can be specfied with input/output/inout pin/bus/bundle.

TECHLIB-9088

NAME

TECHLIB-9088

SUMMARY

Incompletely/Incorrectly specified data (divided_by/multiplied_by/edges/shifts) in generated clock '%s' in cell '%s', hence would not be translated.

DESCRIPTION

Incompletely/Incorrectly specidied data (divided_by/multiplied_by/edges/shifts) in generated clock <GeneratedClockName> in cell <CellName>, hence would not be translated. \n\nGenerated clock definition in .lib must contain one of the construct among divided_by, muliplied_by and edges/shifts combination. One of these is required for translation of generated clock. Specify divided_by/multiplied_by for clock generation through frequency division/multiplication. Edges must be specified along with shifts but not vice versa. Either edges or an edge shift combination is expected, in case of clocks generated through edge derivation. Edges/Shifts must be specified as triplet.

TECHLIB-9089

NAME

TECHLIB-9089

SUMMARY

Missing generated pin name in generated clock '%s' specification in cell '%s', hence would not be translated.

DESCRIPTION

Missing clock pin in generated clock <GeneratedClockName> specification in cell <CellName>, hence would not be translated. \n\nCheck the definition of generated clock <GeneratedClockName> and specify the clock pin.

TECHLIB-9090

NAME

TECHLIB-9090

SUMMARY

More than one clock generation construct specified in generated clock '%s' specification in cell '%s', hence would not be translated.

DESCRIPTION

More than one clock generation construct specified in generated clock <GeneratedClockName> specification in cell <CellName>, hence would not be translated. \n\nGenerated clock <GeneratedClockName> is specified with more than one method of clock generation (divided_by/multiplied_by/edges or edge/shift combination). A combination of clock generation methods results in ambiguity as tool cannot decide which method to be chosen out of these to translate the generated clock appropriately. Specify a single clock generation construct to allow its translation.

TECHLIB-9091

NAME

TECHLIB-9091

SUMMARY

Incorrect pulling_resistance_unit value specified in the library, hence ignoring

DESCRIPTION

Incorrect pulling_resistance_unit value specified in the library, hence ignoring. \n\npulling_resistance_unit can be only specified with following mentioned values (1ohm, 10ohm, 100ohm, 1kohm). Specify one of these to rectify the library.

TECHLIB-9092

NAME

TECHLIB-9092

SUMMARY

Invalid timing type specified in the arc from clear/preset pin '%s' to pin '%s', ignoring arc .

DESCRIPTION

The specified timing_type attribute is invalid between the source pin and related_pin.\n\nIt is most likely that you have specified a combinational timing arc from the clear/preset pin to the output pin.

TECHLIB-9093

NAME

TECHLIB-9093

SUMMARY

Incorrect timing_type specified in timing group of pin '%s' with related pin name '%s' in cell '%s', ignoring arc.

DESCRIPTION

This message is issued when the incorrect timing_type is specified. Such timing arc will be ignored.

Arcs from clock_gate_clock_pin and clock_gate_enable_pin to clock_gate_out_pin should be of combinational timing_type. To fix the issue, re-characterize the library with appropriate settings, such that the correct timing_type is defined.

TECHLIB-9095

NAME

TECHLIB-9095

SUMMARY

Negative Pulling Resistance specified for pin '%s' in cell '%s', setting the value to 0.

DESCRIPTION

Negative Pulling Resistance specified for pin (<PinName>) in cell (<CellName>), setting the value to 0. \n\nPulling resistance is used to specify the resistance of a pull_up or pull_down device. A negative pulling resistance would produce a current flow in opposite direction, hence a value 0 is set. Specify a positive value to define pulling resistance.

TECHLIB-9096

NAME

TECHLIB-9096

SUMMARY

Pulling resistance specified for a non pull_up/pull_down pin '%s' in cell '%s'.

DESCRIPTION

Pulling resistance specified for a non pull_up/pull_down pin (<PinName>) in cell (<CellName>). \n\nPulling resistance can only be specified for pull_up/pull_down devices. Specify the device as

pull_up/pull_down by using driver_type attribute to rectify the problem.

TECHLIB-9097

NAME

TECHLIB-9097

SUMMARY

No pulling resistance unit specified for pulling resistance of pull_up/pull_down devices in cell '%s'.

DESCRIPTION

This message is issued when the pulling resistance is specified without unit. Valid unit values are 1ohm, 10ohm, 100ohm, and 1kohm. To fix the issue, re-characterize the library with appropriate settings, such that the unit of pulling resistance is defined.

TECHLIB-9098

NAME

TECHLIB-9098

SUMMARY

Cell '%s' is redefined but cannot be overwritten.

DESCRIPTION

Cell (<CellName>) is redefined but cannot be overwritten. Cell redefinitions in a library are not allowed. To resolve the issue, modify the cell definition by changing name of cells such that all the cells are distinct.

TECHLIB-9099

NAME

TECHLIB-9099

SUMMARY

Scaled cell '%s' is redefined but cannot be overwritten.

DESCRIPTION

Scaled cell (<CellName>) is redefined but cannot be overwritten. Scaled cell redefinitions in a library are not allowed. To resolve the issue, modify the scaled cell definition by changing the PVT condition name such that all the scaled cells are distinct in that cell.

TECHLIB-9100

NAME

TECHLIB-9100

SUMMARY

The data pin and enable pin in Tlatch construct are same for pin '%s' in cell '%s'.This will be ignored

DESCRIPTION

This is ignored

TECHLIB-9101

NAME

TECHLIB-9101

SUMMARY

The Tlatch construct is not effective.timing_model_type attribute needs to be defined in cell '%s'.This Tlatch contruct will be ignored

DESCRIPTION

This is ignored

TECHLIB-9102

NAME

TECHLIB-9102

SUMMARY

Incorrectly specified slew measurement points. Reported slews falling beyond the range (0.0 - 100.0).

DESCRIPTION

Incorrectly specified slew measurement points. Reported slews falling beyond the range (0.0 - 100.0). To resolve the issue, check/modify the definitions of the slew measurement thresholds and the slew_derate_from_library construct such that the reported slew range falls in between (0 - 100). To calculate reported slew use, (measured slew upper - measured slew lower) slew derate factor

TECHLIB-9103

NAME

TECHLIB-9103

SUMMARY

The slew_derate_from_library and Input slew measurement points produce reported slews which fall beyond the range (0.0 - 100.0).

DESCRIPTION

This warning is issued if reported slew threshold is computed to be beyond the range (0.0-100.0).\n\nThe slew derate from library is the factor which defines the relationship between the reported and measured slew thresholds for the library. The formula is as follows - \n\n delta reported = delta measured / slew_derate_from_library \n\n 'delta' signifies the difference between 'slew_upper' and 'slew_lower'. \n\nIf delta reported comes out to be greater than hundred with the measure thresholds and slew derate specified, then the reported slews will fall beyond 0-100 range - which is not possible. In such case the above warning is issued. To avoid this warning, make sure proper values of slew_derate_from_library and Input slew measurement points are specified in the timing library.

TECHLIB-9104

NAME

TECHLIB-9104

SUMMARY

Slew derate from library would be assumed to be 1 and the derating would be applied using this value as slew thresholds are specified on the command line and not specified in the library.

DESCRIPTION

Slew derating would not be applied as slew thresholds are specified on the command line and not specified in the library. \n\nTo rectify the issue specify thresholds and slew derating factor (slew_derate_from_library) inside the library.

TECHLIB-9105

NAME

TECHLIB-9105

SUMMARY

Slew_derate_from_library specified as 0 <= x >1 in the library where x is the value of slew_derate.

DESCRIPTION

Slew_derate_from_library specified as 0 <= x >1 in the library where x is the value of slew_derate. To rectify the issue change slew derating factor (slew_derate_from_library) inside the library.

TECHLIB-9106

NAME

TECHLIB-9106

SUMMARY

Tool detected missing threshold parameters in your .lib, and substituted the proper default values. To provide explicit setting of thresholds, update your .lib and retranslate; or, specify the appropriate settings. For accurate results, it is necessary that the slew measurement points used during Spice characterization of the library are provided to the delay calculator. The threshold points are crucial for timing analysis and should be specified correctly.

DESCRIPTION

Tool detected missing threshold parameters in your .lib, and substituted the proper default values. To provide explicit setting of thresholds, update your .lib and retranslate; or, specify the appropriate settings. For accurate results, it is necessary that the slew measurement points used during Spice characterization of the library are provided to the delay calculator. \n\nTo specify the thresholds in input technology library, specify the following constructs in the library.\n1. input_ threshold_pct_fall\n2. input_threshold_pct_rise\n3. output_threshold_pct_fall\n4. output_threshold_pct_rise\n5. slew_lower_threshold_pct_fall\n6. slew_lower_threshold_pct_rise\n7. slew_upper_threshold_pct_fall\n8.slew_upper_threshold_pct_rise \n\nTo specify the same through command line, use the following command line options:\n -ir, -if, -dr, -df, -sr, -sf, -tr, -tf, \n -slew_measure_lower_rise, -slew_measure_lower_fall, \n -slew_measure_upper_rise, -slew_measure_upper_fall

TECHLIB-9107

NAME

TECHLIB-9107

SUMMARY

Thresholds specified both in library and on command line. Command line values will be used.

DESCRIPTION

Thresholds specified both in library and on command line. Command line values will be used. \n\nTo avoid the warning, specify the thresholds either on command line or in the library.

TECHLIB-9108

NAME

TECHLIB-9108

SUMMARY

'%s' not specified in the library, using .lib default of '%s'.

DESCRIPTION

This warning is encountered if the construct (<ThresholdConstruct>) is missing from the library. This construct in the timing library defines how the delay of the characterized cells has been deduced. For example a input_threshold_pct_rise of 30 and output_threshold_pct_rise of 60 means that the delay value in the tables are the time difference between the input rising to 30% of its values and output rising to 70% of its value. If this is missing, then a value of (<PercentageValue>) is assumed. \n\n To avoid this warning make sure that the timing libraries have the correct values of (<ThresholdConstruct>) specified.

TECHLIB-9109

NAME

TECHLIB-9109

SUMMARY

slew_derate_from_library not specified in the library, using .lib default of 1.

DESCRIPTION

The slew_derate_from_library not specifed in the library, using .lib default of 1.\n\nTo clear the warning, specify the slew_derate_from_library value in the library.

TECHLIB-9110

NAME

TECHLIB-9110

SUMMARY

Single data point found in the axis point redefinition of template '%s' in cell '%s'. Axis point is useless and would not be used in table lookup.

DESCRIPTION

Single data point found in the axis point redefinition of template (<TemplateName>) in cell (<CellName>). Axis point is useless and would not be used in table lookup. \n\nTo clear the warning, modify the axis point definition in the library. For lookup, at least two points should be specified.

TECHLIB-9111

NAME

TECHLIB-9111

SUMMARY

Illegal [0-100] delay thresholds specified in the library. Library can be translated by using -force command line option however it is recommended that library should be fixed by providing the correct/legal delay threshold points. Tool when forced to translate the library containing 0-100 delay thresholds, assumes 50-50 delay thresholds (liberty defaults). For accurate results, it is necessary that the delay threshold points used during Spice characterization of the library are provided to the delay calculator.

DESCRIPTION

Illegal [0-100] delay thresholds specified in the library. Library can be translated by using -force command line option however it is recommended that library should be fixed by providing the correct/legal delay threshold points. Tool when forced to translate the library containing 0-100 delay thresholds, assumes 50-50 delay thresholds (liberty defaults). For accurate results, it is necessary that the delay threshold points used during Spice characterization of the library are provided to the delay calculator. \n\nThe threshold points are crucial for timing analysis and should be specified correctly. Otherwise, it may cause potential problems with delay calculation results. A better solution is to modify the library for legal thresholds if possible.

TECHLIB-9112

NAME

TECHLIB-9112

SUMMARY

Illegal [0-100] delay thresholds specified in the library. Library translated by using -force command line option. It may cause potential problems with delay calculation results. It is recommended that library is fixed and translated again.

DESCRIPTION

Illegal [0-100] delay thresholds specified in the library. Library translated by using -force command line option. It may cause potential problems with delay calculation results. It is recommended that library is fixed and translated again. \n\nTool when forced to translate the library containing 0-100 delay thresholds, assumes 50-50 delay thresholds (liberty defaults). For accurate results, it is necessary that the delay threshold points used during Spice characterization of the library are provided to the delay calculator.

TECHLIB-9113

NAME

TECHLIB-9113

SUMMARY

Illegal [0-100] slew measurement thresholds specified in the library. Library can be translated by using -force command line option however it is recommended that library should be fixed by providing the correct/legal slew measurement points. Tool when forced to translate the library containing 0-100 slew measurement thresholds, assumes 20-80 measured slew (liberty defaults). For accurate results, it is necessary that the slew measurement points used during Spice characterization of the library are provided to the delay calculator.

DESCRIPTION

Illegal [0-100] slew measurement thresholds specified in the library. Library can be translated by using -force command line option however it is recommended that library should be fixed by providing the correct/legal slew measurement points. Tool when forced to translate the library containing 0-100 slew measurement thresholds, assumes 20-80 measured slew (liberty defaults). For accurate results, it is necessary that the slew measurement points used during Spice characterization of the library are provided to the delay calculator. \n\nThe threshold points are crucial for timing analysis and should be specified correctly. Otherwise, it may cause potential problems with delay calculation results. A better solution is to modify the library for legal thresholds if possible.

TECHLIB-9114

NAME

TECHLIB-9114

SUMMARY

Illegal [0-100] slew measurement thresholds specified in the library. Library translated by using -force command line option. It may cause potential problems with delay calculation results. It is recommended that library is fixed and translated again.

DESCRIPTION

Illegal [0-100] slew measurement thresholds specified in the library. Library translated by using -force command line option. It may cause potential problems with delay calculation results. It is recommended that library is fixed and translated again. \n\nTool when forced to translate the library containing 0-100 slew measurement thresholds, assumes 20-80 measured slew (liberty defaults). For accurate results, it is necessary that the slew measurement points used during Spice characterization of the library are provided to the delay calculator.

TECHLIB-9115

NAME

TECHLIB-9115

SUMMARY

Could not over write the definition of the Bus %s in the cell %s. There might be a scalar pin of the same name defined earlier.

DESCRIPTION

Could not over write the definition of the Bus <bus_name> in the cell <cell_name>. There might be a scalar pin of the same name defined earlier.\n\nThere might be certain pin names which can conflict with the bus name and range. Remove or rename such pin names.

TECHLIB-9118

NAME

TECHLIB-9118

SUMMARY

The statetable for the %s %s is syntactically incorrect. This may be because of %s.

DESCRIPTION

This message is issued when the statetable is incorrectly defined. This might be due to incorrectly placed commas/colons. To fix the issue, re-characterize the library with appropriate settings, such that the statetable is correctly defined.

TECHLIB-9119

NAME

TECHLIB-9119

SUMMARY

Missing related pin %s for a timing group of pin %s in cell %s.

DESCRIPTION

This message is issued when the related_pin is specified for a timing group but is not defined in the cell. To fix the issue, re-characterize the library with appropriate settings, such that the related_pin is defined.

TECHLIB-9120

NAME

TECHLIB-9120

SUMMARY

Duplicate definition found for pin/bus/bundle %s in cell %s. Overwriting the duplicate definition.

DESCRIPTION

Duplicate definition found for <RelatedPin> in cell <Cell>. Overwriting the duplicate definition.\n\nCheck for possible errors. It is recommended that such redifinition is examined before loading the .lib as this could result in loss of information.

TECHLIB-9121

NAME

TECHLIB-9121

SUMMARY

Mismatch in bit_from/bit_to values while overwriting the bus_type for bus %s in cell %s.

DESCRIPTION

This message is issued when there is mismatch in the attributes bit_from/bit_to values while overwriting the bus_type for bus. To fix the issue, re-characterize the library with appropriate settings, such that the attributes bit_from/bit_to are defined correctly.

TECHLIB-9122

NAME

TECHLIB-9122

SUMMARY

Multiple statetables found in cell %s. Only the last statetable definition will be preserved.

DESCRIPTION

Multiple statetables found in cell <Cell>. Only the last statetable definition will be preserved. A cell having multiple statetables is considered to be an incorrect style of modelling. Thus only the latest statetable definition is preserved.

TECHLIB-9123

NAME

TECHLIB-9123

SUMMARY

Slew threshold difference '%s' is less than 1%.

DESCRIPTION

Slew threshold difference (<Rise>/<Fall>) is less than 1%.\n\nThis library might not be usable with some of the downstream tools.

TECHLIB-9124

NAME

TECHLIB-9124

SUMMARY

Missing when or sdf_cond attributes in the min_pulse_width group of pin '%s' in cell '%s'.

DESCRIPTION

Missing when or sdf_cond attributes in the min_pulse_width group of pin <Pin> in cell <Cell>.\n\nAttributes when and sdf_cond define the enabling condition for the timing check. Both attributes are required in the min_pulse_width group.

TECHLIB-9125

NAME

TECHLIB-9125

SUMMARY

Missing axis name in template definition '%s'.

DESCRIPTION

Missing axis name in template definition <Template name>. Number of template variables in a template should correspond with the number of Index statements.

TECHLIB-9127

NAME

TECHLIB-9127

SUMMARY

Multiple '%s' were detected at (Line %d). Using the last value.

DESCRIPTION

The last value of the multiple definitions would be used.

TECHLIB-9128

NAME

TECHLIB-9128

SUMMARY

Lookup tables are only supported in 'table_lookup' libraries. Table seen at line %d. Verify that the delay_model for this library is table_lookup.

DESCRIPTION

Table can be seen when delay model type is defined as table_lookup. The library needs to be reviewed.

TECHLIB-9129

NAME

TECHLIB-9129

SUMMARY

Missing third axis name in template definiton '%s', assuming 'related_out_total_output_net_capacitance/equal_or_opposite_output_net_capacitance'.

DESCRIPTION

Missing third axis name in template definiton <Template Name>, assuming 'related_out_total_output_net_capacitance/equal_or_opposite_output_net_capacitance'.\n\nThird axis name is not specified in the 3D template definition, assuming it to be 'related_out_total_output_net_capacitance/equal_or_opposite_output_net_capacitance' for timing/power template respectively. To supress this behavior specify the name of the third axis in the template definition.

TECHLIB-9131

NAME

TECHLIB-9131

SUMMARY

Unnamed '%s' found in input technology library. This is incorrect liberty Syntax.

DESCRIPTION

The library does not have pin/cell/library name defined in the library. The input technology library should have pin/cell/library name defined. Check the library correctness.

TECHLIB-9132

NAME

TECHLIB-9132

SUMMARY

Identified more than one leakage_power groups with same condition in cell '%s', Last definition will be retained.

DESCRIPTION

More than one leakage_power groups with same condition identified in cell <CellName>. The last definition will be retained

TECHLIB-9133

NAME

TECHLIB-9133

SUMMARY

Identified more than 1 power_gating_pin/retention_pin attributes for pin %s (Line %d). First definition would be retained.

DESCRIPTION

Found multiple power_gating_pin/retention_pin constructs for same pin. Specify only one power_gating_pin/retention_pin construct for a pin in the library cell.

TECHLIB-9134

NAME

TECHLIB-9134

SUMMARY

Multiple unit definitions detected (Line %d). A library can only have one definition for capacitive_load_units. First definition would be retained.

DESCRIPTION

The first value of the multiple unit definitions would be used.

TECHLIB-9135

NAME

TECHLIB-9135

SUMMARY

%s (Line %d) has both attributes 'power_level' & 'related_pg_pin' defined. power_level would be ignored.

DESCRIPTION

The power group should be reviewed for correctness.

TECHLIB-9136

NAME

TECHLIB-9136

SUMMARY

Single axis point encountered for %s axis in table '%s'.

DESCRIPTION

Single axis point encountered for (<AxisName>) in table (<TableName>). Ignoring axis else TLFC may not compile this library successfully\n\nThe indicated axis <AxisName> of the two-dimensional table <TableName> in the input technology library has only one coordinate point. Hence the values in the table are independent of this axis. Therefore, one-dimensional table in TLF file corresponding to this input technology library table is generated. This does not result in any loss of data.

TECHLIB-9137

NAME

TECHLIB-9137

SUMMARY

Mismatch in bus width in timing arc with related pin '%s' in pin '%s' of cell '%s'. Ignoring the timing arc.

DESCRIPTION

The bus width of path between source bus pin and target bus pin should match otherwise that timing arc would be ignored.

TECHLIB-9138

NAME

TECHLIB-9138

SUMMARY

The 'default_operation_condition' should be defined after the 'operation_condition' group. Check the library for correctness.

DESCRIPTION

The attribute 'default_operation_condition' should be defined in the library after the operation_condition' group. This is done to ensure the validity of the properties signified by these attributes.

TECHLIB-9139

NAME

TECHLIB-9139

SUMMARY

'%s' not found in the library. Assuming '%s'

DESCRIPTION

The attribute leakage_power_unit is found missing in the library. Assuming it to be 1nW.\n\nTo avoid this assumption, specify (leakage_power_unit) in the library.

TECHLIB-9140

NAME

TECHLIB-9140

SUMMARY

No timing sense found for the timing arc at (line no : %d) for cell %s. This is a required attribute for delay timing arcs.

DESCRIPTION

Timing Sense is a required attribute for delay arcs. If missing can cause issues during timing analysis.

TECHLIB-9141

NAME

TECHLIB-9141

SUMMARY

Identified delay/slew table(s) for timing arc at (line no :%d) with timing type '%s' for cell '%s'. This timing group is check arc and cannot have delay/slew tables.

DESCRIPTION

The cell_rise, cell_fall, rise_transition. fall_transition table are not expected in min_pulse_width arc. These arcs can have only rise_constraint or fall_constraint tables.

TECHLIB-9142

NAME

TECHLIB-9142

SUMMARY

Mismatch between number of values(%d) defined in template '%s' and number of values(%d) characterized in table, on line no. %d.

DESCRIPTION

If any library template has n*m entries, then its corresponding table entries values should be n*m.

TECHLIB-9143

NAME

TECHLIB-9143

SUMMARY

Timing group defined in library has either missing or incorrectly defined lookup tables(s) for cell '%s'. This timing group will be ignored.

DESCRIPTION

Timing groups in library without any delay, transition, or constraint tables are not allowed. The timing group without any indices on lookup table or its referred template is not allowed. All such timing groups in the library will be ignored. To resolve the issue, modify the timing arc definition by adding cell_rise rise_transition/rise_constraint table or cell_fall/fall_transition/fall_constraint table.

TECHLIB-9144

NAME

TECHLIB-9144

SUMMARY

The statetable for the %s %s is syntactically incorrect. This may be because the number of %s columns (%d) is %s than %d

DESCRIPTION

This message is issued when there is a mismatch in number of entries in statetable and number of entries in the table header for next state/current state/inputs. To fix the issue, re-characterize the library with appropriate settings, such that the statetable is defined correctly.

TECHLIB-9145

NAME

TECHLIB-9145

SUMMARY

Cell '%s' has interface_timing attribute set to true and it also has statetable defined. The statetable will be ignored.

DESCRIPTION

The library cell does not require to have a statetable defined if the cell definition has interface_timing attribute set to true. In the case both interface_timing attribute and statetable are defined for a cell, the state table will be ignored and interface_timing attribute would be honored. In this case, to enable tool honor the statetable, either set the interface_timing attribute to false in the cell definition or remove the attribute from cell definition

TECHLIB-9147

NAME

TECHLIB-9147

SUMMARY

The 'default_operating_condition' '%s' is not defined in the library. This will be ignored and nominal operating condition will be used for analysis. To avoid this error, you need to add the missing operating condition definition in the library and then re-run.

DESCRIPTION

This error is issued when the default_operating_condition definition is missing in the library. In such cases, the nominal operating condition is used to proceed with the analysis. However, this might

lead to unexpected analysis results and may impact signoff quality. To rectify the error, either re-characterize the library or add the definition of the missing operating condition in the library.

TECHLIB-9148

NAME

TECHLIB-9148

SUMMARY

The pin class value for power_gating_pin attribute at line no '%d' for pin '%s' is not recognized type. It will be ignored.

DESCRIPTION

The valid pin class values for power_gating_pin attribute are power_pin_[1-5]. The values other than this will be ignored. To resolve this issue, modify the power pin class values with valid values in the library.

TECHLIB-9149

NAME

TECHLIB-9149

SUMMARY

For cell '%s', the bundle group '%s' (on line %d) does not have the mandatory attribute '%s' present.

DESCRIPTION

This message is issued when mandatory attribute in library is missing. The attribute mentioned is an essential attribute for a bundle group. The library loading cannot proceed without this. To fix the issue, re-characterize the library with appropriate settings, such that all mandatory attributes are

defined in the library.

TECHLIB-9150

NAME

TECHLIB-9150

SUMMARY

Could not open file %s for %s

DESCRIPTION

Could not open file <InputFileName> for reading\n\nThe input technology file <InputFileName> either does not exist or is unreadable. Provide the correct file name or change the file permissions.

TECHLIB-9152

NAME

TECHLIB-9152

SUMMARY

Unknown Liberty %s '%s' encountered. Ignoring

DESCRIPTION

Unknown Liberty entity encountered. Ignoring.\n\nSyn2Tlf does not support this construct at present.

TECHLIB-9153

NAME

TECHLIB-9153

SUMMARY

Duplicate definition for attribute '%s' encountered. The last definition will be retained.

DESCRIPTION

Duplicating definition for attribute encountered. The last definition will be retained.

TECHLIB-9154

NAME

TECHLIB-9154

SUMMARY

Unknown value '%s' encountered for Liberty simple attribute '%s'. Ignoring

DESCRIPTION

Unknown value <value> encountered for Liberty simple attribute <name>. Ignoring.\n\nSyn2Tlf does not support the specified value <value> for the simple attribute <name> at present.

TECHLIB-9155

NAME

TECHLIB-9155

SUMMARY

Syntax error/unsupported construct '%s'

DESCRIPTION

(<InputFileName>, <LineNumber>) Syntax error/unsupported construct\n\nSyntax error or unsupported construct has been encountered at the indicated line number <LineNumber> in the input technology file <InputFileName>. Check for the correctness of the syntax at the specified line number. In case of correct syntax, the error could be because Syn2Tlf does not support this construct at present. In that case, contact the Syn2Tlf support team (india_dsm@cadence.com).

TECHLIB-9156

NAME

TECHLIB-9156

SUMMARY

Syntax error: library header is missing or this file may not be a liberty file.

DESCRIPTION

Syntax error: library header is missing. The input tech file does not contain the library header. Correct the library to contain a valid library header.

TECHLIB-9157

NAME

TECHLIB-9157

SUMMARY

Memory allocation failed

DESCRIPTION

Memory allocation failed\n\nThe size of the input technology library is very large and the machine on which Syn2Tlf is being run does not have sufficient swap space for translation. Run Syn2Tlf on a machine with higher swap space.

TECHLIB-9161

NAME

TECHLIB-9161

SUMMARY

Group '%s' is ignored. It is either empty or has attributes which are not relevant for current tool.

DESCRIPTION

This message is issued when the group is defined either without any attributes or has attributes which are not relevant for existing tool being used. For example, group has only power related attributes which are not used in Tempus.

TECHLIB-9162

NAME

TECHLIB-9162

SUMMARY

Illegal comments in a statetable %s of the cell %s

DESCRIPTION

This message is issued when some illegal symbols are found in the statetable definition. These are more likely to be unclosed or runaway nested comments.

TECHLIB-9164

NAME

TECHLIB-9164

SUMMARY

The group name is larger than %d characters. Such large names would cause problems in downstream tools. Rename the group to remove this error.

DESCRIPTION

The group name cannot be larger than the limit specified. The downstream tools might not be able to handle such large names. Rename the group to meet the size limit.

TECHLIB-9166

NAME

TECHLIB-9166

SUMMARY

Multiple library groups are defined in this text file. Only the first library will be parsed. The remaining libraries in the file will be ignored.

DESCRIPTION

Multiple library groups are defined in this text file. Only the first library will be parsed. The remaining libraries in the file will be ignored.

TECHLIB-9167

NAME

TECHLIB-9167

SUMMARY

Found complex attribute in user defined group. As per liberty specification, complex attributes are not allowed in user defined groups. The attribute will be ignored.

DESCRIPTION

Found complex attribute in user defined group. As per liberty specification, complex attributes are not allowed in user defined groups. The attribute will be ignored.

TECHLIB-9168

NAME

TECHLIB-9168

SUMMARY

Unknown value '%s' encountered for Liberty simple attribute '%s'. Ignoring

DESCRIPTION

Unknown value <value> encountered for Liberty simple attribute <name>. Ignoring.\n\nSoftware does not support the specified value <value> for the simple attribute <name> at present.

TECHLIB-9170

NAME

TECHLIB-9170

SUMMARY

Multiple definitions of the fanout length '%d' for the wire_load group. The first definition would be retained

DESCRIPTION

This message is issued when same fanout length is defined more than once with different values in wire_load group. The same fanout length cannot have multiple definition. First definition will be retained and rest will be ignored.

VOLTUS-1186

NAME

VOLTUS-1186

SUMMARY

Option %s is valid only under multi-die model.

DESCRIPTION

Run set_rail_analysis_mode -die_model muti-die to set correct die model.

VOLTUS-5348

NAME

VOLTUS-5348

SUMMARY

Option %s is not valid under multi-die mode.

DESCRIPTION

Use component_mapping_file in "set_advanced_package_options" to set them.

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WHATIF-2

NAME

WHATIF-2

SUMMARY

The option '-outFile' is obsolete and will be removed in the next major release. To specify the prefix of the constraints file and the directory in which the constraints file will be generated, use the '-filePrefix' and the '-dir' options.

DESCRIPTION

This message is generated when using obsolete options. These options can be removed in future and the present flow may not work. Updation in script is required.

WHATIF-3

NAME

WHATIF-3

SUMMARY

The setWhatIfPortPriority command is obsolete and will be removed in the next major release. To set the port priority, use the setWhatIfTimingMode command.

DESCRIPTION

setWhatIfPortPriority is now obsolete and has been replaced by setWhatIfTimingMode -portPriority. The -driveCell and -portParam options are not options passed to setWhatIfTimingMode (-driveCell is now cellType, -portParam is now portParam)

Example:

The command

\t setWhatIfPortPriority -driveCell

Becomes:

\t setWhatIfTimingMode -portPriority cellType

The command

\t setWhatIfPortPriority -portParam

Becomes:

\t setWhatIfTimingMode -portPriority portParam