作业3

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4.1

4.1.1

Regwrite 1

ALusrc 0

ALU operation 10

MemWrite 0

MemRead 0

MemtoReg 0

4.1.2

寄存器堆，ALU，数据选择器

4.1.3

都产生了输出。数据存储单元，立即数生成单元产生的输出不用

4.7

4.7.1

R型：

Register Read->I-Mem/D-Mem->Register File->Mux->ALU->MUX->Register Setup

用时30+250+150+25+200+25+20=700ps

4.7.2

lw：

Register Read->I-Mem/D-Mem->Register File->Mux->ALU->I-Mem/D-Mem->Mux->Register Setup

30+250+150+25+200+250+25+20=950ps

4.7.3

sw:

Register Read->I-Mem/D-Mem->Register File->Mux->ALU->I-Mem/D-Mem

30+250+150+25+200+250=905ps

4.7.4

beq:

Register Read->I-Mem/D-Mem->Register File->Mux->ALU->single gate->Mux->Register Setup

30+250+150+25+200+5+25+20=705ps

4.7.5

I型：

Register Read->I-Mem/D-Mem->Register File->Mux->ALU->Mux->Register Setup

30+250+150+25+200+25+20=700ps

4.7.6

CPU最小时钟周期取决于最长的指令延迟，即最小时钟周期为950ps。

PLA实现图

布尔表达式：

$$ALUSrc = ld + sd = I_0I_1I_2'I_3'I_4'I_5'I_6' + I_0I_1I_2'I_3'I_4'I_5I_6'$$

$$MemtoReg = ld = I_0I_1I_2'I_3'I_4'I_5'I_6'$$

$$RegWrite = R - format + ld = I_0I_1I_2'I_3'I_4I_5I_6' + I_0I_1I_2'I_3'I_4'I_5'I_6'$$

$$MemRead = ld = I_0I_1I_2'I_3'I_4'I_5'I_6'$$

$$MemWrite = sd = I_0I_1I_2'I_3'I_4'I_5I_6'$$

$$Branch = beq = I_0I_1I_2'I_3'I_4'I_5I_6$$

$$ALUOp1 = R - format = I_0I_1I_2'I_3'I_4I_5I_6'$$

$$ALUOp0 = beq = I_0I_1I_2'I_3'I_4'I_5I_6$$

电路图如下：