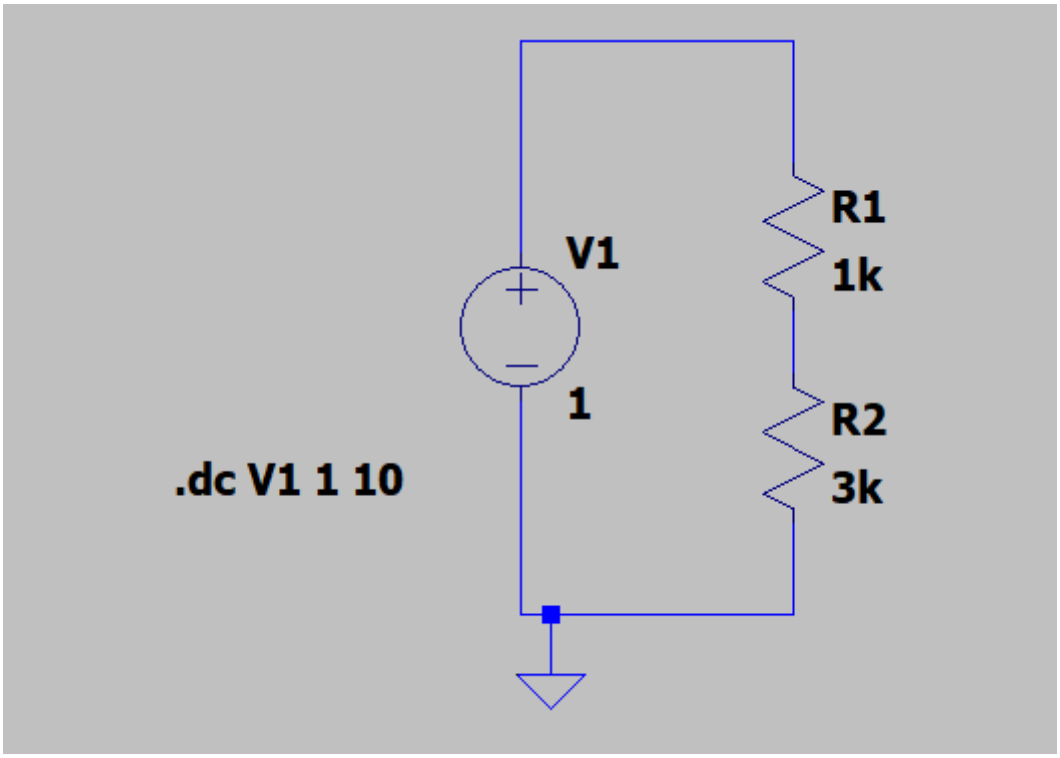
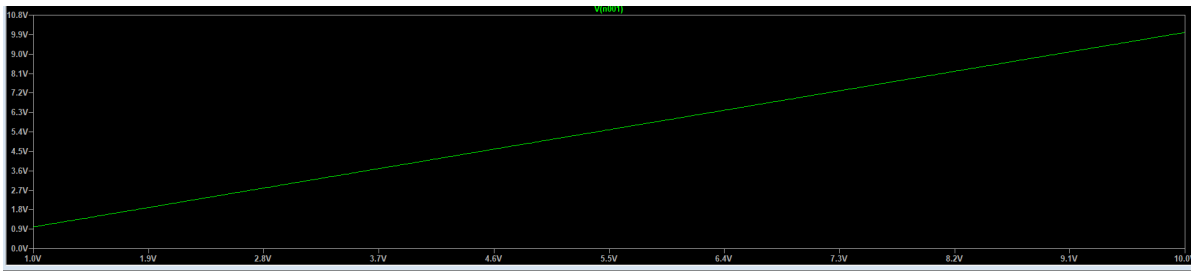
Tutorial

1.The bigger the **threshold voltage** compared as a ratio to the supply voltage, the slower the FET works

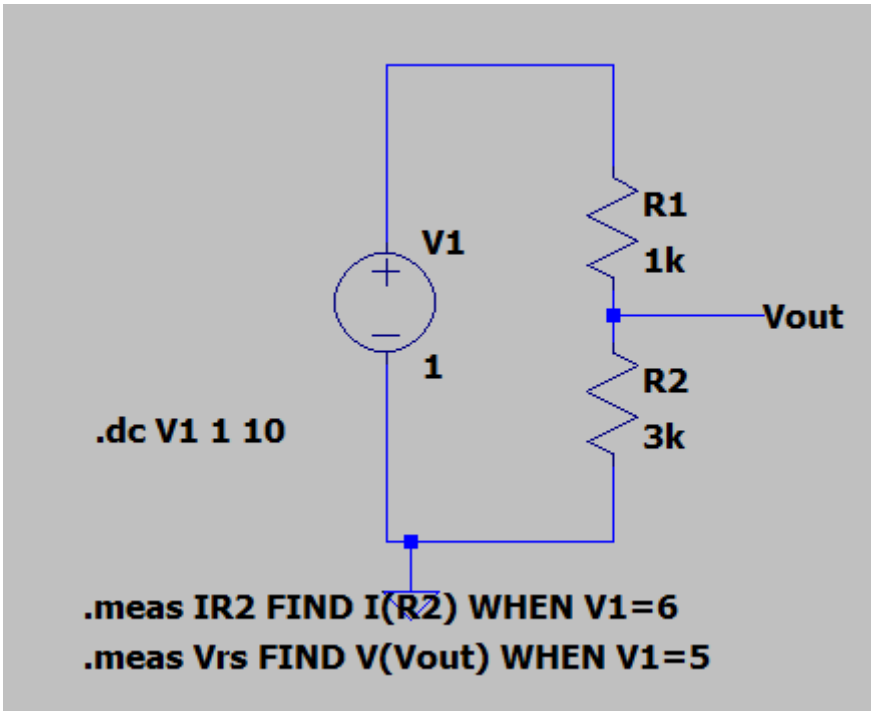
Ltspice command line

.dc: It is used for DC analysis where you can set the voltage from x to y





.meas: measure a certain value of a certain node when input voltage(or any other voltage at a point)

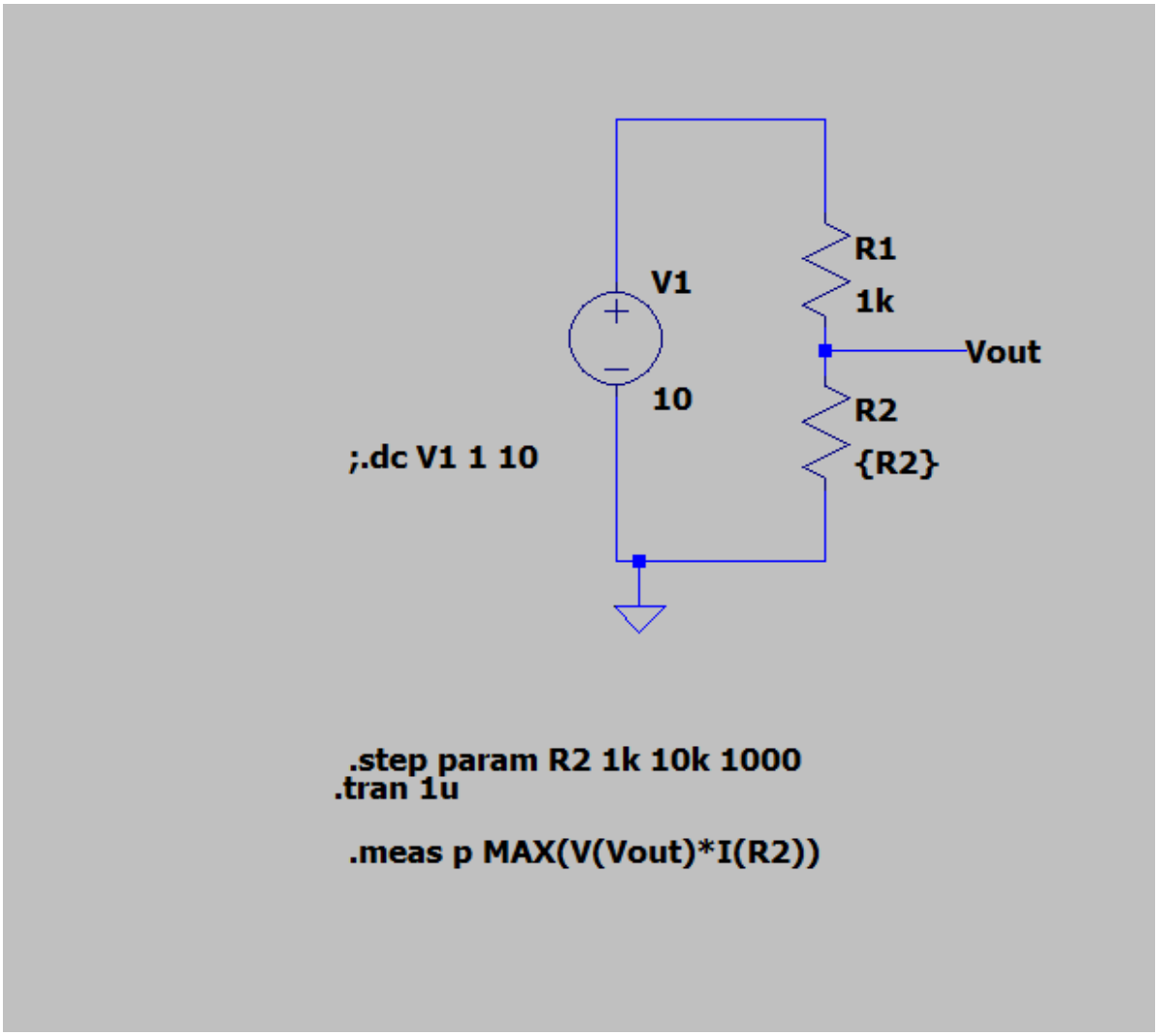


SPICE Error Log: C:\Program Files\LTC\LTspiceXVII\Draft1.log

```
Circuit: * C:\Program Files\LTC\LTspiceXVII\Draft1.asc


ir2: i(r2)=0.0015 at 6
vrs: v(vout)=3.75 at 5


Date: Sat Oct 23 15:12:27 2021
Total elapsed time: 0.034 seconds.

tnom = 27
temp = 27
method = trap
totiter = 2003
traniter = 0
tranpoints = 0
accept = 0
rejected = 0
matrix size = 3
fillins = 0
solver = Normal
Matrix Compiler1: 50 bytes object code size  0.0/0.0/[0.0]
Matrix Compiler2: 175 bytes object code size  0.0/0.0/[0.0]
```

.param: As well as simulating a circuit with variable input voltage, its often useful to know how it will perform if one component or parameter is altered.

As shown in the figure below

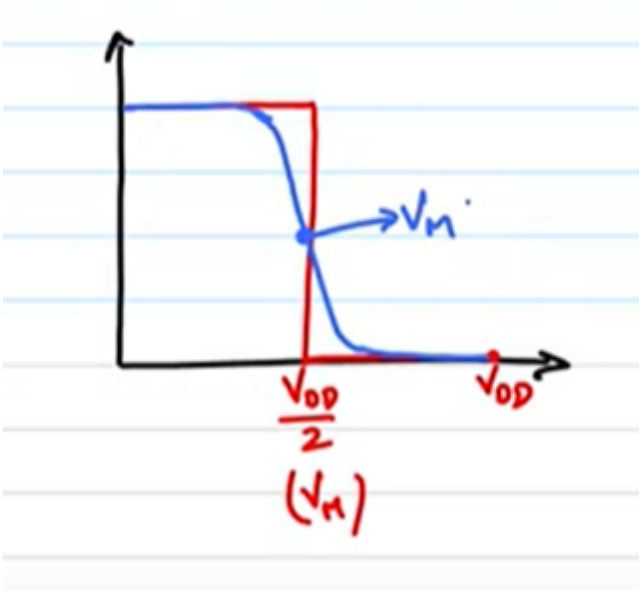


This type of command line will change the value of R2 in the step way then measure the power at different size

In the inverter, in order to make the transistors equivalent to each other,you have to make the p type transistors wider cause the mobility of hole is smaller than the mobility of electron.

Noise margin

Let's look at an ideal inverter characteristic:



Let's assume that when $v_{in} < v_m \rightarrow vin$ is logic 0 $\rightarrow v_o$ is logic high. same for when $v_{in} > v_m$ ....

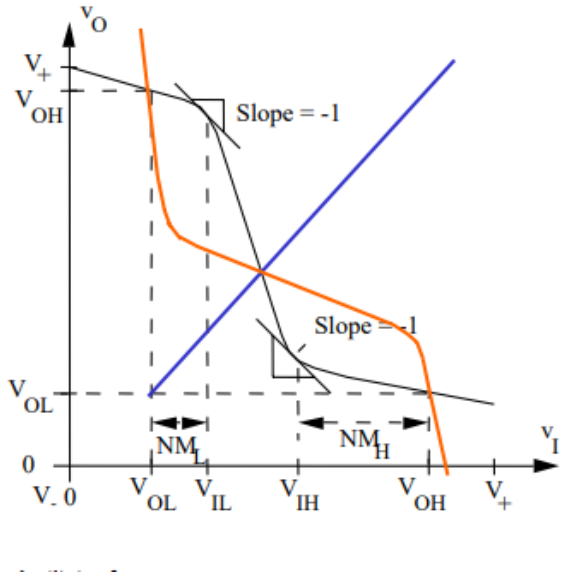
Logic Voltage Levels

V_{OL}: Nominal voltage corresponding to a low logic state at the output of a logic gate for $v_I = V_{OH}$. Generally $V_- \leq V_{OL}$.

V_{OH}: Nominal voltage corresponding to a high logic state at the output of a logic gate for $v_I = V_{OL}$. Generally $V_{OH} \leq V_+$.

V_{IL}: Maximum input voltage that will be recognised as a low input logic level.

V_{IH}: Minimum input voltage that will be recognised as a high input logic level.



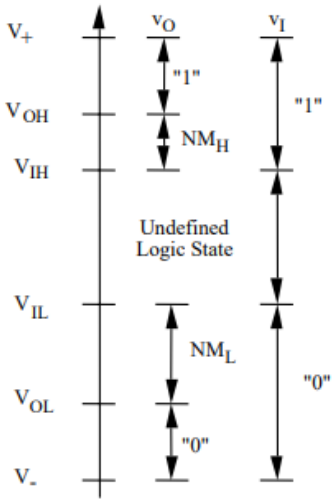
Noise Margins

NM_L: Noise margin associated with a low input level

$NM_L = V_{IL} - V_{OL}$

NM_H: Noise margin associated with a high input level

$NM_H = V_{OH} - V_{IH}$



Dynamic Response of Logic Gates

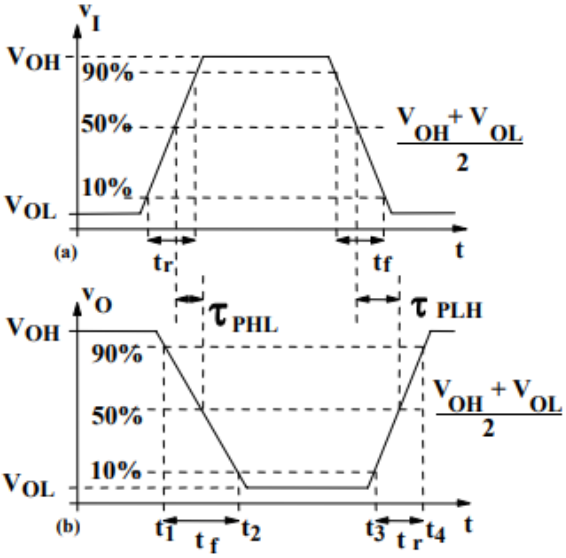
- Rise time t_r: time required for the transition from $V_{10\%}$ to $V_{90\%}$.
- Fall time t_f: time required for the transition from $V_{90\%}$ to $V_{10\%}$.

$$V_{10\%} = V_{OL} + 0.1(V_{OH} - V_{OL})$$
$$V_{90\%} = V_{OL} + 0.9(V_{OH} - V_{OL})$$

- Propagation delay τ_P: difference in time between the input and output signals reaching $V_{50\%}$.

$$V_{50\%} = (V_{OH} + V_{OL})/2$$

$$\tau_P = \frac{\tau_{PLH} + \tau_{PHL}}{2}$$



Switching waveforms for an idealised inverter
(a) Input voltage signal (b) Output voltage waveform

We want the noise margin in inverter as big as possible.