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1

1.1 A

The smallest clock period is 9 ns. That's the t_{PD} of the two inverters, plus t_{PD} for the first D register, plus the t_S of the second register.

1.2 B

The new circuit would not work correctly, because the t_H of the second register would not be met.

1.3 C

S0 = 0, S1 = 0

1.4 D

S0 = 0, S1 = 1

1.5 E

The skew actually helps us - we can now have a clock period of 8 ns.

2

```
module jk
        (input j, k, preset, clear, clk,
         output q, qbar);

        reg state;

        always @(posedge clk or negedge preset or negedge clear) begin
                if (preset && claer) begin  // standard operation
                        case ({j, k})
                                2'b00: state <= state;
                                2'b01: state <= j;
                                2'b10: state <= j;
                                2'b11: state <= ~state;
                                default: state <= state;
                        endcase
                end
                else if (~preset) begin  // set state
                        state <= 1;
                end
                else if (~clear) begin  // clear state
```

```
                    state <= 0;
                end
            end

            assign q = state;
            assign qbar = ~q;

endmodule
```