TSMC 0.18um
DW_TSMC_SCB971 DesignWare®
Library Release Notes

Release 2.3.1, June 12, 2000

SYNOPSYS®

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1. Introduction

This Release Notes accompanies Release 2.3.1 of the DW_TSMC_SCB971 DesignWare® (DW) library, which is a limited production release of the standard cell library for the TSMC 0.18um CL018G process.

This specification includes detailed information on Release 2.3.1, and summary information about previous versions of this library, if available. This document is not intended to replace any existing user guide, but rather to provide specific information on this library release.

Details about this Release 2.3.1 can be found in two files of Bill of Materials in the release library directory.

2. Release 2.3.1 Highlights

This section gives highlights on the patch release 2.3.1 of the DW_TSMC_SCB971 DesignWare@ library. Users of the library should thoroughly review all sections in this Release Notes for more details.

- Contents of this release: standard cells, I/Os, single and dual-port RAMs.
- Enhanced PAE support with diffusion area lefs for core/IO views.
- Larger diode sizes for better PAE fixes in RAMs.

For continuity the highlights of the previous minor release (2.3) are listed below.

- Avanti view generation and support for place-and-route.
- Chip Architect and Physical Compiler view generation and support.
- Parasitic spice netlist generation for standard cells and TSMC IO.
- Support for PowerMill and TimeMill.
- Support for 2.5D extraction with cap.data file.
- Merger of all standard cells into one chunk: core.
- Pseudo clock cells (PCLK) are removed.
- Strapping of standard cells for EM improvement.
- Synopsys .lib updated with max_tran.
- AppNotes and Bill of Materials, included with this release.
- Silicon Ensemble .ini and map files.
- Virtuoso drf and map files.

3. Library Release Summary

3.1. Library Contents

3.1.1. Standard Cells

The standard cell segments contain the cells based on Synopsys cell list S0004A, detailed in the Bill of Materials document BOMDW_TSMC_2.3.1.pdf.

3.1.2. Memories

This release includes ProMA single port and dual port synchronous RAMs.

3.1.3 I/Os

TSMC 0.18um I/O library v150b is integrated in this release. Section 10 of this Release Notes contains release information from TSMC about this I/O library.

3.1.4. Library Views

This Library includes views for the following tools (file types are given where appropriate):

- Schematics and symbols: Cadence Composer
- Synthesis: Synopsys Design Compiler:

  *.lib, *.db - compatible with DC versions up to 99.05.

  core.slib, core.sdb
- Chip Architect and Physical Compiler
- VHDL/Mentor-MTI: ModelSim
- Simulation: Synopsys VCS, Cadence Verilog-XL, Mentor-MTI ModelSim
- Static Timing Analysis models: Synopsys PrimeTime
- LEF and technology file for Place and Route: Silicon Ensemble, CT-Gen (includes TLF). SE version of 5.3 and above needs to be used to effectively address the PAE effects.
- Avant! Place and Route: Apollo
- Layout: gdsii
- Netlist: spice for LVS, spice with parasitics information for Synopsys PowerMill, TimeMill, etc.
- Physical verification: DRC, LVS, and ANT rule decks based on TSMC 0.18um Dracula Rule v1.2, TA-10A5-4001.
- RC Extraction: Arcadia technology file

- PowerMill, TimeMill technology files
- Avant! Milkyway tech files

3.1.5. Documentation

This release 2.3.1 includes these documents in the library directory:

- Databook: HTML-formatted databook for Synopsys standard cells, RAMs, and TSMC IO cells
- TSMC's I/O library v150b Product Brochure
- DW_TSMC_SCB971 Release 2.3.1 Library Release Notes, May 8, 2000
- Synopsys' Bill of Materials

  BOMDW_TSMC_SCB971_2.3.1.pdf
- Synopsys' AppNotes v1.3 for Silicon Ensemble Place-and-Route
- Synopsys' Guidelines v1.0 for Power Routing
- Synopsys' AppNotes v1.0 for Milkyway Database, for Apollo Place-and-Route guideline and Avanti view generation.
- TSMC' SSO Guideline, Preliminary, January 31, 2000.
- Synopsys' AppNotes on ProMA Power Routing guidelines

3.2. Process Support

3.2.1. Process Name

This library was based on TSMC 0.18um 1P6M Salicide 1.8V/3.3V CL018G Process.

3.2.2. Metal Layers Support

This library supports all routing metal layers 4, 5, 6.

3.2.3. Design Rule Version and Waivers

The following design rule document was used for QA testing of this library release:

- TSMC 0.18um Logic 1P6M Salicide 1.8/3.3V Design Rule, Document No.T-018-LO-DR-001-D1 (new), i.e. TA-10A5-4001 (old), Revision 1.2, March 23rd, 1999

3.3. Operating and Characterization Conditions

Release 2.3.1 follows TSMC operating corner definitions. Per TSMC's indication, this library release does not support derating data. The timing characterization was performed at the 3 Process/Temperature/ Voltage corners shown in the following tables using post-correlated HSPICE models supplied by TSMC. The user is advised not to create his/her own operating conditions as the timing will not change because the derating factors are zero.

TABLE 1. Release 2.3.1 Core Cell Default Library Operating Corners

Library Operating Corner	Temperature	Voltage	Process SPICE Model or Derating Factor
Best Case	0 ^{o}C.	1.98 V	Fast
Typical Case	+25 ^{o}C.	1.80 V	Typical
Worst Case	+125 ^{o}C.	1.62 V	Slow

TABLE 2. Release 2.3.1 IO Cell Default Library Operating Corners

Library Operating Corner	Temperature	Voltage	Process SPICE Model or Derating Factor
Best Case	0 ^{o}C.	3.6 V	Fast
Typical Case	+25 ^{o}C.	3.3 V	Typical
Worst Case	+125 ^{o}C.	3.0 V	Slow

4. Library Structure

The content is as per the library structure defined in Bill of Materials:

BOMDW_TSMC_SCB971_2.3.1.pdf

5. Library Quality Assurance

This library final testing was done using the tools and versions listed in the Bill of Materials

BOMDW_TSMC_SCB971_2.3.1.pdf

6. Enhancements and Bug Fixes

6.1. Enhancements

Library Release 2.3.1 contains these enhancement

- 7 cells have been redesigned and all views regenerated. In 2 of the 7 cells, M2 pins were changed slightly to remove a DRC when m4 power stripes were used. Remaining 5 cells were reported with tool generated layouts instead of hand generated ones. No design changes were done to these cells.
- The antenna entries have been separated from core and IO lef and has been enhanced to include diffusion areas for antenna fixes with 5.3 Silicon Ensemble.

- The “shape feedthru” has been changed to “shape abutment” in the lef as Silicon Ensemble generates more predictable power routes with the latter than the former.
- Apollo views have been enhanced by including the diffusion area information of pins for adressing antenna effects.
- Mill tool tech files have been updated for a higher VGS/VDS range.
- The wire load models have been removed from the io.lib and will be taken from the core chunk when used in a design.
- Family specific prefixes have been added to RAMs to remove chances of any accidental over writing of RAM subcells.
- All unused test inputs in RAMs are tied off to ground.

6.2. Bug Fixes

Library Release 2.3.1 contains the following bug fixes.

(1) The spice netlist with parasitcs for core cells has been updated to include hld1a0 cell.

(2) strmin_cust has been updated to have separate layer numbers for PACTIVE and NACTIVE.

(3) A minor verilog model update to fix some warnings in VCS.

(4) Pin extension and obstruction layer positions were altered to match wide-metal spacings in RAMs.

6.3. Filing Synopsys Technical Action Requests (STARs)

Please email your issues to sls_support@synopsys.com. They will be forwarded to STAR for follow up actions.

7. Known Issues and Solutions (if applicable)

The following lists all known issues in this library release.

7.1. Verilog/Vital I/O Models:

The cells that have PAD pin as either pullup or pulldown, for example pull down cell PDD12DGZ, have been modeled in Verilog such that the PAD pin goes to high impedance state instead of a weak low or weak high. Since the cells have been designed as having the very weak pullup and pulldown circuit, this behavior of Verilog models discourages the user to use these cells as pullup or pulldown cells.

7.2. Physical Compiler v1.1:

DEF out from Physical Compiler v1.1 is not correct, and can create warnings when read into Silicon Ensemble. This will be fixed in Physical Compiler v1.2. The following is a section of DEF from PC, v1.1,

ROW ROW_51 corner 2001440 2001440 S DO 1 BY 1 STEP 0 470000 ;

ROW ROW_51 corner 2001440 2001440 S DO 1 BY 1 STEP 470000 0 ;

This should have been

ROW ROW_51 corner 2001440 2001440 S DO 1 BY 1 STEP 470000 470000

7.3. Silicon Ensemble:

(1) The bus name notations in DEF files come out different from verilog netlist when a DEFout is done from Silicon Ensemble.

Verilog	Def
\A[0]	A\[0\]

^^^^^^ <- Should be A[0]

This creates mismatches between extracted parasitics in DSPF and verilog netlist during back annotation phase. Please check for this inconsistency and make changes, if necessary, to DEF for fixing this problem

(2) After clock tree generation the ctgen flow has a problem when "verilog out" needs to be done from it. The problem here is that the IOs have VSS as ground and standard cells have GND. This results in errors during the verilog read phase. The workarounds are

- If you need to do a "verilog out" remove the PVSS* cells from the verilog netlist read in.
- Do a def out instead of verilog out and thus get over this problem.

(3) When using m4 or m6 power stripes the variable SROUTE.ALLOWOVERLAPINSTACKVIA needs to be set to “true”. This will allow connection of stripes to the rings. However while connecting power ports on IOs this variable needs to be set to “false” to prevent formation of rectangular vias.

(4) “Verify Library” gives the following ignorable warnings on a “core only” library.

50 Warning(s) [173]: abutment/feedthru libPin doesn't end at macro edge.

50 Warning(s) [175]: feedthru libPin has multiple paths across macro.

With IO library “Verify Library” crashes. We have sent a test-case to Cadence for analysis.

(5) “Verify Technology” gives the following ignorable warnings with IOs. Problem [134] can be easily removed by setting variable “verify.technology.max.featuresize” to a value above all feature sizes in the specific design.

#---{21 Problem(s) [134]: unreasonable via width.}

#---{1 Problem(s) [194]: GCell size is less than track spacing.}

#---{1 Warning(s) [196]: GCell size is less than track spacing.}

7.4. Antenna support with SE5.3:

The Antenna flow has changed quite a bit in SE5.3.

(1) The antenna lef is **not** read in directly using “Input LEF” construct of SE. The addition of diffusion areas in to antenna lef is not readable by “Input LEF’.

(2) The variable “wroute.addition.lefname” needs to be set in se.ini. This forces wroute to directly read in the antenna lef during routing. Wroute understands the diffusion area constructs.

USAGE: set var wroute.addition.lefname “<filename>”

(3) However, wroute reads **only** one antenna lef so the user needs to ‘cat’ the antenna lefs for core/IO and update the se.ini wroute.addition.lefname. We have sent a testcase to Cadence to remove this wroute limitation (Case ID 1321220).

(4) The core lef should be present first in the combined antenna lef as this only has the metal layers defined in it.

(5) The “END LIBRARY” statement should be present only once at the end of the file in the combined antenna lef.

7.5. TSMC IO Library v150b:

(1) The Resistance models are not defined in the SPICE netlist and so even if all devices are matching one may get mismatches in DEVICE MATCHING SUMMARY BY TYPE. A typical mismatch is like this.

RES		68	0	0	0
RES	PR	0	16	0	0
RES	NR	0	34	0	0
RES	ND	0	18	0	0

This needs modification in SPICE netlist by TSMC by tagging sub-type to the resistance.

(2) The Design Compiler warning "PAD cell has more than one PAD pin" for cell PDX001DG is ignorable as per TSMC.

(3) The Design Compiler warning "cell has unused input pins" in cell PDDW02DGZ is waived by TSMC.

(4) The IO cells PDUSDGZ and PDUDGZ have an internal gate connected to the buses directly and hence results in antenna violations. This has been flagged to TSMC.

(5) With bonding pads, Apollo's 'geNewDRC' (like 'verify geometry' in SE) generates false violations. Error occurs between PAD's pad pins and metals of bonding PAD. It is connected via abutment.

7.6. PowerMill:

(1) WARNING: PowerMill:0x2040d525: Negative bulk-source bias: element x2.m116, vbs=-1.8 This warning is ignorable.

(2) WARNING:PowerMill:0x2040e526:Element x1.m0 outside tech_file range (vg=1.8, vd=-0.686206,vs=-0.686206)

This happens because the delta_vt value by default in the tech file from -0.5 below gnd to 0.5 above vdd. This can be ignored.

(3) For some very high channel length transistors the SPICE model from TSMC does not contain the device model. Thus the “mill” tech file will also not support them. In these cases the information is taken from the nearest size transistors.

a. nd w=1.180 l=36.745

b. nd w=12.045 l=31.800

c. pd w=5.000 l=24.850

d. pd w=15.045 l=31.280

are the "nd" and "pd" model transistors where this issue was noticed.

7.7 Dracula:

(1) For pattern density requirements when metal-bars in m4/m5/m6 are placed over rams, false violations are seen. This happens because the bitcell has an exclusion layer in it and when the metal-bars are placed over the rams, the deck excludes that piece of metal which runs on top of the bit cell and reports some false DRC violations on the remaining metal chunk. A change in the deck has been suggested to TSMC to get over this issue.

(2) LVS device size mismatches were noticed in specific cases when large number of memories were present in a design. The unused delay chain fragments with input of the first inverter connected to ground is randomly matched by Dracula. Per “openbook” the E option in LVSCHK (already present in Dracula deck) should fix this problem. The version 4.7.0399 used for our QA does not fix this. A test-case has been sent to Cadence.

7.8 Memories:

(1) Because of floating nodes and unconnected nodes in dual port and single port ram spice netlist, LOGLVS (in Dracula) generates some warnings in the file PRINT.OUT. These are ignorable.

Sample warning are like these

```
========
 PROCESSING INPUT FILE: ram1.spice
 *** WARNING : FLOATING NET: a1          IN SUBCKT cseldec2_1p
 *** WARNING : FLOATING NET: n0          IN SUBCKT rw1p_4_1_g
 *** WARNING : FLOATING NET: n0          IN SUBCKT rw1p_4_4_g
 *** WARNING : I/O PIN oe          OF SUBCKT outreg4x_1p  IS NOT CONNECTED
INSI
DE SUBCKT DEFINITION
 *** WARNING : I/O PIN oe          OF SUBCKT outreg1x_1p  IS NOT CONNECTED
INSI
DE SUBCKT DEFINITION
 *** WARNING : FLOATING NET: n0          IN SUBCKT rw1p_4_1_p
```

*** WARNING : FLOATING NET: n0 IN SUBCKT rw1p_4_4_p

========

(2) The LEF generated by ProMA has blockages on all layers above m3. The number of layers in the technology is decided by the “maxObstLayer” in tech.cp. This value is set to “5” for this library and hence the obstruction will always be generated till m5. Please update the lef as per the design requirement while using it on m4/m6 designs.

7.9 Apollo:

The following ignorable warnings are generated from Apollo during Place & Route with the library.

(1) **** WARNING:Layer (m5) pitch (0.56) may not be optimal.

recommended range: wire-via(0.61) via-via(0.66)

**** WARNING:Layer (m6) pitch (1.12) may not be optimal.

recommended range: wire-via(0.95) via-via(1.00)

(2) During Timing driven placement the following warnings are flagged.

WARNING : No. of timing port on cell PVDD2DGZ.TIM is set as 0 falsely.

WARNING : There is no timing port on cell PVDD2DGZ.TIM.

WARNING : No. of timing port on cell PVSS2DGZ.TIM is set as 0 falsely.

WARNING : There is no timing port on cell PVSS2DGZ.TIM.

These cells do not have timing and hence the above can be ignored.

7.10 Known Deficiencies:

- Memories
  - Memory pins are protected by diodes, but the diffusion and gate area information are not present in the LEF for the router to fix metal/diffusion antenna rules.
  - “max_tran” and “max_fanout” entries not present in RAM models.
- IOs
  - Composer symbols/schematics are not released by TSMC and so are absent in this library.
- Generic
  - TLF/CTLF 4.1 version is not supported in this release.
  - Gated clock cells will be added for Power Compiler.
  - Calibre decks are not supported in this release. But TSMC provides Calibre decks and so they can be obtained from TSMC in case the user wants to verify with Calibre.

The above known deficiencies will be addressed in future releases.

8. Special Notes

This following sections describe special issues that the user should be aware of regarding this release,

including known problems and solutions.

8.1 Silicon Ensemble Version

While running place and route, please use Silicon Ensemble version 5.3.46 or newer.

8.2 ProMA Version

The suggested version of ProMA (Memory Compiler) to be used with this library is 3.0.3.

8.3 Layer Mapping

This Release 2.3.1 follows the layer mappings defined in TSMC's "Acceptance Requirements for TSMC libraries, Revision 1.2, August 2, 1999: Appendix B."

8.4. IO Filler Cells

The IO filler cells that are less than order 20 do not have a slot in them inside the metal structure and so when those fillers are piled up, the width of the metal combined together exceeds the minimum allowable metal width resulting in fat metal violations. So care should be taken in the IO filler placement.

9. Library Release History

Library DW_TSMC_SCB971 Release 2.3.1 is the first release with both single port and dual port RAMs, and TSMC IO library v150b.

Library SC_SCB971 Release 2.0.0 was the first time release to Synopsys external customer.

10. TSMC's Release Information for IO library v150b

The following information is provided by TSMC for TSMC's 0.18um IO library v150b.

10.1. Library Information

Library Name: TPZ973G

Technology : 0.18um, LOGIC 1.8V/3.3V Process, Salicide

SPICE Model: TA-10A5-6001 SPICE model v1.4

Version : 150b

Cell Type : IO

Cell Number: 143 Cells + 2 Pad Cells + 8 Feeder Cells (detailed list available in Bill of Materials document BOMDW_TSMC_2.3.1.pdf)

IO SPICE files tpz973g_1.2.spi and tpz973g_3.spi: when using this I/O library, the user can take either one of two approaches:

(1) separate standard cell ground from I/O ground (provided by PVSS1DGZ and PVSS2DGZ, respectively) or

(2) use common standard cell ground and I/O ground provided by I/O cell PVSS3DGZ.

For (1), the LVS SPICE netlist should use tpz973g_1_2.spi.

For (2), the LVS SPICE netlist should use tpz973g_3.spi.

10.2. Update History

(1) Added 32 cells with schmitt triggered input buffer
(2) Added 22 cells with controllable pullup/pulldown:
(3) Canceled 10 cells with both small driving current and output slew rate control:
(4) Modified the ’PAD->C’ predriver part circuit.
(5) Added ’PFEED35’.
(6) Added ’PCORNERDG_L’ for linear bonding usage.
(7) Modified 16mA series circuits to prevent leakage (when 5 volt input)

10.3 Characterization Conditions

TYPICAL : VDDIO=3.3V, VDDCORE=1.8V, Temp=25 ^{0}C
Process=NMOS : Typical, PMOS : Typical
BEST : VDDIO=3.6V, VDDCORE=1.98V, Temp=0 ^{0}C
Process=NMOS : Fast, PMOS : Fast
WORST : VDDIO=3.0V, VDDCORE=1.62V, Temp=125 ^{0}C
Process=NMOS : Slow, PMOS : Slow