DesignWare Silicon Libraries
DW_TSMC_SCB971_2.3.1

Bill of Materials Document Contents

TechSpecifications - library contents and technology info
LibBOM - library files & directory structure
EDB - details of electronic databook files and directory structure
Tools_versions - list of tools supported and version tested
IOlist
Corelist
Docs - list of documentation available for the library
GDSlayertable

		Notes
Library Name:	DW_TSMC_SCB971	
Library release version:	2.3.1	
ProcessVendor:	TSMC	
Technology (um):	0.18	
Process:	SCB971	
Min metal layers:	4	although the process allows 3 layer metal routing, we have set the minimum to 4, as memories cannot be used in a 3 metal layer process
Max metal layers:	6	
SPICE model version:	1.5	TSMC 0.18um Logic 1P6M Salicide 1.8V/3.3V Spice Models, 8-31-99, Document # TA-10A5-6001.
Design Rules version:	1.2	TSMC 0.18um Logic 1P6M Salicide 1.8V/3.3V Design Rule, 3-23-99, Document # TA-10A5-4001.
DRC deck version:	1.2D	Dracula DRC Command File v1.2D
LVS deck version:	1.5D	Dracula LVS Command File v1.5D
ANT deck version:	1.2C	Antenna Dracula DRC Command File v1.2C
GDS layer information:	TSMC	details in GDS layer table sheet
Library contents		
SNPS developed		
Standard cells		
- number of cells (list)	662 (list S0004A)	
Single-port RAM	yes	
Dual-port RAM	yes	
Vendor/customer provided		
I/Os		TSMC
- I/O voltage - core voltage	3.3V (5V tol) - 1.8V	
- number of cells (list)	153 (tpz973g digital library v150)	
- ESD solution	TSMC	
- I/O width (um)	40	
- bonding pitch (um)	40 (staggered)	
Operating/characterization conditions		
core		
best corner (P, V, T)	fast-fast, 1.98V, 0C	
typ corner (P, V, T)	typ-typ, 1.8V, 25C	
worst corner (P, V, T)	slow-slow, 1.62V, 125C	
I/Os		
best corner (P, V, T)	fast-fast, 3.0V, 0C	
typ corner (P, V, T)	typ-typ, 3.3V, 25C	
worst corner (P, V, T)	slow-slow, 3.6V, 125C	
Derating factors		
best corner (k_voltage, k_temp)	0, 0	
typ corner (k_voltage, k_temp)	0, 0	
worst corner (k_voltage, k_temp)	0, 0	
Special requirements/notes		

Bill of Materials - Libraries

Top level directory:
<...>/taipei/SC_SCB971_2.3.1

Directory structure		Files	Description	Notes	Tool(s)	Prov. by
		BOMDW_TSMC_SCB971_2.3.1.pdf	this document			SNPS
		README	readme file with usage info			SNPS
tech/	arcadia/	atf_Mlm.rul	Arcadia parasitic extractor tech file		Arcadia	SNPS
	dracula/	DRC_Mlm, LVS_Mlm, AntNN	Dracula DRC , ANT and LVS (incl.ERC) decks	M=4,5,6=# of metal layers NN=01,...,10 **TAPE-OUT view**	Dracula	TSMC
	milkyway/	milkyway_Mlm.tf	Milkyway tech files	M=4,5,6 =# of metal layers	Apollo	SNPS
	mill/	mill.typ, mill.bccom,mill.wccom	typ, best, worst case technology files to be used by *Mill tools		TimeMill PowerMill	SNPS
	se/	se_Mlm.ini, se2gdsii_Mlm.map, cap_Mlm.data	Silicon Ensemble P&R setup files	M=4,5,6 =# of metal layers	Silicon Ens.	SNPS
	virtuoso/	tsmc.strmin, display.drf, strmin_cust, layer.drf	Layout viewer tech files	**TAPE-OUT view**	Virtuoso	TSMC
doc/	appnotes/	power_routing_1.0.pdf, apollo_1.0.pdf silicon_ensemble_1.3.pdf, tpz973g_sso_pre.pdf proma_power_routing_1.0.pdf	Application notes			SNPS
	edb/	*detailed structure presented on separate EDB sheet*	Electronic data books			SNPS
	releasenotes/	RNDW_TSMC_SCB971_2.3.pdf/text/ps/fm	Release notes (pdf, txt, ps & txt)			SNPS
core/	apollo/cell_frame/CEL/	cel files	Apollo P&R GDSII/abstract views	**TAPE-OUT view**	Apollo	SNPS
	apollo/cell_frame/FRAM/	fram files	Apollo P&R abstract view	**TAPE-OUT view**	Apollo	SNPS
	apollo/cell_frame/TIM/	tim files	Apollo timing driven P&R view	**TAPE-OUT view**	Apollo	SNPS
	apollo/cell_frame/	lib, lib_1, lib_bck	Milkyway pointer files	**TAPE-OUT view**	Apollo	SNPS
	apollo/frame_only/CEL/	UnitTile*	Apollo P&R GDSII/abstract view place holder		Apollo	SNPS
	apollo/frame_only/FRAM/	fram files	Apollo P&R abstract view		Apollo	SNPS
	apollo/frame_only/TIM/	tim files	Apollo timing driven P&R view		Apollo	SNPS
	apollo/frame_only/	lib, lib_1, lib_bck	Milkyway pointer files		Apollo	SNPS
	composer/sch/dw_core/	cell shematic and symbol file database	Shematic and symbol files	**TAPE-OUT view**	Virtuoso	SNPS
	composer/symbol/dw_core/	cell symbol file database	Symbol files		Composer	SNPS
	gdsii/	core.gdsii	GDSII view for tapeout purposes	**TAPE-OUT view**		SNPS
	release_list/	core.txt	text list of all I/O cells available in the library			SNPS
	scripts/	procSDF, procSDF.txt	script to modify SDF and documentation		VSS	SNPS
	se/ctlf/	core_fast.ctlf, core_typ.ctlf, core_slow.ctlf	Cadence compiled timing files		Silicon Ens. CT-gen	SNPS
	se/lef/	core_Mlm.lef, antenna_core_Mlm.lef	Silicon Ensemble source file		Silicon Ens.	SNPS
	se/tlf/	core_fast.tlf, core_typ.tlf, core_slow.tlf	Cadence ASCII timing files	**TAPE-OUT view**	Silicon Ens. CT-gen	SNPS
	spice/lvs	core.spice	SPICE netlist for LVS	**TAPE-OUT view**	Dracula, etc.	SNPS
	spice/mill	core_full.spice	SPICE netlist with parasitics information	**TAPE-OUT view**	TimeMill PowerMill	SNPS

Directory structure		Files	Description	Notes	Tool(s)	Prov. by
	synopsys/db/nopower/	core_fast.db, core_typ.db, core_slow.db, core.sdb	.db files		Design Comp. PrimeTime, etc.	SNPS
	synopsys/db/power/	core_fast.db, core_typ.db, core_slow.db, core.sdb	.db files w/ power info		Design Comp. PrimeTime, etc.	SNPS
	synopsys/idm/Mlm/DEF/	cellname	Chip Architect - cell port info		Chip Architect	SNPS
	synopsys/idm/Mlm/IDMPLAYOUT/	<cellnames>	Chip Architect - cell layout info		Chip Architect	SNPS
	synopsys/idm/Mlm/MISC/	pre_read_design.tcl, post_read_design.tcl, version	Chip Architect - scripts		Chip Architect	SNPS
	synopsys/idm/Mlm/PDLLIB/	viaTypesAndRules, core.pdl	Chip Architect - tech info		Chip Architect	SNPS
	synopsys/idm/Mlm/SYSTEM/		empty dir. used at chip level		Chip Architect	SNPS
	synopsys/lib/nopower/	core_fast.lib, core_typ.lib, core_slow.lib, core.slib	.lib files	**TAPE-OUT view**	Library Comp.	SNPS
	synopsys/lib/power/	core_fast.lib, core_typ.lib, core_slow.lib, core.slib	.lib files w/ power info	**TAPE-OUT view**	Library Comp.	SNPS
	synopsys/pdb/	core_Mlm.pdb	Physical Compiler source files		Phys. Comp.	SNPS
	synopsys/plib/	core_Mlm.plib	Physical Compiler source files	**TAPE-OUT view**	Phys. Comp.	SNPS
	verilog/	core.v	Verilog library source file		Verilog-XL VCS	SNPS
	vital/	core.vhd, core_components.vhd, core_tables.vhd	VHDL library source file		VSS	SNPS
io/tpz973g_v150	apollo/Mlm/cell_frame/CEL/	cel files	Apollo P&R GDSII/abstract views	**TAPE-OUT view**	Apollo	TSMC
	apollo/Mlm/cell_frame/FRAM/	fram files	Apollo P&R abstract view	**TAPE-OUT view**	Apollo	TSMC
	apollo/Mlm/cell_frame/TIM/	tim files	Apollo timing driven P&R view	**TAPE-OUT view**	Apollo	TSMC
	apollo/Mlm/cell_frame/	lib, lib_1, lib_bck	Milkyway pointer files	**TAPE-OUT view**	Apollo	TSMC
	apollo/Mlm/frame_only/CEL/		Apollo P&R GDSII/abstract view place holder		Apollo	TSMC
	apollo/Mlm/frame_only/FRAM/	fram files	Apollo P&R abstract view		Apollo	TSMC
	apollo/Mlm/frame_only/TIM/	tim files	Apollo timing driven P&R view		Apollo	TSMC
	apollo/Mlm/frame_only/	lib, lib_1, lib_bck	Milkyway pointer files		Apollo	TSMC
	gdsii	io_Mlm.gdsii		**TAPE-OUT view**		TSMC
	release_list/	io.txt	text list of all I/O cells available in the library			SNPS
	se/lef/	io_Mlm.lef, antenna_io.lef	Silicon Ensemble source files		Silicon Ens.	TSMC
	se/tlf/	io_fast.tlf, io_typ.tlf, io_slow.tlf	Cadence ASCII timing files	**TAPE-OUT view**	Silicon Ens. CT-gen	SNPS
	se/ctlf/	io_fast.ctlf, io_typ.ctlf, io_slow.ctlf	Cadence compiled timing files		Silicon Ens. CT-gen	SNPS
	spice/lvs	io.spice, io_PVSS3.spice	SPICE netlist for LVS	**TAPE-OUT view**	Dracula, etc.	TSMC
	spice/mill	io_full.spice, io_PVSS3_full.spice	SPICE netlist with parasitics information	**TAPE-OUT view**	TimeMill PowerMill	SNPS
	synopsys/db/power	io_fast.db, io_typ.db, io_slow.db, io.sdb	.db files, w/ power data		Design Comp. PrimeTime, etc.	SNPS
	synopsys/idm/Mlm/DEF	<cellnames>	Chip Architect - cell port info		Chip Architect	SNPS
	synopsys/idm/Mlm/IDMPLAYOUT/	<cellnames>	Chip Architect - cell layout info		Chip Architect	SNPS
	synopsys/idm/Mlm/MISC/	pre_read_design.tcl, post_read_design.tcl, version	Chip Architect - scripts		Chip Architect	SNPS
	synopsys/idm/Mlm/PDLLIB	viaTypesAndRules, io.pdl	Chip Architect - tech info		Chip Architect	SNPS
	synopsys/idm/Mlm/SYSTEM/		empty dir used at chip level		Chip Architect	SNPS
	synopsys/lib/nopower	io_fast.lib, io_typ.lib, io_slow.lib, io.slib	.lib files	**TAPE-OUT view**	Design Comp.	SNPS
	synopsys/lib/power	io_fast.lib, io_typ.lib, io_slow.lib, io.slib	.lib files w/ power info	**TAPE-OUT view**	Design Comp.	SNPS

Directory structure		Files	Description	Notes	Tool(s)	Prov. by
	synopsys/pdb/	io_Mlm.pdb	Physical Compiler source files		Phys. Comp.	SNPS
	synopsys/plib/	io_Mlm.plib	Physical Compiler source files	**TAPE-OUT view**	Phys. Comp.	SNPS
	verilog/	io.v	Verilog library source file		Verilog-XL VCS	SNPS
	vital/	io.vhd, io_components.vhd, io_table.vhd	VHDL library source file		VSS	SNPS
mem/common/		layer.tech, proma.tech				
	apollo/	proma2a	script to create milkyway views for memories			
mem/<memtype>/	char/	incap and prop delay files used by ProMA	ProMA Compiler source timing file	<mem_type>= ram_1_speed_sync	ProMA 2.0+	SNPS
	compiler/	assembly.cp, rules_err.proto, pre_rules.cp, post_rules.cp	ProMA Compiler rule files		ProMA 2.0+	SNPS
	gdsii/	cells.gdsii	GDSII view for tapeout purposes	**TAPE-OUT view**		SNPS
	scdf/	cells.scdf	ProMA Compiler source timing file		ProMA 2.0+	SNPS
	spice/	cells.spice	SPICE netlist for LVS comparison	**TAPE-OUT view**		SNPS
	tech/	tech.cp	ProMA Compiler source tech file		ProMA 2.0+	SNPS

Synopsys HTML electronic databooks file structure details						
Top level directory:						
<...>/taipei/SC_SCB971_2.3.1						
Directory structure				**Files**	**Comments**	**Notes**
doc/	edb/			dwsl_databook_toc.html, dwsl_macrocell_frame.html, dwsl_macrocell_groups.html, dwsl_macrocell_instructions.html, tsmc_macrocell_groups.html, tpz973g_general.pdf		
		core	html	core_common_params.html, <cell>.html		
			symbols	<cell>.gif		
			truth_tables	<cell>.tt		
		io/tpz973gwc		index.html, cindex.html, catalog.html, <cell>.html		
			sym	<cell>.gif		
		io/tpz973gtc		index.html, cindex.html, catalog.html, <cell>.html		
			symbols	<cell>.gif		
		io/tpz973gbc		index.html, cindex.html, catalog.html, <cell>.html		
			symbols	<cell>.gif		
		images		*.gif	general images: logos, bullets, etc.	
		general_datasheets		dwsl_toc.html, dwsl_overview.html, dwsl_core.html, tpz973g_general.pdf		
			memory/proma/	proma_ram_compiler.html, *.gif		
			memory/proma/hs-hd-1p-sr	proma_hs-hd-1p-sr.html, *.gif		
			memory/proma/hs-hd-2p-sr	proma_hs-hd-2p-sr.html, *.gif		

			Standard cells	I/Os	Memories	
Design Phase	**Tool**	**Company**	**Current Test Version**	**Current Test Version**	**Current Test Version**	**Deliverables**
Verilog Sim.	VCS	Synopsys	5.1	5.1	5.1*	.v
	Verilog-XL	Cadence	2.7	2.7	2.7*	.v
	SDF Annotator	Cadence	2.3.3	2.3.3	2.3.3*	
	SDF Interface	Cadence	5.4.1	5.4.1	5.4.1*	
SDF compatib.			2.1	2.1	2.1*	
VHDL/Vital Sim.	VHDL System Simulator (VSS)	Synopsys	99.05	99.05		.vhd
	ModelSim (VHDL)	Mentor/MTI	5.3	5.3	5.3*	.vhd
SDF compatib.			2.1	2.1	2.1*	
Synthesis	Design Compiler	Synopsys	99.05	99.05	99.05*	.db, .lib, .slib, .sdb, (ITS - mem)
	Module Compiler	Synopsys	99.05	99.05	n/a	.db, .lib, .slib, .sdb
Physical Synthesis	Physical Compiler	Synopsys	1.1	1.1		z
Static timing	PrimeTime	Synopsys	99.05	99.05	99.05*	.db, .lib (STAMP - mem)
	PathMill (tr. level)	Synopsys	5.4	5.4		tech files
Dynamic timing an.	TimeMill	Synopsys	5.4	5.4		tech files
Design planning	Chip Architect	Synopsys	3.31	3.31		idm
Place&Route	Silicon Ensemble	Cadence	5.3.46	5.3.46	5.2.136*	.lef, .tlf, .ctlf, tech files
	TLF	Cadence	3.1	3.1	3.0	.tlf, .ctlf
	Apollo-II	Avant!	99.4.3.3.1	99.4.3.3.1	appnote	fram, tim, cel & tech files
	Wroute	Cadence	2.2.26	2.2.26	2.1.26*	.lef
	CT-Gen	Cadence	3.4.0	3.4.0	3.4.0*	.tlf, .ctlf
	QPlace	Cadence	5.1.55	5.1.55		.lef
Verification	Dracula	Cadence	4.7.0399	4.7.0399	4.7.0399	GDSII, SPICE netlist, techfiles
Schematic entry	Composer	Cadence	DFII 4.4.3.72	DFII 4.4.3.72	DFII 4.4.3.72*	symbols
Layout editor	Virtuoso	Cadence	4.4.3.72	4.4.3.72		symbols, schematics, tech files
Extraction	Arcadia	Synopsys	5.4	5.4		.rul
Design for Test	Test Compiler	Synopsys	99.05	99.05		.db, .lib
Power Est./Opt.	Power Compiler (&Design Power)	Synopsys	99.05	99.05		.db, .lib (w/power)
	PowerMill	Synopsys	5.4	5.4		tech files
Reliability	RailMill	Synopsys	5.4	5.4		tech files
Memory Compiler	ProMA Compiler	Synopsys	n/a	n/a	3.0.3	ProMA specific files

* views generated by ProMA Compiler

List of I/Os provided by TSMC

technology (um)	0.18
technology name	SCB971
process	thick oxide
core voltage (V)	1.8
I/O voltage (V)	3.3
Input tolerance (V)	5
Pitch (um)	40
List name	tpz973g_v150

Cell Name	Cell Description	Drives	Cells
	Input buffers		**8**
PDIDGZ	Input Pad, 5V tolerant		1
PDUDGZ	Input Pad with Pull-Up, 5V tolerant		1
PDDDGZ	Input Pad with Pull-Down, 5V tolerant		1
PDISDGZ	Schmitt Trigger Input Pad, 5V tolerant		1
PDUSDGZ	Schmitt Trigger Input Pad with Pull-Up, 5V-Tolerant		1
PDDSDGZ	Schmitt Trigger Input Pad with Pull-Down, 5V-Tolerant		1
PDUWDGZ	Input Pad with Enable Controlled 40k Pull-Up		1
PDDWDGZ	Input Pad with Enable Controlled 40k Pull-Down		1
	Clock buffers		**18**
PCKHxCDG	High Drive, Internal CMOS Clock Buffer	1,2,3	3
PCKHxSDG	High Drive, Internal Schmitt Trigger CMOS Clock Buffer	1,2,3	3
PCKxCDG	Very fast, Internal Clock Buffer	1,2,3,4,5,6	6
PDCHxDGZ	High Drive, CMOS Input Clock Pad, 5V-Tolerant	1,2,3	3
PDSHxDGZ	High Drive, Schmitt Trigger Input Clock Pad, 5V-Tolerant	1,2,3	3
	Output buffers		**10**
PDOxCDG	CMOS Output Pad	2,4,8,12,16,24mA	6
PROxCDG	CMOS Output Pad with Limited Slew Rate	8,12,16,24mA	4
	Three-state output buffers		**10**
PDTxDGZ	CMOS 3-state Output Pad, 5V-Tolerant	2,4,8,12,16,24mA	6
PRTxDGZ	CMOS 3-state Output Pad with Limited Slew Rate, 5V-Tolerant	8,12,16,24mA	4
	Bidirectional buffers		**80**
PDBxDGZ	CMOS 3-state Output Pad with Input, 5V-Tolerant	2,4,8,12,16,24mA	6
PRBxDGZ	CMOS 3-state Output Pad with Input and Limited Slew Rate, 5V-Tolerant	8,12,16,24mA	4
PDBxSDGZ	CMOS 3-state Output Pad with Input, 5V-Tolerant	2,4,8,12,16,24mA	6
PRBxSDGZ	CMOS 3-state Output Pad with Input and Limited Slew Rate, 5V-Tolerant	8,12,16,24mA	4
PDUxDGZ	CMOS 3-state Output Pad with Input and Pull-Up, 5V-Tolerant	2,4,8,12,16,24mA	6
PRUxDGZ	CMOS 3-state Output Pad with Input, Pull-Up, and Limited Slew Rate, 5V-Tolerant	8,12,16,24mA	4
PDUxSDGZ	CMOS 3-state Output Pad with Input and Pull-Up, 5V-Tolerant	2,4,8,12,16,24mA	6
PRUxSDGZ	CMOS 3-state Output Pad with Input, Pull-Up, and Limited Slew Rate, 5V-Tolerant	8,12,16,24mA	4
PDDxDGZ	CMOS 3-state Output Pad with Input and Pull-Down, 5V-Tolerant	2,4,8,12,16,24mA	6
PRDxDGZ	CMOS 3-state Output Pad with Input, Pull-Down, and Limited Slew Rate, 5V-Tolerant	8,12,16,24mA	4
PDDxSDGZ	CMOS 3-state Output Pad with Input and Pull-Down, 5V-Tolerant	2,4,8,12,16,24mA	6

Cell Name	Cell Description	Drives	Cells
PRDxSDGZ	CMOS 3-state Output Pad with Input, Pull-Down, and Limited Slew Rate, 5V-Tolerant	8,12,16,24mA	4
PDDWxDGZ	CMOS 3-state Output Pad with Input and Enable Controlled 40k Pull-Down	2,4,8,12,16,24mA	6
PRDWxDGZ	CMOS 3-state Output Pad with Input, Limited Slew Rate and Enable Controlled 40k Pull-Down	8,12,16,24mA	4
PDUWxDGZ	CMOS 3-state Output Pad with Input and Enable Controlled 40k Pull-Up	2,4,8,12,16,24mA	6
PRUWxDGZ	CMOS 3-state Output Pad with Input, Limited Slew Rate and Enable Controlled 40k Pull-Up	8,12,16,24mA	4
	Miscellaneous		**17**
PVDDxDGZ	Vdd Pad	1,2	2
PVSSxDGZ	Vss Pad	1,2,3	3
PCORNERDG(_L)	Corner pad		2
PFEEDx	Filler	01,1,2,5, 10,20,35,50	8
PADIZ40	Inside Bonding Pad		1
PADOZ40	Outside Bonding Pad		1
	Special I/Os		**10**
PDXOExDG	Crystal Oscillator with High Enable	1,2,3	3
PDXOxDG	Crystal Oscillator	1,2,3	3
PCI33DGZ	3-state Output 33MHz PCI Buffer Pad with Input and Limited Slew Rate, 5V tolerant	1	1
PCI33SDGZ	3-state Output 33MHz PCI Buffer Pad with Input and Limited Slew Rate, 5V tolerant	1	1
PCI66DGZ	3-state Output 66MHz PCI Buffer Pad with Input and Limited Slew Rate, 5V tolerant	1	1
PCI66SDGZ	3-state Output 66MHz PCI Buffer Pad with Input and Limited Slew Rate, 5V tolerant	1	1
	TOTAL CELLS		**153**

		S0004A	
Cell name	**Cell description**	**Drives**	**Cells**
		(#types)	
	Buffers	***6***	**42**
buf1a[n]	Non-inverting internal buffer	1,2,3,6,9,15, 27	7
clk1a[n]	Non-inverting internal clock buffer	2,3,6,9,15,27,54	7
clk1b[n]	Inverting internal clock buffer	2,3,6,9,15,27,54	7
inv1a[n]	Inverting internal buffer	1,2,3,6,9,15,27	7
tri1a[n]	Non-inverting internal 3-state buffer, high enable	1,2,3,6,9,15,27	7
tri1b[n]	Inverting internal 3-state buffer, high enable	1,2,3,6,9,15,27	7
	Complex gates	***31***	**186**
ao1a[n]	AND2A into OR2A	1,2,3,6,9,15	6
ao1b[n]	AND2B into OR2A	1,2,3,6,9,15	6
ao1c[n]	AND2C into OR2A	1,2,3,6,9,15	6
ao1d[n]	AND2A into OR2B	1,2,3,6,9,15	6
ao1e[n]	AND2B into OR2B	1,2,3,6,9,15	6
ao1f[n]	AND2C into OR2B	1,2,3,6,9,15	6
ao2a[n]	AND2A into OR3A	1,2,3,6,9,15	6
ao2e[n]	AND2B into OR3B	1,2,3,6,9,15	6
ao2h[n]	AND2B into OR3C	1,2,3,6,9,15	6
ao2i[n]	AND2C into OR3C	1,2,3,6,9,15	6
ao4a[n]	AND2A, AND2A into OR2A	1,2,3,6,9,15	6
ao4b[n]	AND2B, AND2A into OR2A	1,2,3,6,9,15	6
ao4c[n]	AND2C, AND2A into OR2A	1,2,3,6,9,15	6
ao4d[n]	AND2B, AND2B into OR2A	1,2,3,6,9,15	6
ao4e[n]	AND2B, AND2C into OR2A	1,2,3,6,9,15	6
ao4f[n]	AND2C, AND2C into OR2A	1,2,3,6,9,15	6
oa1a[n]	OR2A into AND2A	1,2,3,6,9,15	6
oa1b[n]	OR2B into AND2A	1,2,3,6,9,15	6
oa1c[n]	OR2C into AND2A	1,2,3,6,9,15	6
oa1d[n]	OR2A into AND2B	1,2,3,6,9,15	6
oa1e[n]	OR2B into AND2B	1,2,3,6,9,15	6
oa1f[n]	OR2C into AND2B	1,2,3,6,9,15	6
oa2a[n]	OR2A into AND3A	1,2,3,6,9,15	6
oa2c[n]	OR2C into AND3A	1,2,3,6,9,15	6
oa2i[n]	OR2C into AND3C	1,2,3,6,9,15	6
oa4a[n]	OR2A, OR2A into AND2A	1,2,3,6,9,15	6
oa4b[n]	OR2B, OR2A into AND2A	1,2,3,6,9,15	6
oa4c[n]	OR2C, OR2A into AND2A	1,2,3,6,9,15	6
oa4d[n]	OR2B, OR2B into AND2A	1,2,3,6,9,15	6
oa4e[n]	OR2B, OR2C into AND2A	1,2,3,6,9,15	6
oa4f[n]	OR2C, OR2C into AND2A	1,2,3,6,9,15	6
	D latches	***3***	**18**
ldf1a[n]	D latch	1,2,3,6,9,15	6
ldf1b[n]	D latch, low enable	1,2,3,6,9,15	6
ldf2a[n]	D latch, low clear	1,2,3,6,9,15	6

		S0004A	
Cell name	**Cell description**	**Drives**	**Cells**
		(#types)	
	Scan D latches	***3***	**18**
ldmf1a[n]	Scan D latch	1,2,3,6,9,15	6
ldmf1b[n]	Scan D latch, low enable	1,2,3,6,9,15	6
ldmf2a[n]	Scan D latch, low clear	1,2,3,6,9,15	6
	DFFs	***13***	**78**
fdef1a[n]	DFF with enable	1,2,3,6,9,15	6
fdef2a[n]	DFF with enable, low clear	1,2,3,6,9,15	6
fdef2c[n]	DFF with enable, low clear, inverted output	1,2,3,6,9,15	6
fdef3a[n]	DFF with enable, low preset	1,2,3,6,9,15	6
fdf1a[n]	DFF	1,2,3,6,9,15	6
fdf1b[n]	DFF, low clock	1,2,3,6,9,15	6
fdf1c[n]	DFF, inverted output	1,2,3,6,9,15	6
fdf1d[n]	DFF, low clock, inverted output	1,2,3,6,9,15	6
fdf2a[n]	DFF, low clear	1,2,3,6,9,15	6
fdf2b[n]	DFF, low clear and clock	1,2,3,6,9,15	6
fdf2c[n]	DFF, low clear, inverted output	1,2,3,6,9,15	6
fdf3a[n]	DFF, low preset	1,2,3,6,9,15	6
fdf3b[n]	DFF, low preset and clock	1,2,3,6,9,15	6
	Scan DFFs	***13***	**78**
fdesf1a[n]	Scan DFF with enable	1,2,3,6,9,15	6
fdesf2a[n]	Scan DFF with enable, low clear	1,2,3,6,9,15	6
fdesf2c[n]	Scan DFF with enable, low clear	1,2,3,6,9,15	6
fdesf3a[n]	Scan DFF with enable, low preset	1,2,3,6,9,15	6
fdmf1a[n]	Scan DFF	1,2,3,6,9,15	6
fdmf1b[n]	Scan DFF, low clock	1,2,3,6,9,15	6
fdmf1c[n]	Scan DFF, inverted output	1,2,3,6,9,15	6
fdmf1d[n]	Scan DFF, low clock, inverted output	1,2,3,6,9,15	6
fdmf2a[n]	Scan DFF, low clear	1,2,3,6,9,15	6
fdmf2b[n]	Scan DFF, low clear and clock	1,2,3,6,9,15	6
fdmf2c[n]	Scan DFF, active low clear, inverted output	1,2,3,6,9,15	6
fdmf3a[n]	Scan DFF, low preset	1,2,3,6,9,15	6
fdmf3b[n]	Scan DFF, low preset and clock	1,2,3,6,9,15	6
	Basic Adders	***6***	**18**
fa1a[n]	1-bit full adder	1,2,3	3
fa1b[n]	1-bit full adder, CI inverted	1,2,3	3
fa2a[n]	1-bit full adder, COUT inverted	1,2,3	3
ha1a[n]	1-bit half adder	1,2,3	3
ha1b[n]	1-bit half adder, B inverted	1,2,3	3
ha2a[n]	1-bit half adder, CO inverted	1,2,3	3
	Gates	***23***	**126**
and2a[n]	2-input AND gate	1,2,3,6,9,15	6
and3a[n]	3-input AND gate	1,2,3,6,9,15	6
and4a[n]	4-input AND gate	3,6,9,15	4

		S0004A	
Cell name	**Cell description**	**Drives**	**Cells**
		(#types)	
and6a[n]	6-input AND gate	3,6,9,15	4
and2b[n]	2-input AND gate, one input inverted; equivalent to 2-input NOR gate, one input inverted	1,2,3,6,9,15	6
and2c[n]	2-input AND gate, two inputs inverted; equivalent to 2-input NOR gate	1,2,3,6,9,15	6
and3b[n]	3-input AND gate, one input inverted; equivalent to 3-input NOR gate, two inputs inverted	1,2,3,6,9,15	6
and3c[n]	3-input AND gate, two inputs inverted; equivalent to 3-input NOR gate, one input inverted	1,2,3,6,9,15	6
and3d[n]	3-input AND gate, three inputs inverted; equivalent to 3-input NOR gate	1,2,3,6,9,15	6
and4e[n]	4-input AND gate, four inputs inverted; equivalent to 4-input NOR gate	3,6,9,15	4
or2a[n]	2-input OR gate	1,2,3,6,9,15	6
or3a[n]	3-input OR gate	1,2,3,6,9,15	6
or4a[n]	4-input OR gate	3,6,9,15	4
or6a[n]	6-input OR gate	3,6,9,15	4
or2b[n]	2-input OR gate, one input inverted; equivalent to 2-input NAND gate, one input inverted	1,2,3,6,9,15	6
or2c[n]	2-input OR gate, two inputs inverted; equivalent to 2-input NAND gate	1,2,3,6,9,15	6
or3c[n]	3-input OR gate, two inputs inverted; equivalent to 3-input NAND gate, one input inverted	1,2,3,6,9,15	6
or3d[n]	3-input OR gate, three inputs inverted; equivalent to 3-input NAND gate	1,2,3,6,9,15	6
or4e[n]	4-input OR gate, four inputs inverted; equivalent to 4-input NAND gate	3,6,9,15	4
xor2a[n]	2-input XOR gate	1,2,3,6,9,15	6
xor2b[n]	2-input XOR gate, one input inverted	1,2,3,6,9,15	6
xor3a[n]	3-input XOR gate	1,2,3,6,9,15	6
xor3b[n]	3-input XOR gate, one input inverted	1,2,3,6,9,15	6
	Multiplexers, decoders	***6***	**36**
mx2a[n]	2:1 multiplexer	1,2,3,6,9,15	6
mx2d[n]	2:1 multiplexer, inverting output	1,2,3,6,9,15	6
mx3a[n]	3:1 multiplexer	1,2,3,6,9,15	6
mx3d[n]	3:1 multiplexer, inverted output	1,2,3,6,9,15	6
mx4a[n]	4:1 multiplexer	1,2,3,6,9,15	6
mx4e[n]	4:1 multiplexer, inverted output	1,2,3,6,9,15	6
	Booth encoders and product generators	***5***	**15**
mule2a[n]	booth encoder	1,2,3	3
mulpa1b[n]	booth partial product generator (inv. 2:1 mux gated to 2:1 mux)	1,2,3	3
mulpa2b[n]	booth partial product generator (2:1 mux gated to 2:1 mux)	1,2,3	3
mulpa3b[n]	booth partial product generator (2:1 mux into inverting ao4a)	1,2,3	3
mulpa4b[n]	booth partial product generator (2:1 mux into ao4a)	1,2,3	3
	MC Adders	***14***	**42**
fac1b[n]	1-bit full adder, CI inverted	1,2,3	3

		S0004A	
Cell name	**Cell description**	**Drives**	**Cells**
		(#types)	
fac2a[n]	1-bit full adder, COUT inverted	1,2,3	3
faccs1b[n]	1-bit full carry select adder, CI inverted, no sum output	1,2,3	3
faccs2a[n]	1-bit full carry select adder, COUT inverted, no sum output	1,2,3	3
faccs3a[n]	1-bit full carry select adder, no carry in, no sum output	1,2,3	3
facs1b[n]	1-bit full carry select adder, CI inverted	1,2,3	3
facs2a[n]	1-bit full carry select adder, COUT inverted	1,2,3	3
facs3a[n]	1-bit full carry select adder, no carry in	1,2,3	3
facs4a[n]	1-bit full carry select adder, no carry in	1,2,3	3
facsf1b[n]	1-bit full adder, CI inverted	1,2,3	3
facsf2a[n]	1-bit full adder, COUT inverted	1,2,3	3
hacs1b[n]	1-bit carry select adder, CI inverted	1,2,3	3
hacs2a[n]	1-bit carry select adder, COUT inverted	1,2,3	3
hacs3a[n]	1-bit carry select adder, no carry in	1,2,3	3
	Micellaneous	***2***	**5**
hld1a0	Bus hold cell	n/a	1
filler	Core filler cell	"1", "2", "4", "8"	4
TOTAL CELLS			**662**
TOTAL FUNCTIONS			**125**

DOCUMENTATION

Electronic databooks

Standard cell databook
I/O databook (TSMC)
Memories:
ProMA Compiler General Datasheet
Single-port RAM General Datasheet
Dual-port RAM General Datasheet
Note: memory instance specific datasheets are generated by ProMA Compiler (html and text)

Application notes

SSO Guidelines for TSMC 973g library
Power Routing Guidelines (DesignWare Silicon Libraries for TSMC 0.18µm/1.8V process)
Apollo Place & Route Application Note
Design Procedure with Silicon Ensemble Using the DesignWare Silicon Library
DesignWare ProMA Memories Power Routing

Layer name	Purpose	Stream	Datatype
ref	drawing	0	0
PWELL	drawing	1	0
NWELL	drawing	2	0
DIFF	drawing	3	0
PDIFF	drawing	11	0
NDIFF	drawing	12	0
OD2	drawing	4	0
POLY1	drawing	13	0
POLY2	drawing	14	0
POLY3	drawing	9	0
POLY4	drawing	10	0
N2V	drawing	61	0
N3V	drawing	5	0
N5V	drawing	6	0
PIMP	drawing	7	0
NIMP	drawing	8	0
PH	drawing	35	0
ESD	drawing	30	0
ESD5V	drawing	36	0
RPO	drawing	34	0
CONT	drawing	15	0
METAL1	drawing	16	0
VIA12	drawing	17	0
METAL2	drawing	18	0
VIA23	drawing	27	0
METAL3	drawing	28	0
VIA34	drawing	29	0
METAL4	drawing	31	0
VIA45	drawing	32	0
METAL5	drawing	33	0
VIA56	drawing	39	0
METAL6	drawing	38	0
VIA67	drawing	21	0
METAL7	drawing	22	0
PAD	drawing	19	0
For MIXED-MODE purpose			
BPI	drawing	20	0
VTP	drawing	23	0
VTN	drawing	24	0
VTDP	drawing	25	0
VTDN	drawing	26	0
COW	drawing	47	0
LPP	drawing	48	0
CTM2	drawing	67	2
CTM3	drawing	67	3
CTM4	drawing	67	4
CTM5	drawing	67	5
NTN	drawing	129	0
For P&R purpose			
prBoundary	drawing	62	0
For Pin Text Purpose			
METAL1	pin	40	0

Layer name	Purpose	Stream	Datatype
ref	drawing	0	0
PWELL	drawing	1	0
METAL2	pin	41	0
METAL3	pin	42	0
METAL4	pin	43	0
METAL5	pin	44	0
METAL6	pin	45	0
METAL7	pin	46	0
Dummy layers for LVS/DRC checking			
BJTDUMMY	drawing	49	0
PSUB2	drawing	50	0
HOTWL	drawing	51	0
RWDUMMY	drawing	52	0
RPDUMMY	drawing	54	0
RMDUMMY	drawing	69	0
VCDUMMY	drawing	53	0
CDUMMY	drawing	68	0
DIODUMMY	drawing	56	0
PTDIODE	drawing	37	0
EXCL	drawing	55	0
TRAN	drawing	57	0
SDI	drawing	58	0
TEXT	drawing	59	0
DRCDUMMY	drawing	60	0
DPDUMMY	drawing	65	0
PLDUMMY	drawing	66	0
DRC error report layers			
marker	error	63	0
marker	warning	64	0
For SRAM process			
CELLIMP	drawing	70	0
BC1	drawing	71	0
BC2	drawing	72	0
BTC	drawing	73	0
VCC	drawing	74	0
RODUMMY	drawing	75	0
ESEXCL	drawing	76	0
CPDUMMY	drawing	77	0
PDIMP	drawing	78	0
PUIMP	drawing	79	0
For DRAM Process			
CELLBRC1	drawing	80	0
BLBRC2	drawing	81	0
DNWELL	drawing	82	0
P1W	drawing	83	0
P1R	drawing	84	0
SAC	drawing	85	0
C1	drawing	86	0
C2	drawing	87	0
DPITCH	drawing	88	0
PLMIDE	drawing	89	0