

Generator-Based Design of a Radiation Hardened Timing-Based Sensor Frontend for Space

Lydia Lee

Advisor: Kristofer Pister

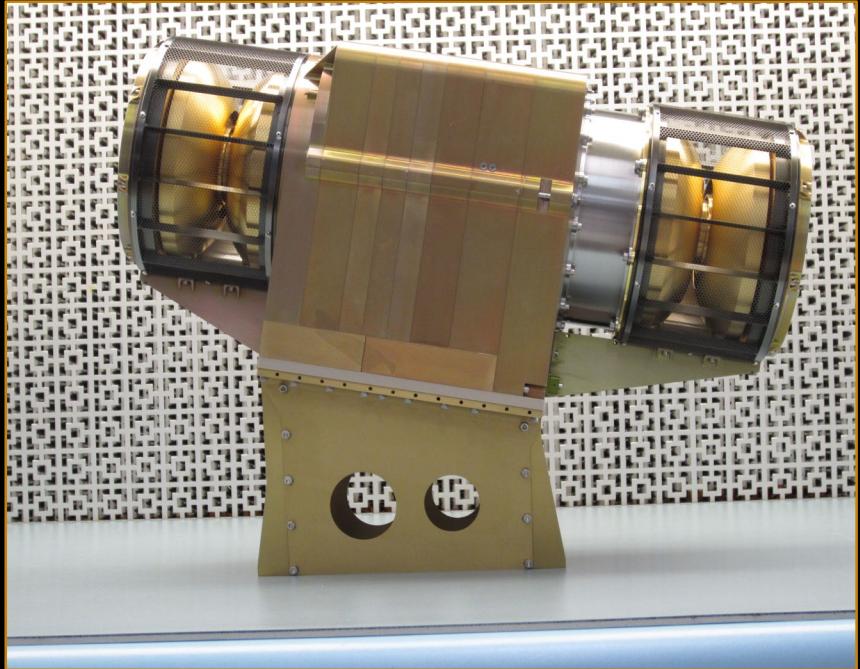
1. Background and Motivation

2. Prior and Ongoing Work

- a. Accounting for Radiation Effects
- b. Analog to Digital Pulse Conversion
- c. Circuit Design and Automation

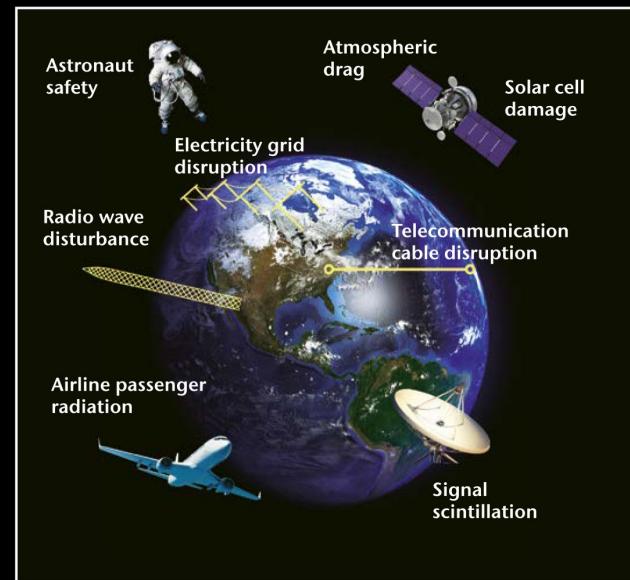
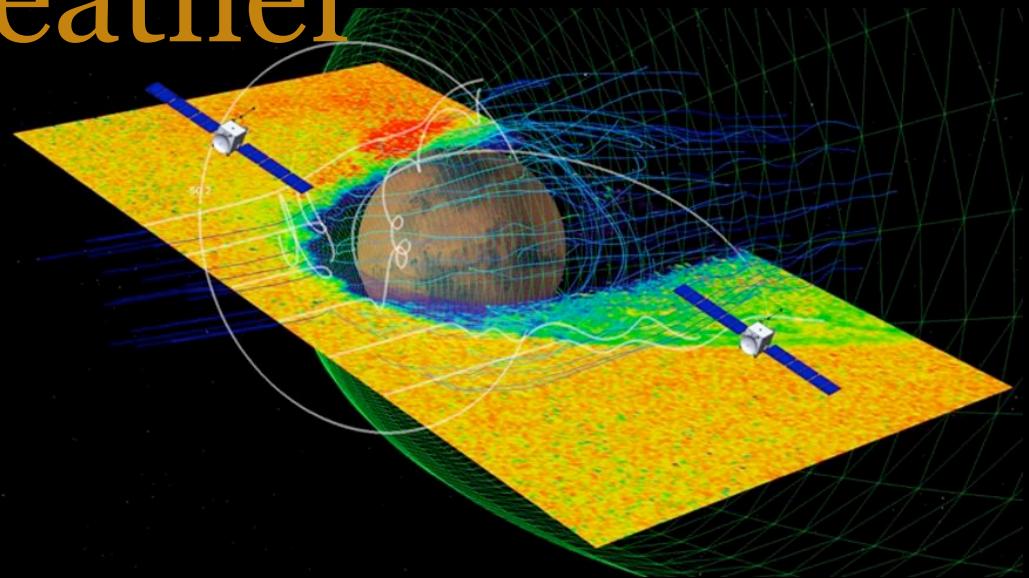
3. Future and Proposed Work

SPAN-Ion and Space Weather



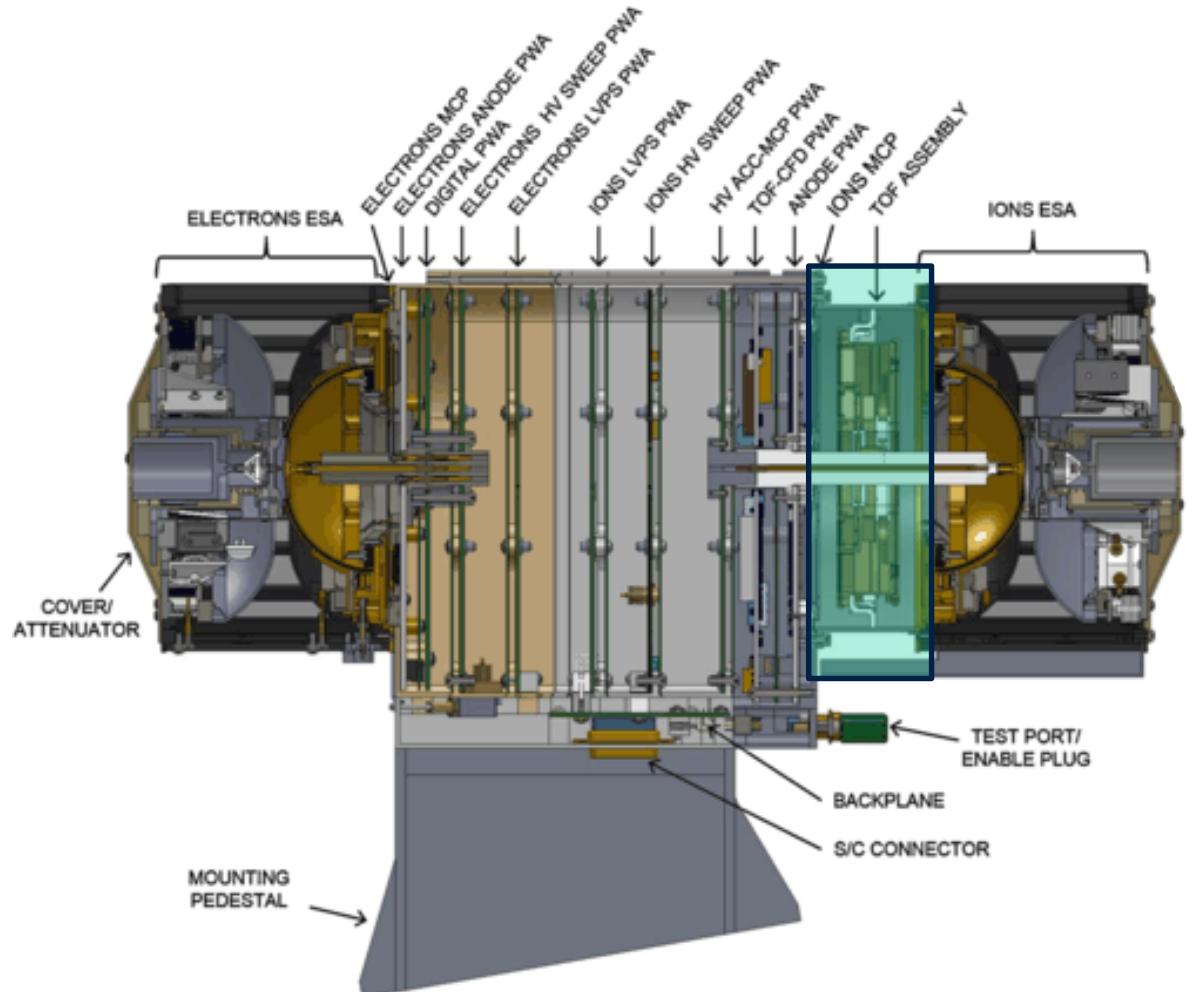
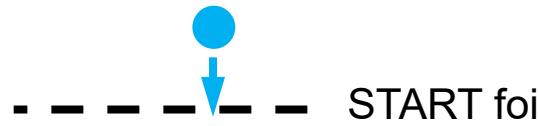
Instrument: Solar Probe Analyzer for Ions

Measures: Ion composition and 3D distribution of solar wind plasma (positively charged ions)



SPAN-Ion Mass Spec

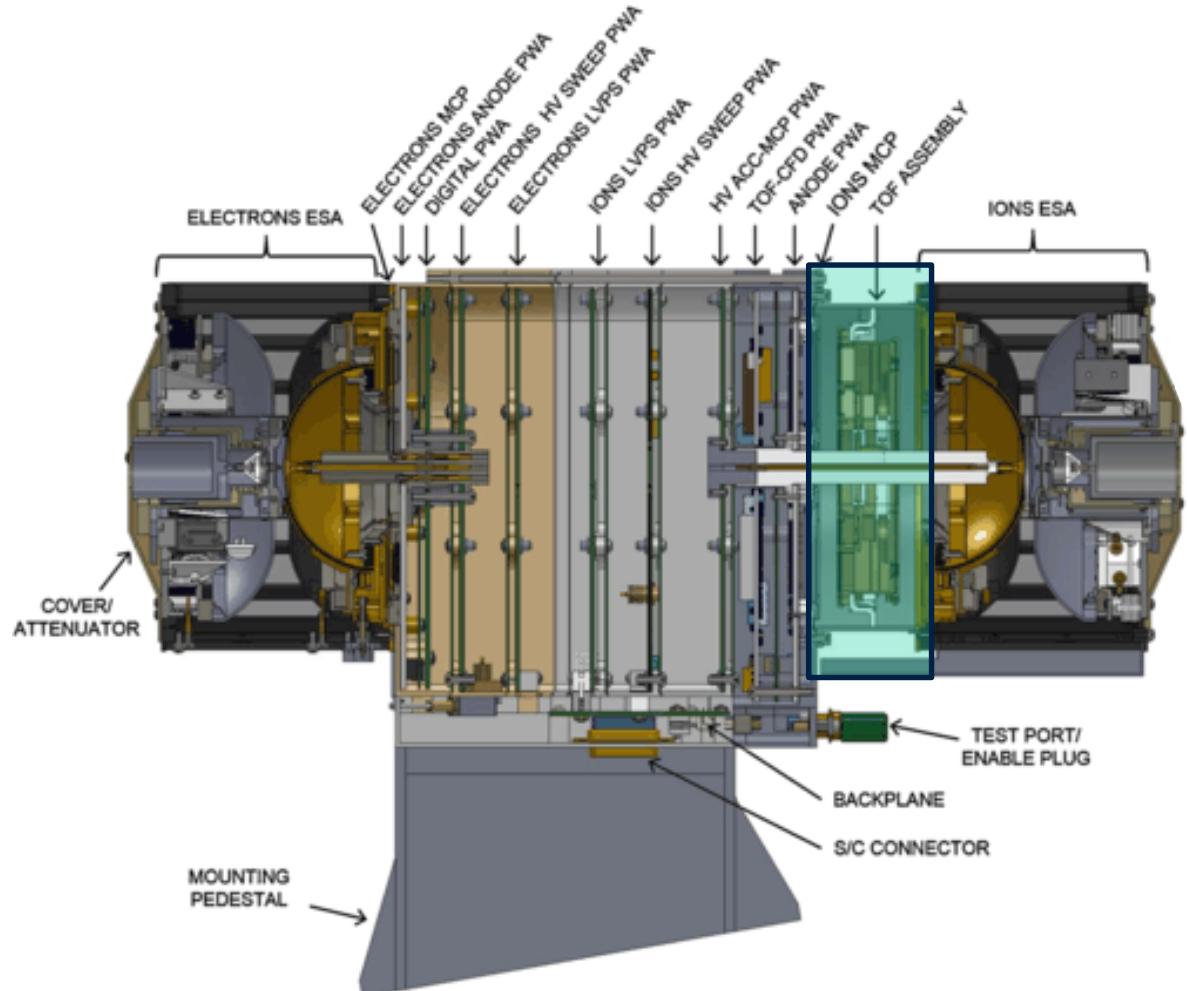
$$qV = \frac{1}{2}m\dot{x}^2$$



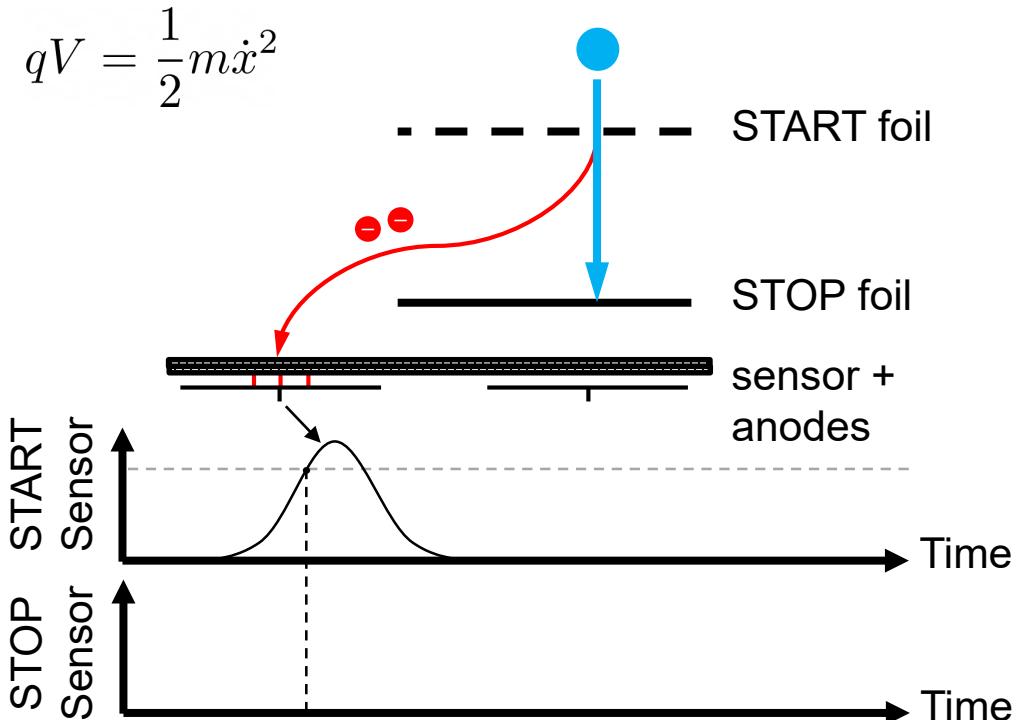
[1]

[1] Kasper, J.C., Abiad, R., Austin, G. et al. Solar Wind Electrons Alphas and Protons (SWEAP) Investigation: Design of the Solar Wind and Coronal Plasma Instrument Suite for Solar Probe Plus. *Space Sci Rev* 204, 131–186 (2016). <https://doi.org/10.1007/s11214-015-0206-3>

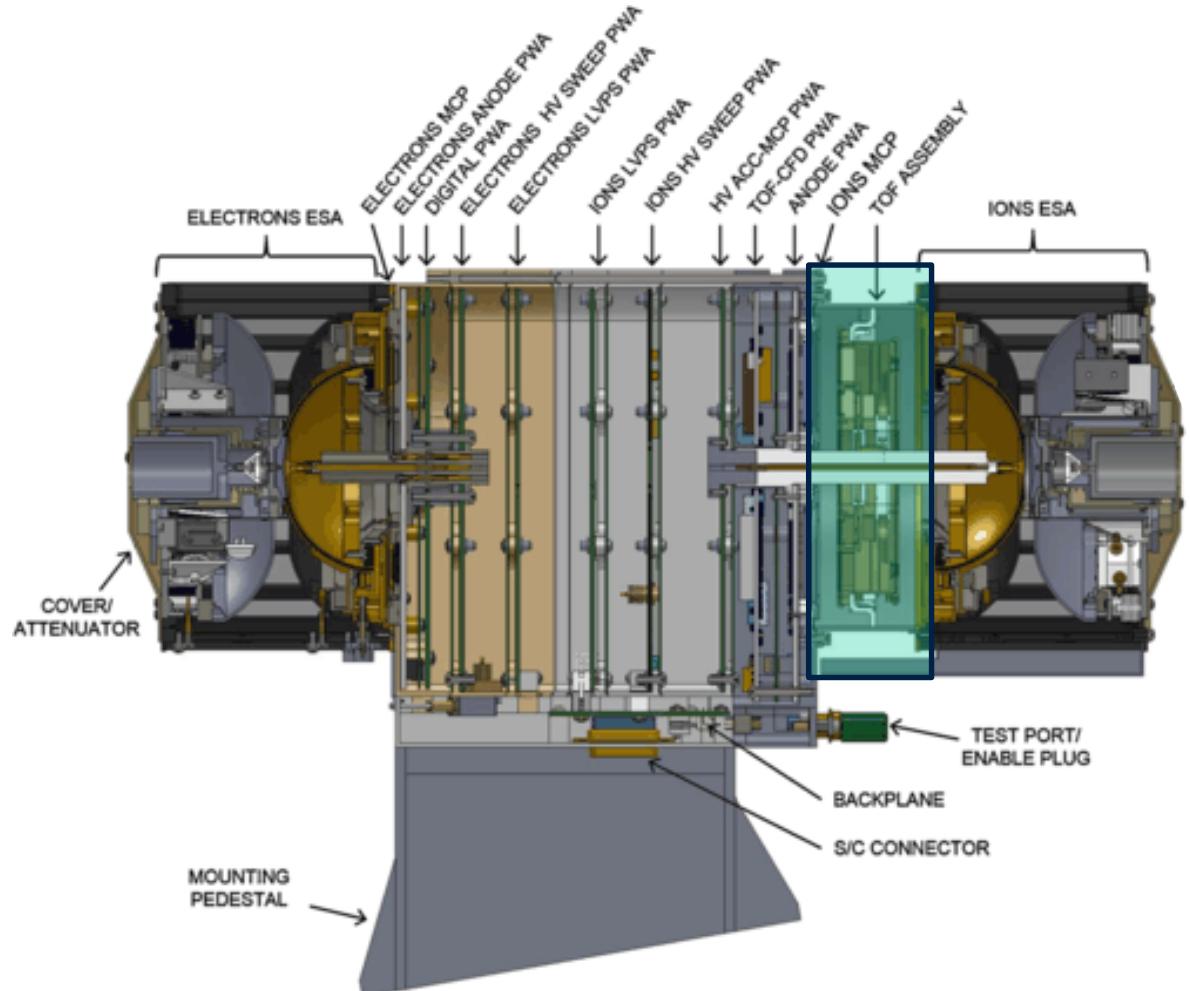
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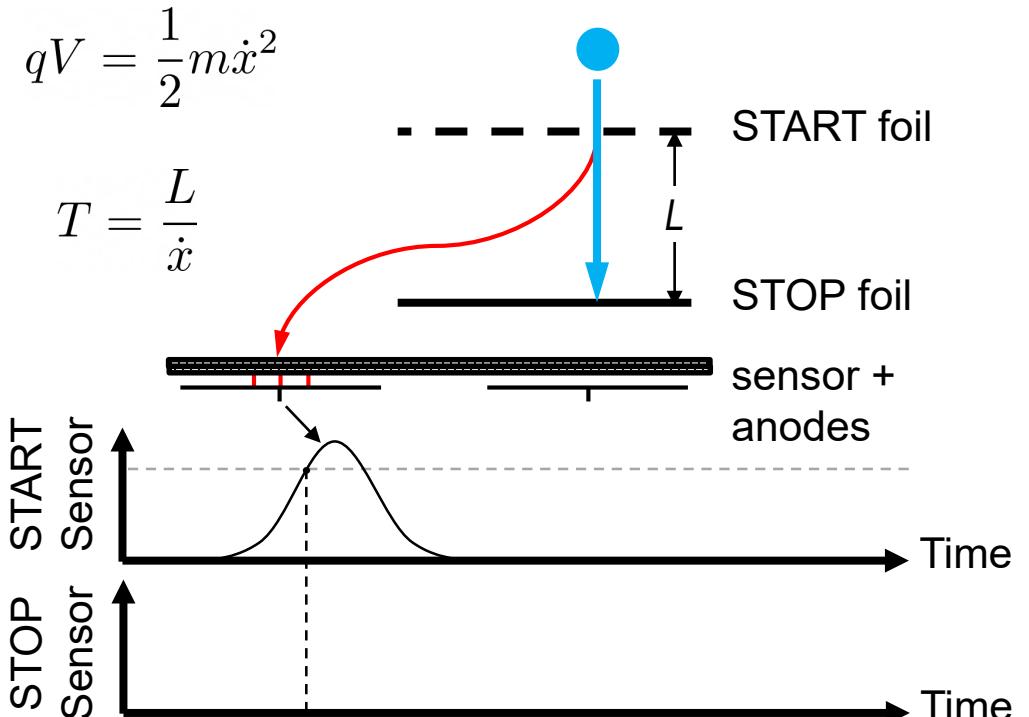
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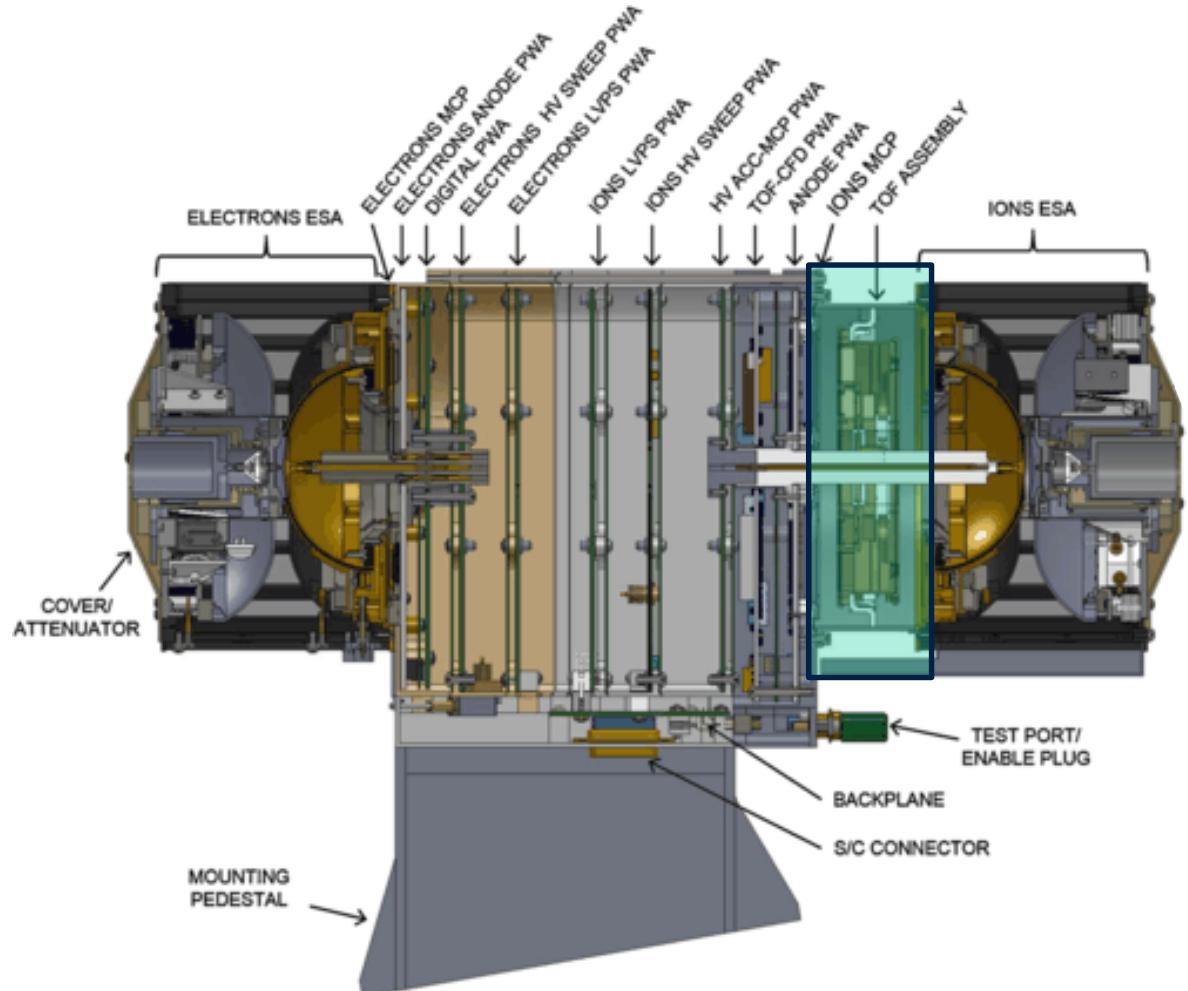
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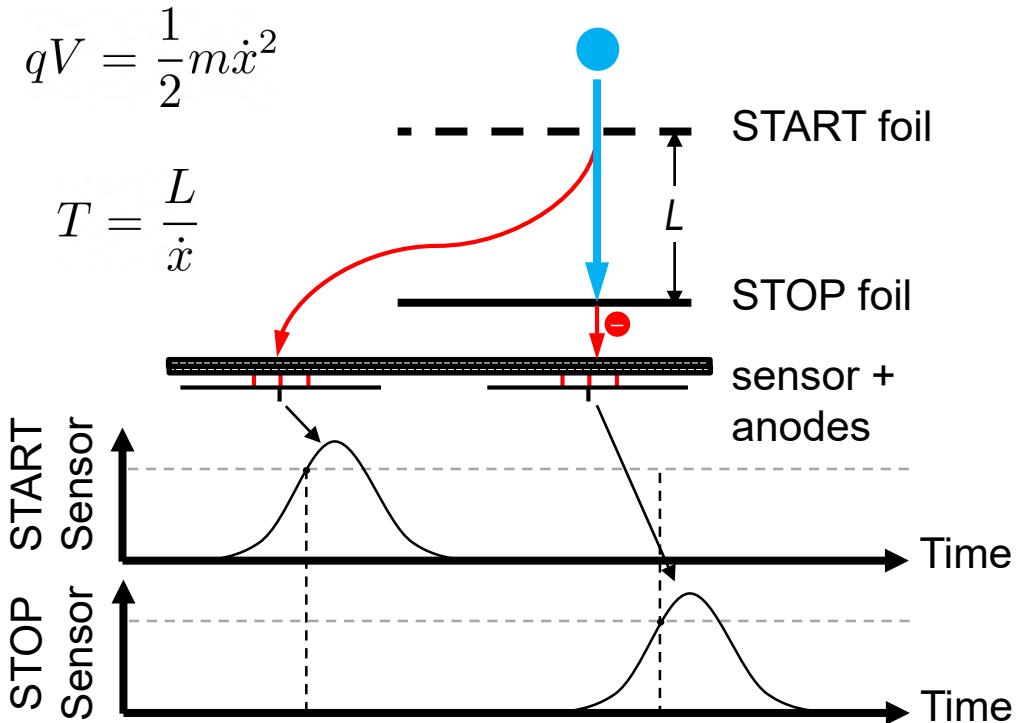
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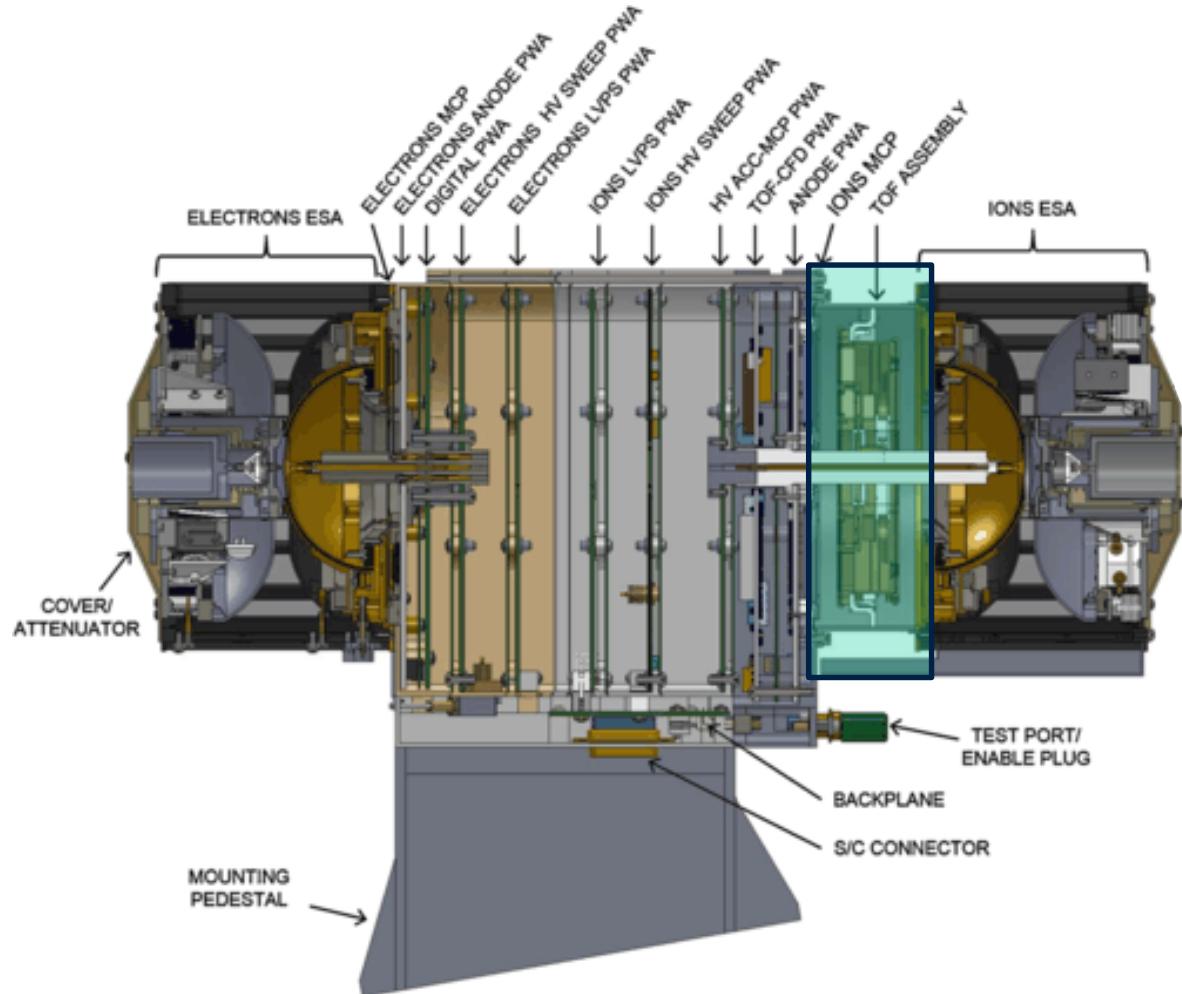
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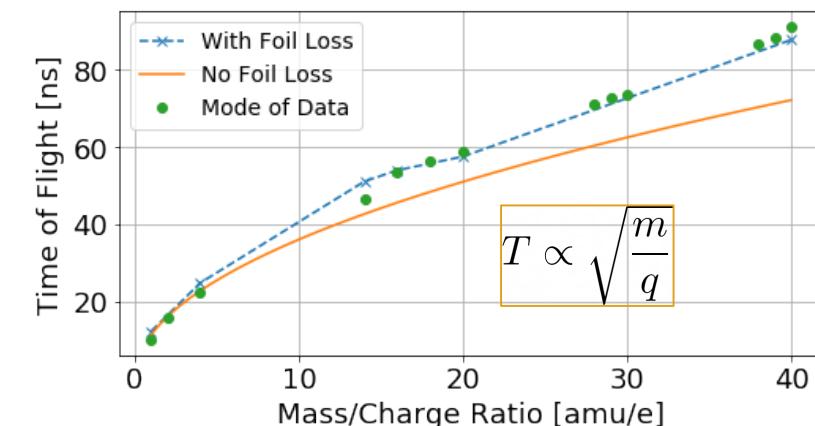
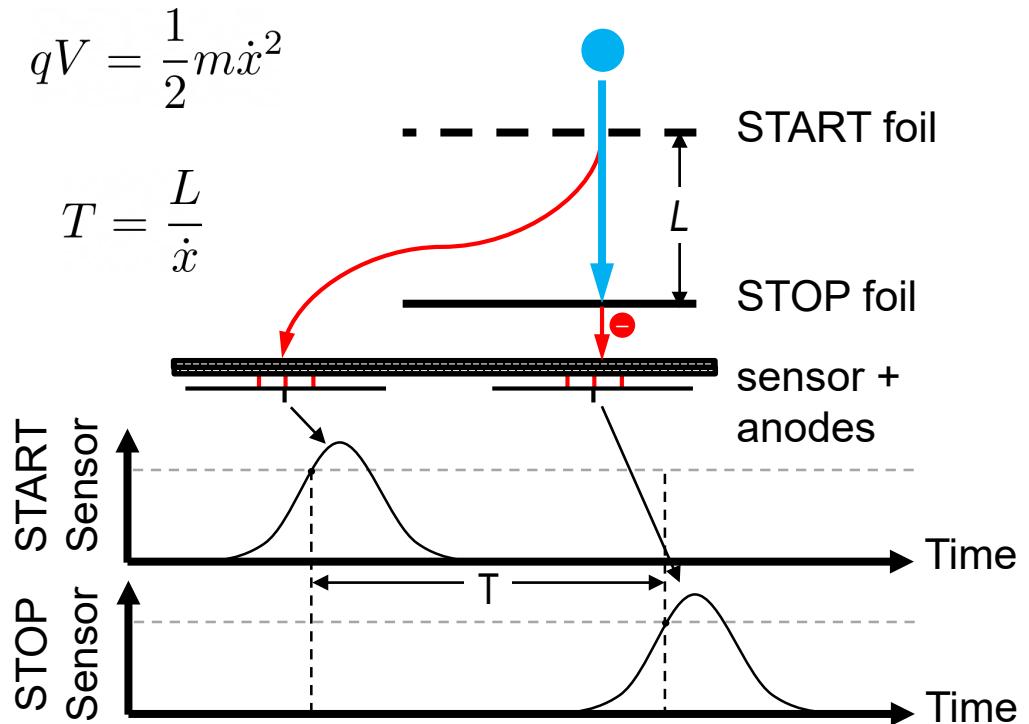
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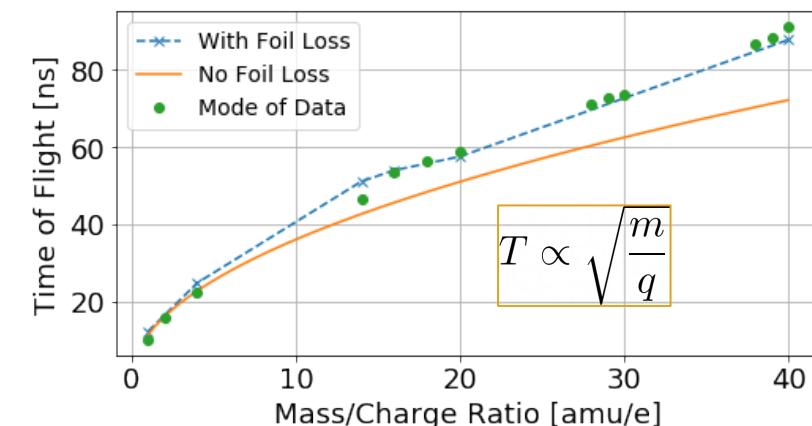
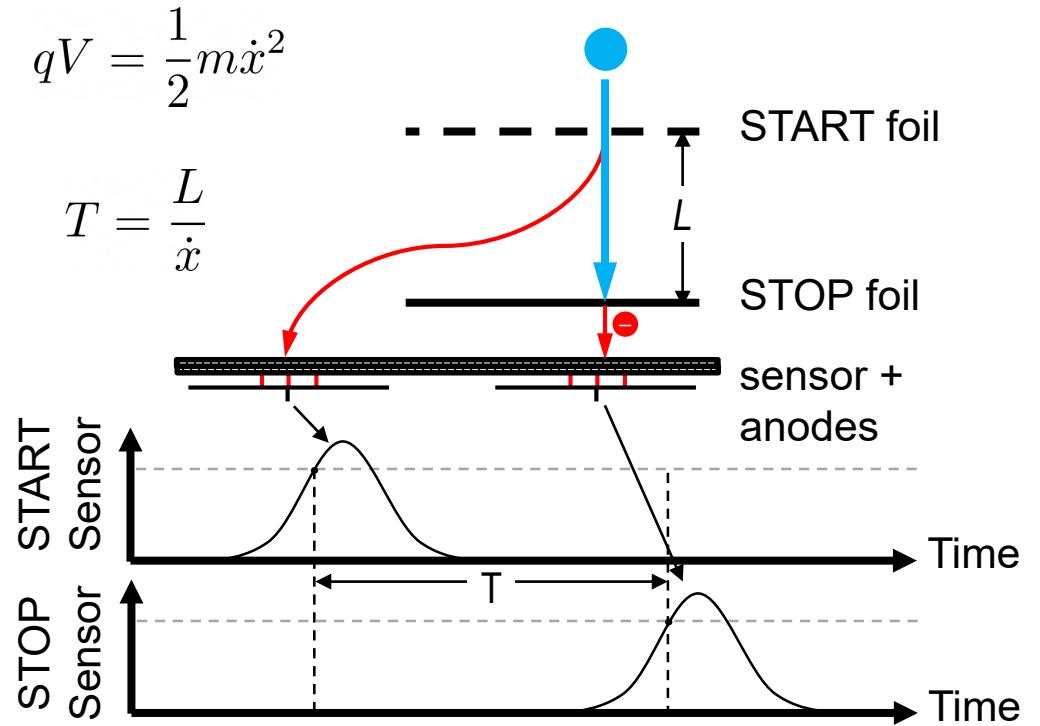
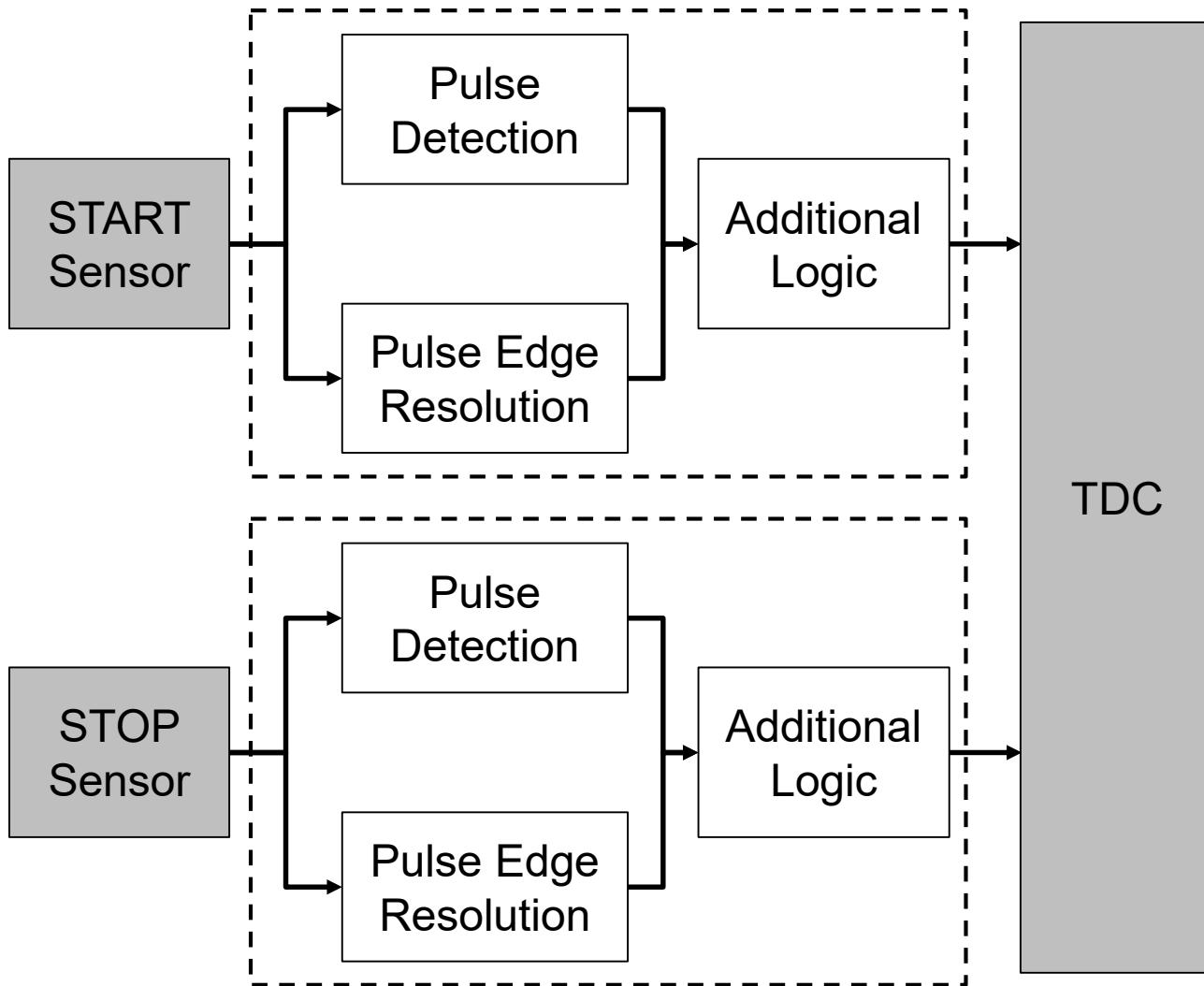
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SPAN-Ion Mass Spec



Hardware Reuse in Space

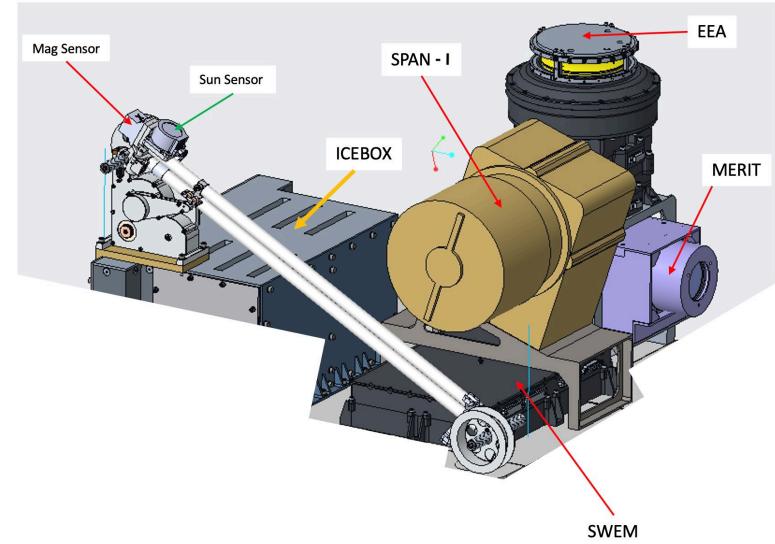


MAVEN STATIC



PSP (SPAN-I V1)

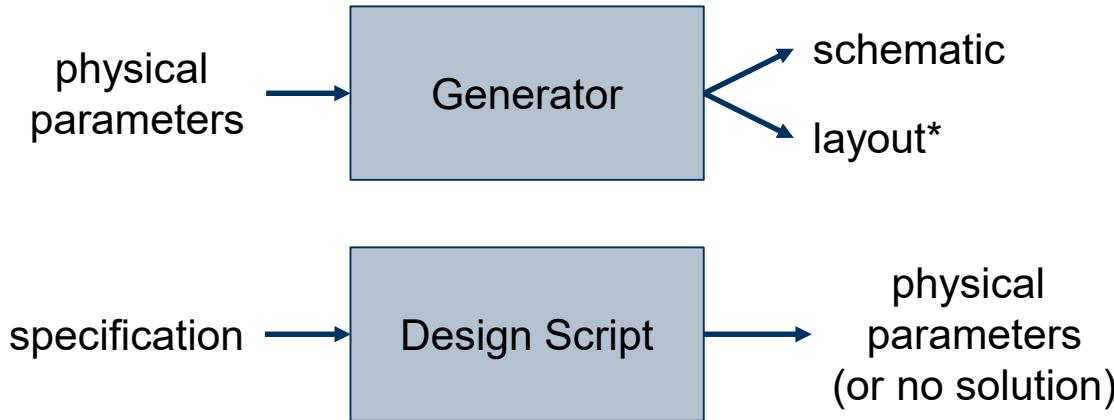
- Same mechanical setup
- APL ASIC for constant fraction discriminator



HERMES/EscapADE (SPAN-I V2)

- Same mechanical setup
- Sensor changed for higher throughput; ASIC needs redesign

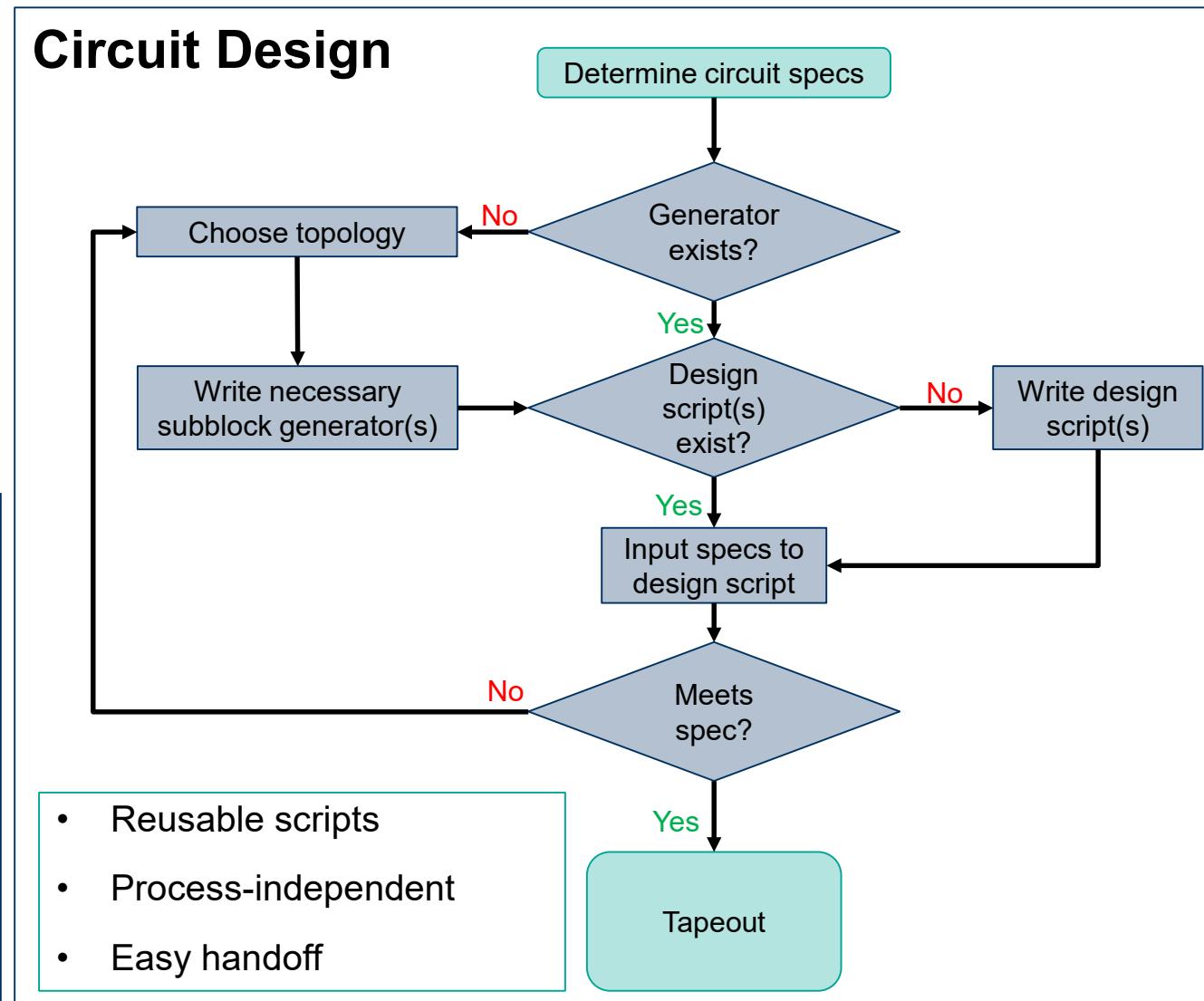
BAG Design Flow



Single-Chip Mote Optical Programming

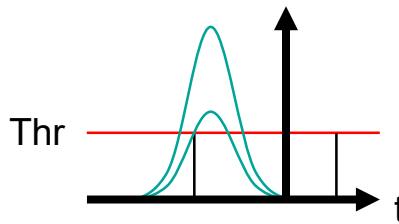


	RX V1	RX V2	Lighthouse
Irrad.	>1.5mW/mm ²	<20μW/mm ²	<10μW/mm ²
BER	6(10 ⁻⁴)	2(10 ⁻⁸)	10 ⁻³
Yield	Unknown	≥99% (2.6σ)	
Area	130μm×130μm		
Active Power	~1.5μW	~15μW	



Pulse Decisions and Related Works

Basic Threshold



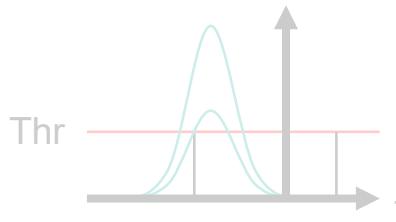
- + Extremely simple
- Significant walk

*combined constant fraction and time-over-threshold

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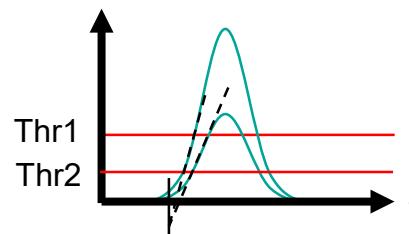
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Dual Threshold [1][2]



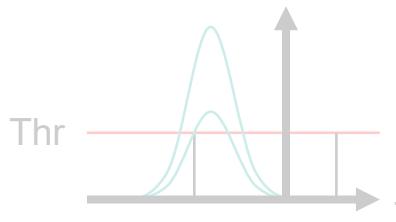
- + Flexible interpolation method can produce walk $\sim 5\text{-}10\text{ps}$
- >1 TDC channel

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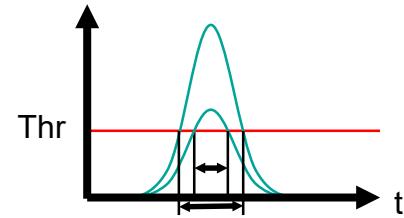
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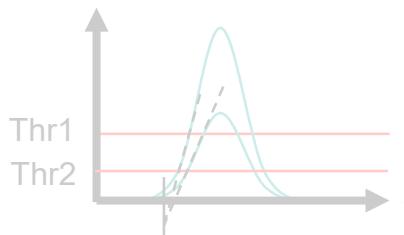
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Time Over Thresh. [3][5*]



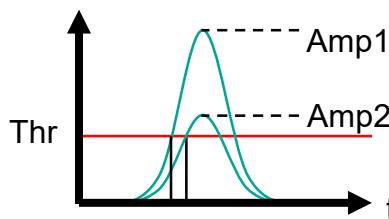
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- + Minimal extra hardware
- 1 TDC per pulse
- Requires prior pulse shape knowledge

Dual Threshold [1][2]



- + Flexible interpolation method can produce walk ~5-10ps
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TDC + Amplitude



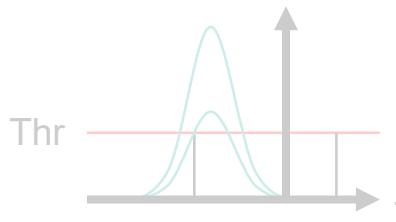
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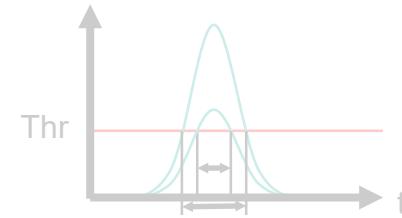
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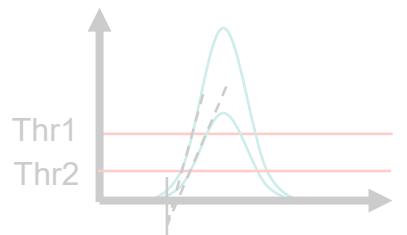
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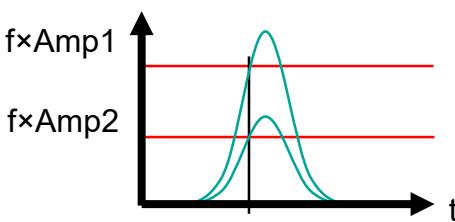
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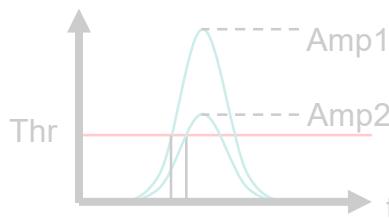
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Const. Fraction [4][5*]



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- + 1 TDC for both pulses
- Shape-dependent trigger frac.

TDC + Amplitude



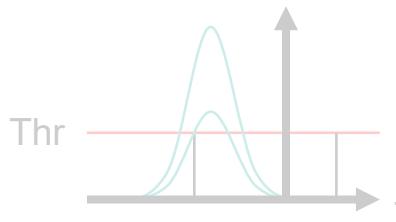
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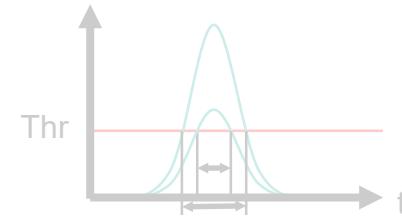
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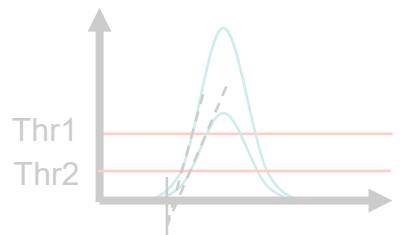
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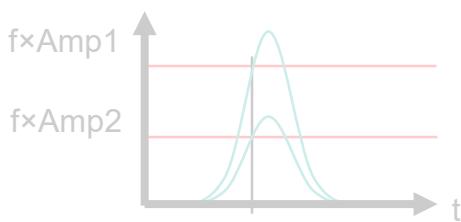
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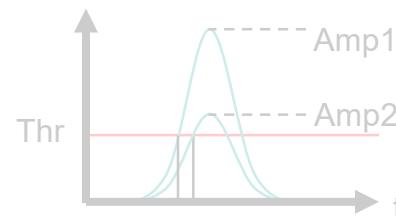
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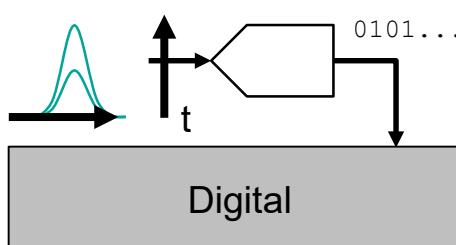
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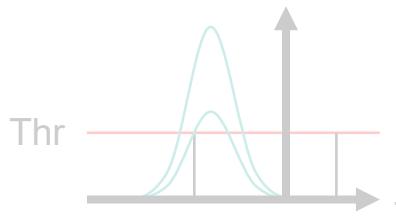
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- ADC necessarily very fast (read: power-hungry)

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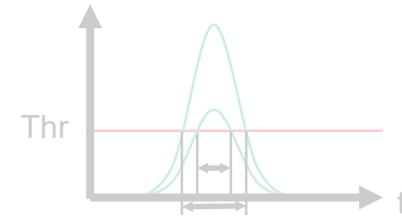
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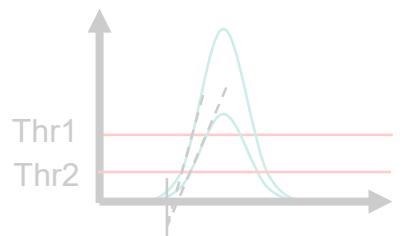
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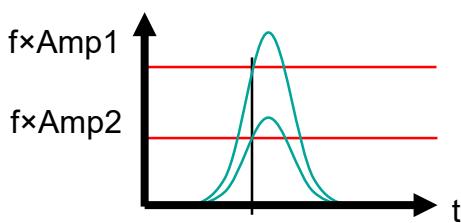
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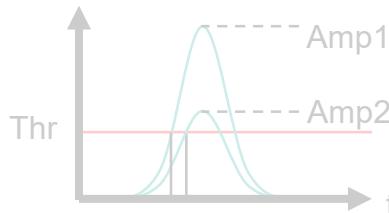
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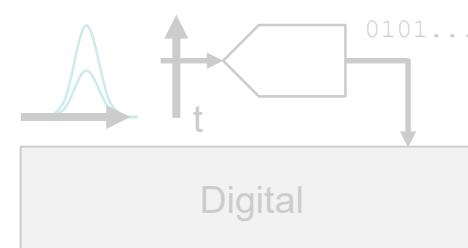
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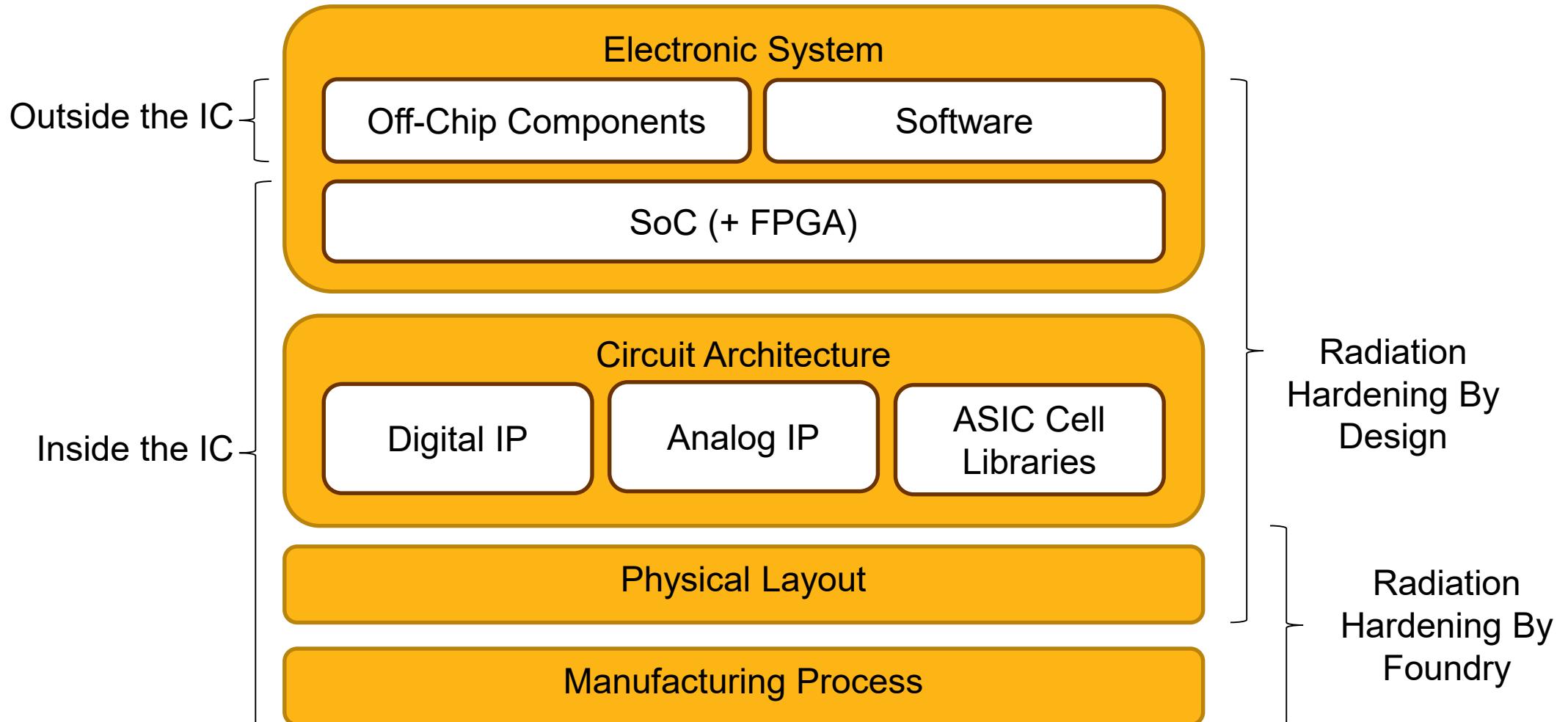
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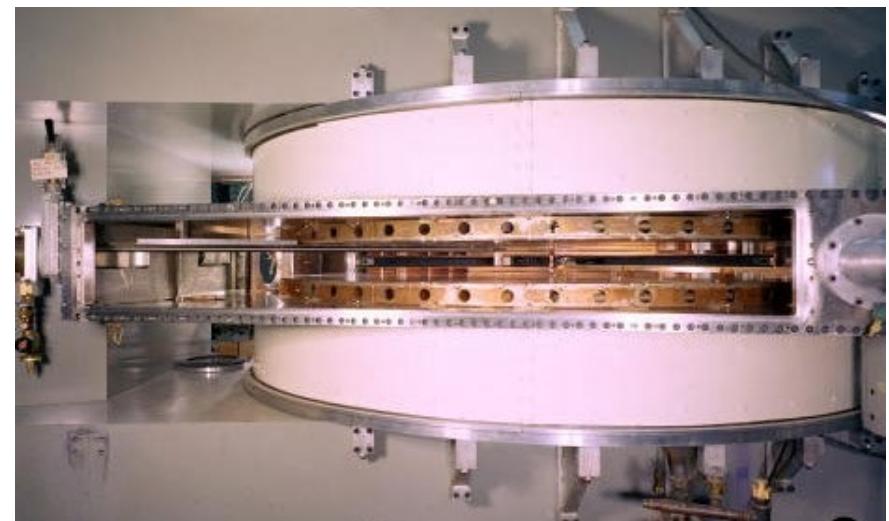
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Layers of Radiation Hardening

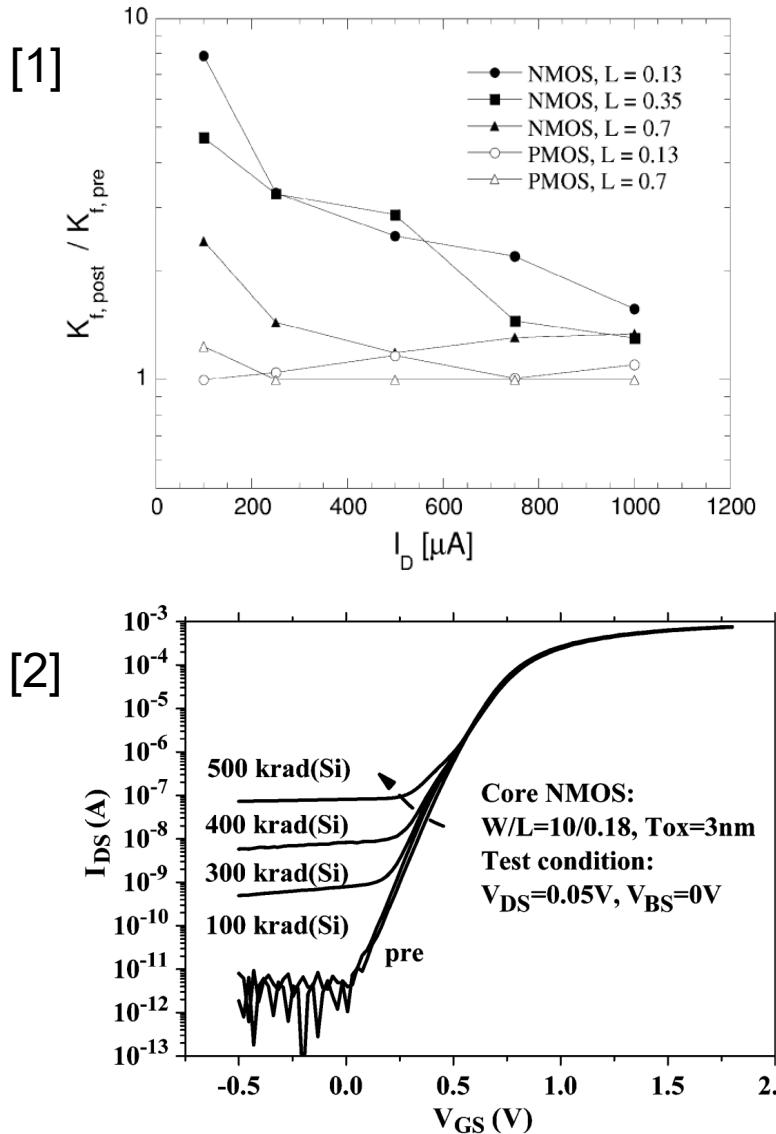


Radiation Specification

- LET [MeV.cm²/mg] = $dE/dx * 1/\rho$
- fluence [1/m²] = total # of particles through a unit area
- dose [Gy] = LET × fluence × 1.6e-7 Gy.mg/MeV
- **Total Ionizing Dose:** 100krad (Cobalt-60)
- **Single Event Effects:** 1-100MeV.cm²/mg
 - 10-1000 particles/cm² for 100krad

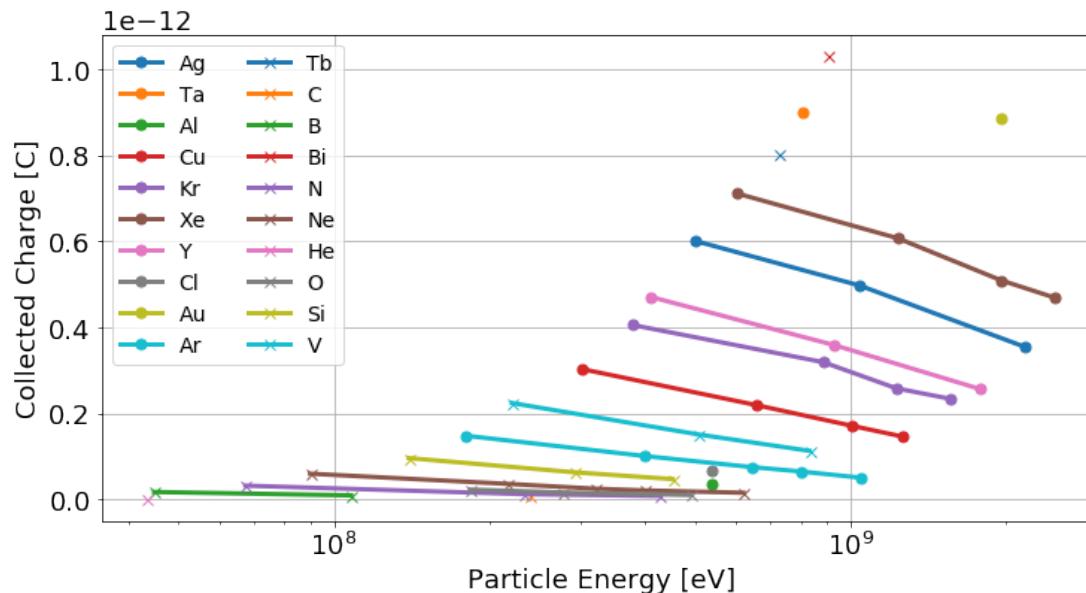
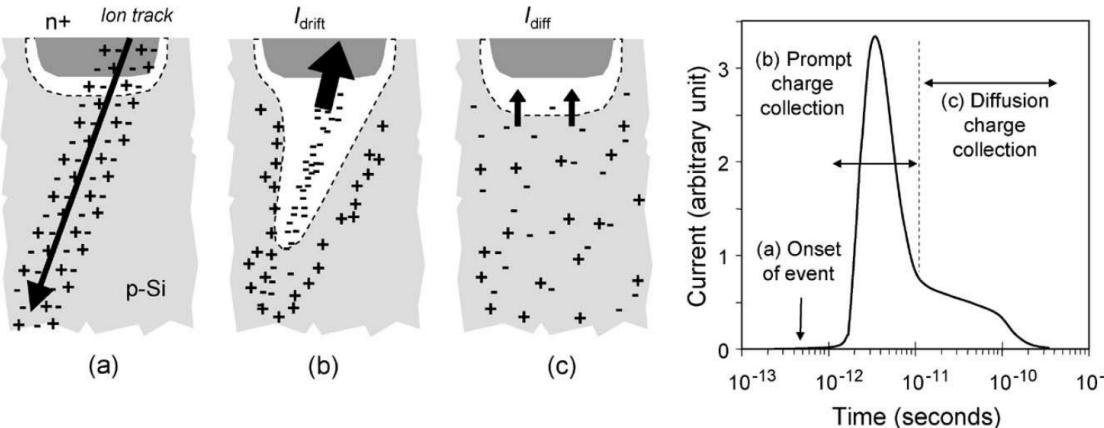


Emulating Total Ionizing Dose



- **General:**
 - FS corner (in addition to other corners of course)
 - Minimum temp 20°C lower than standard
- **MOSFETs:**
 - Inserted leakage source-to-drain current source, 2 orders of magnitude
 - Manually calculated increased flicker noise (1 order of magnitude)
 - Manual mismatch injection
- **Diodes/Bipolar:**
 - Increased junction reverse bias current by 3 orders of magnitude

Emulating Single Event Effects



$$I(t) = \frac{Q}{\tau_f - \tau_r} (e^{-t/\tau_f} - e^{-t/\tau_r})$$

- **Time constants:**
 - Rise: singles to hundreds of ps
 - Fall: tens of ps to low singles of ns
- **Sensitive Volume Depth (Si):** $\sim 1\mu\text{m}$
- **Silicon:** $\sim 3.6\text{eV/ehp}$
- Current injected via Cadence deepprobe

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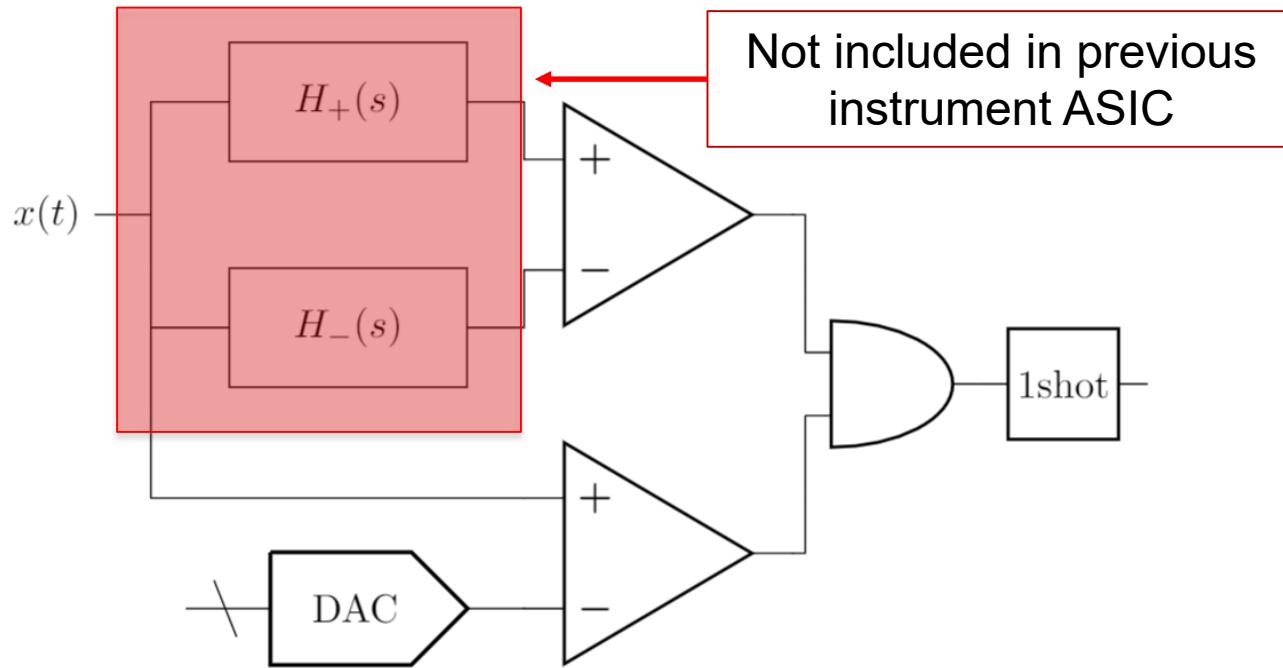
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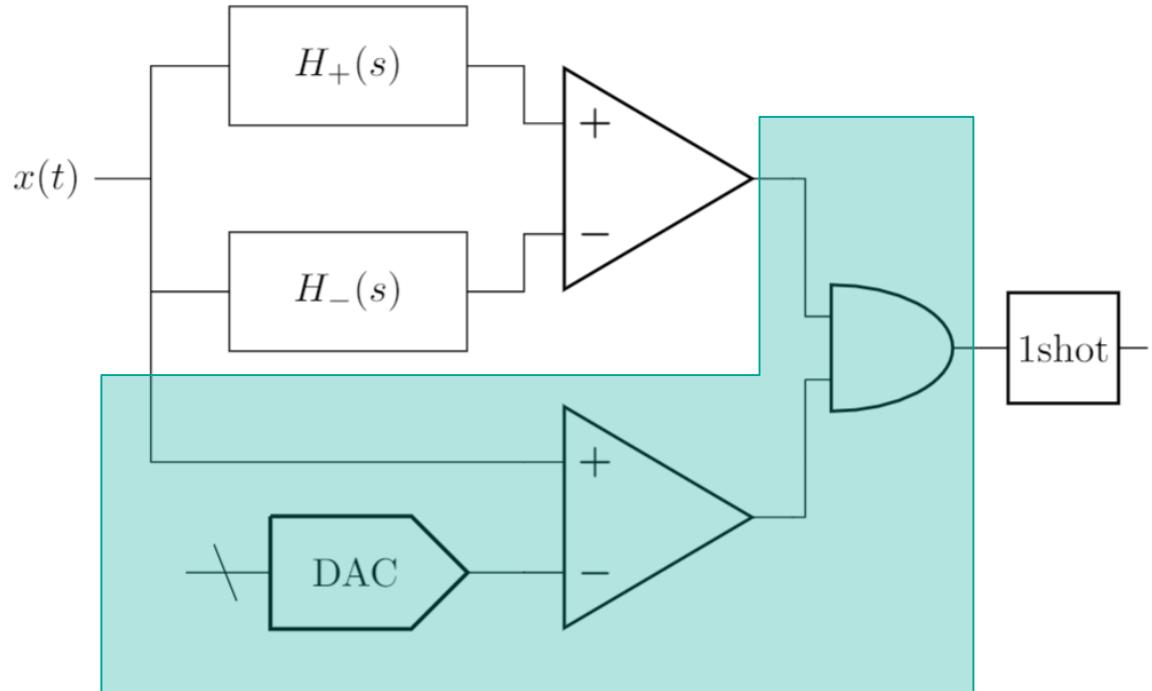
CFD Architecture

- Avoid triggering on noise
- <2 output triggers per event
- Monotonically increasing count rate vs. event rate
- No clipping
- Tunable trigger fraction



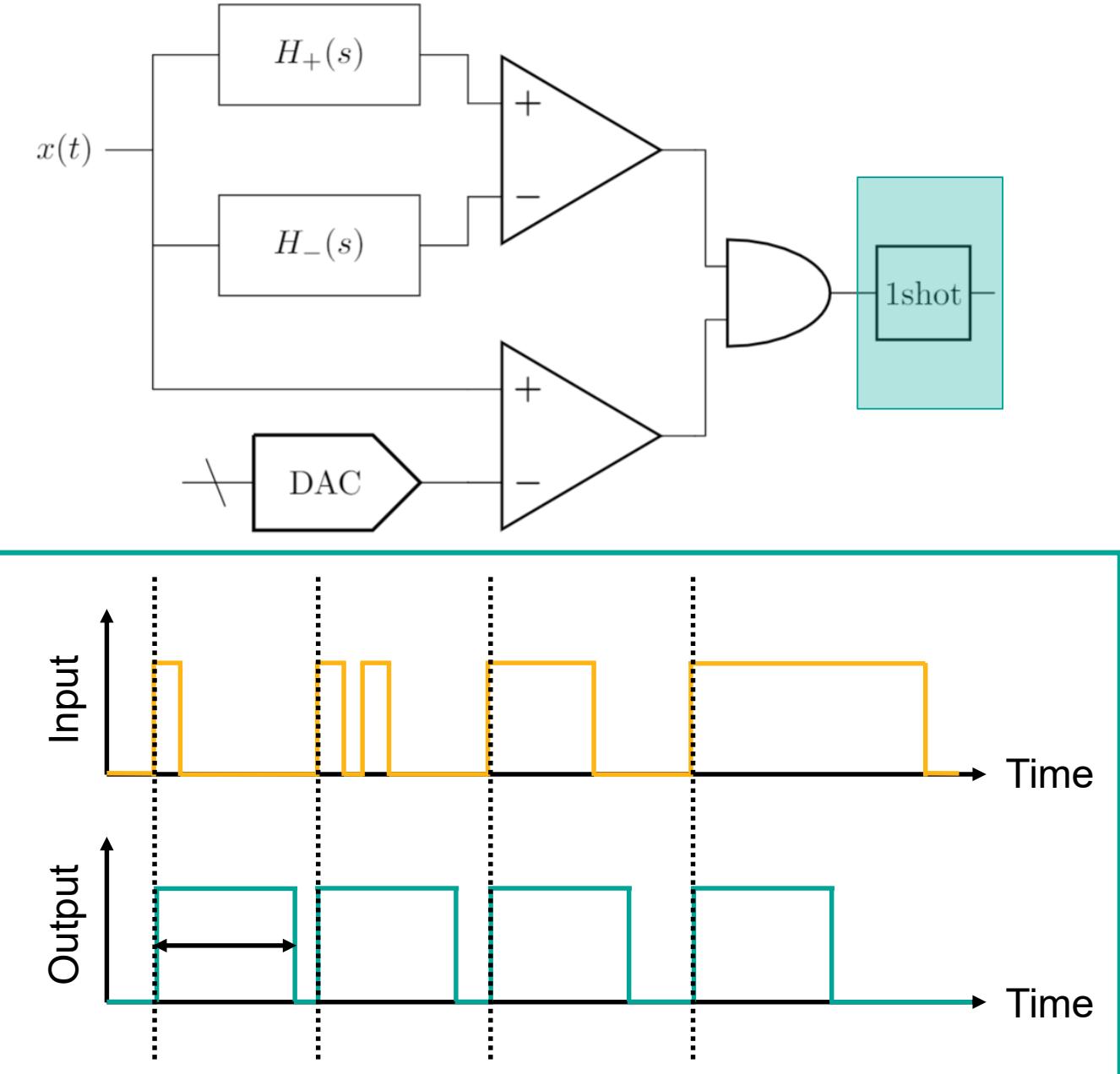
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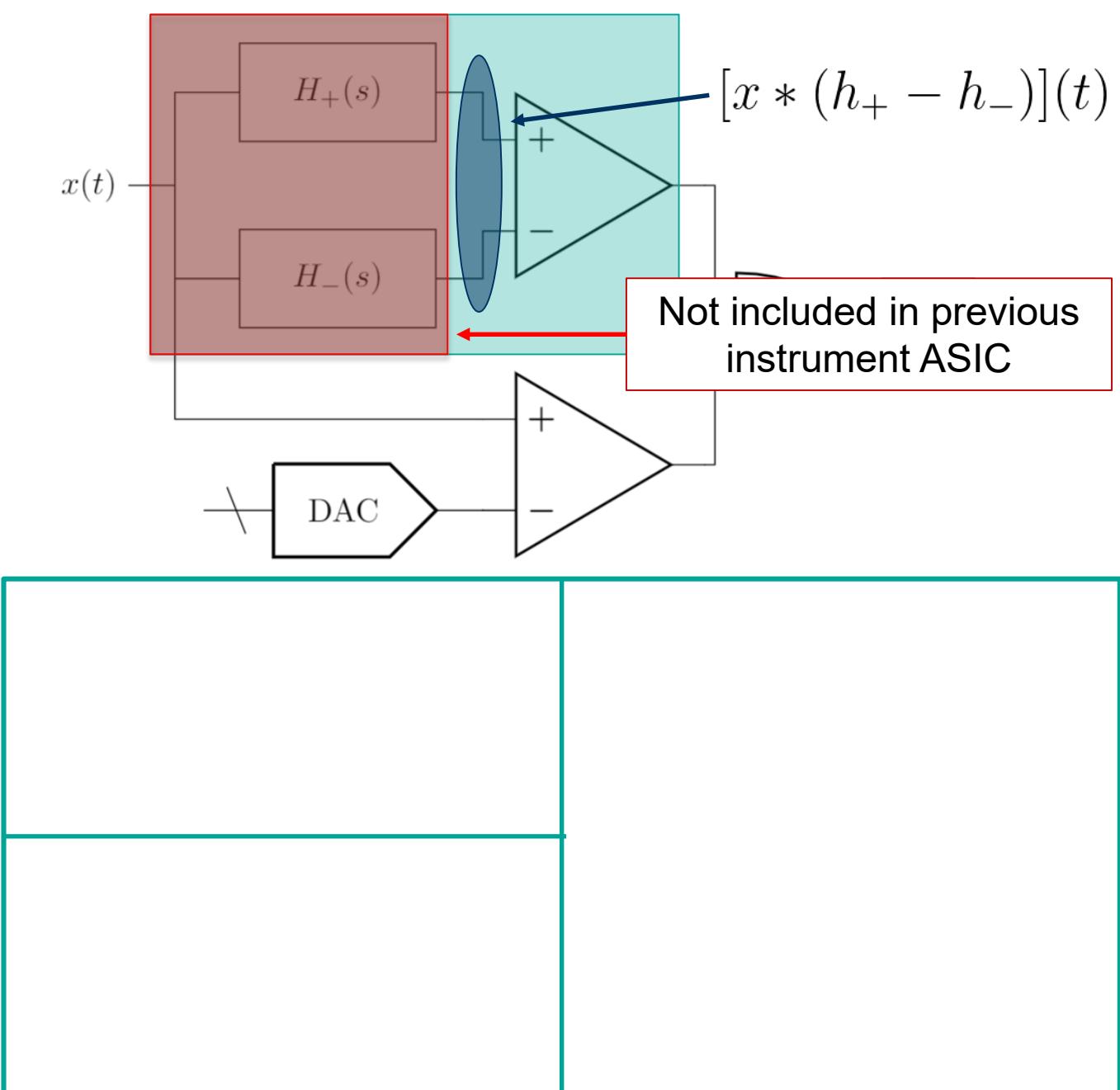
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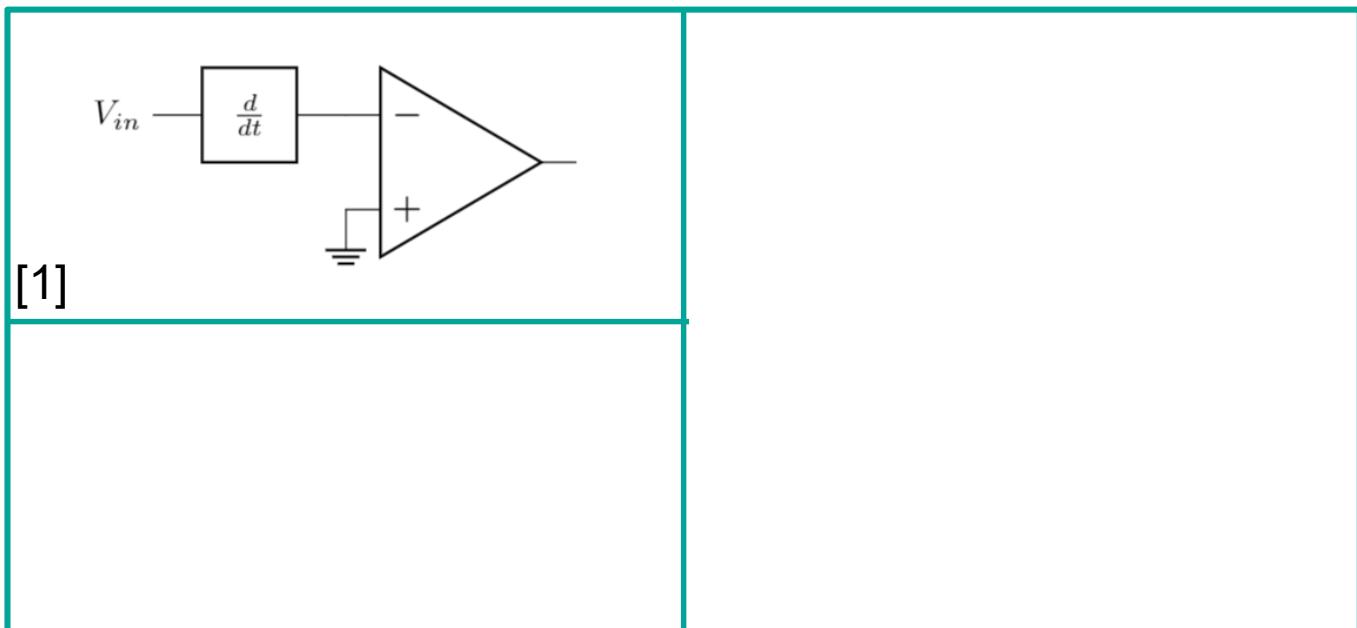
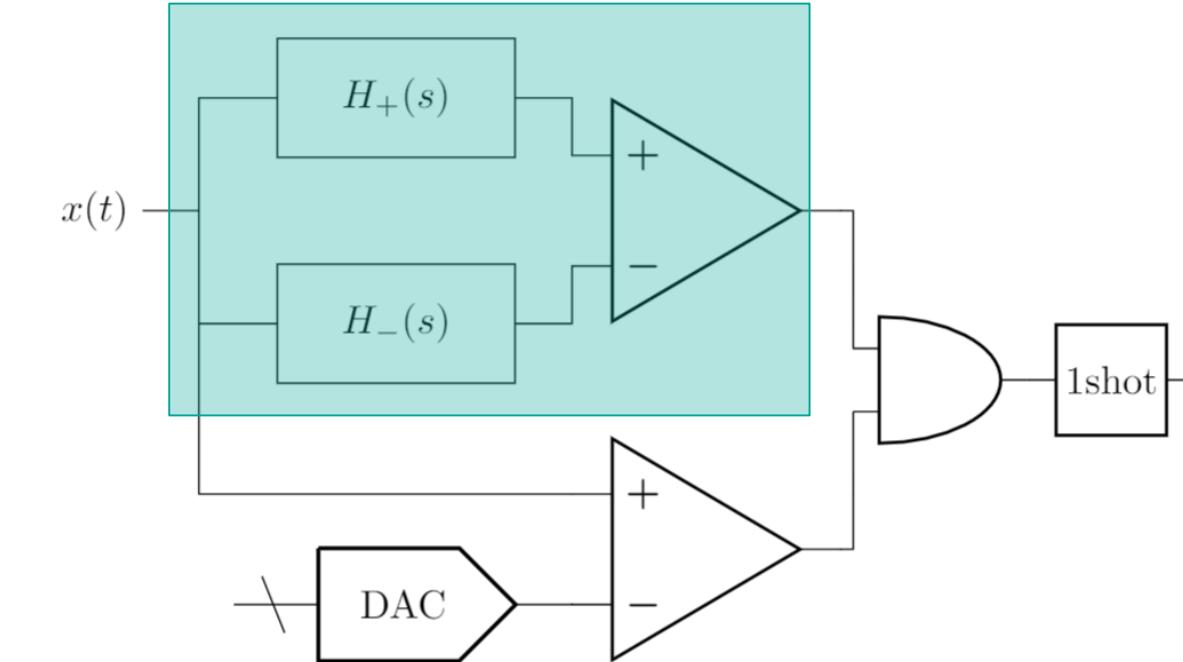
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- No clipping



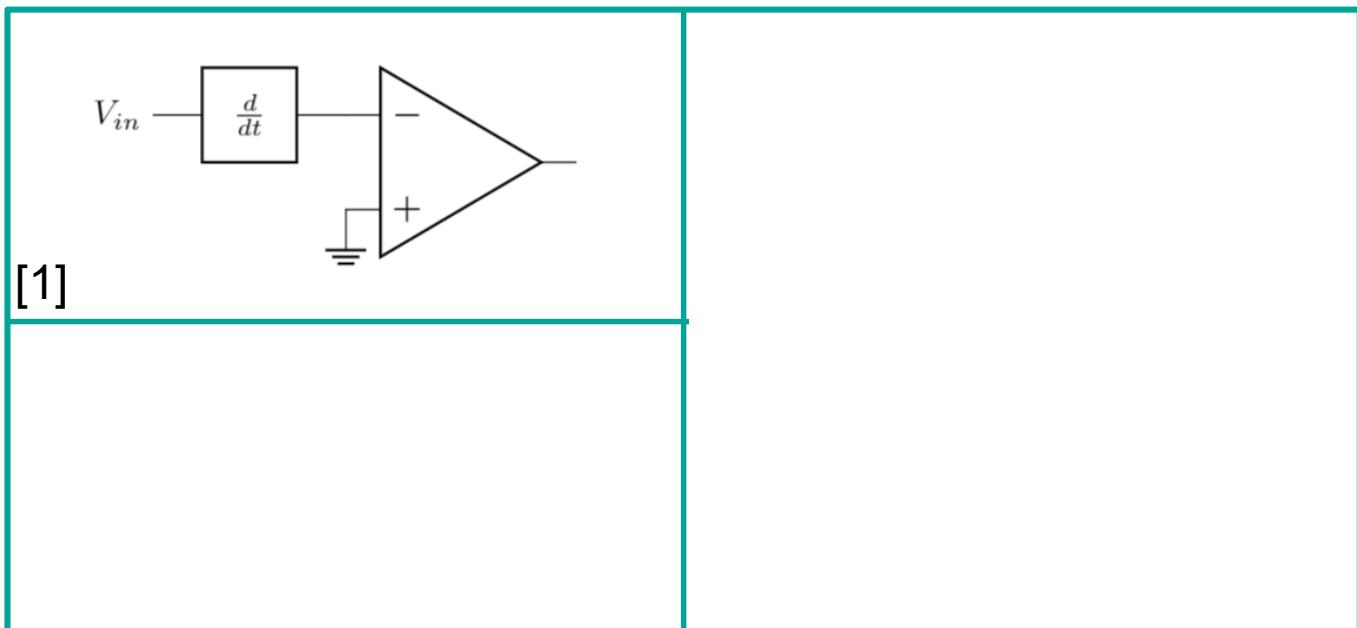
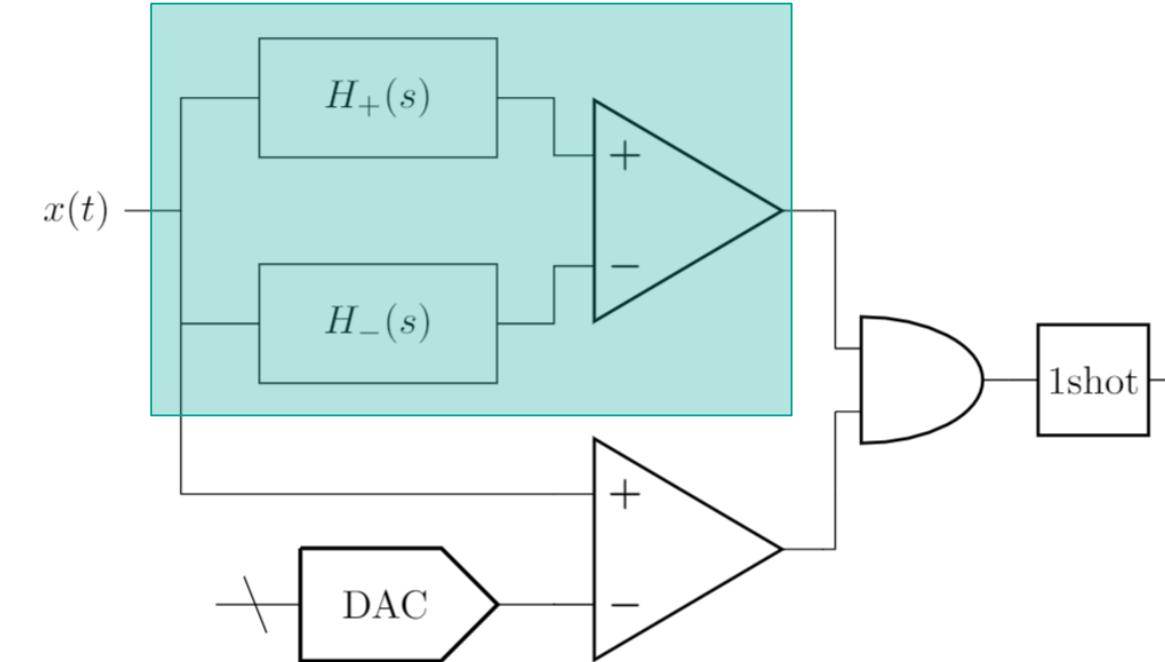
CFD Architecture

- Avoid triggering on noise
- <2 output triggers per event
- Monotonically increasing count rate vs. event rate
- Tunable trigger fraction
- No clipping



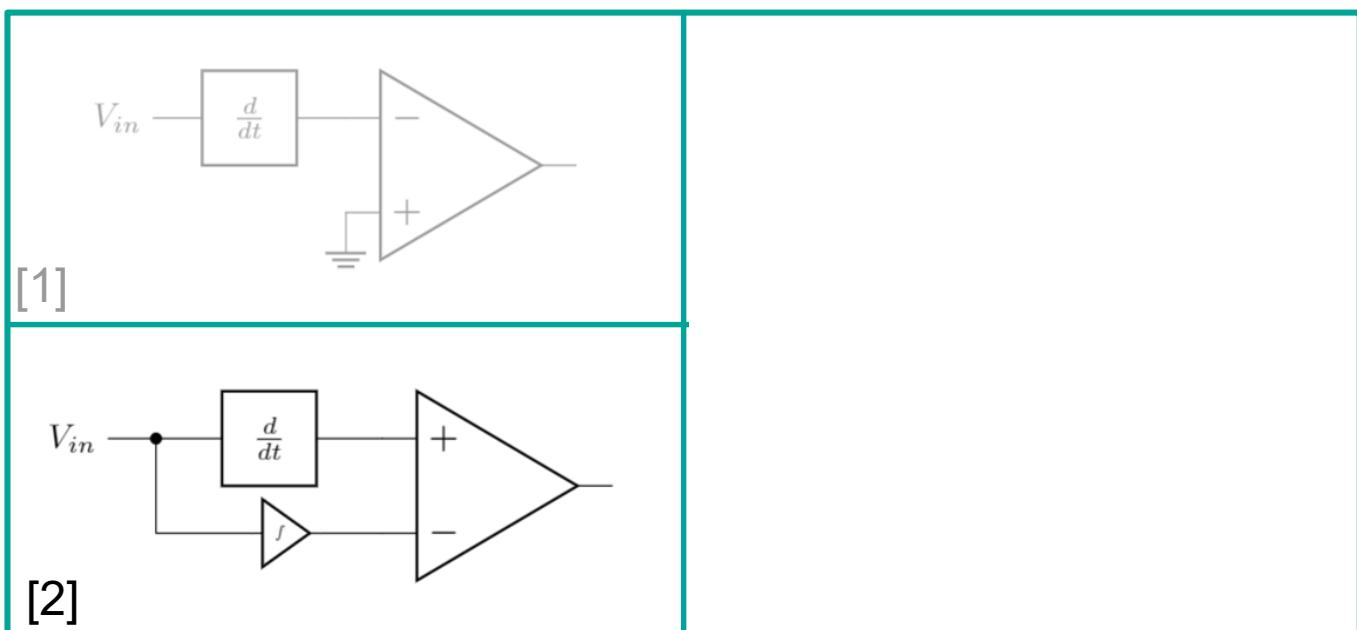
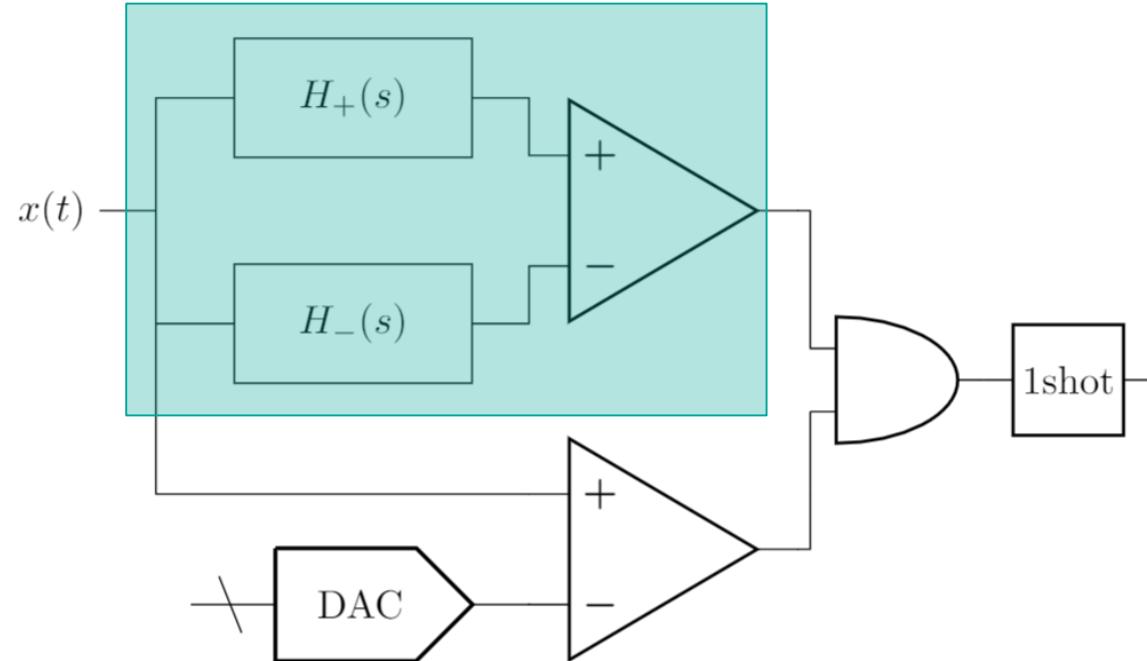
CFD Architecture

- Avoid triggering on noise
- <2 output triggers per event
- Monotonically increasing count rate vs. event rate
- Tunable trigger fraction
- No clipping



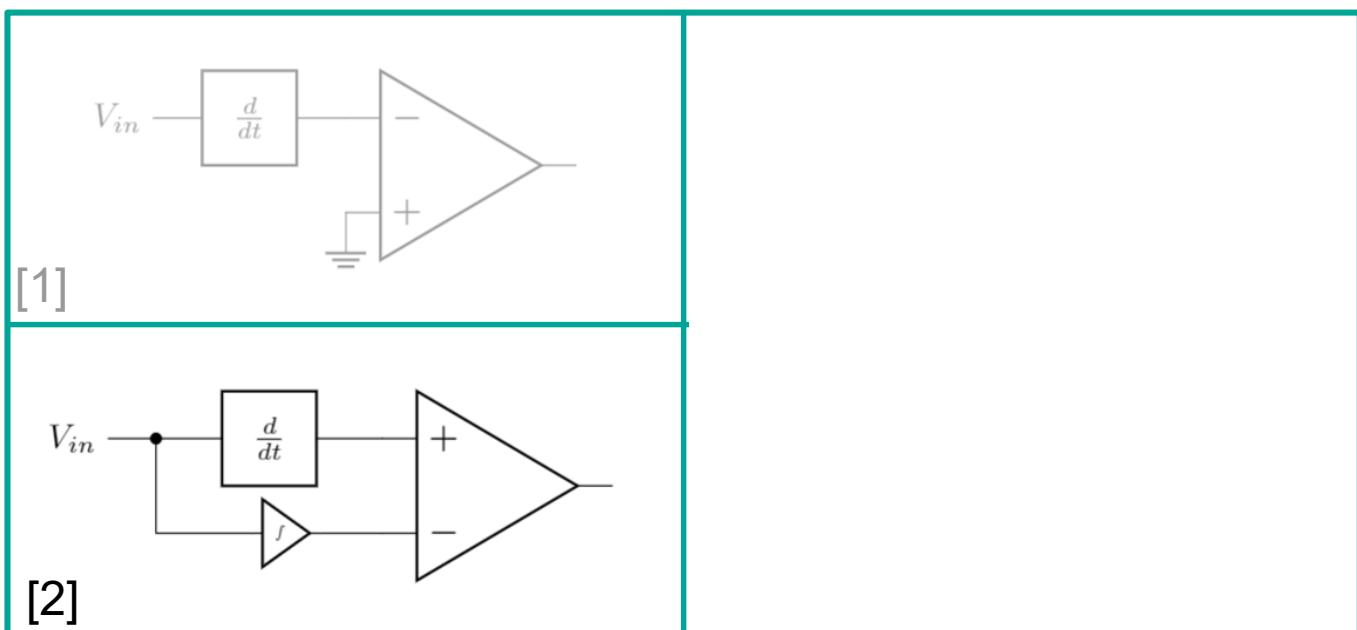
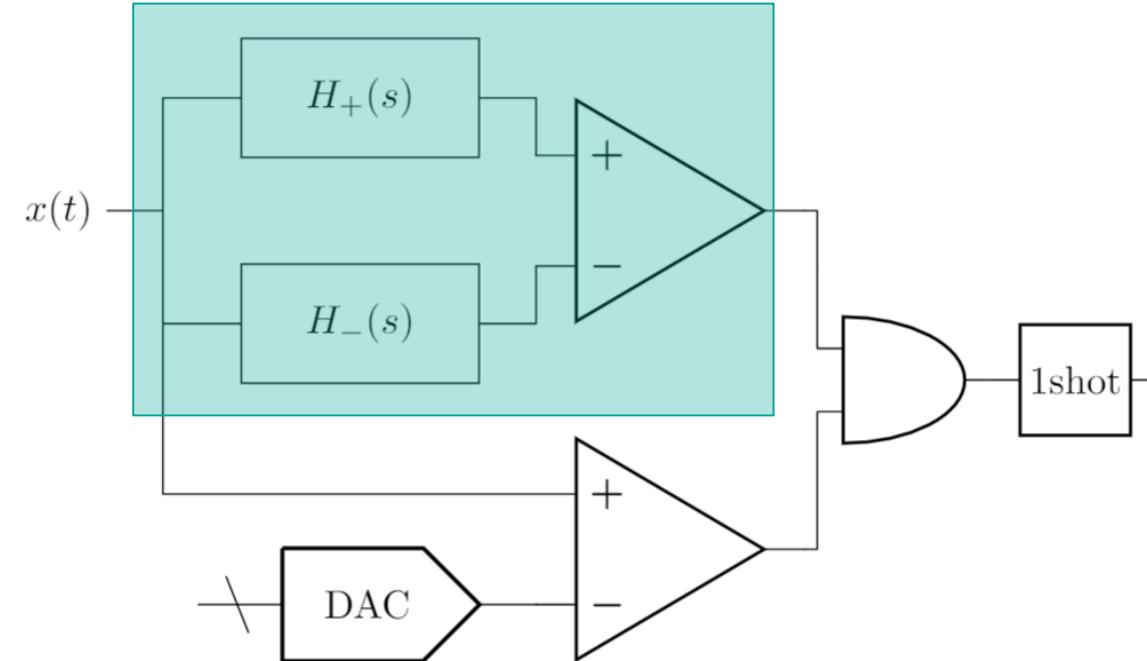
CFD Architecture

- Avoid triggering on noise
- <2 output triggers per event
- Monotonically increasing count rate vs. event rate
- Tunable trigger fraction
- No clipping



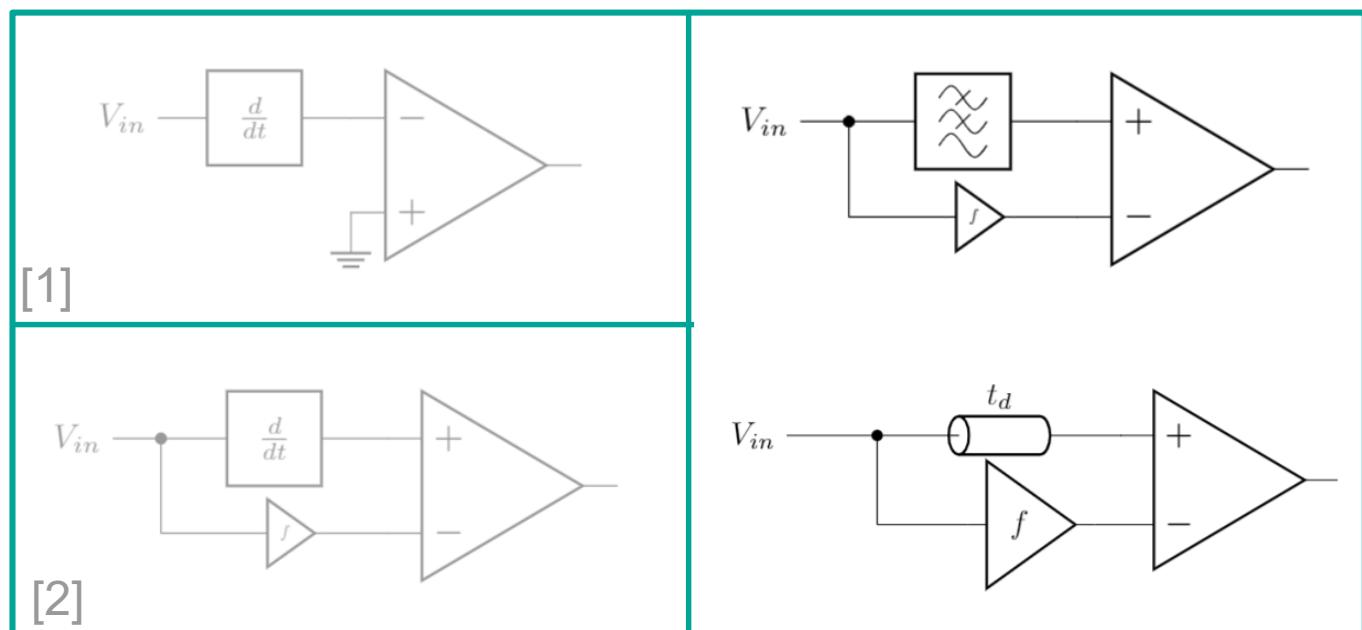
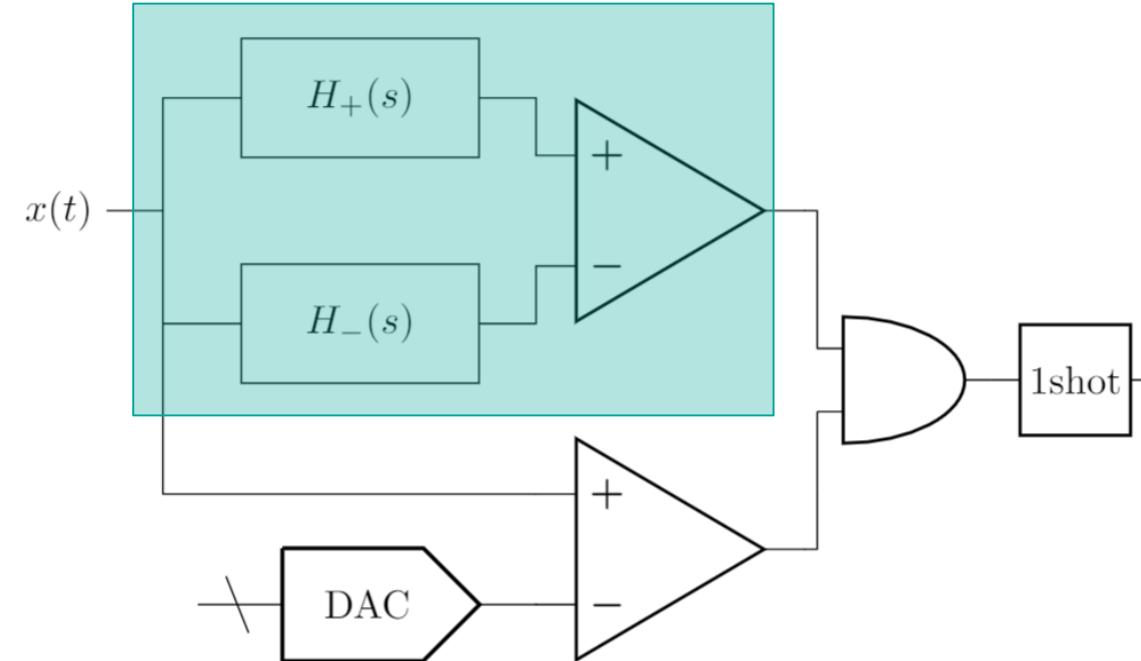
CFD Architecture

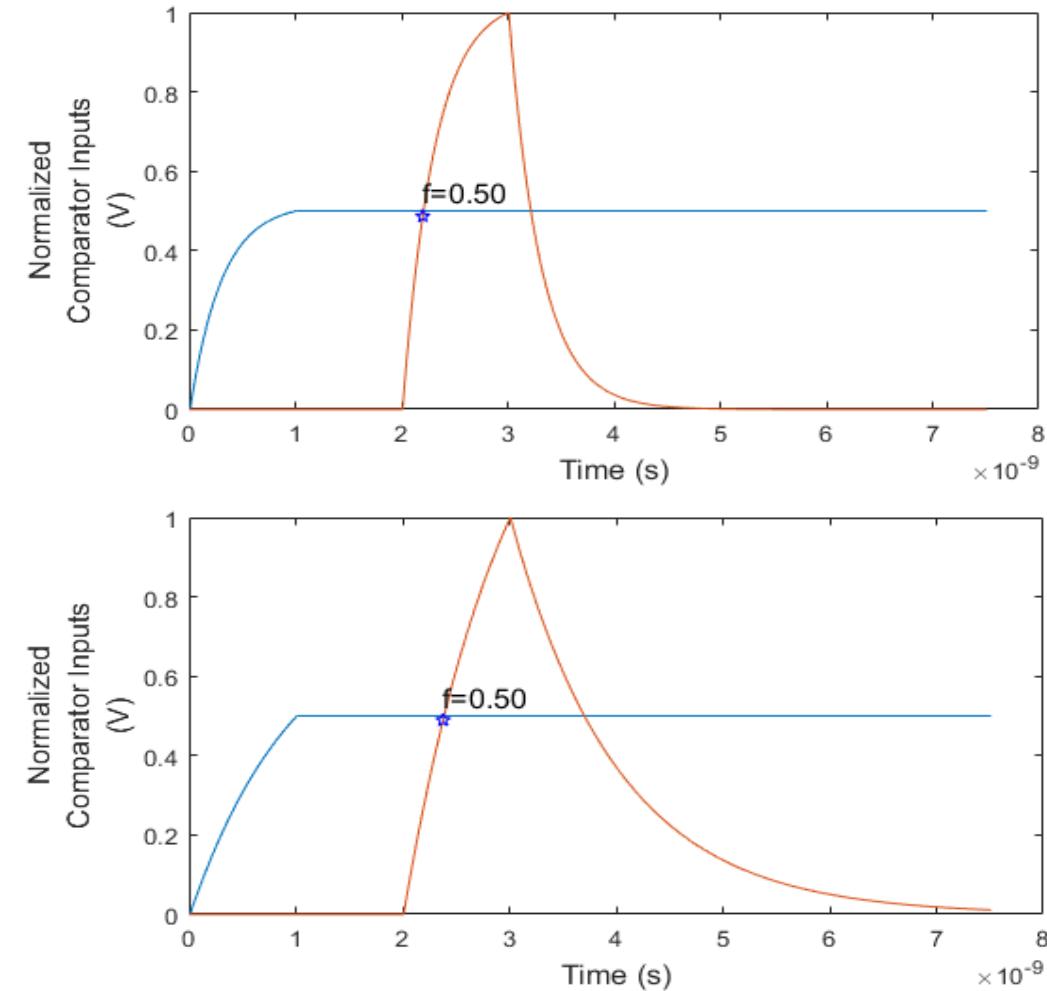
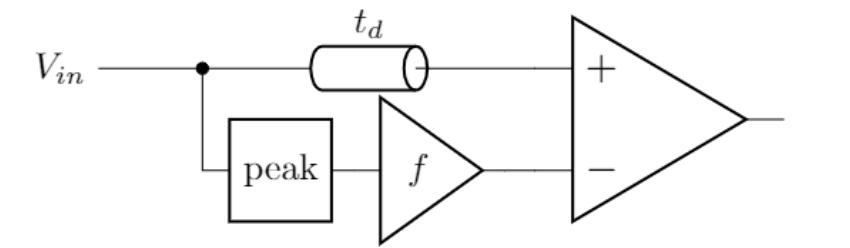
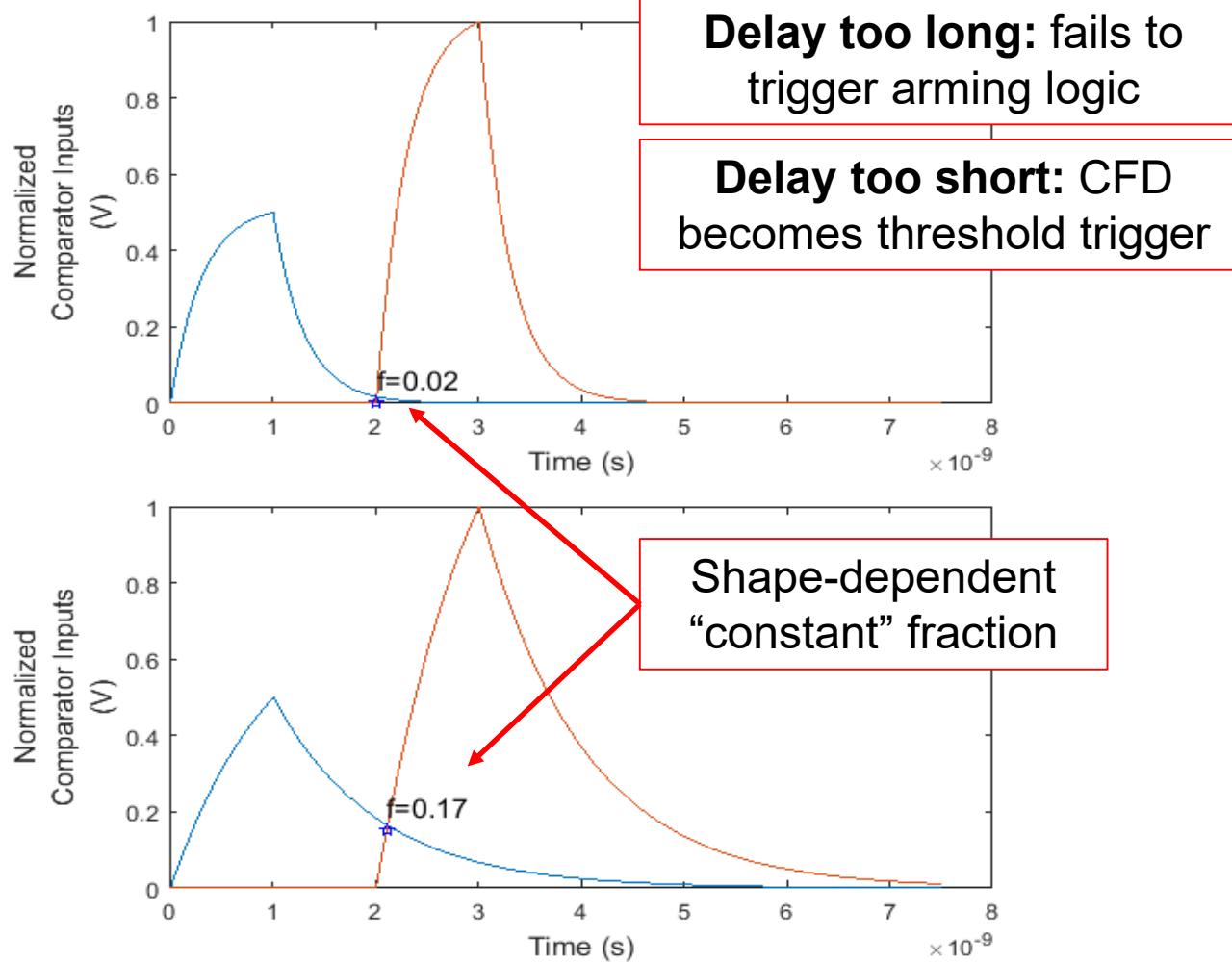
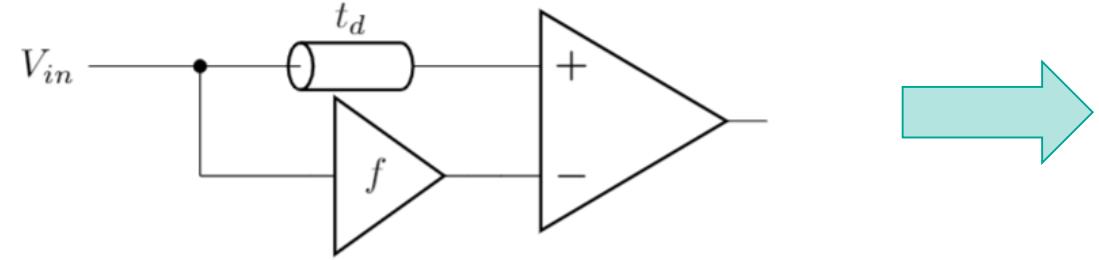
- Avoid triggering on noise
- <2 output triggers per event
- Monotonically increasing count rate vs. event rate
- Tunable trigger fraction
- No clipping



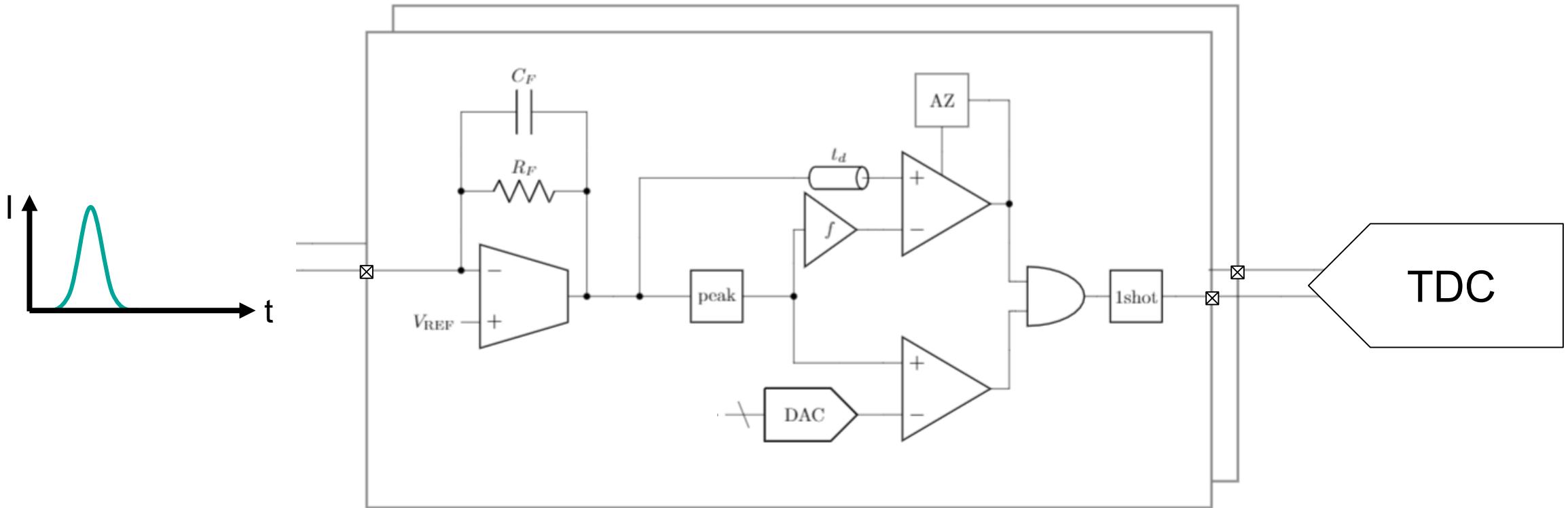
CFD Architecture

- Avoid triggering on noise
- <2 output triggers per event
- Monotonically increasing count rate vs. event rate
- Tunable trigger fraction?
- No clipping

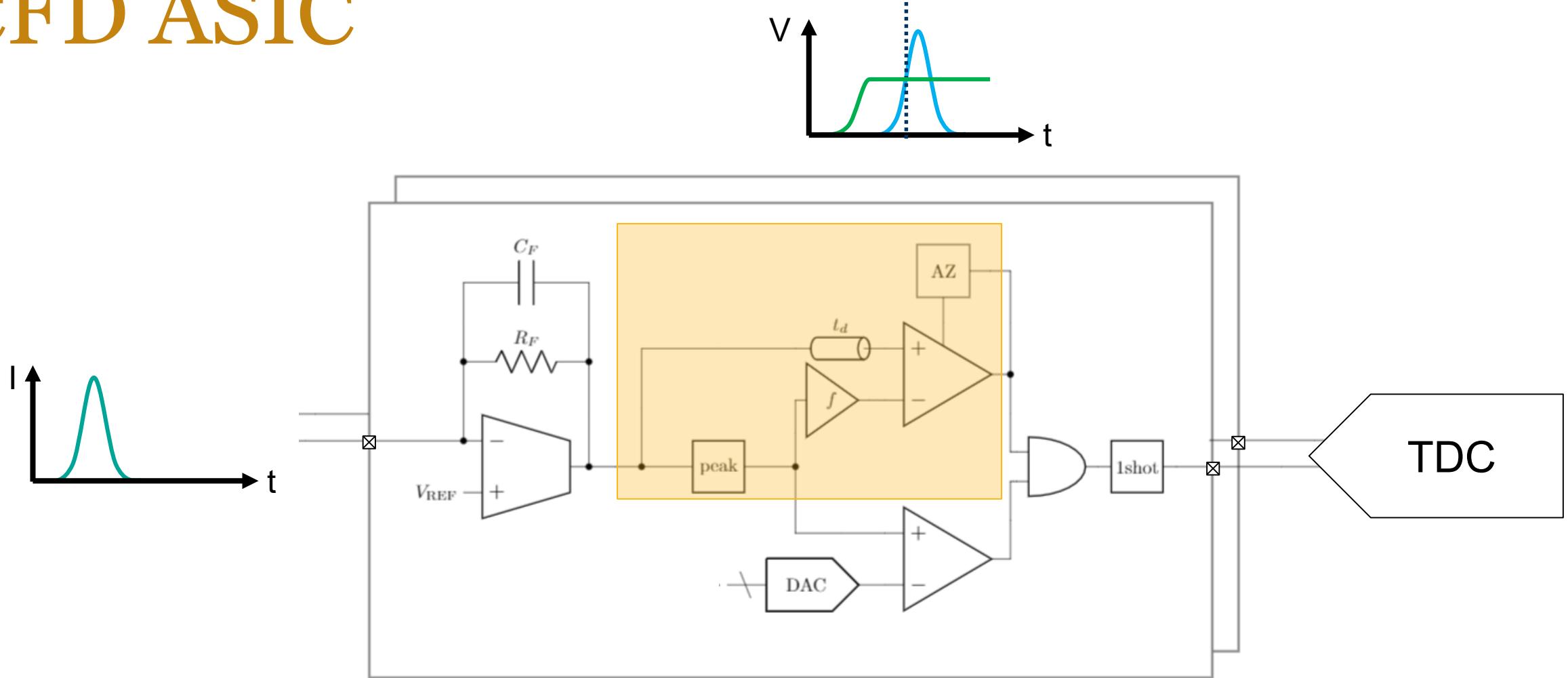




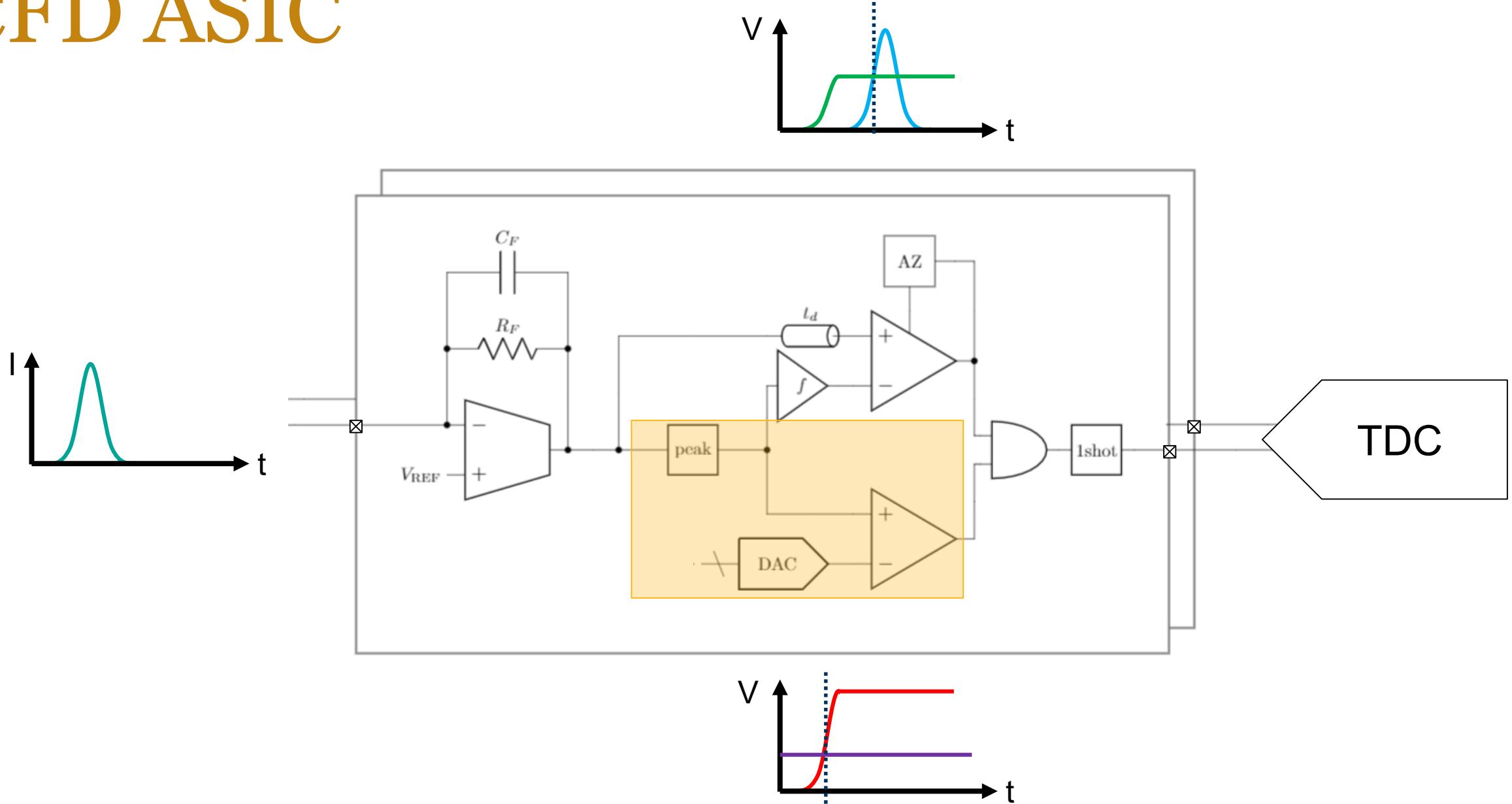
CFD ASIC



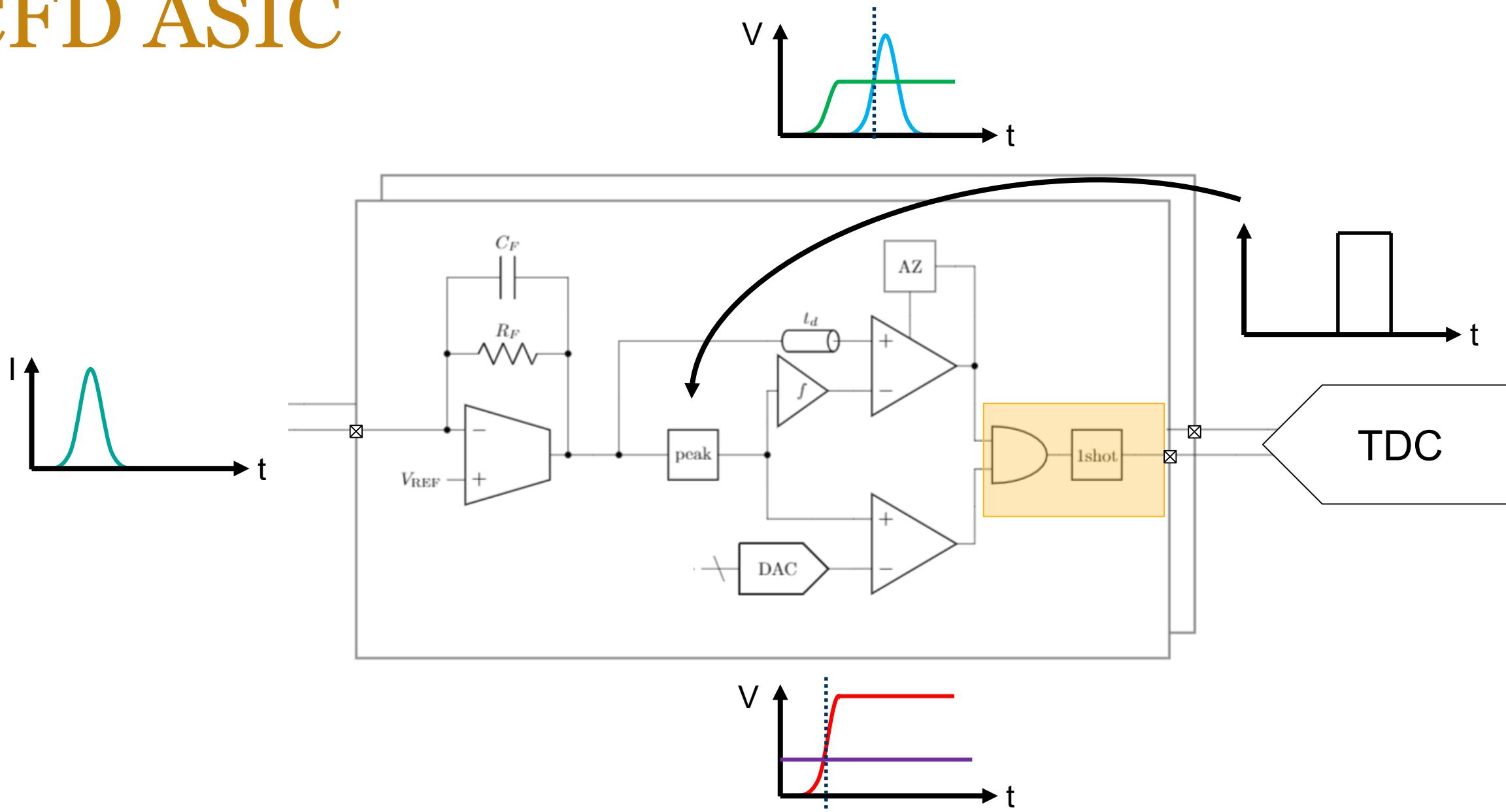
CFD ASIC



CFD ASIC

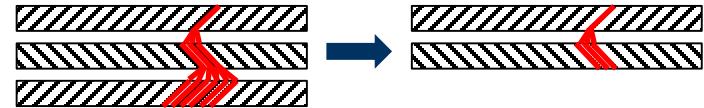


CFD ASIC

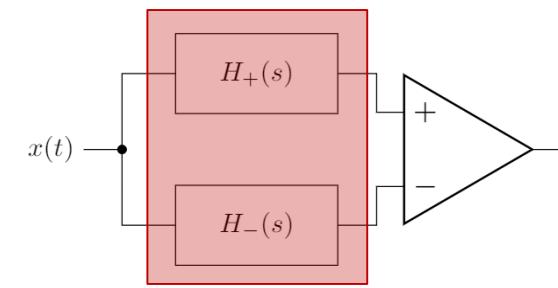


Target Performance

	SPAN-I V1	Target	
Input Charge	40-60Me-	2-3Me-	Z-stack → chevron MCP = lower gain, higher max count rate
Maximum Event Rate	<1Mevent/s	10Mevent/s	
Signal Chain Integration	ASIC + Discrete	ASIC	
Timing Walk w/o Shaping	<100ps	N/A	
Timing Walk w/ Shaping	N/A	400ps	
Jitter (Fixed Pulse Shape)	<100ps _{rms}	<100ps _{rms}	~600-700ps required to distinguish adjacent high m/q
SEU Tolerance	Immune	Immune	
TID Tolerance	100krad	100krad	Calculated by SSL
Power	3-4mA _Q	3mA	
Area	Unknown	<2mm × 2mm	Constrained by shuttle area



Red = not included in V1 ASIC



~600-700ps required to distinguish adjacent high m/q

Calculated by SSL

Constrained by shuttle area

1. Background and Motivation

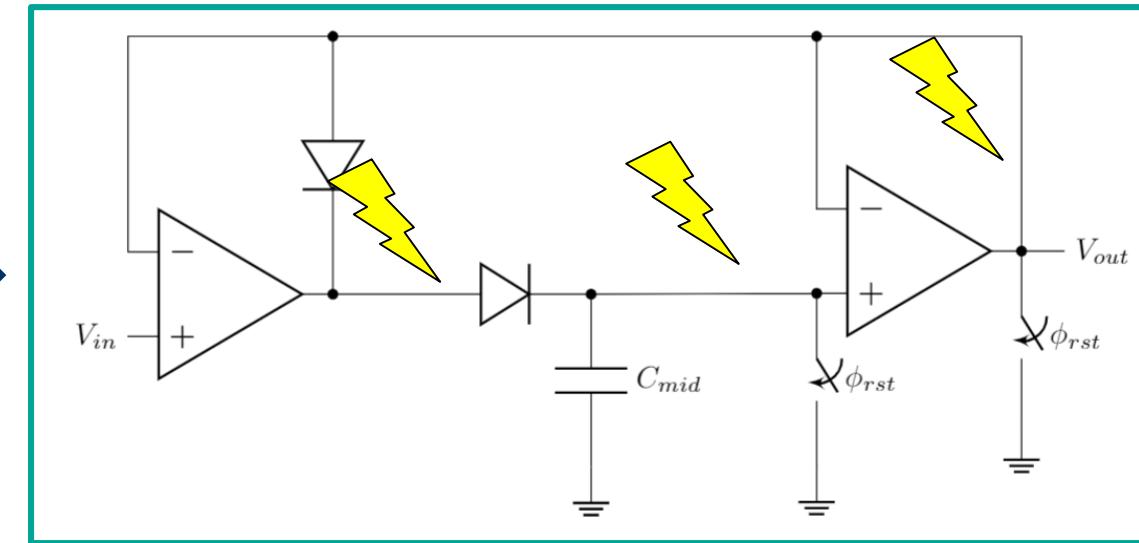
2. Prior and Ongoing Work

- a. Accounting for Radiation Effects
- b. Analog to Digital Pulse Conversion
- c. Circuit Design and Automation

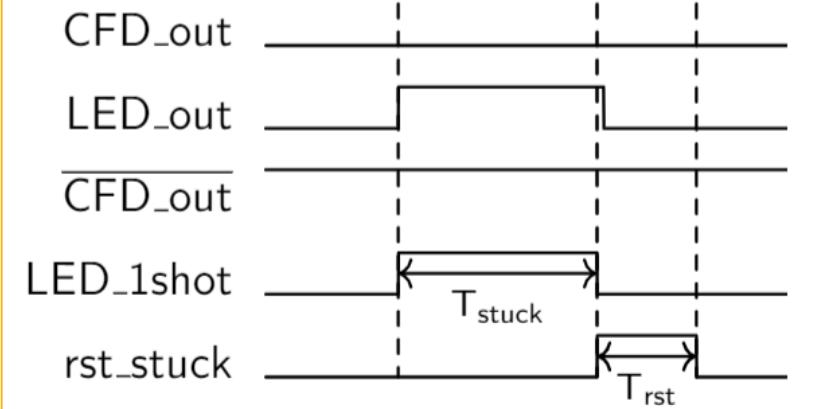
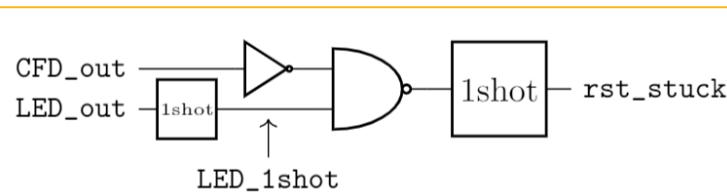
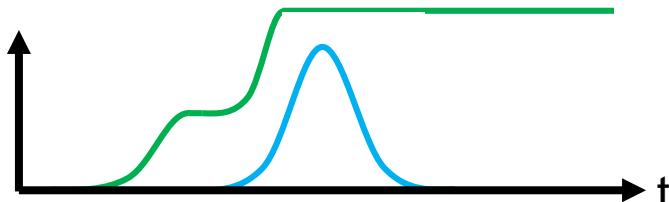
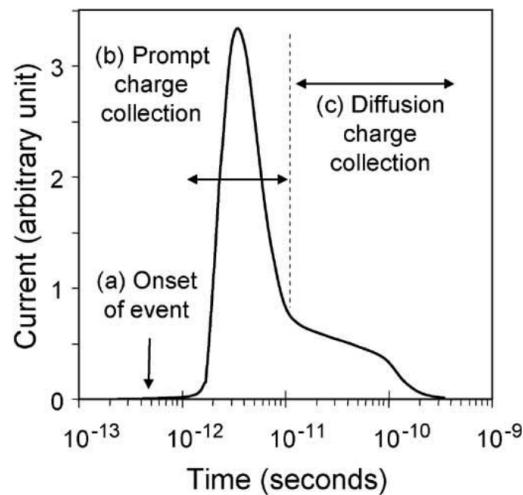
3. Future and Proposed Work

Peak Detector

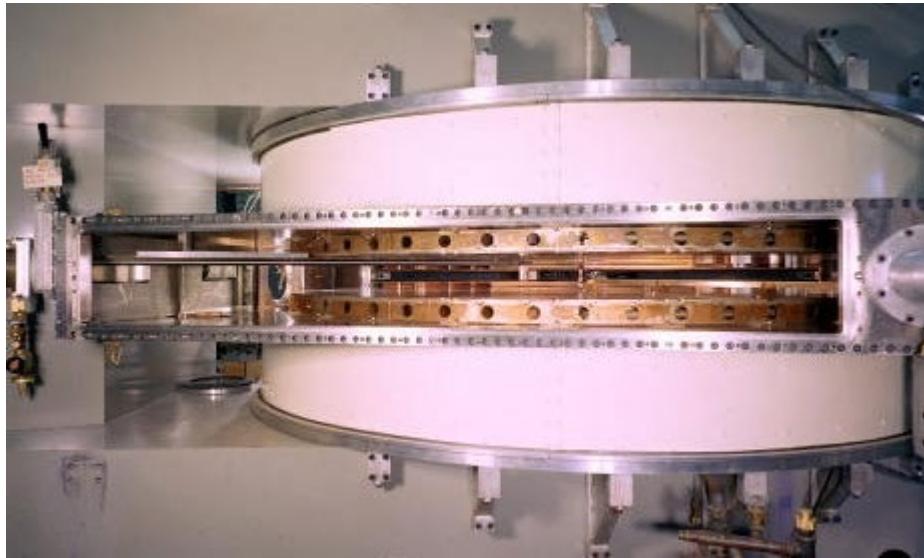
settling error given BW
static error
input bias
reset pulse width
max quiescent current



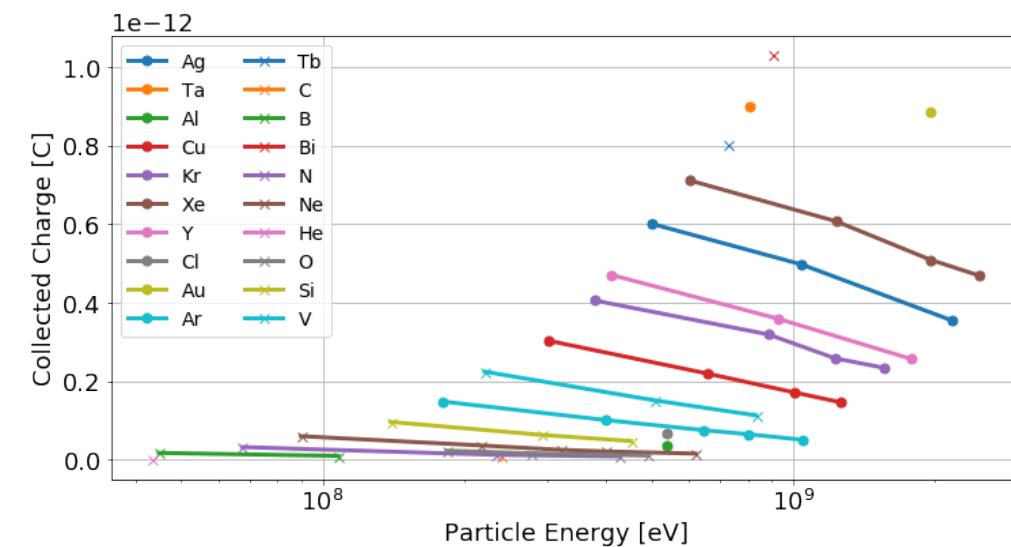
amp parameters
capacitor size
switch sizing
diode parameters



ASET Rate in the Peak Detector

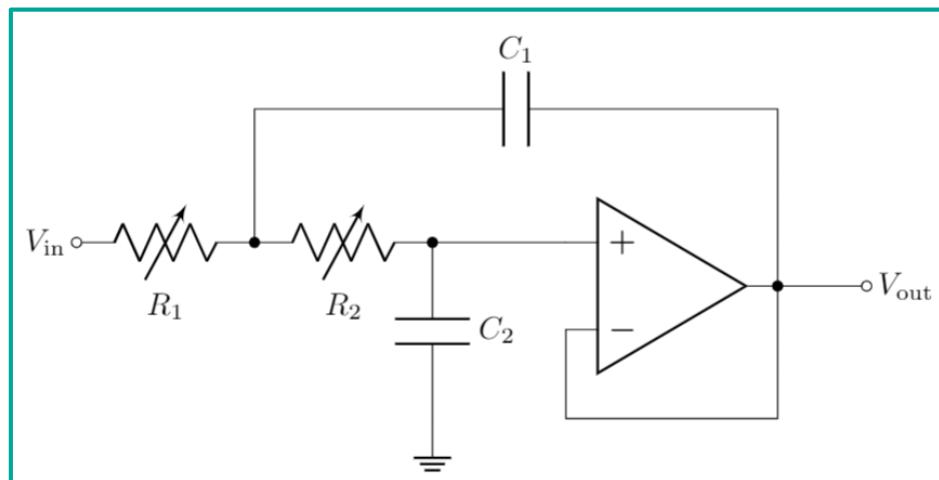
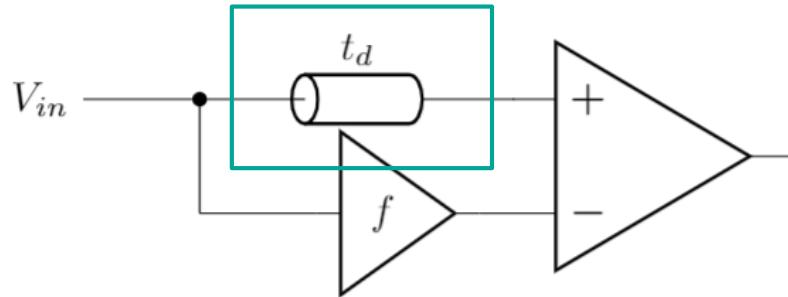


- **Sensitive volume depth (Si):** $\sim 1\mu\text{m}$
- **Flux:** $\leq 10^7 \text{ ions}/(\text{cm}^2.\text{s})$
- **Est. pk det. sensitive area:** $\sim 2000\mu\text{m}^2$
- **Typical valid flux:** $\sim 10\text{k event/s}$



200 ions/s \ll 10k event/s

On-Chip Delay



- **Theoretically:** $[T_{rise,in}, \min(T_{event}, T_{stuck})]$
- 2nd order Bessel filter (maximally flat group delay $t_{delay} = 1/\omega_o$)

$$\frac{3\omega_0^2}{s^2 + 3s\omega_0 + 3\omega_0^2} = \frac{\frac{1}{R_1 R_2 C_1 C_2}}{s^2 + s \frac{1}{C_1} \frac{R_1 + R_2}{R_1 R_2} + \frac{1}{R_1 R_2 C_1 C_2}}$$

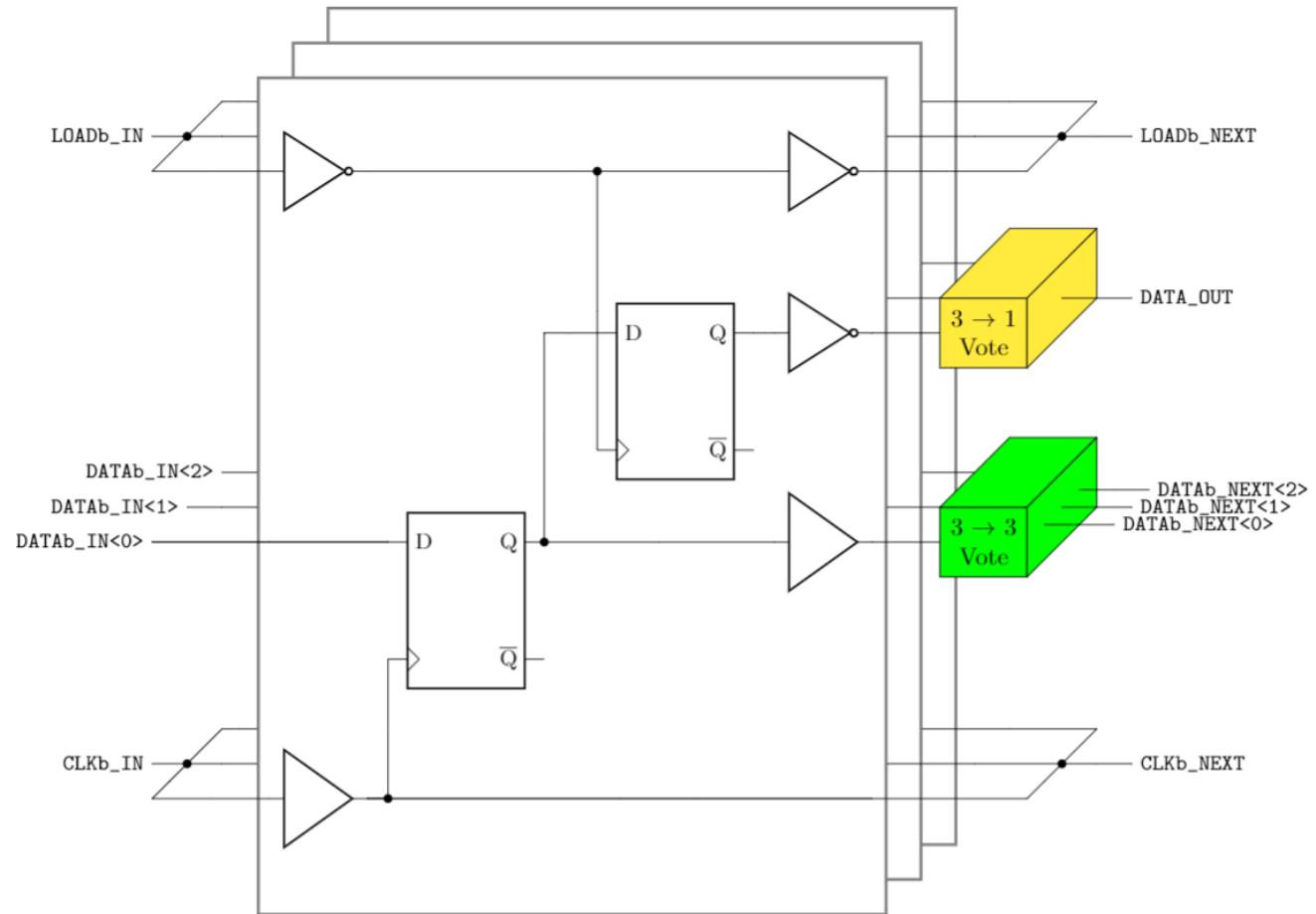
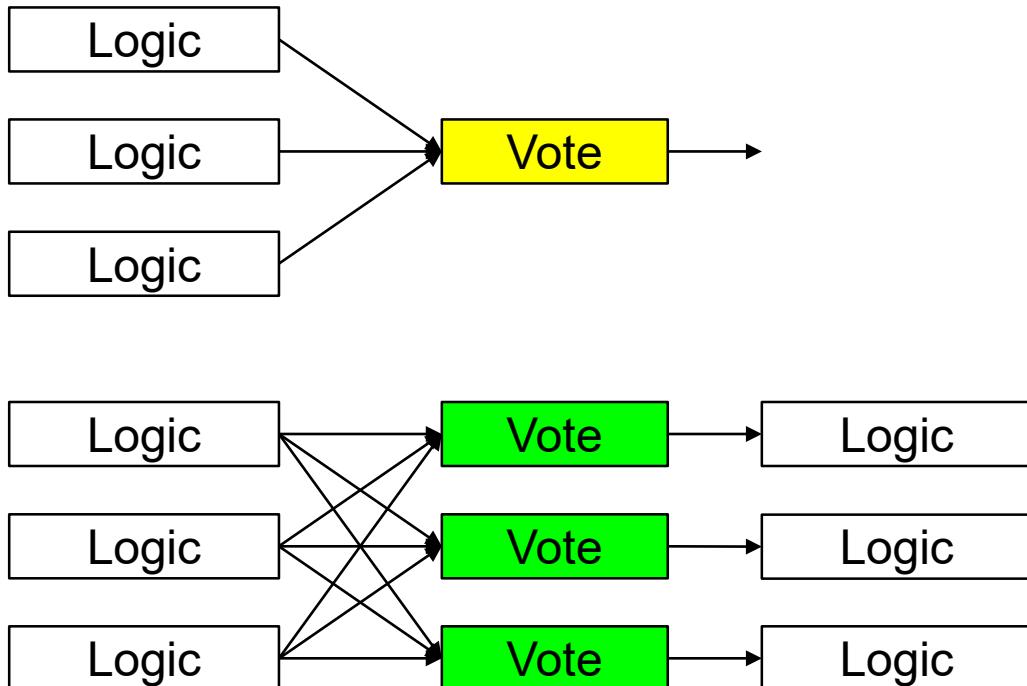
- Choose C_1 and C_2 , then satisfy two conditions

$$R_1 R_2 = \frac{1}{3\omega_0^2 C_1 C_2} \quad R_1 + R_2 = \frac{1}{C_2 \omega_0}$$

Hardening Scan

- Recommendation: $15\mu\text{m}$ spacing between redundant nodes

- Internally: DICE latches



Signal Chain Performance

	SPAN-I V1	Target	Schematic Simulation
Input Charge	40-60Me-	2-3Me-	-
Maximum Event Rate	<1Mevent/s	10Mevent/s	-
Signal Chain Integration	ASIC + Discrete	ASIC	-
Timing Walk w/o Shaping	<100ps	N/A	<50ps
Timing Walk w/ Shaping	N/A	400ps	310ps
Jitter (Fixed Pulse Shape)	<100ps _{rms}	<100ps _{rms}	180ps _{rms}
SEU Tolerance	Immune	Immune	Immune/Won't Lock
TID Tolerance	100krad	100krad	-
Power	3-4mA _Q	3mA	2.9mA _{avg}
Area	Unknown	<2mm × 2mm	?

1. Background and Motivation

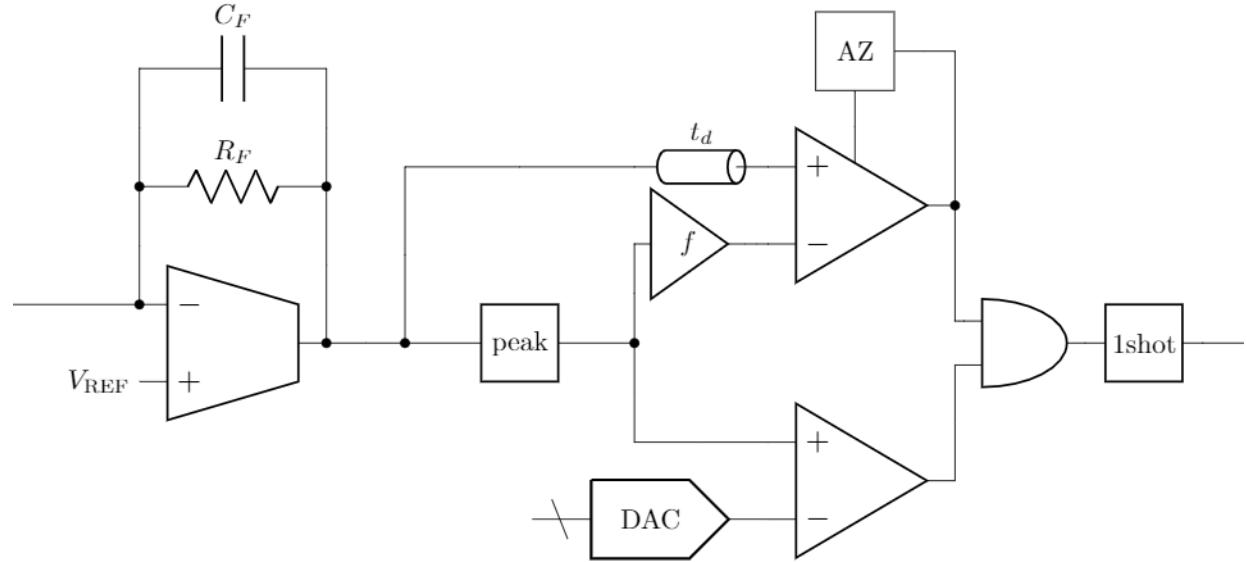
2. Prior and Ongoing Work

- a. Accounting for Radiation Effects
- b. Analog to Digital Pulse Conversion
- c. Circuit Design and Automation

3. Future and Proposed Work

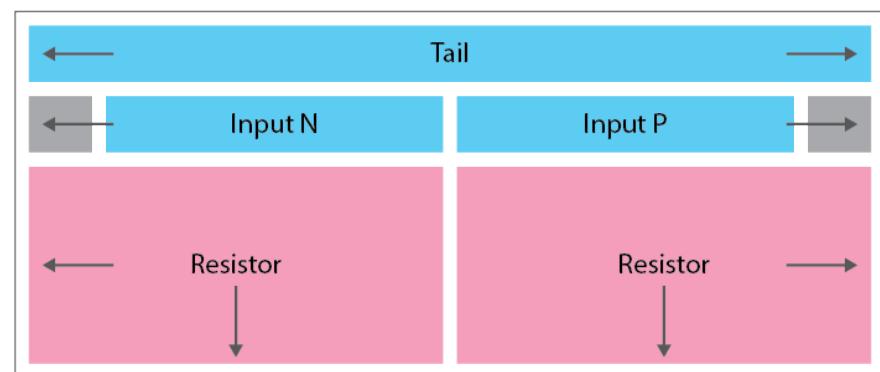
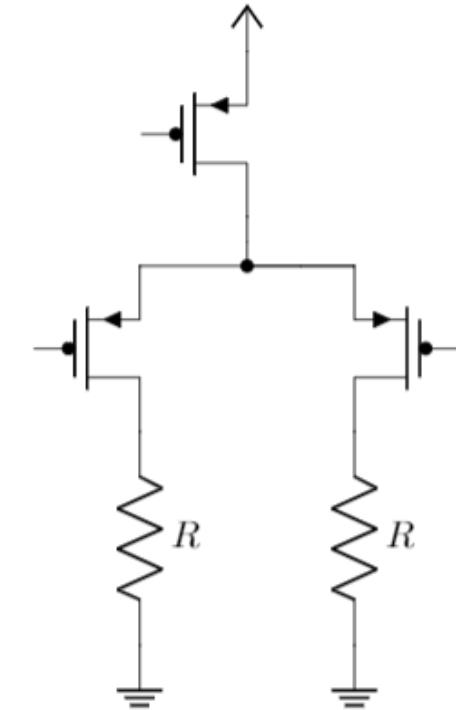
Immediate Deadlines

- **Tapeout:** July 21, 2021
- **Delivery:** Late 2021/Early 2022
- **Products:**
 - CFD ASICs with on-chip
 - Scripts for major CFD subblocks
 - Measurement scripts to inject SETs into
 - BAG infrastructure for running Monte Carlo sims



Layout Generation

- Manual layout is slow
- Incorporate into iteration loop → accounts for parasitics
- LayGO = Layout with Gridded Objects [1]
 - Shares the same benefits as BAG
 - DRC clean-by-construction
 - Established in several $\geq 28\text{nm}$ nodes (bulk and FDSOI) on BWRC servers



Full Rad Hard CFD Design Script

Input Pulse Definition

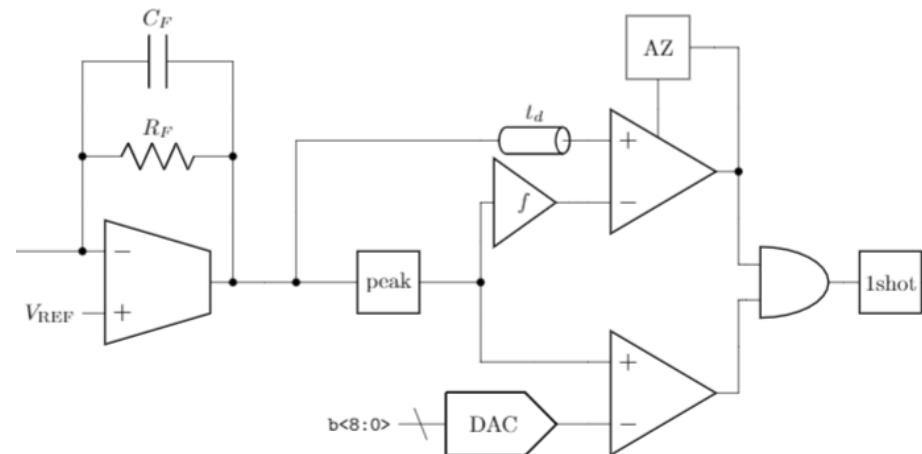
files of input current waveforms
min/max scale factors
max event rate
parallel and series impedances

CFD Macro Parameters

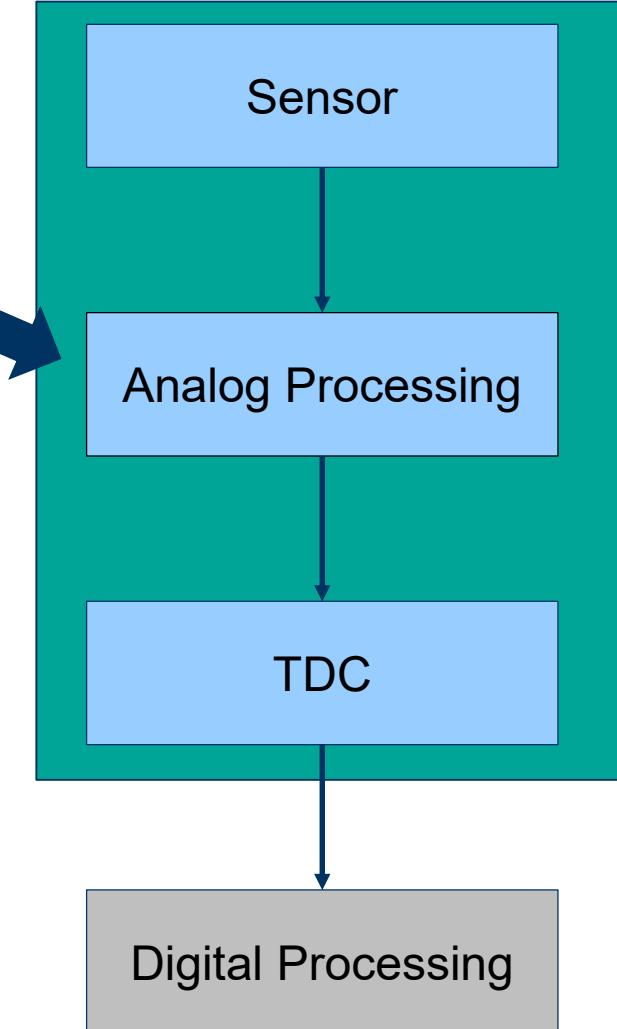
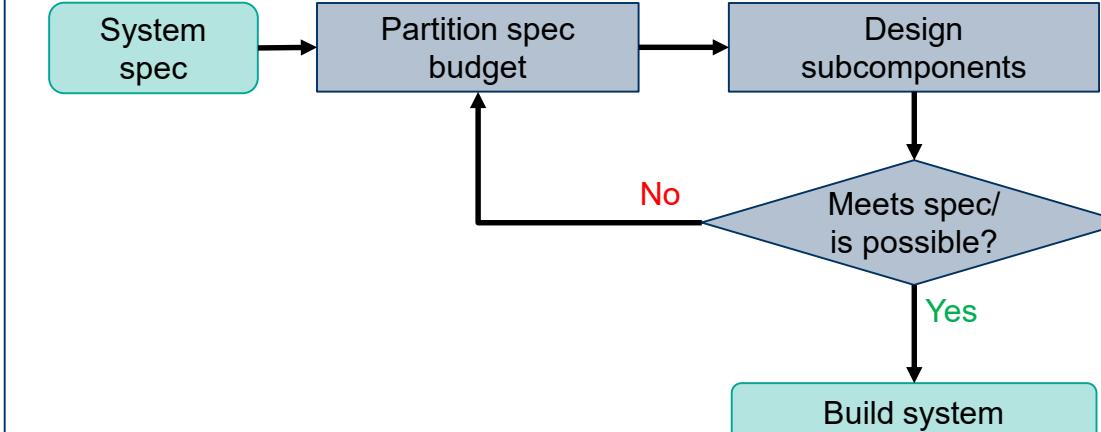
max timing walk
max output jitter
preamp bandwidth
supply, max average power, etc.

Other Parameters

(table of SET Q, T_r , T_f)
(TID leakage factors)
(optimization criterion)
(tolerances, device flavors, etc.)



System Optimization



Time-to-Digital Conversion

- **SPAN-Ion Now:** Discrete, TAC + 12b ADC, 1 channel

Part 1: TAC + ADC

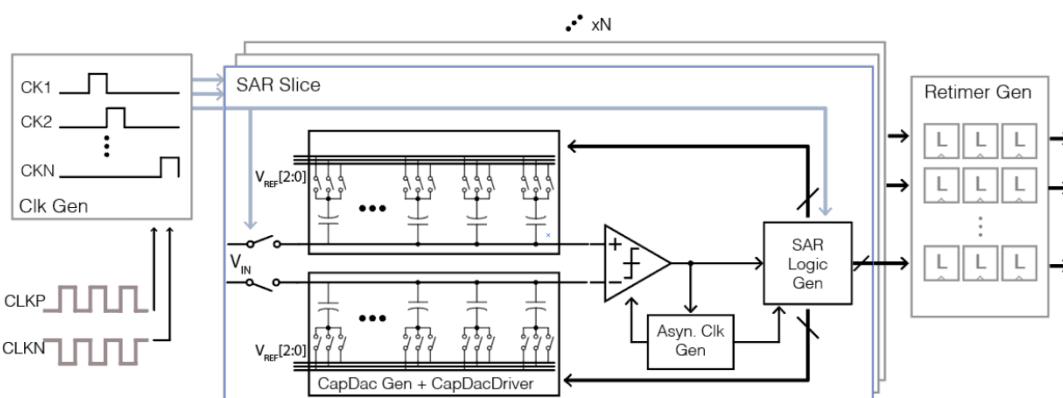
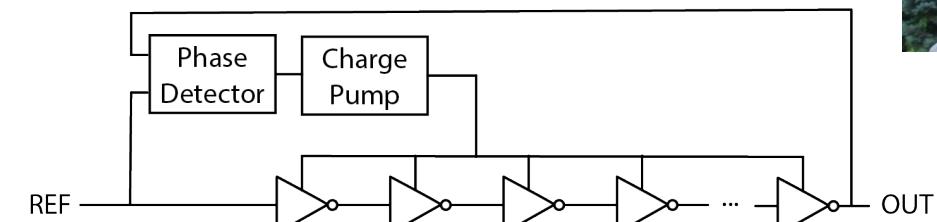


Figure 4.1: Architecture of time-interleaved ADC generator.

[1]

Part 2: DLL-Based TDC

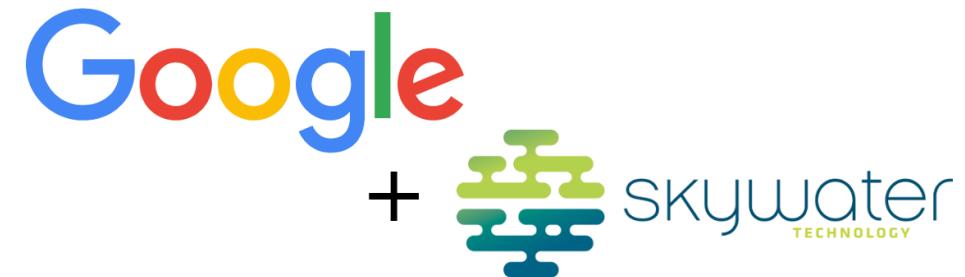
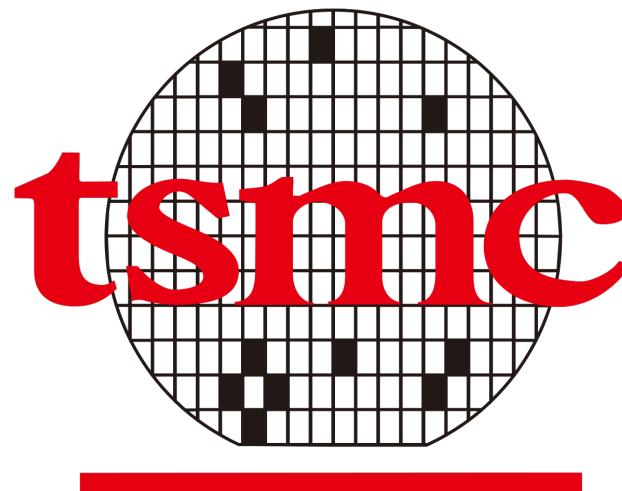


DLL array? [3]
Looped vernier? [4]
Intra-cell interpolation? [2]
Something else???



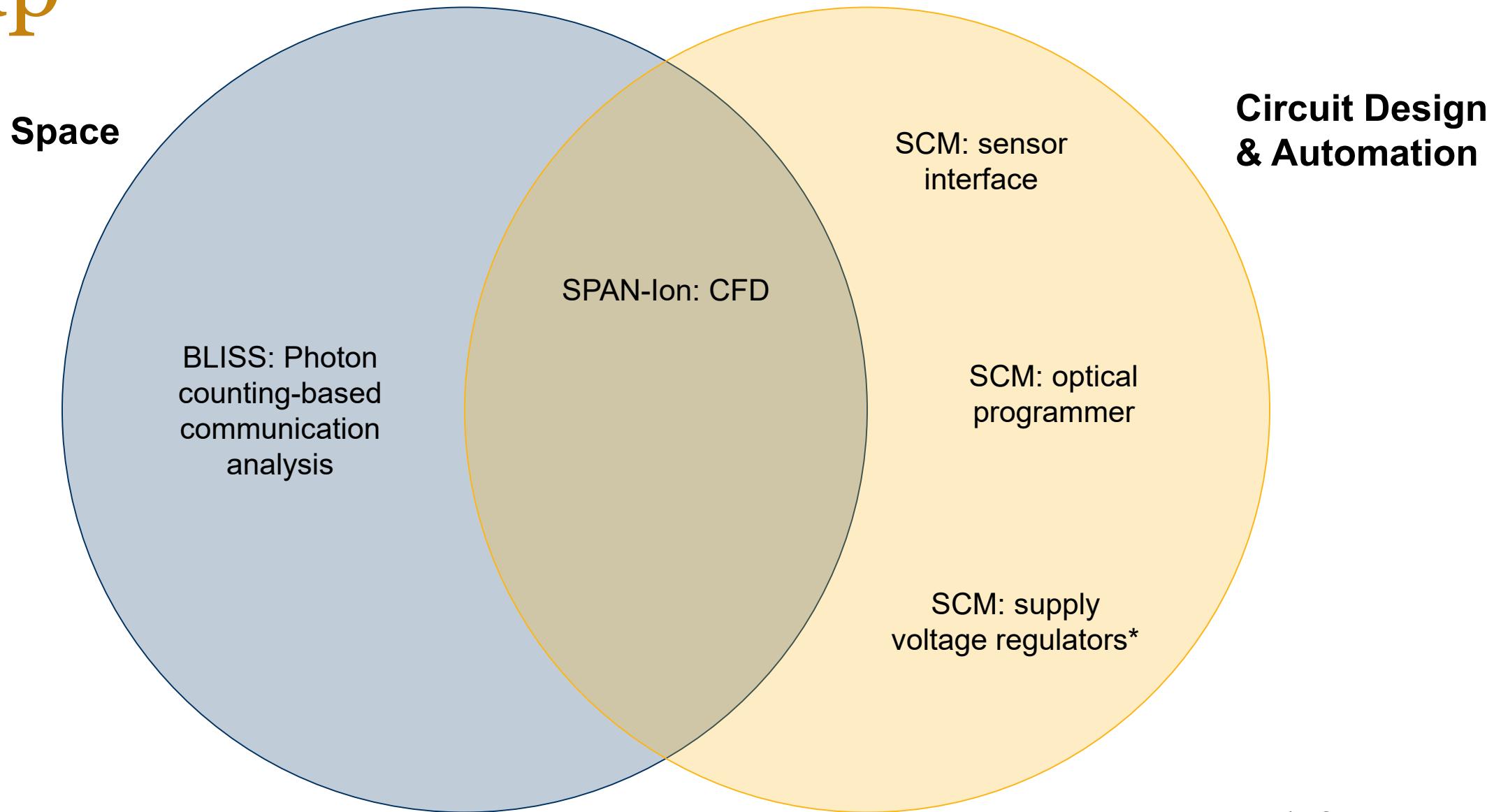
Button-Press Tapeout

- Full frontend optimization: maximize signal processing performance given power constraint
- Tape out in multiple process nodes; many options



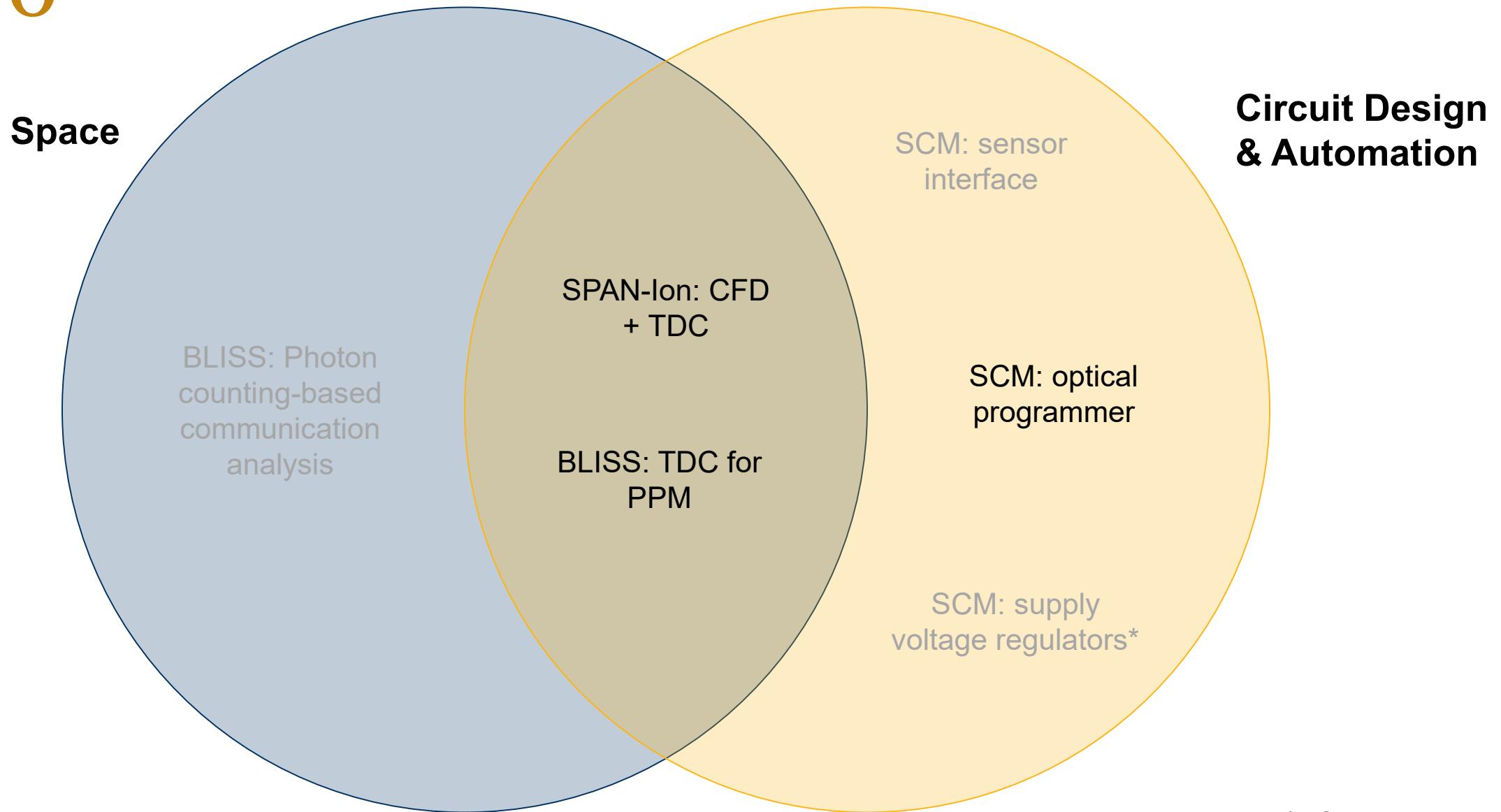
FOSS 130nm Production PDK
github.com/google/skywater-pdk

Recap



*MS Jackson Paddock

To Do



*MS Jackson Paddock

Proposed Timeline

Summer 2021

- Tape out CFD ASIC in TSMC180 (July 21) and build test setup. Choose TDC architecture.
- Test SCM optical RX.

Fall/Winter 2021

- Test CFDs separately and deliver to SSL for radiation testing and system integration.
- Begin design scripts for rad hard TDC.

Spring 2022

- Complete CFD +TDC design loop with layout; tape out CFD + TDC in >1 process.
- Tape out photon-counting sensor array + TDC for PPM-based receiver.

Summer 2022

- Test CFD + TDC and time-tagging TDC performance and radiation hardness.
- Build optical communication test setup with FPGAs implementing remainder of PPM receiver.

Fall/Winter 2022

- Characterize photon-counting sensor array + TDC, then ground test 1AU equivalent link.

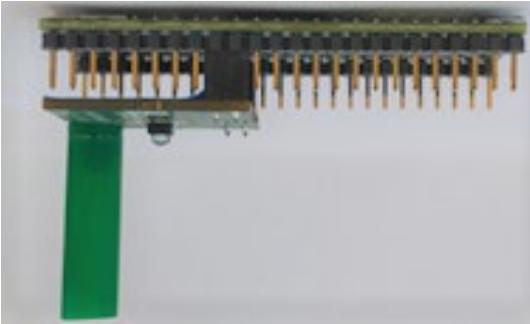
Spring/Summer 2023

- Finish thesis work, (hopefully) graduate

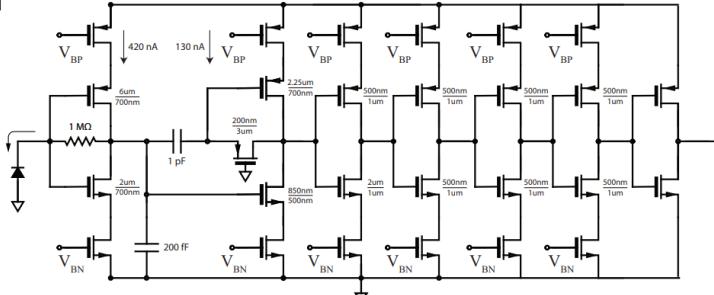
Thank you!

Single Chip Mote: Optical Programming

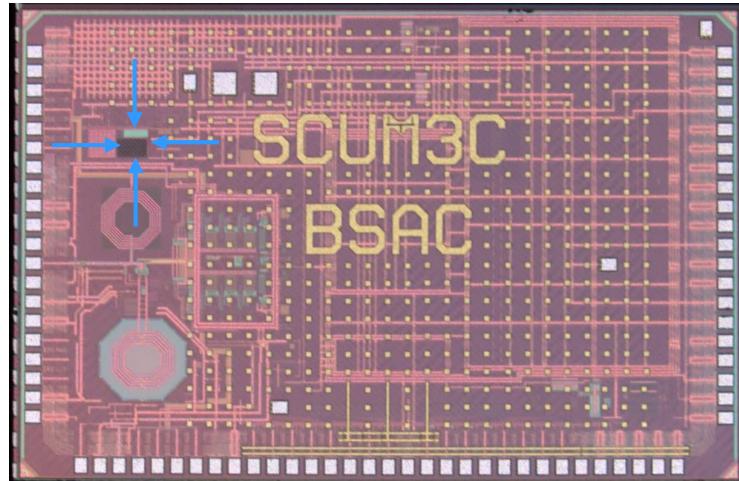
Optical Programming



[1]



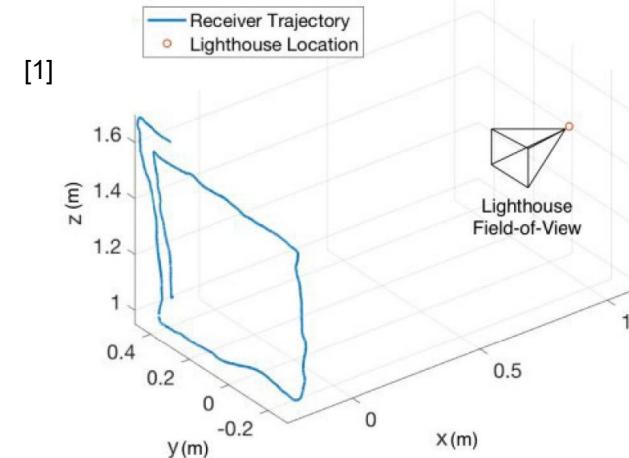
- + Super low RX power ($\sim 1.5\mu\text{W}$)
- High TX power ($>1.5\text{mW/mm}^2$)
- Poor/no DC rejection



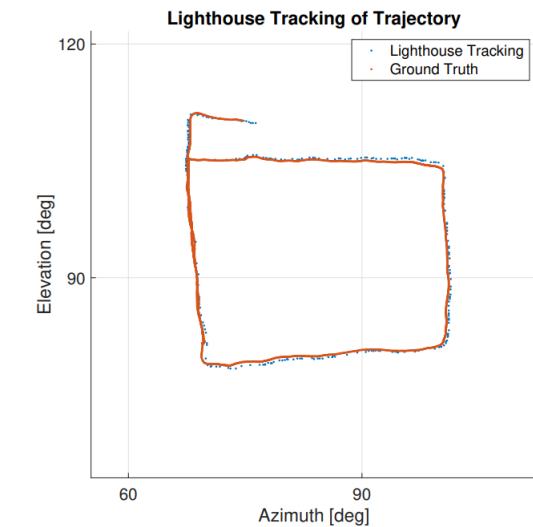
	RX V1	RX V2	Lighthouse	
Irrad.	$>1.5\text{mW/mm}^2$	$<20\mu\text{W/mm}^2$	$<10\mu\text{W/mm}^2$	
BER	$6(10^{-4})$	$2(10^{-8})$	10^{-3}	
Yield	Unknown	$\geq 99\%$ (2.6σ)		
Area	$130\mu\text{m} \times 130\mu\text{m}$			
Active Power	$\sim 1.5\mu\text{W}$	$\sim 15\mu\text{W}$		

Lighthouse Localization

Experimental Setup with Receiver Trajectory

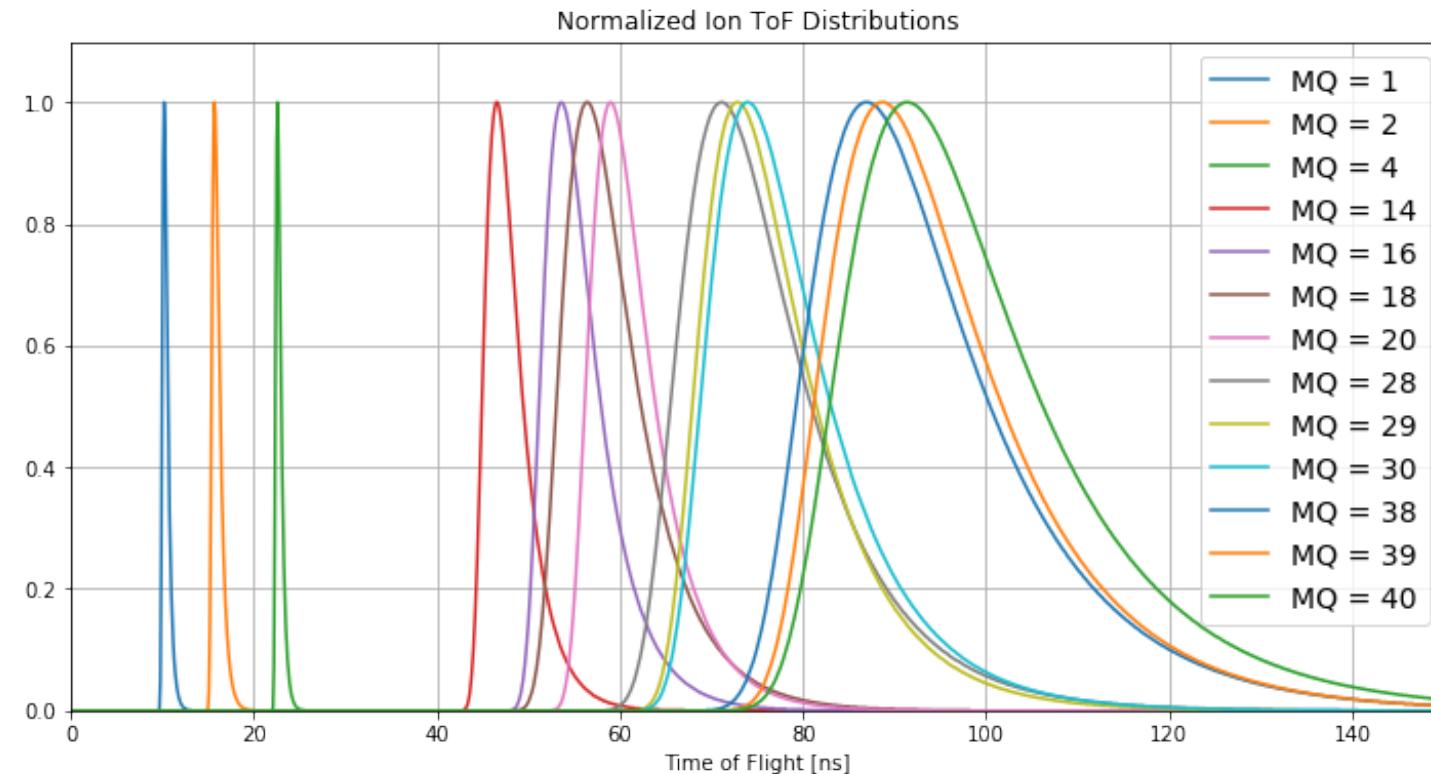


[1]



Straggling in Time-of-Flight

- Primarily due to nonuniform ion velocity prior to acceleration
- Can be corrected with a reflectron



*SSL data fit to Moyal distribution
(raw data not available)

RHBF: Edgeless/Enclosed Transistors

Advantages:

- Reduced oxide near channel reduces TID effects

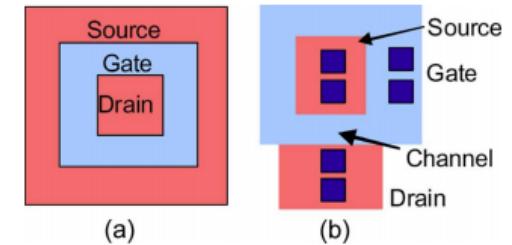


Fig. 13. (a) Edgeless and (b) an enclosed-source transistor.

Disadvantages:

- Nonstandard for most PDKs (special LVS+PEX, DRC difficult)
- Matching isn't great
- 2D current profile = effective width hairy
- Increased node cap relative to standard devices

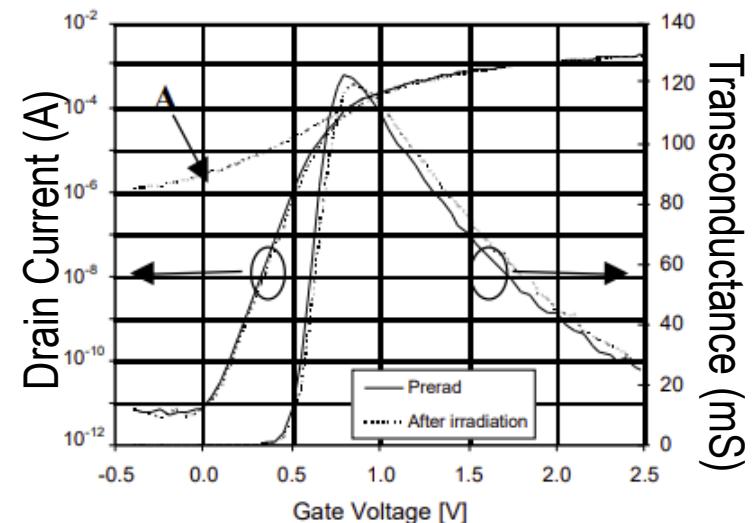
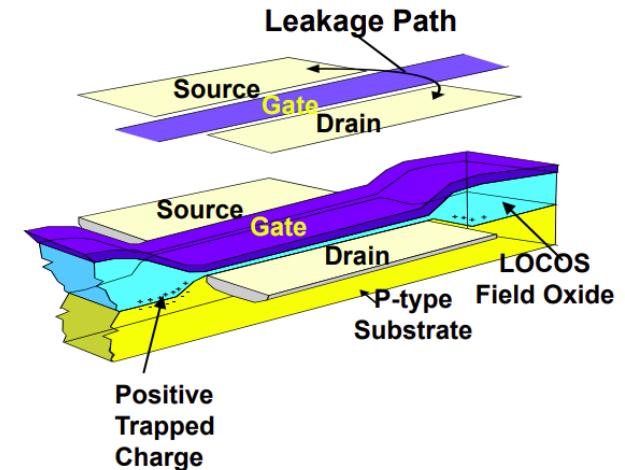
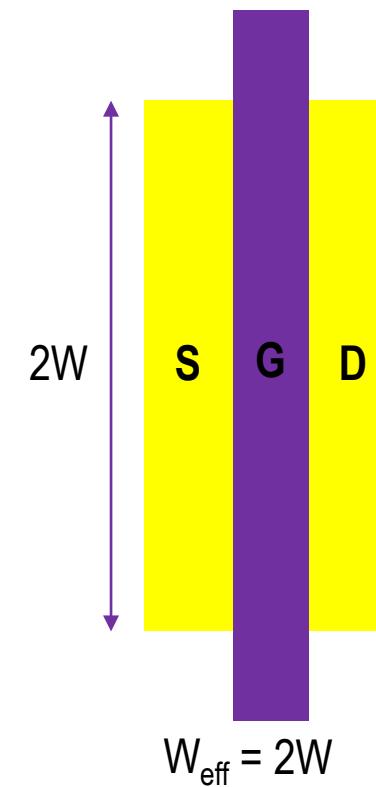
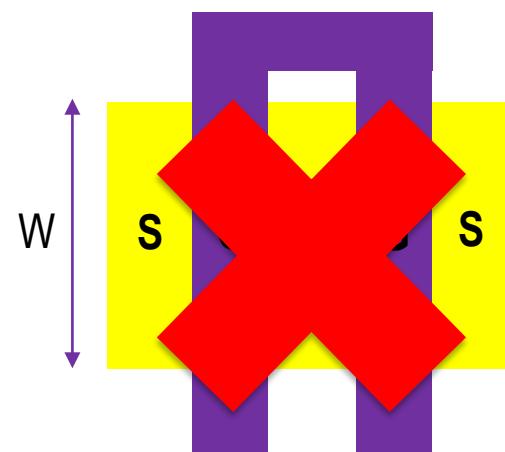
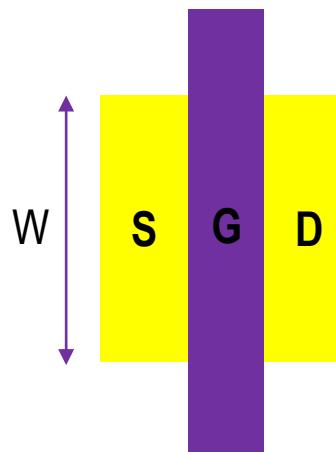


Figure 1: Drain current (log scale) and transconductance before and after 30 Mrad (SiO₂) for an edgeless n-channel ($L = 0.28 \mu\text{m}$) and drain current for a normal n-channel ($L = 0.28 \mu\text{m}$) after 1 Mrad (SiO₂) (curve A).

RHBD: Bigger Devices

- Large effective area good in general for matching
- Generally, large devices “spread out” problems
- Wider fingers \rightarrow less degradation



RHBD: Device Wells and Inverter Chains

- Inverter chains quench pulses.
 - Example: INV2 is struck, OUT2 glitches high, INV3 PMOS injects charge to shorten the glitch on OUT3
- Sharing wells can reduce pulse duration (and by proxy, SEE x-section)

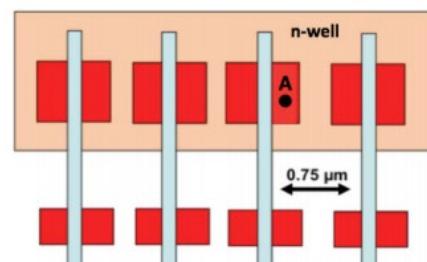
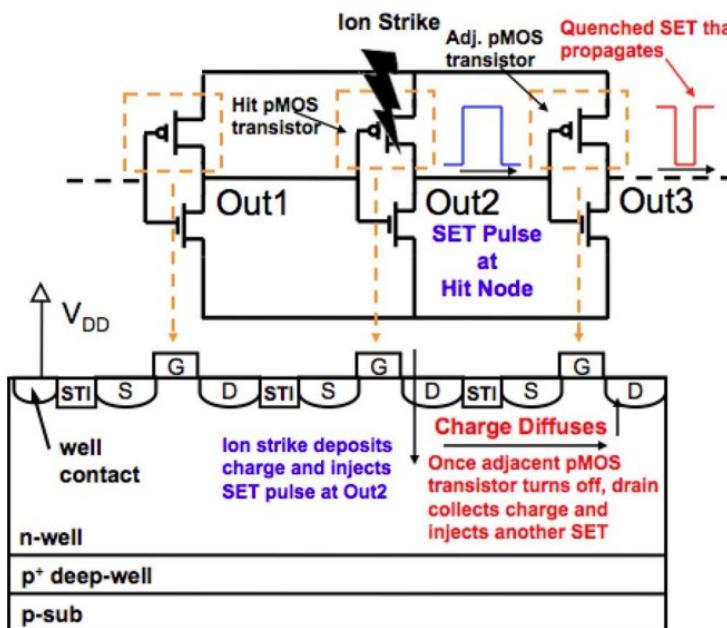


Fig. 2. Layout of the 65 nm target inverter chain where each row of inverters shared a common n-well (common n-well).

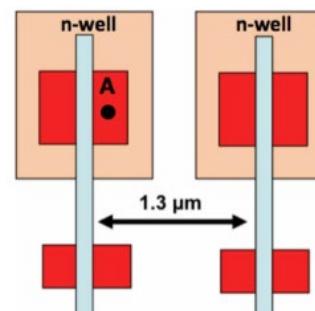
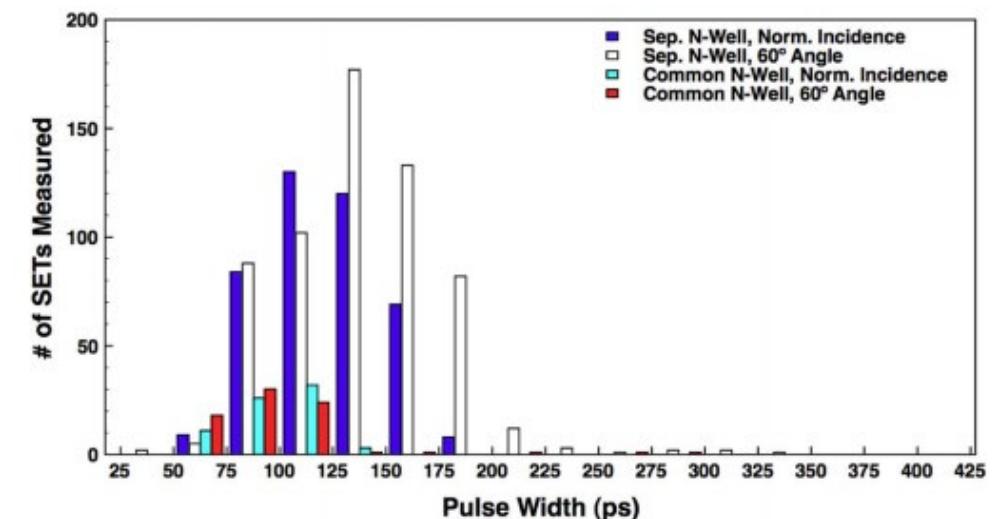
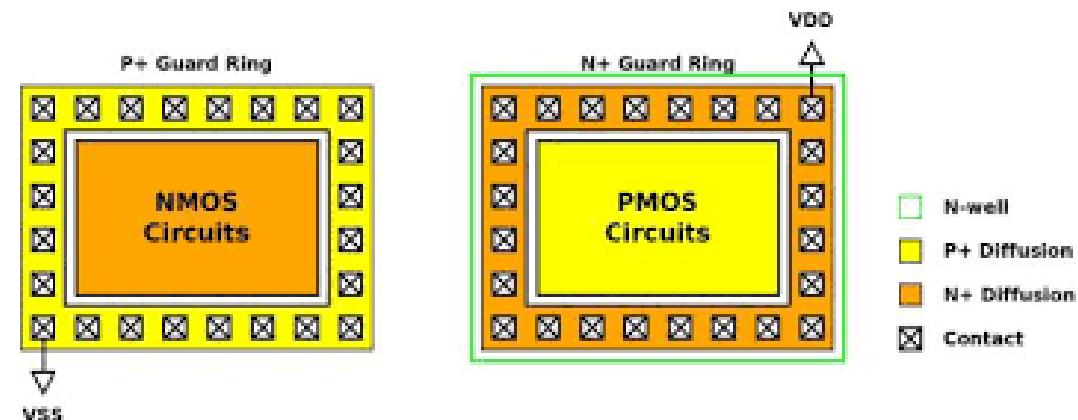
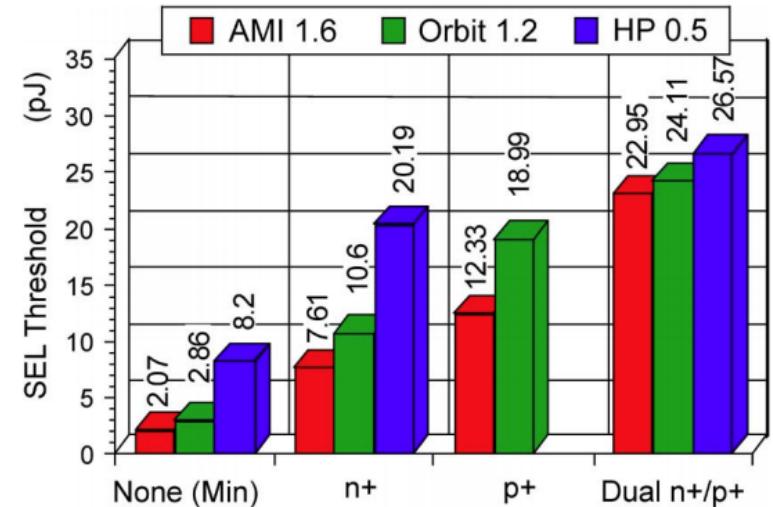


Fig. 3. Layout of the 65 nm target inverter chain where each inverter had its own separate n-well (separate n-well).

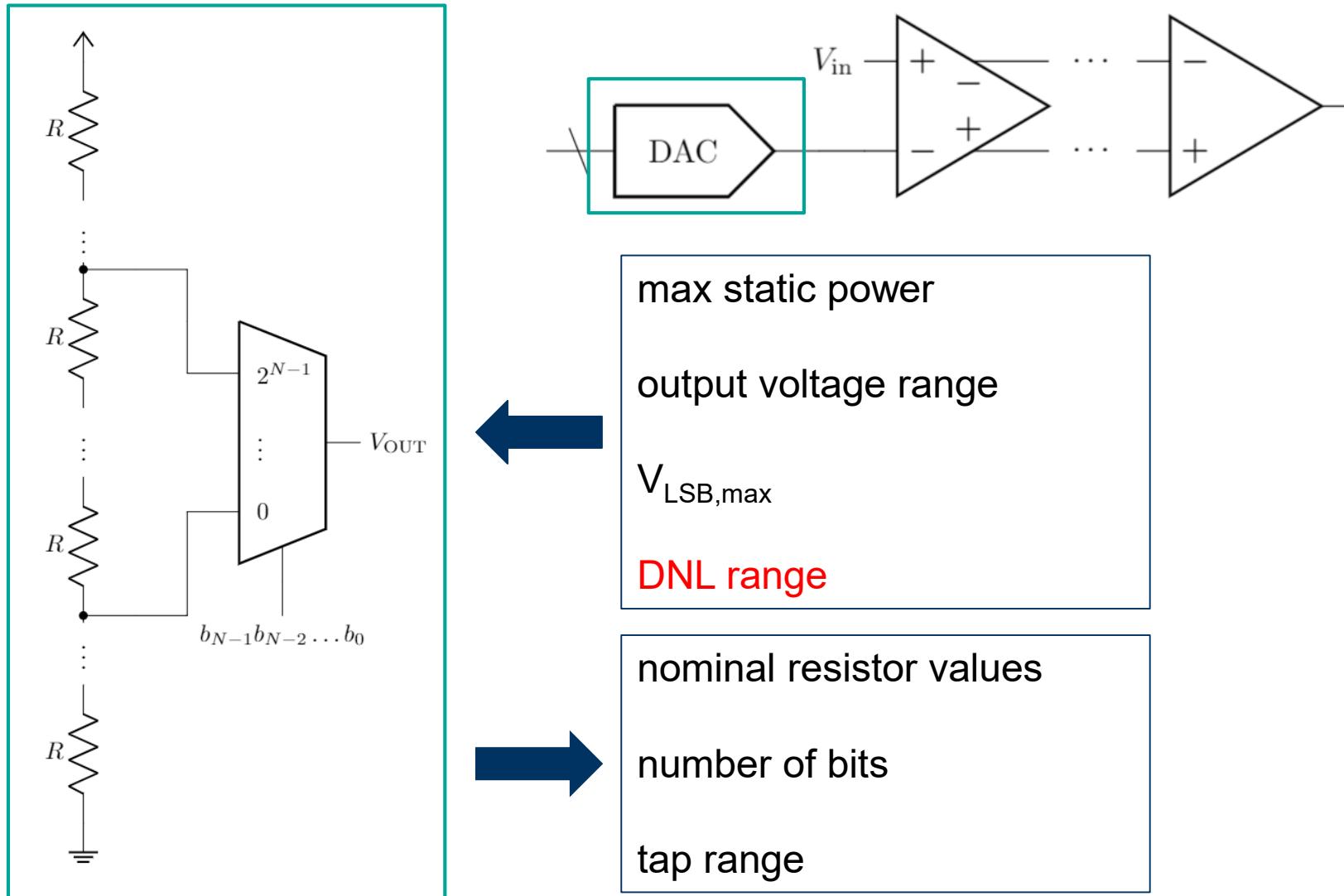


RHBD: Guard Rings and ESD

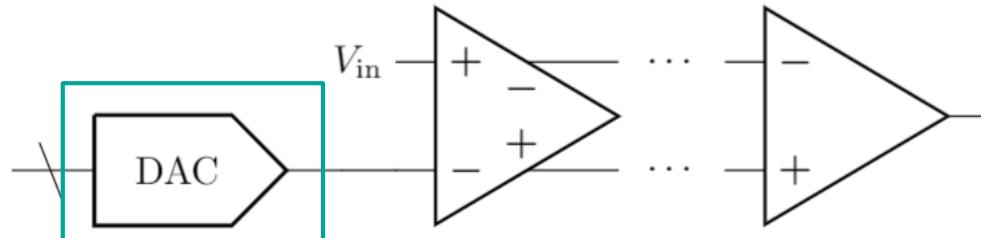
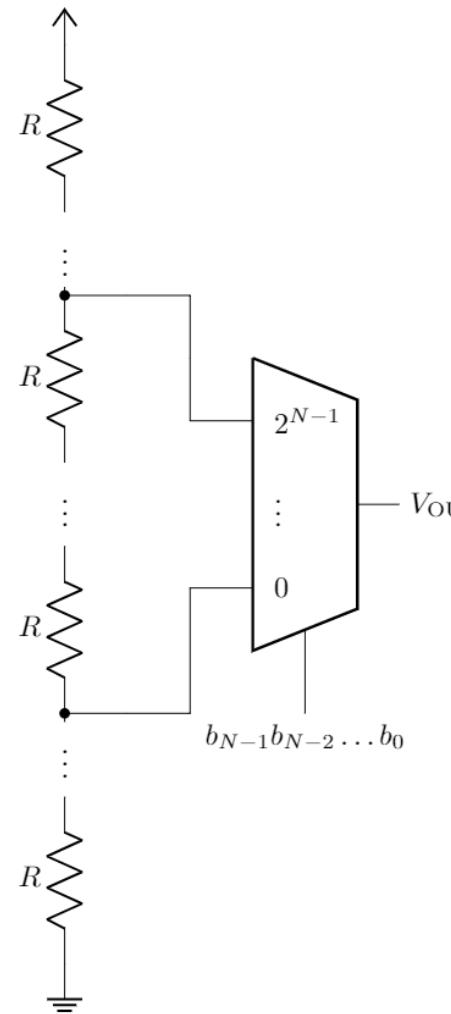
- Latchup prevention
 - Form low-Z path from well boundaries to supply
 - Prevents voltage spikes in wells turning on parasitic BJTs
- Latchup DRC common in modern PDKs
 - Very common for ESD, large-area wells



Threshold Branch

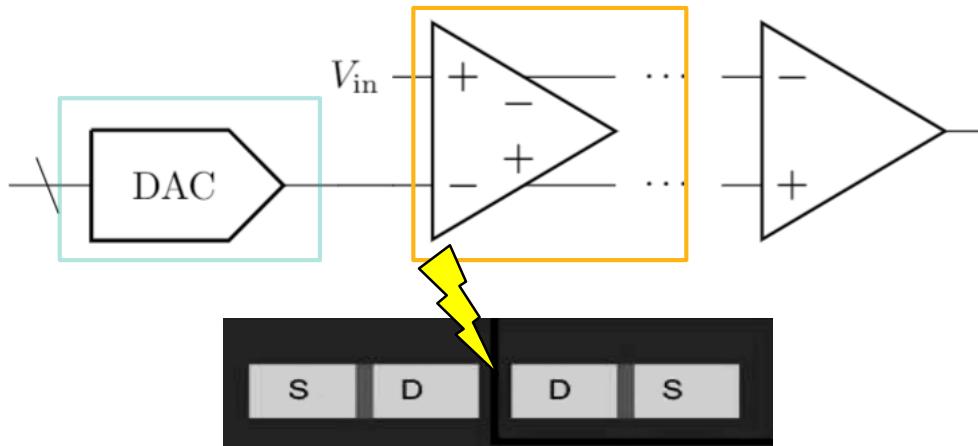
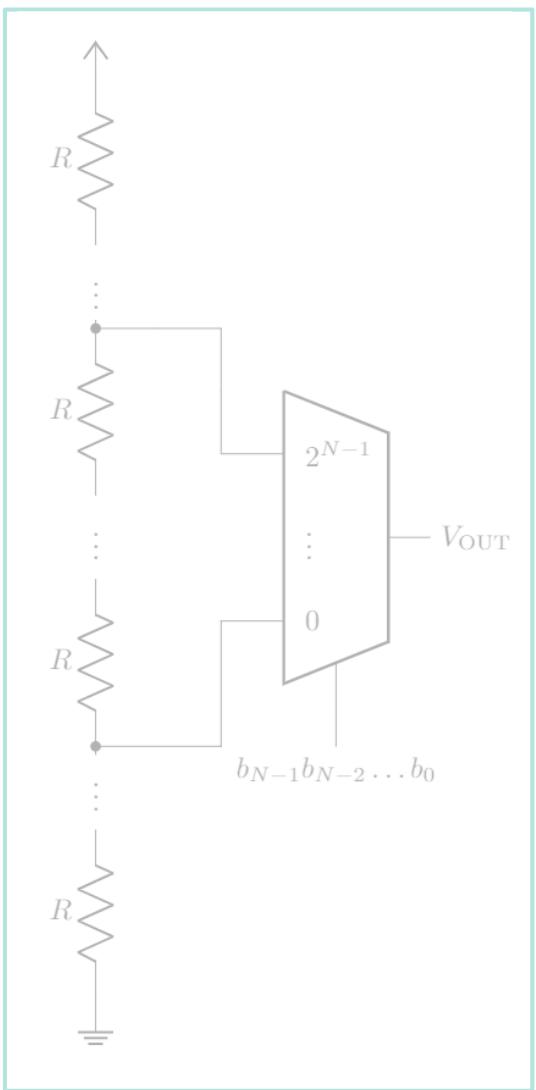


Threshold Branch

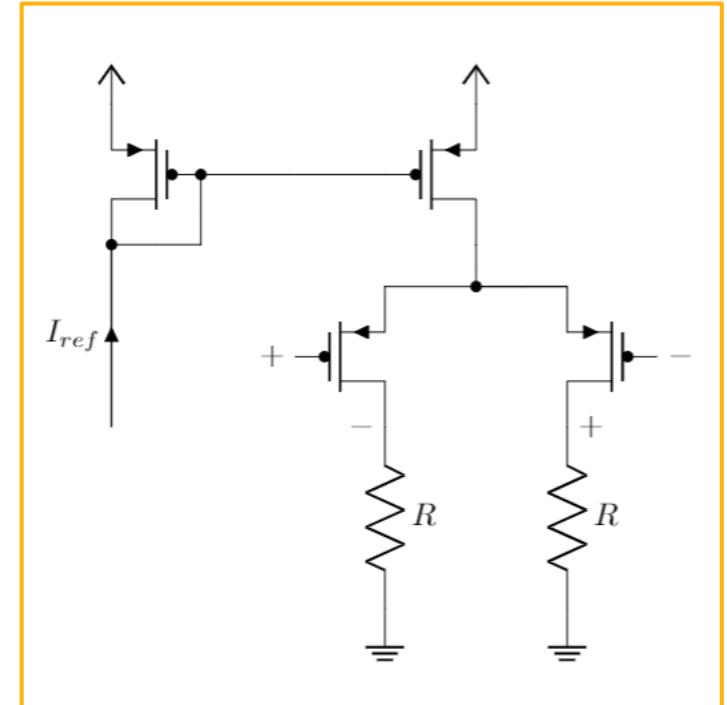


- $V_{LSB} = 3.5\text{mV}$
- 8 bits: [253mV, 1.153V]
- Binary mux (massive shared wells)
- I/O pad for testing/override

Threshold Branch

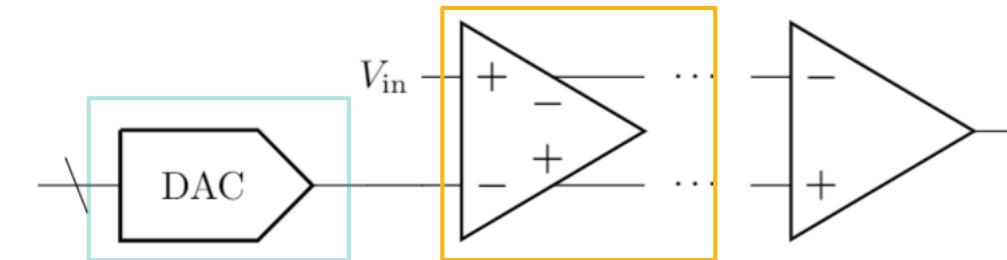
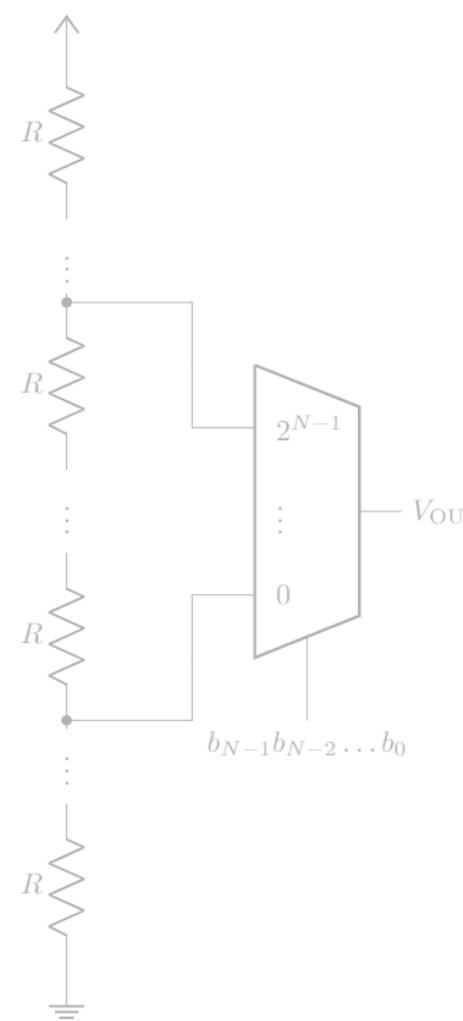


max static power
input (+ output) bias
gain bounds
min bandwidth given C_{load}
max input-referred noise
unity gain phase margin

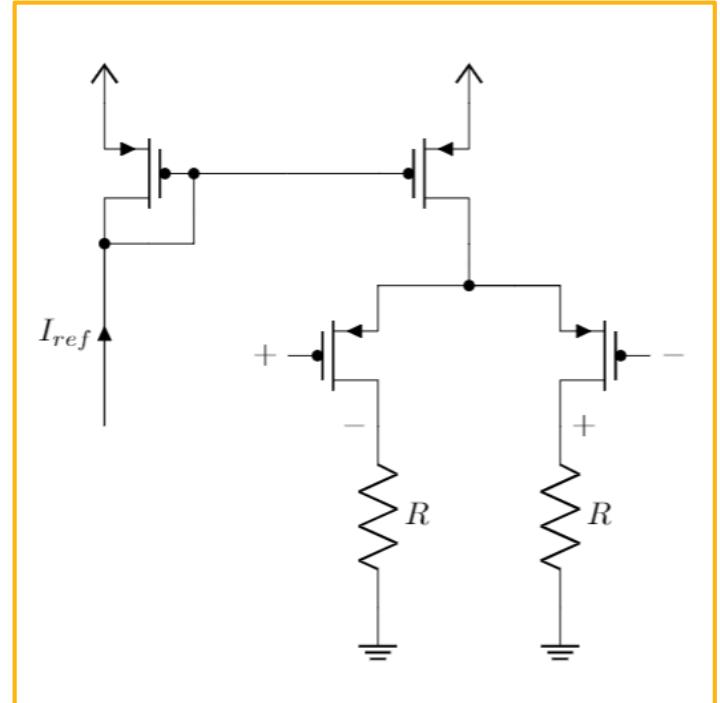


nominal resistor values
device sizes
gain, bandwidth, etc.

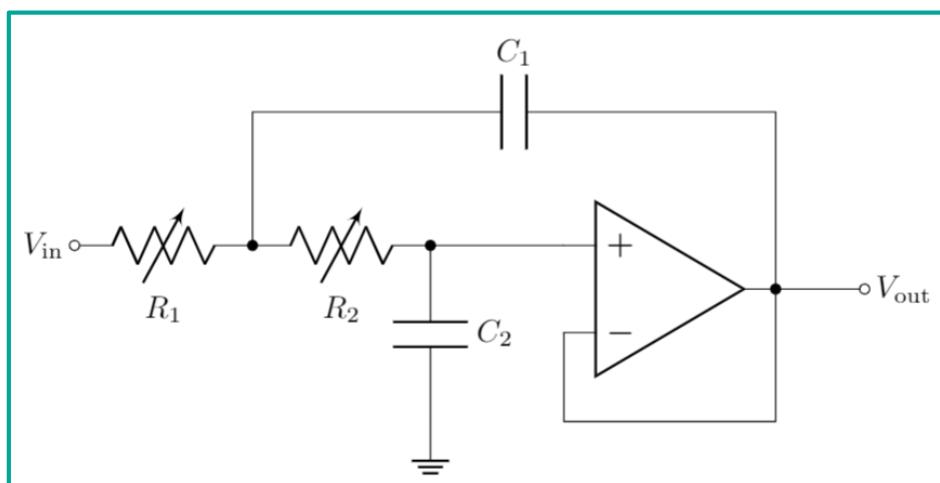
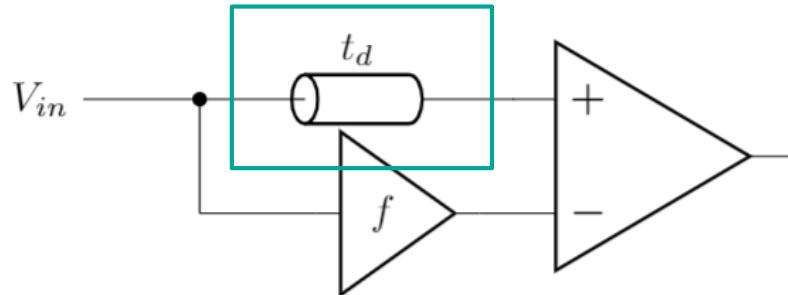
Threshold Branch



- Low gain, high speed stages
- Known current + resistors → no CMFB (saves power)
- No mismatch models ☹



Zero Crossing Detector



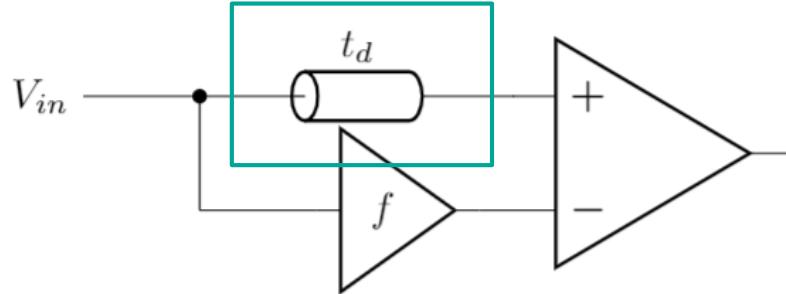
- **Theoretically:** $[T_{\text{rise,in}}, \min(T_{\text{event}}, T_{\text{stuck}})]$
- 2nd order Bessel filter (maximally flat group delay $t_{\text{delay}} = 1/\omega_0$)

$$\frac{3\omega_0^2}{s^2 + 3s\omega_0 + 3\omega_0^2} = \frac{\frac{1}{R_1 R_2 C_1 C_2}}{s^2 + s \frac{1}{C_1} \frac{R_1 + R_2}{R_1 R_2} + \frac{1}{R_1 R_2 C_1 C_2}}$$

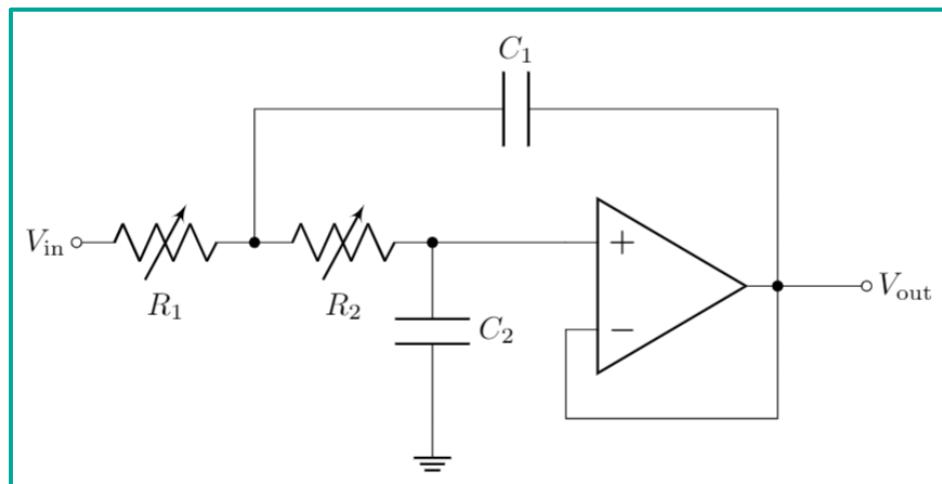
- Choose C1 and C2, then satisfy two conditions

$$R_1 R_2 = \frac{1}{3\omega_0^2 C_1 C_2} \quad R_1 + R_2 = \frac{1}{C_2 \omega_0}$$

Zero Crossing Detector



- **Theoretically:** $[T_{rise,in}, \min(T_{event}, T_{stuck})]$
- **Practically:** $[T_{rise,in}, \sim 1/f_{bw,signal}]$



target group delay

capacitor values

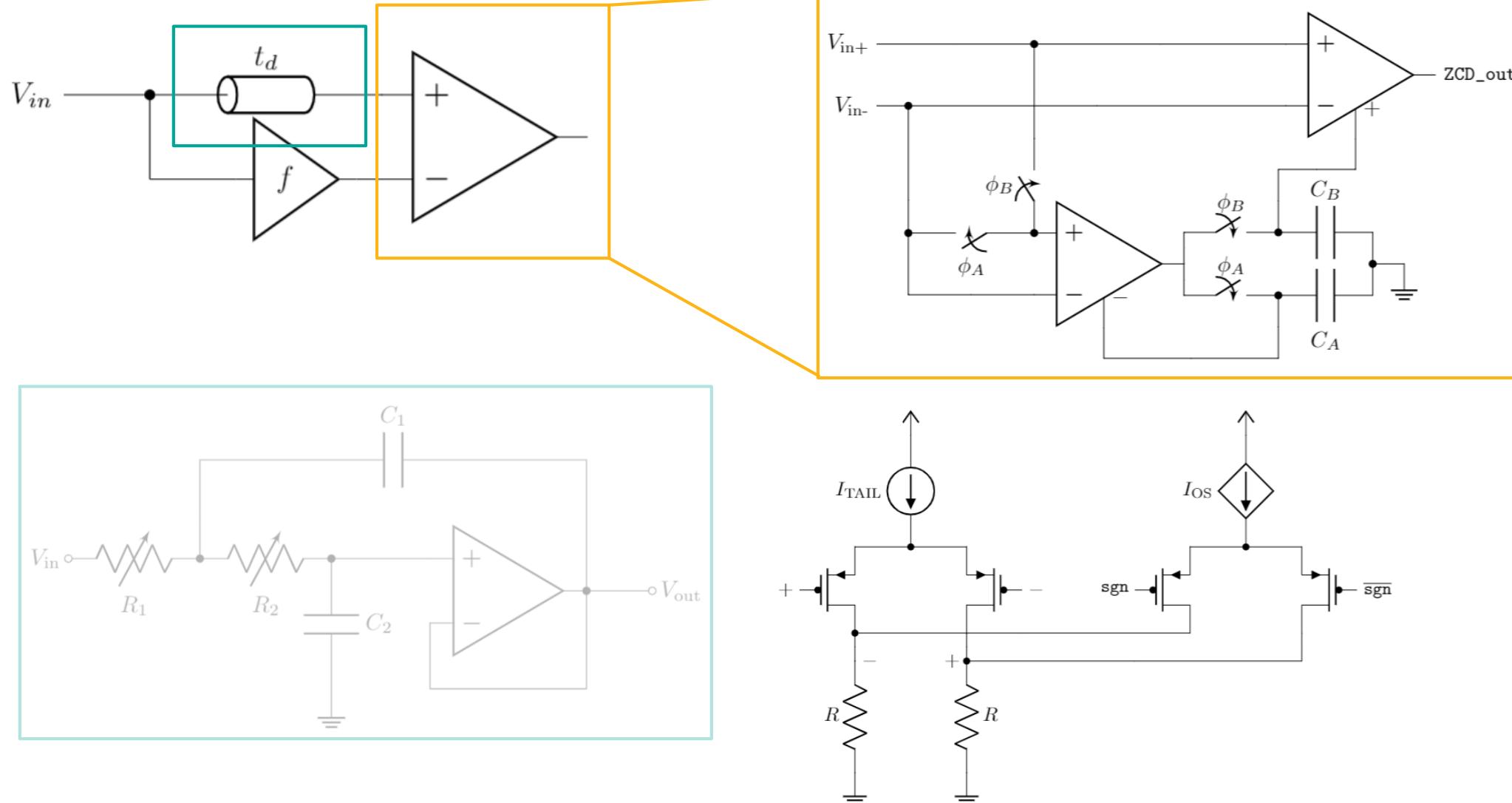
static error

max quiescent current

amplifier parameters

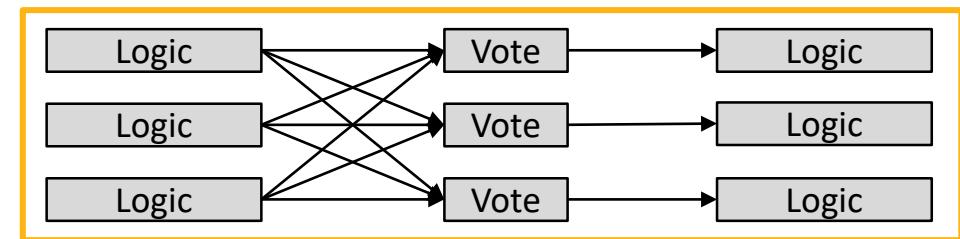
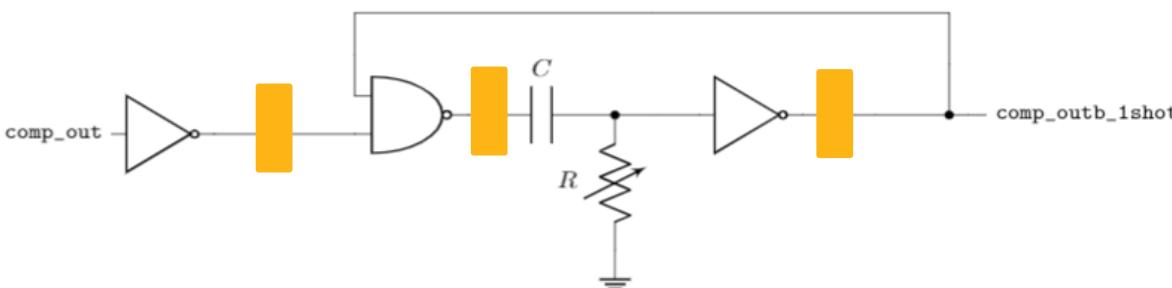
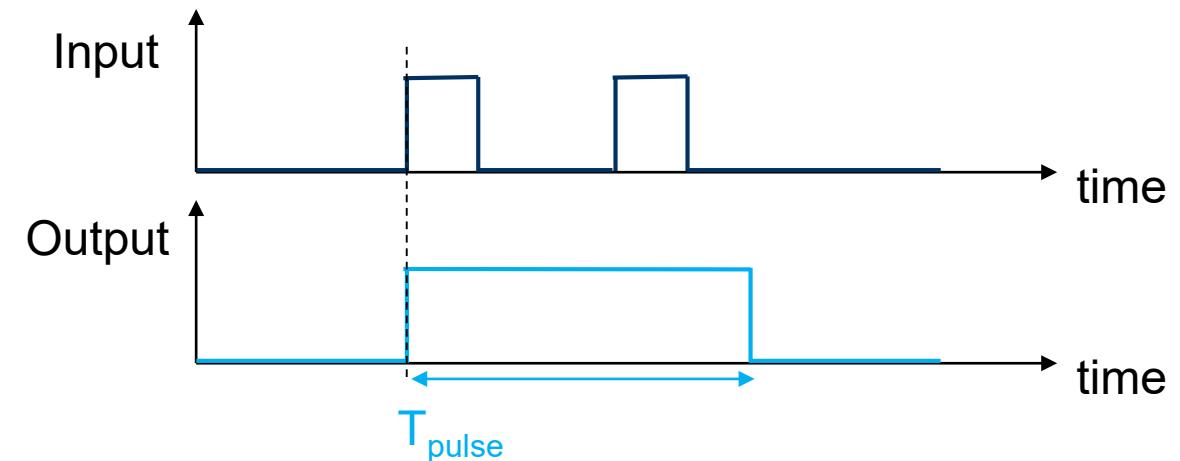
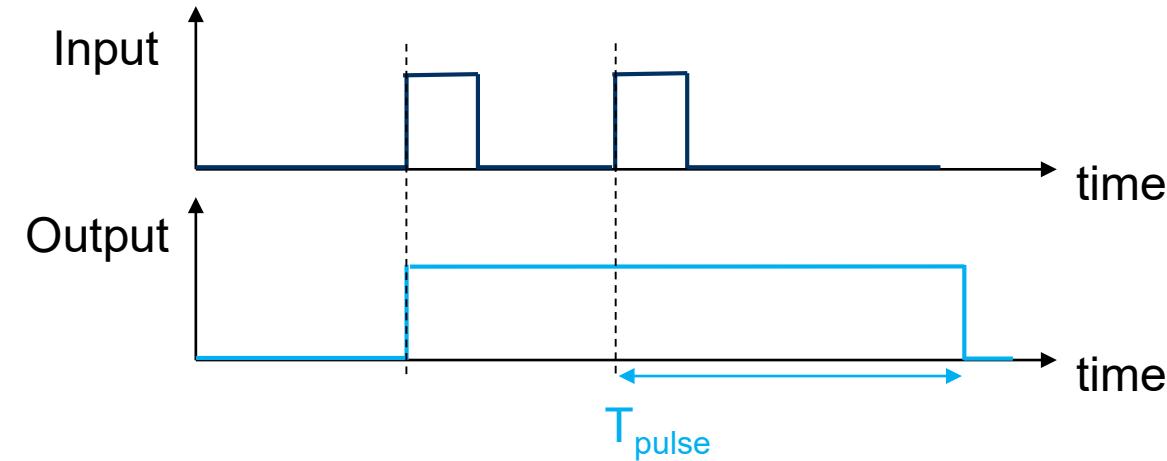
nominal passive values

Zero Crossing Detector



1-Shot Pulse Generator

- Retiggerable (left) vs. nonretriggerable (right)

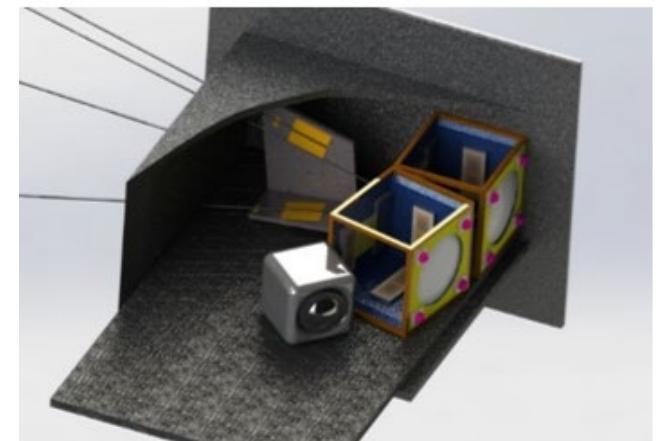
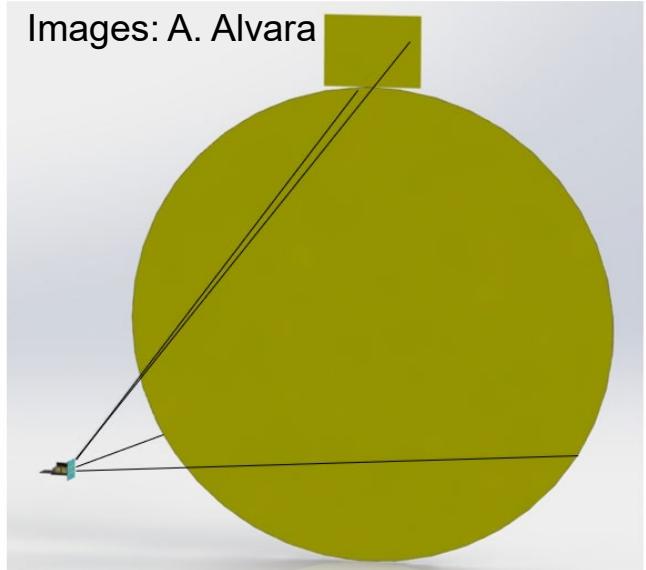


Time-of-Flight: Closing the Loop

- Blocks → signal chain
- Layout generation
- Co-optimization and making systems less “temperamental”
- Including a time-to-digital converter (currently in exploratory phase)
- Tape out in multiple process nodes

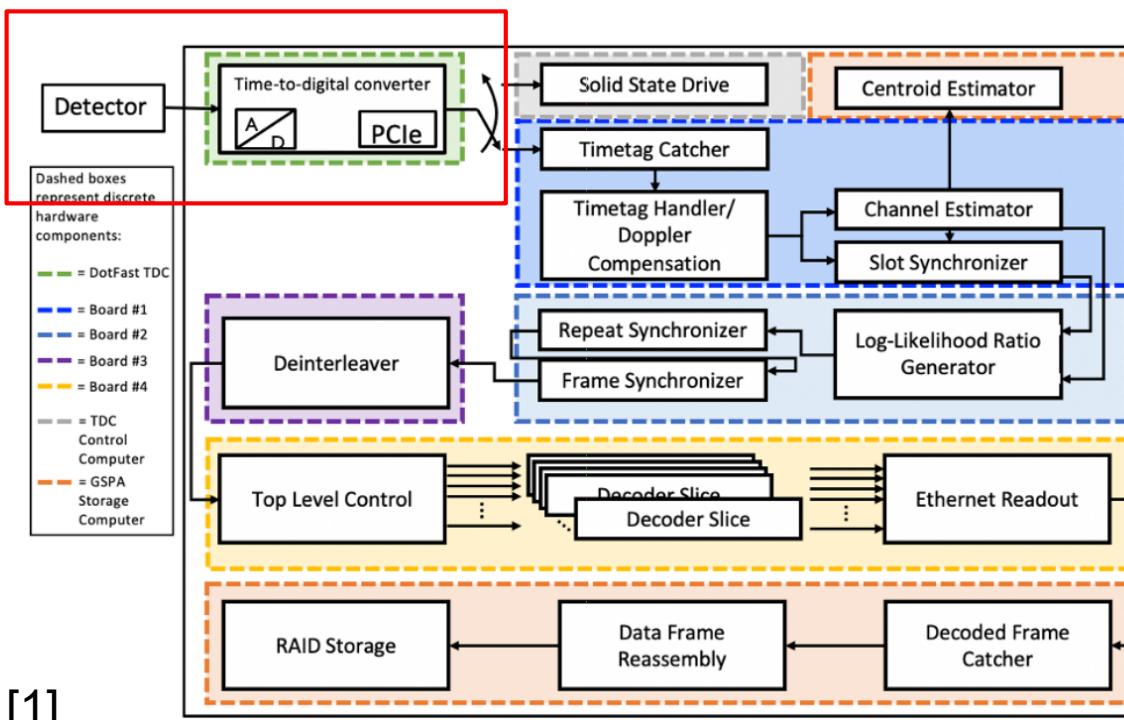
BLISS

- **Size:** smaller than a CubeSat, larger than a ChipSat
- **Mass:** $\ll 1\text{kg} \rightarrow \text{MEMS, integration is key!}$
- **Propulsion:** solar sail
- **Current Goal:** Near-Earth object imaging



BLISS: Timing-Based Communication

- Signal-starved communication → photon-counting receiver
- Serially Concatenated PPM → TDC-based receiver



[1]

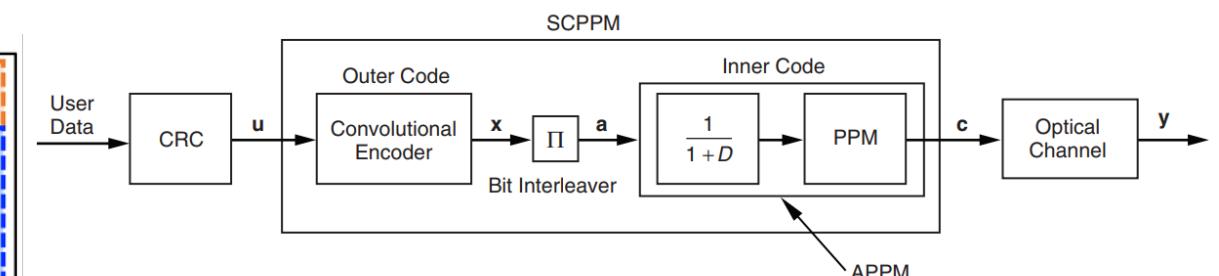


Fig. 2. The SCPPM encoder structure.

[2]

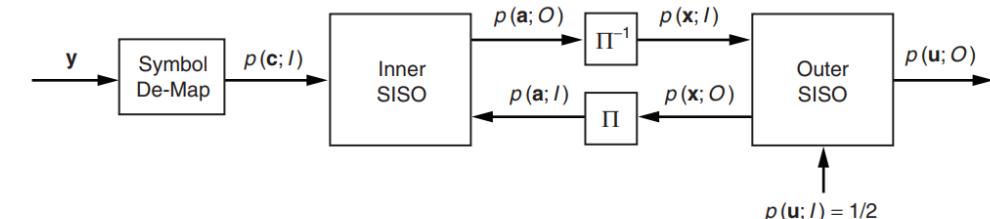
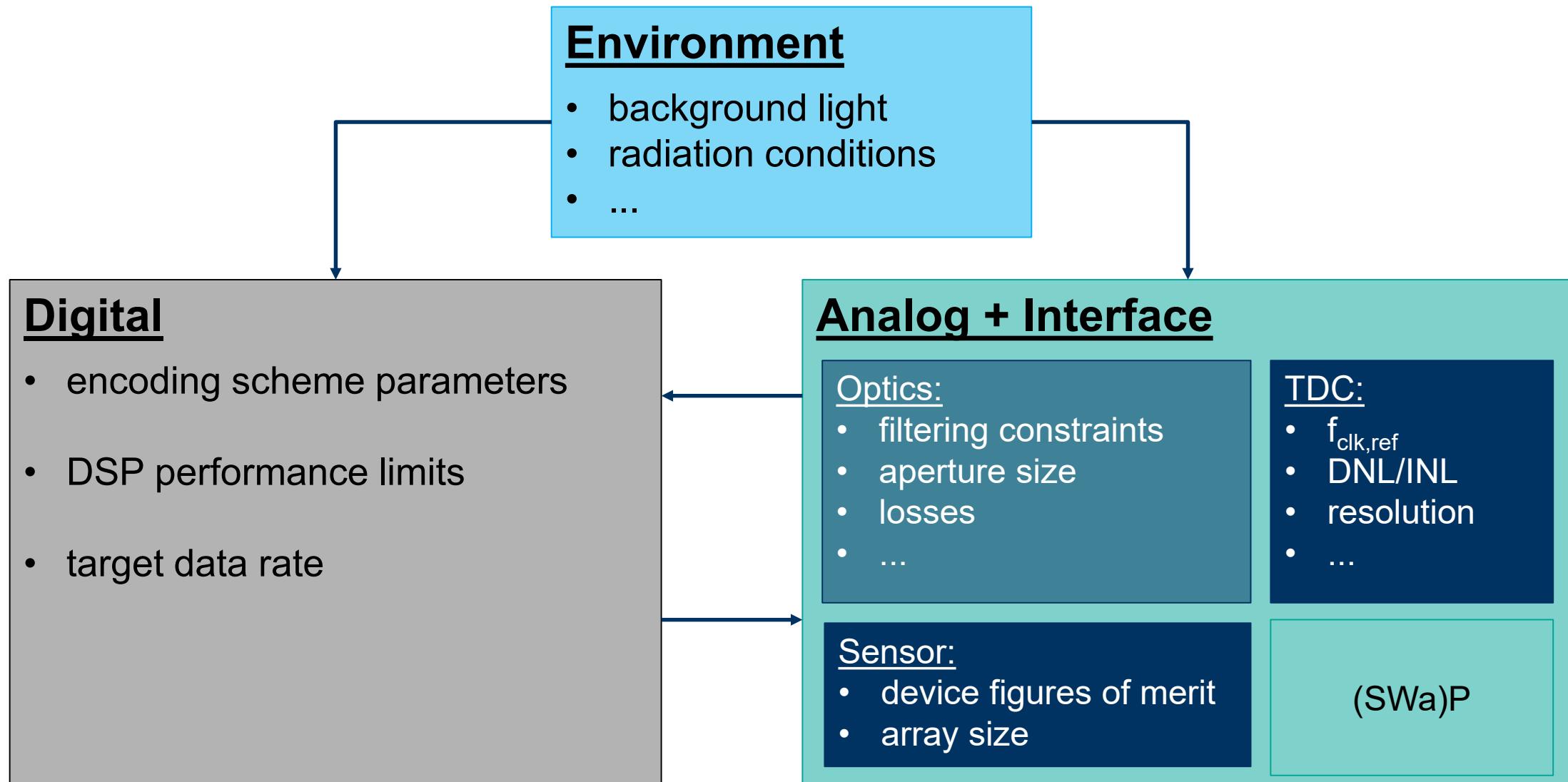
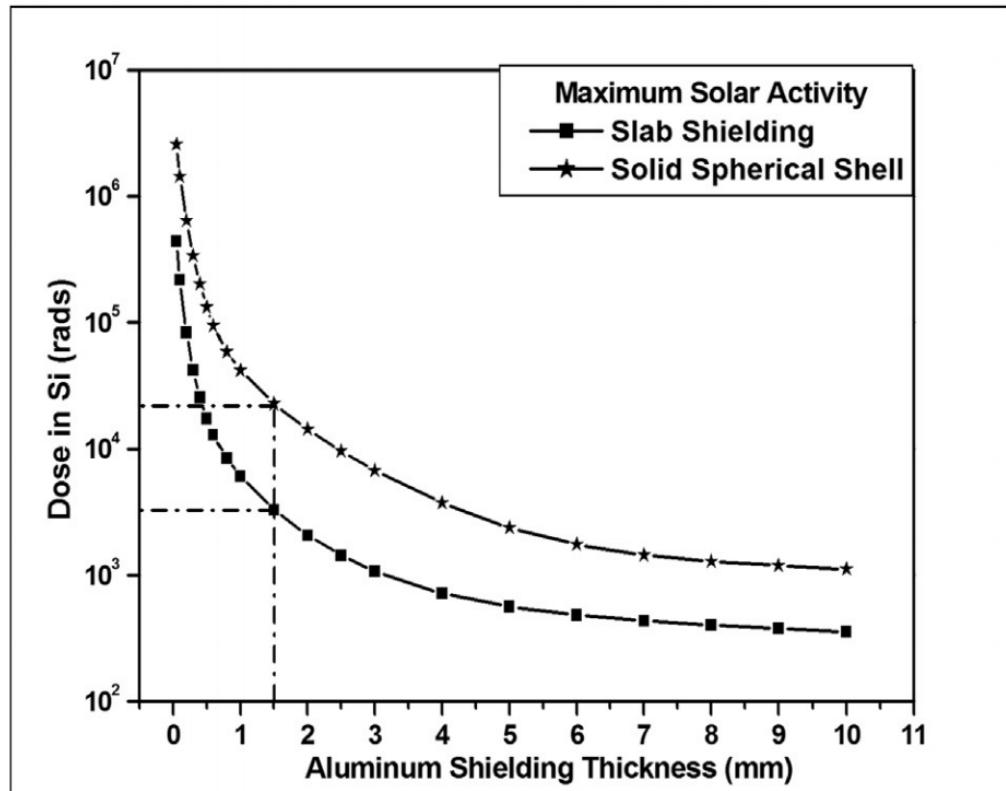


Fig. 4. SCPPM decoder.

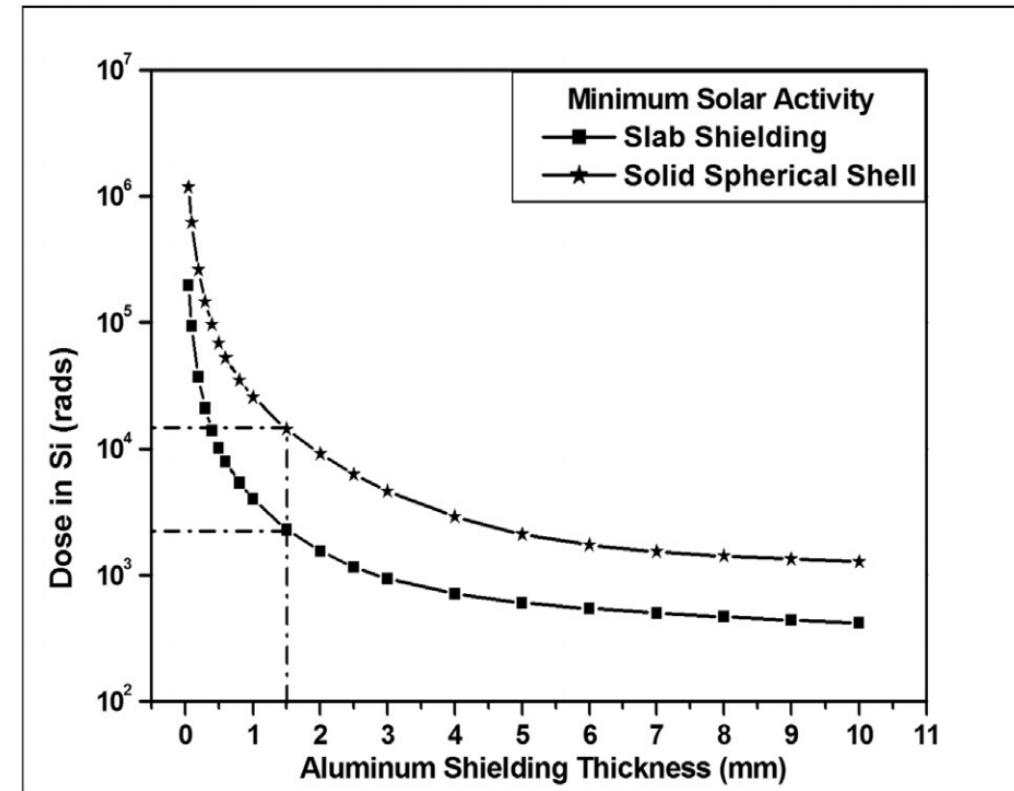
BLISS: Communication Co-Optimization



Total Ionizing Dose Over Time



(a)



(b)

Fig. 5. Total ionizing dose-depth curves for Si as a target material for a 3 year polar mission and using a Al slab shield and a Al solid spherical shield during (a) maximum solar activity and (b) minimum solar activity.

SPAN-I: Testing Hooks & Environment

Scan:

- Preamp resistor
- Delay line resistors
- Comparator AZ gain
- Attenuator
- DAC code
- One-shot pulse length
- Peak detector bypass + disable

Pads (Beyond the Usual):

- DAC output/threshold (AI/O)
- LDO output (AI/O)

Standalone Test Structures:

- Peak detector (rad validation)
- Delay filter
- Bandgap (rad validation)

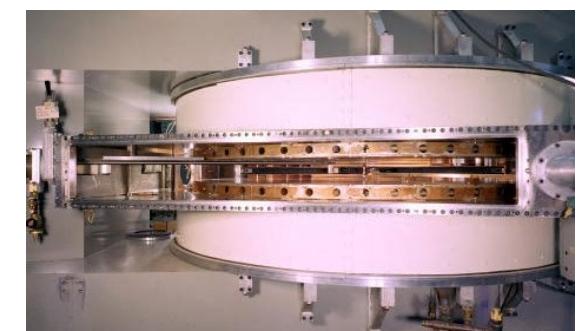
Alternative Signal Chains:

- Pad-out for external delay line
- Threshold-only chain

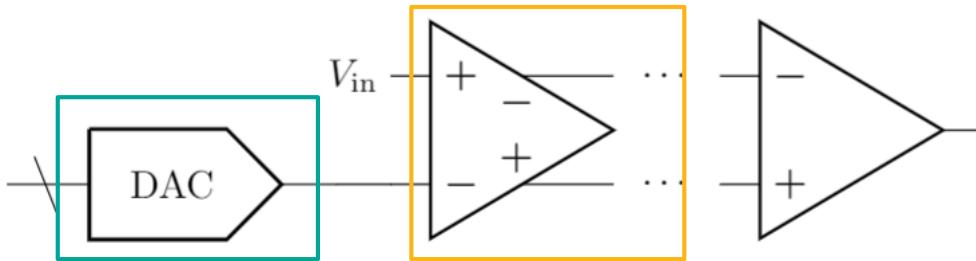
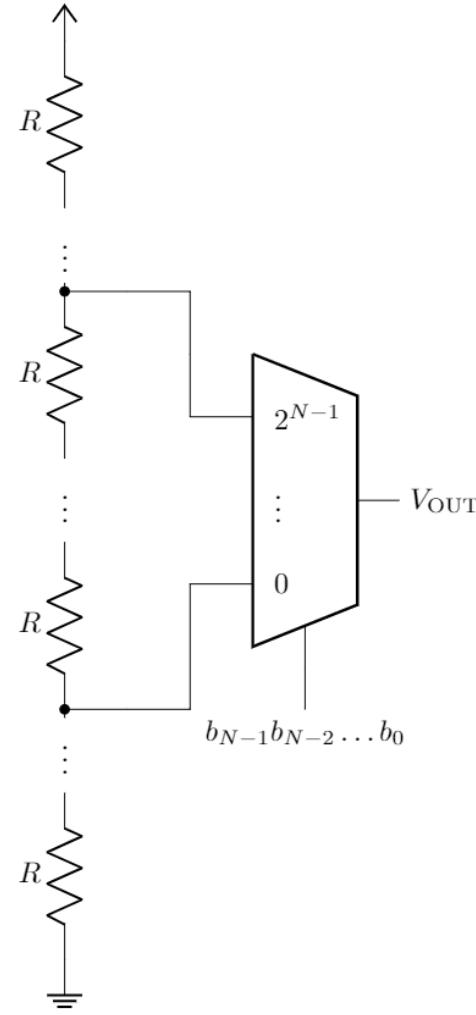


TID: 100krad (Cobalt-60)

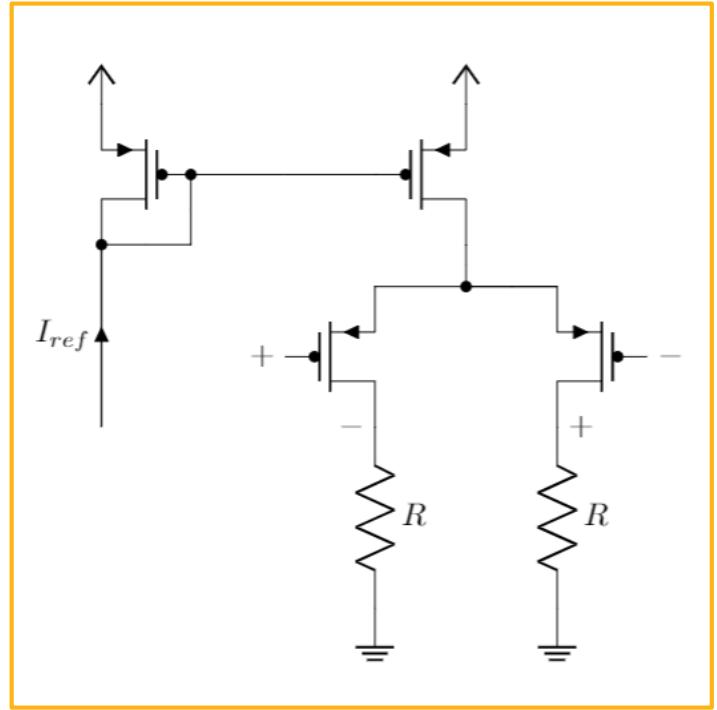
SEE: LET 1-100MeV.cm²/mg



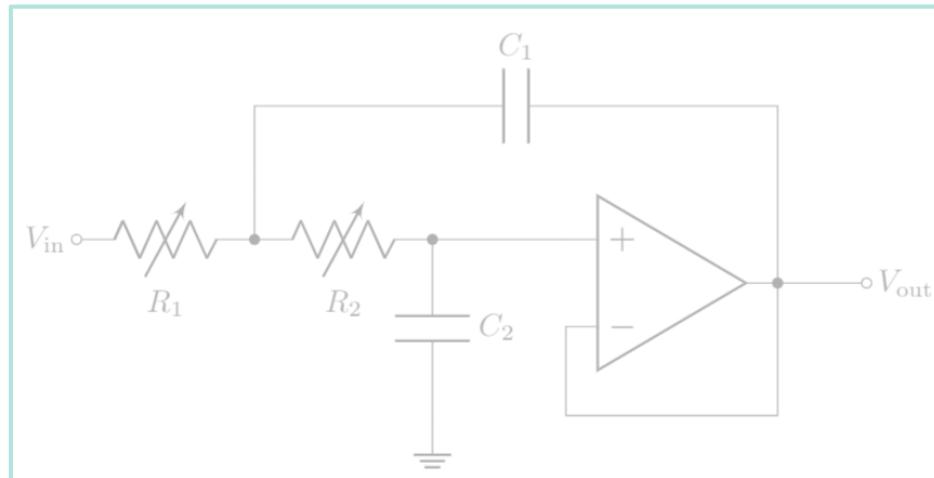
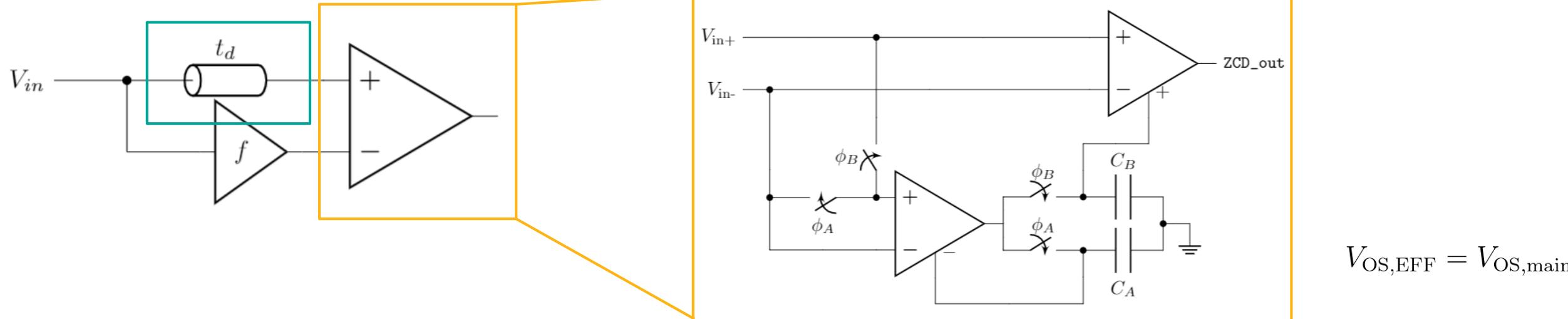
Leading Edge Detector



Parameter	Spec 1	Spec 2
Pulse Height	$300\mu\text{A}$	3mA
Rise Time	100ps	10ps
Pulse Width	1ns	100ps
Min Time Between Pulses	100ns $(\leq 10\text{Mevent/s})$	
Worst-Case Output Rising Edge Jitter	130.8ps	166.4ps
Linear Input Noise Voltage	$1.0\text{mV}_{\text{rms}}$	
I_{avg}	$665\mu\text{A}$	

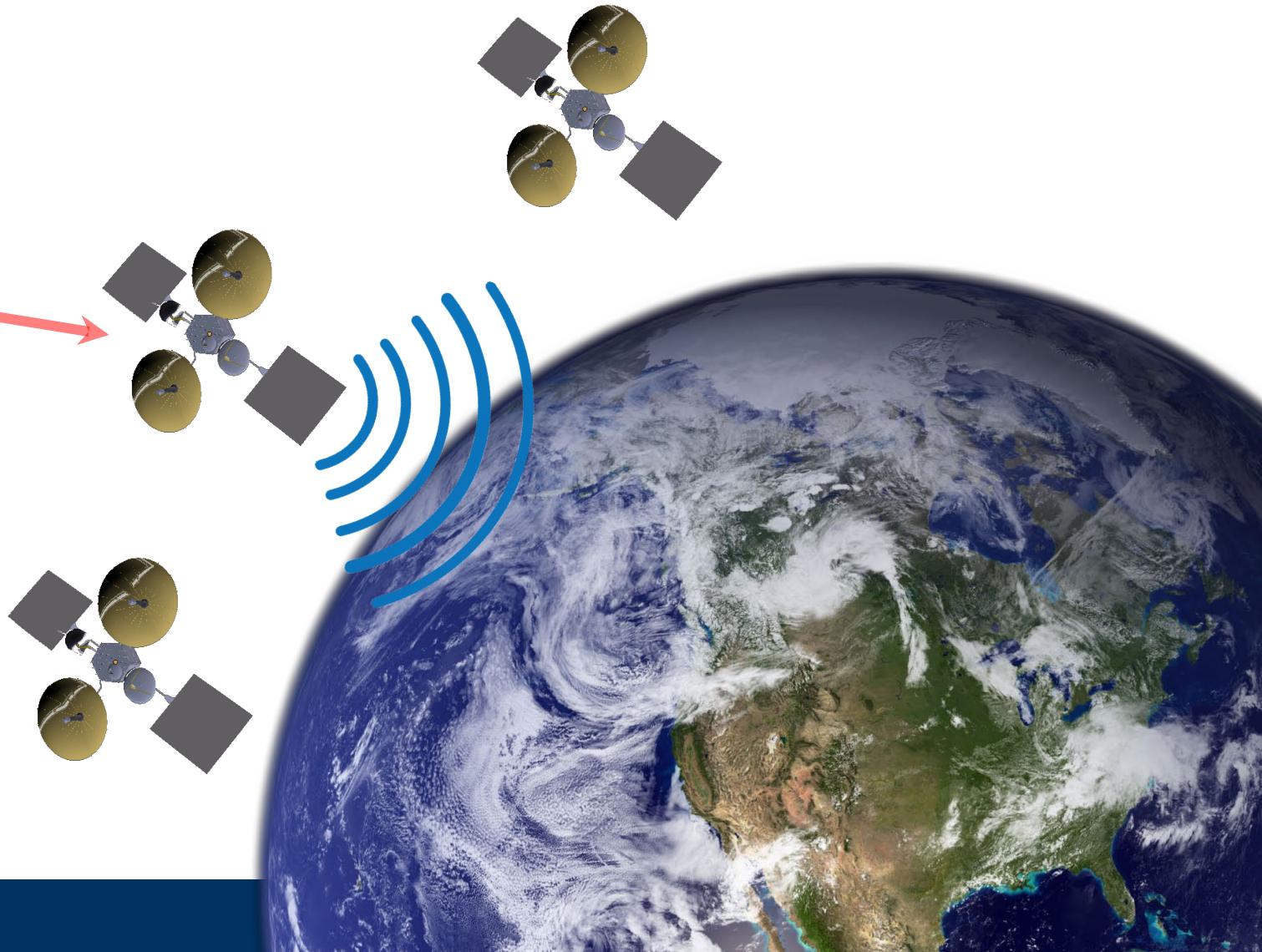
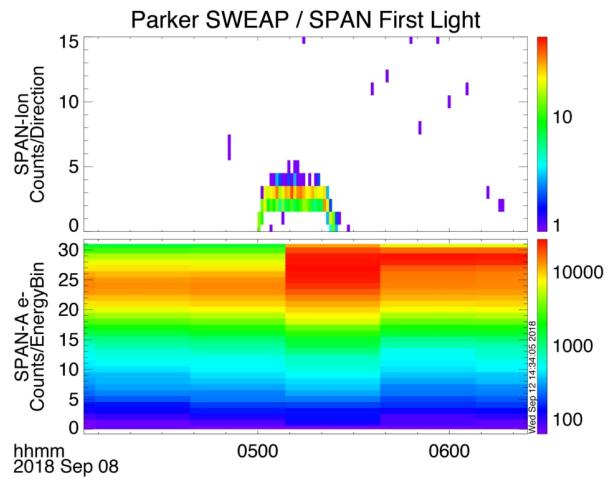
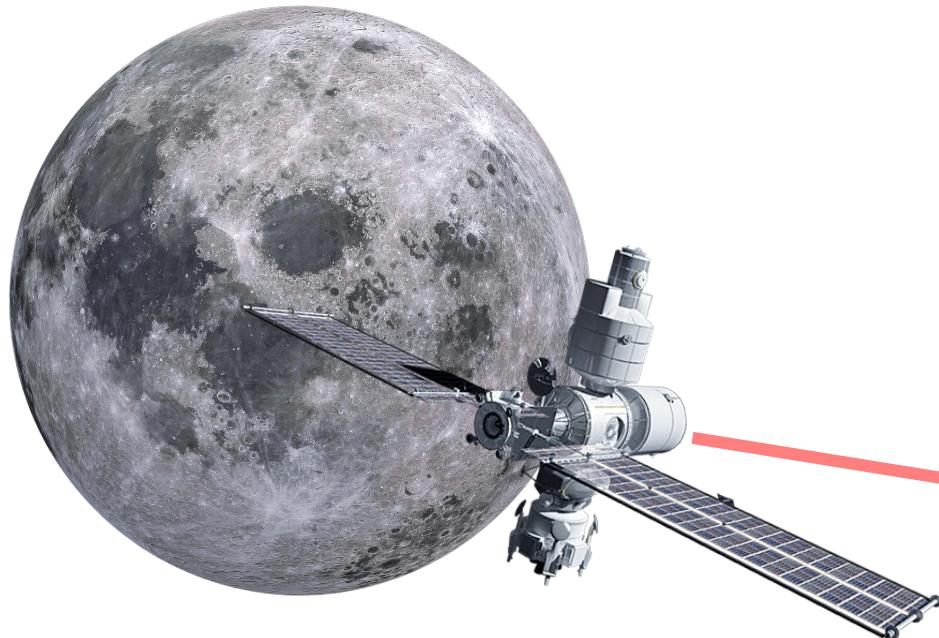


Zero Crossing Detector



Parameter	Spec 1	Spec 2
Pulse Height	300 μ A	3mA
Rise Time	100ps	10ps
Pulse Width	1ns	100ps
Min Time Between Pulses	100ns (≤ 10 Mevent/s)	
Worst-Case Output Rising Edge Jitter	178.3ps	136.3ps
Linear Input Noise	2.74mV _{rms}	
I_{avg}		840 μ A

Broad Overview



Sensors in Space

Imagers

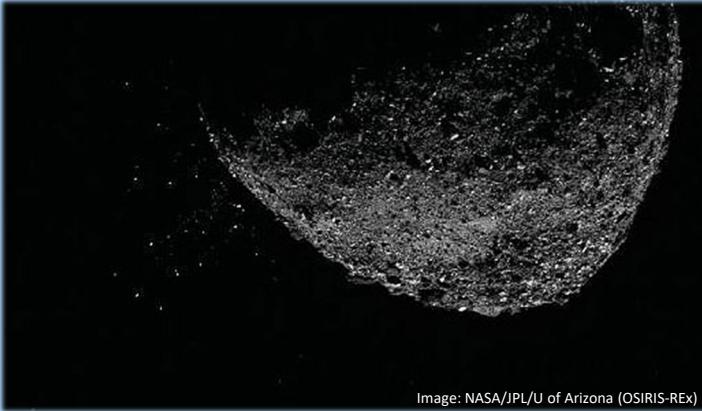


Image: NASA/JPL/U of Arizona (OSIRIS-REx)

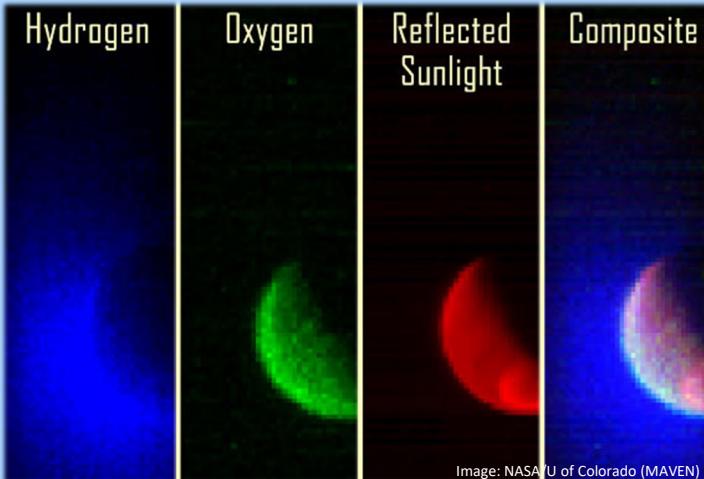


Image: NASA/U of Colorado (MAVEN)

Detection & Ranging

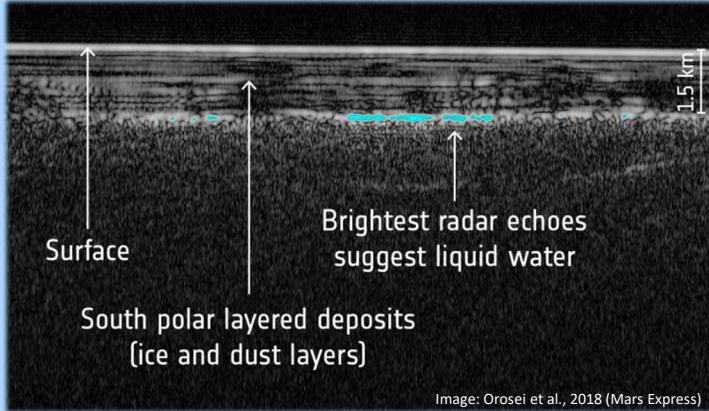


Image: Orosei et al., 2018 (Mars Express)

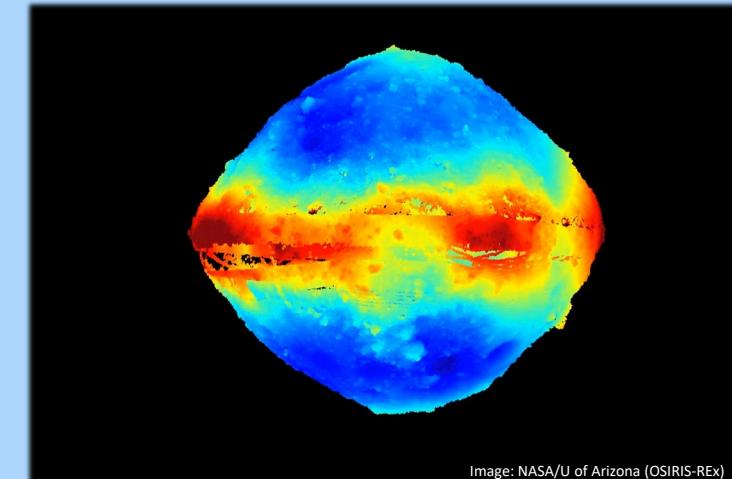


Image: NASA/U of Arizona (OSIRIS-REx)

Mass Spectrometers

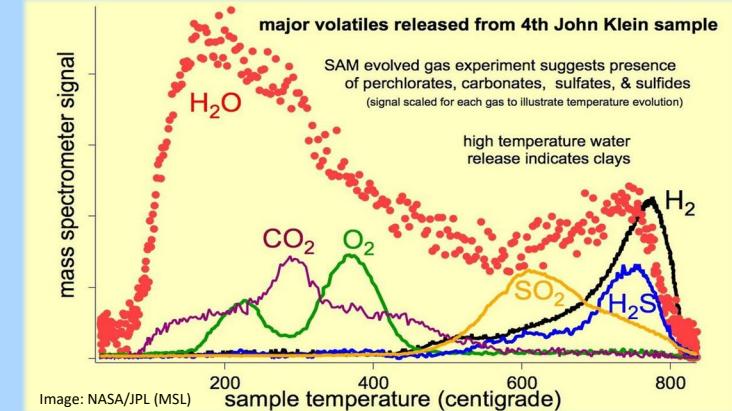


Image: NASA/JPL (MSL)

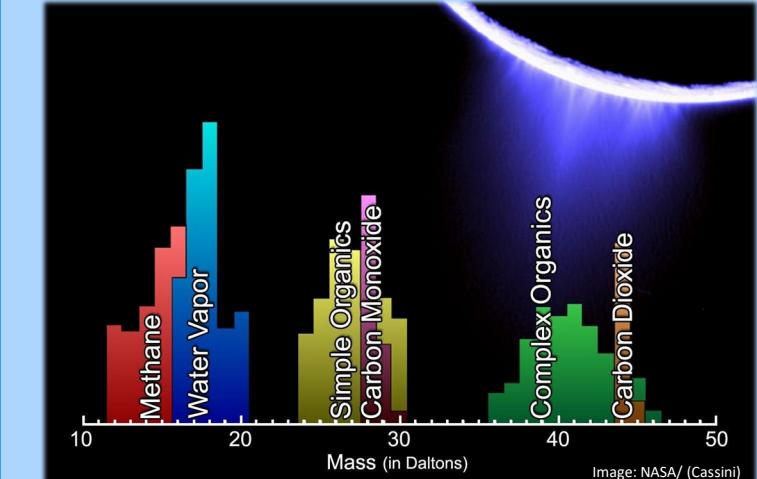
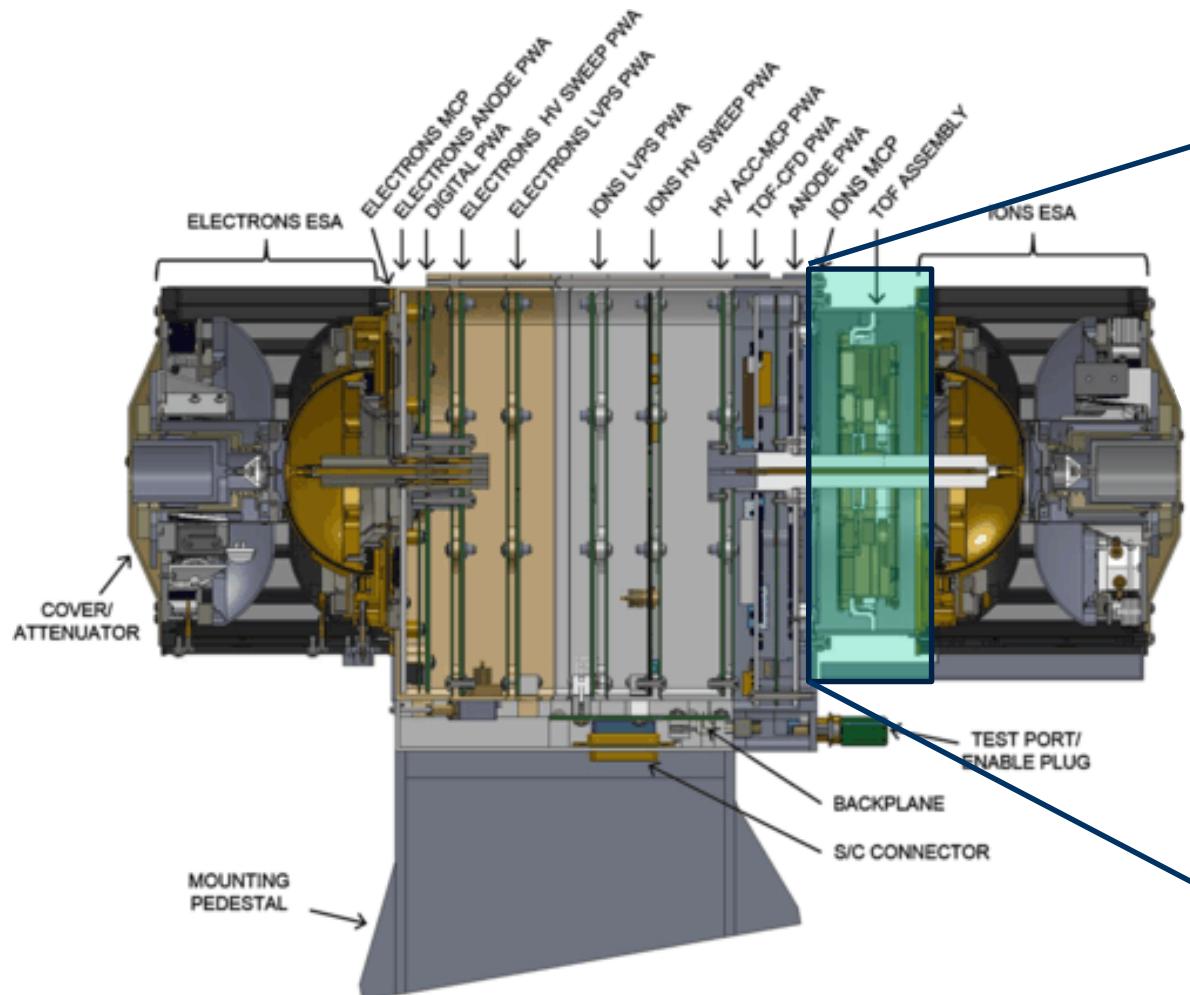
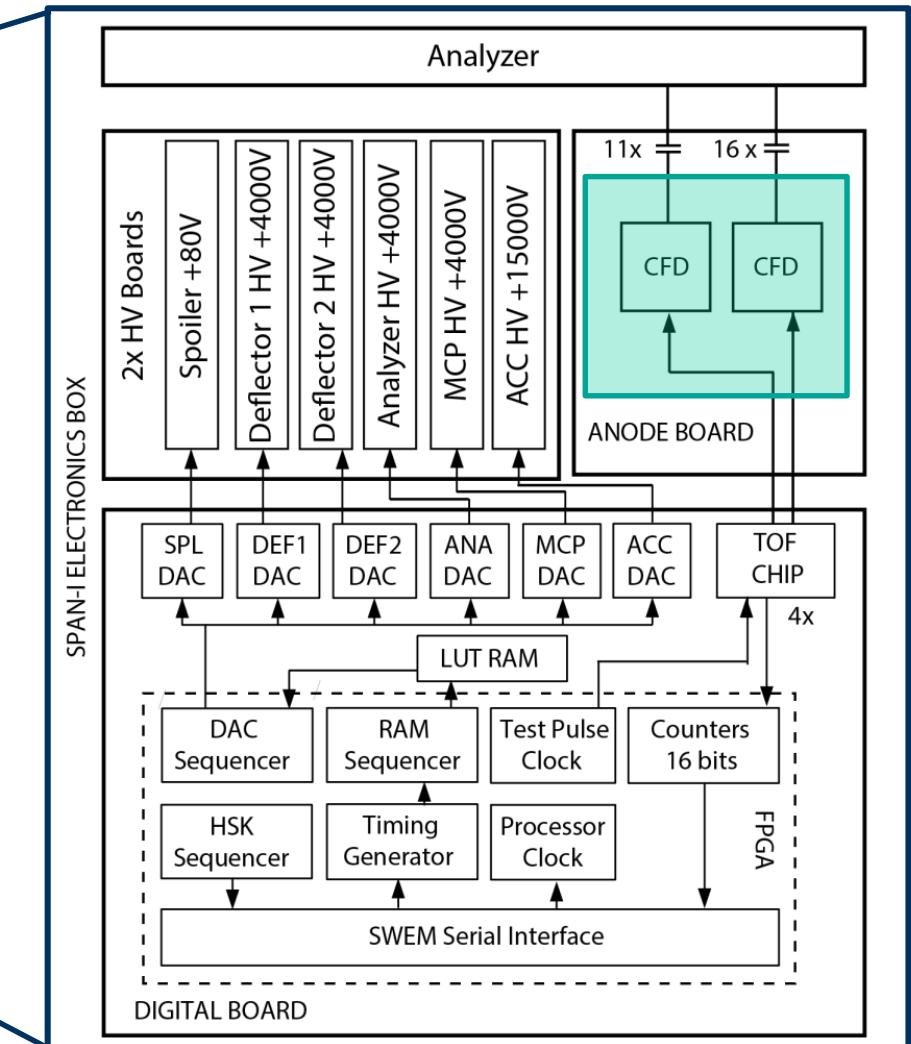


Image: NASA/ (Cassini)

Solar Probe Analyzer for Ions



[1]



Single Chip Mote: Optical Programming

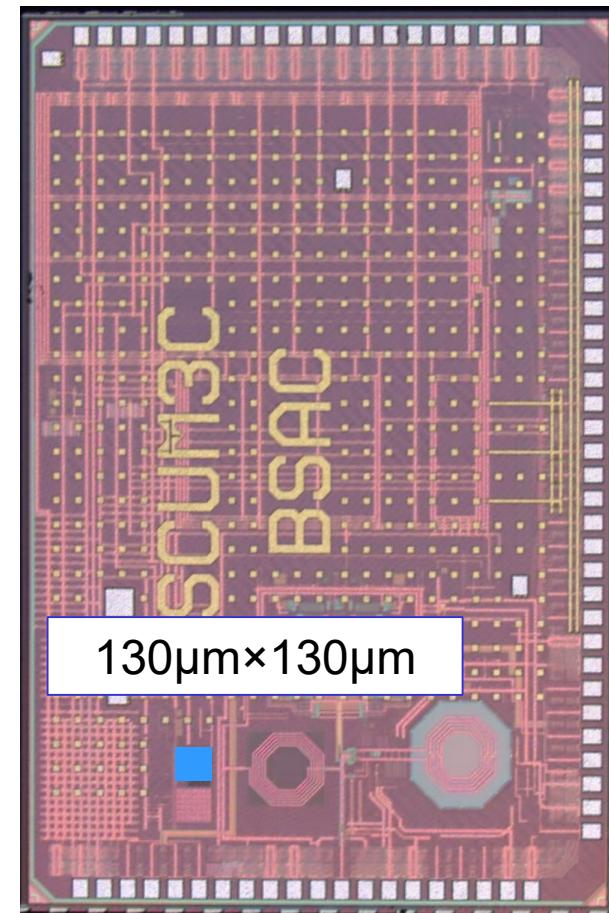
Programming

- PWM with digital counter
- DC balance during programming

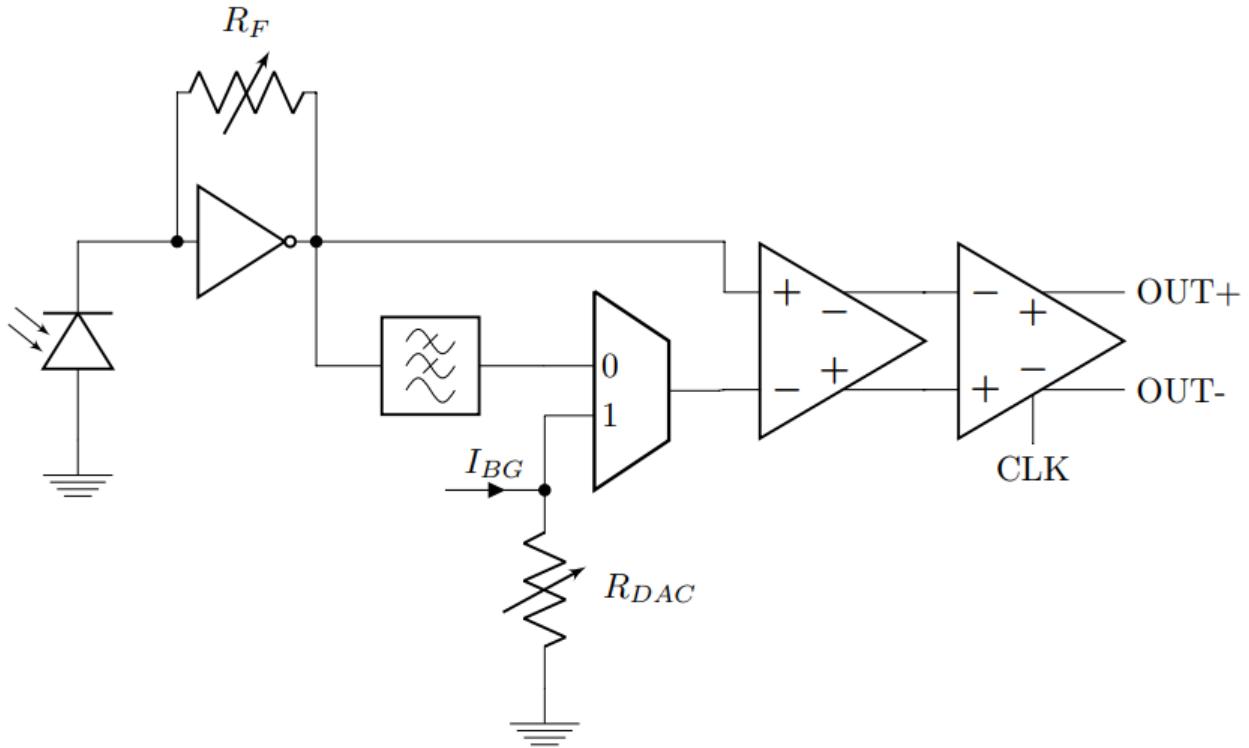
Lighthouse

- NRZ (assume no DC balancing)
- $400\text{nA}_{\text{lighthouse}}$ @ 20cm $\rightarrow 640\text{pA}_{\text{lighthouse}}$ @ 5m

Parameter	Programming	Lighthouse V2
BER	$2(10^{-8})$	10^{-3}
Yield	$\geq 99\%$ (2.6σ)	
Bandwidth	N/A	1.84MHz
Area	$130\mu\text{m} \times 130\mu\text{m}$	
Power		Minimize



Post-Layout Result



201 - 276 pA_{rms}
1.73 - 2.73 nA_{offset}

15.1 - 20.7 mV_{rms}
130 - 205 mV_{offset}

