Lye Heng Foo

Freelance Services & Developer

Penang, Malaysia

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https://lyehengfoo.tk/

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Skills

Web Design (HTML, CSS & JS)	90%
WordPress	90%
Programming & Coding	90%
Physical Design Engineering	90%
Design Automation	90%
App Development	80%
Linux & Cloud Computing (GCP, AWS)	80%
Hardware Automation (Arduino, ESP8266)	70%

Languages (Written)

English

Malay Language

Languages (Spoken)

English

Malay Language

Chinese (Hokkien & Cantonese)

Industrial Experience

Professional Services / Tagme Tech Solutions @ https://tagmetech.tk

Jul 2017 - Current

Web Development Services
Cloud Computing and Services (Google Cloud Platform, Amazon Web Services)
Android Mobile App, WebApp & Software Development
Technical Coaching/Training Provider in IT/Engineering subjects
Hardware Automation using Arduino and ESP8266 Micro-controllers

Web Developer / Freelancer.com

Jul 2017 - Current

Freelancer.com Profile: https://www.freelancer.com/u/lyehengfoo

Website Design & Website Optimization
Website Content Management System (CMS) (WordPress, Joomla & Caboose)
Web Development Frontend (HTML5, CSS, JavaScript, jQuery, BootStrap, W3CSS)
Web Development Backend (PHP, Python, Ruby/Jekyll)
Search Engine Optimization (SEO) Analytics Professional Graphics Design & Video Editing

IC Design Engineer (Senior Member of Technical Staff) / Marvell Semiconductor

Aug 2010 - Jul 2017

Job responsibilities & key accomplishments:
Technical Lead for Physical Design Enginneering - Back-End custom ASIC chip design lead (both Block level and Full-chip level) for the United States of America, Japan and China clients
Physical Design Engineeering - ASIC design from Gate-level Netlist to Physical Design and Timing signoff for Design Tapeout with EDA Tools from Synopsys, Cadence and Mentor Graphics.
Design Automation Tools Development - Enhanced the existing design planning flow (covering die size estimation and cost estimation), floor-planning, power planning and power estimation for a more accurate early-design planning and quotation purposes.
Design Automation Support - Developed and enhanced the ASIC design flow for front-end and back-end design methodology.
Early Technology Process Node Adopter - Pioneered and worked through various design issues for the early process node adoption (includes new cutting edge double patterning 16nm FinFET). Enhanced new design flow and methodology for back-end physical design for this new process node.

Design Automation Engineer (Member of Technical Staff) / Altera (part of Intel Corp now)

Mar 2000 - Aug 2010

Job responsibilities & key accomplishments:
Technical Lead for Design Automation - supporting both front-end and back-end IC Design engineers.
Design Automation through scripts/programs (Cadence SKILL, PERL, shell scripting, C++, Python, Tcl).
Design Methodology Development - circuit simulation and verification methodology, power planning and power modeling methodology.
EDA Design Tools evaluation and qualification.
Supported several EDA design tools - Cadence Virtuoso, Synopsys PrimeTime, Synopsys IC Compiler, Synopsys HSpice and HSIM for design simulation, Synopsys VCS for design verification, DRC and LVS verification tools (i.e. Synopsys IC Validator and Mentor Graphics Calibre), Apache Redhawk and Cadence LEC (formal verification tool)
Pioneered IP library management and infrastructure development (project release handshake mechanism based on Synchronicity DesignSync).
HardCopy/ASIC backend tools and flows development from scratch.
Cadence SKILL based P-CELL for custom layout drawing - In-house pioneer developer from scratch.
Cadence IC6.1 OpenAccess migration - project technical lead.
Project Management roles supporting Design Automation projects.

Custom Layout Design Engineer / Altera (part of Intel Corp now)

Apr 1998 - Mar 2000

Job responsibilities:
ASIC Physical Design (Custom Layout) layout drawing
Layout Floor-planning - Block level and Full-chip level
DRC, LVS and EM verification for the chip design
Layout Design Methodology development and continuous improvement

Manufacturing Engineer (Photo-Lithography Process) / Seagate Technology

1997 - 1998

Job responsibilities:
Technical support for photo-lithography process.
Yield improvement for photo-lithography process to achieve 5-Sigma quality.
Supervision for technicians and factory operators.

Teaching & Coaching Experience

Volunteer Teacher

2014 - Current

I am currently teaching the Weekly Dhamma Class (Buddhist Studies) at Mahindarama Sunday Pali School, Mahindarama Buddhist Temple, Penang, Malaysia. Some of the classes that I covered consists of children from kindergarten and primary school levels. And I am very familiar conducting both physical and online Zoom classes.

Corporate In-House Trainings

1998 - 2017

Conducted many Corporate In-House Trainings as part of Design Automation Engineer & Physical Design Engineer job responsibilities. These include:
Training for tool and automation flows' new users as additional service initiative to the companies that I have worked for.
Training for the tool main users (i.e. design engineers) whenever we deployed a new tool or a new automation flow after I have completed the tool evaluation or developed a new flow or design methodology.
Coaching for new fresh engineers, acting as mentor to them. As a result from these coaching, these new engineers had received more challenging responsibilities and quicker promotion. Most notable feedback from 360-degree feebacks that I received during these years of training and coaching, have had numerous time mentioned that *one of my strength has always been my clear, detailed and focused training/coaching capability.*.

Executive Diploma for Electrical & Electronics Technology

2009 - 2010

I taught the *Micro Processing Systems* and *Digital Signal Processors* modules which are part of the core subjects for the Executive Diploma in Electrical & Electronics Technology.
For this course, I designed all the course materials & assignments for this module based on the course syllabus proposal directly from UTM.
NOTE: This Executive Diploma Programme is a part of the initiative from University of Technology Malaysia (UTM) Kuala Lumpur to promote and enable working adults to study part-time for their career advancement.

Two-Day Course at PSDC for Electronics Higher Diploma.

1999

I taught *Designing with MaxPlus-II* (a Two-Day Short Course) at PSDC for Electronics Higher Diploma.
For this course, I had specially tailored all the course materials to align with Higher Diploma syllabus and ensuring its relevancy to current and future industry needs.
NOTE: This course is a part of Altera/Intel Corporate Social Responsibility (CSR) to promote its free University Program and exposure to FPGA (Field Programmable gate array) to local higher education centres.

Education

University Science of Malaysia, Penang, Malaysia

2002-2005

Master of Science (MSc) in Computer Science
Major: Computational Intelligence and Image Processing - CGPA 3.5

Modules Taken:

- Advanced Distributed Systems Concepts & Design
- Advanced Data Communication & Computer Networks
- Neural Networks & Genetic Algorithms
- Computer Security & Cryptography
- Intelligent Document Processing
- Computer Vision & Image Processing

Research Project: Colour Image Enhancement Technique (Noise Removal For Colour Images)

University of Warwick, Coventry, United Kingdom

1994 - 1997

Bachelor of Engineering (BEng) in Computer Systems Engineering
First Class Honours Degree
Award: **Texas Instrument Prize** for the *Best Overall Graduating Student* in Computer Systems Engineering for Year 1997.

Modules Taken:

- 1st Year Modules - Engineering 1, CSE 2, Computer Systems I, Logic Design, Programming II, Design of Information Structures, Semiconductor Device Electronics & Laboratory, Engineering Laboratory, and Industrial Systems.
- 2nd Year Modules - Computer Systems II, Introduction to Software Engineering, Concurrent programming concepts, Database Systems, Real-time Systems, Signal Processing, Control and Communication, Engineering Laboratory, Engineering Systems Analysis, Electronic Design I, and Automation and Robotics.
- 3rd year Modules - VLSI System Design, VLSI Architecture and Algorithms, Digital Signal Processing, Modelling and Simulation, Control I, and Control II.

Final Year Project: Hardware Design for Lithographic Pattern Generator (in Semiconductor IC Design)

MARA Science College, Kuala Lumpur, Malaysia

1992 - 1994

GCE A-Level - 3A's (Pure Mathematics, Applied Mathematics & Physics)

St. Michael's Institution Secondary School, Ipoh, Perak. Malaysia

1987 - 1991

SPM - 6 A1's and 2 C3's
SRP - 8 A1's

Certifications

Google Clould Platform Fundamentals: Core Infrastructure
» Coursera Certified - Jan 2021

Introduction to Psychology
» Coursera Certified - Jan 2021

Big Data Integration and Processing
» Coursera Certified - Dec 2020

Big Data Modelling and Management Systems
» Coursera Certified - Dec 2020

Graph Analytics for Big Data
» Coursera Certified - Dec 2020

Introduction to Big Data
» Coursera Certified - Dec 2020

Machine Learning With Big Data
» Coursera Certified - Dec 2020

Responsive Website Coding
» Coursera Certified - Nov 2020

Using Python to Access Web Data
» Coursera Certified - Nov 2020

Data Analysis Using Python
» Coursera Certified - Sep 2020

Increase SEO Traffic with WordPress
» Coursera Certified - Sep 2020

Technical Papers

Improved Technique for Merging GDSII Files Exported from Cadence DFII Layout Database
» Altera Technical Symposium 2009

Parasitic Extraction Methodology of Bump Pad Routing
» Altera Technical Symposium 2009

Structured ASIC Macro Cell Timing Model Characterization using NanoTime
» Synopsys SNUG 2008

Adaptive Vector Median Filter (AVMF) and Adaptive Vector with Trimmed-Mean Filtering (AVTMF) for Colour Images
» Robotics, Vision and Signal Processing (ROVISP) Conference 2005