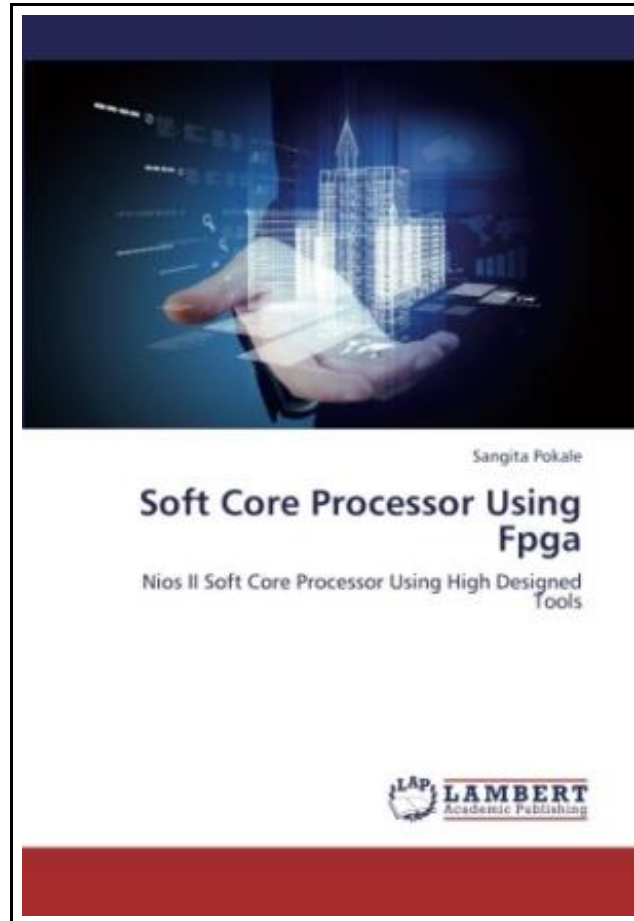


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LAP Lambert Academic Publishing Jun 2013, 2013. Taschenbuch. Book Condition: Neu. 220x150x3 mm. Neuware - This book present an application study in data logging device. The new kind of soft-core processor was designed based on NIOS II technology. The device make use of NIOS II processor provided by ALT ERA to be implemented in FPGA. NIOS II is a versatile embedded processor family that presents high performance and has been created for FPGA. Author targets implementation NIOS II soft core processor from Altera FPGA Platform. Also one of the FPGA vendor XILINX, are providing Micro Blaze & Pico Blaze RISC architecture. This is of 32 bit processing architecture. Author has implemented one simple digital circuit design on implementation of 8 bit asynchronous counter along with multiplexed seven segments LED Display Driver. For HDL based circuit design Xilinx synthesis tool version 9.1 was used. Also after having success in this implementation author has implemented NIOSII soft core processor using QuartusII 10.1 & SOPC Builder Tool from Altera. It reduces the hardware without changing the design by using SOPC approach. It will definitely help the people who are having the field interest in FPGA , ALTERA and NIOS II. 52 pp. Englisch.



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