Design Service PDK group, Marketing & Sales,
Semiconductor Manufacturing International Corporation

SMIC Process Design Kit (PDK)

Release Note & Revision History

PDK Code	SPDK65LLRF_121825_2TM_CDS
EDA Platform	Cadence
Title	SMIC 65nm Logic Low Leakage & RF 1.2/1.8/2.5V 1P10M ~ 1P6M with 2 top metals Cadence PDK
PDK Revision	0.4.1
Release Date	2010-03-09

Document Level: (For Engineering & Quality Document) ☐ Level 1–manual ☑ Level 2–procedure/SPEC/report ☐ Level 3–operation instruction
Security Level: ☐ Security 1 –SMIC confidential ☑ Security 2–SMIC restricted ☐Security 3–SMIC Internal

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RELEASE NOTE

1	**Design Platform and versions:**	Cadence DFII version 5141_USR5 or above, Virtuoso schematic editor, VirtuosoLE & VirtuosoXL, Virtuoso ADE Environment, Spectre 6.2.1, hspiceD, Assura 3.20 or above, including DRC/LVS/RCX.
2	**PDK Reference Manual**	*<pdk_install_directory>*/docs/ PDK_ReferenceManual_65LLRF_121825.pdf
3	**Customization/ Special SPECs**	N/A
4	**Known problem & solutions**	(1) There may be offgrid DRC warning reported in inductor area because of the octagonal shape, user could waive it. (2) There may be M1.4 (min. m1 area) DRC violation in base cell layout like mosfets, diodes…etc for S/D connection or pin connection, this error would disappear when designer connects this metal out in real design.
5	**Update design with new PDK**	Execute utility by typing “PasFlexUpdateLib” in CIW. Please refer to PDK Reference Manual, part-19, “Update CDFs Utility” for details.

REFERENCE DOCUMENTS			
Document NO.	**Doc Rev**	**tech rev**	**Document Title**
TD-LO65-DR-2001	8R	1.3	0.065um Logic 1P10M Salicide 1.0(G) or 1.2(LL)/1.8/2.5.or 3.3V Design Rules
TD-LO65-DR-2002	1T	0.2	65nm Logic 1P10M Salicide 1.0 (1.2 for LL) / 1.8 / 2.5 or 3.3V DFM Rules
TD-LO65-SP-2005	0R	1.0	65nm Logic Low Leakage Salicide 1P10M (1P9M, 1P8M, 1P7M…) 1.2V/1.8V/2.5V (Overdrive to 3.3V) SPICE Model(Version 1.0)
TD-MM65-RM-2001	2R	1.0	65nm Low Leakage 1P10M (1P9M, 1P8M, 1P7M…) salicide 1.2V/1.8V/2.5V RF SPICE Model.

REVISION HISTORY

Doc Rev.	Date	Developer	Reference Documents	DocRev. /techRev.	PDK Revision Hisotry
0.4.1	2010-03-09	Zhiwei Zhao	TD-LO65-DR-2001 TD-LO65-DR-2002 TD-LO65-SP-2005 TD-MM65-RM-2001	8R / 1.3 1T / 0.2 0R / 1.0 2R / 1.0	1) add simulation parameter "nf" in logic mos. 2) modify maximum L and W of rtm1, rtm1_ckt to 20um. 3) fix offGrid bug of rfmos. 4) fix CT.2b(minimum space between two contacts is 0.13um in case contact array is larger or equal to 4X4) error of multi-finger mos. 5) fix DRC bug GT.11(poly enclosed by SN/SP) of mom with poly shielding. 6) fix laddr/waddr issue of dnw mos.
0.4	2009-12-15	Zhiwei Zhao	TD-LO65-DR-2001 TD-LO65-DR-2002 TD-LO65-SP-2005 TD-MM65-RM-2001	8R / 1.3 1T / 0.2 0R / 1.0 2R / 1.0	1) include 1P6M ~ 1P10M pdk 2) include two techfiles: "techfile_dfm.tf" is for layout follow DFM rules 3) add LFD option 4) update design rule TD-LO65-DR-2002

0.3	2009-11-26	Lucy Li	TD-LO65-DR-2001 TD-LO65-SP-2005 TD-MM65-RM-2001	8R / 1.3 0R / 1.0 2R / 1.0	1) update DR to 8R 2) update rf spice model to 2T 3) update spice model to overdirved 4) added DFM options 5) update rf devices to follow new model include rf mos, rf mos varactor, rf resistors 6) added rf mom devices 7) added overdrive 3.3V devices 8) added logic varactors 9) added logic mom
0.2	2009-04-30	Lucy Li	TD-LO65-DR-2001 TD-LO65-SP-2001 TD-MM65-RM-2001	6R / 1.1 2R / 1.0 1T / 0.2	1) debug Junction Varactor gds when length<1.5um 2) update mos parameters editable setup in layout 3) update Assura RCX
0.1	2009-04-28	Lucy Li	TD-LO65-DR-2001 TD-LO65-SP-2001 TD-MM65-RM-2001	6R / 1.1 2R / 1.0 1T / 0.2	Initial