SMIC Process Design Kit (PDK)

Release Note & Revision History

PDK Code	SPDK18EE_183350155_CDBA_CDS
EDA Platform	Cadence
Title	SMIC 0.18um EEPROM 1.8/3.3/5.0/15.5V (2P3M~2P6M) Cadence PDK
PDK Revision	1.6
Release Date	2010-8-10

Document Level: (For Engineering & Quality Document)

☐ Level 1–manual ☑ Level 2–procedure/SPEC/report ☐ Level 3–operation instruction

Security Level:

☐ Security 1 –SMIC confidential ☑ Security 2–SMIC restricted ☐Security 3–SMIC Internal
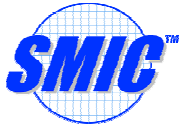
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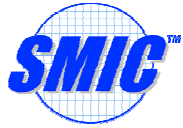|	**RELEASE NOTE**	
1	**Design Platform and versions:**	Cadence DFII version 5141_USR5 or above, Virtuoso schematic editor, VirtuosoLE & VirtuosoXL, Virtuoso ADE Environment, Spectre 6.0 or above Assura 3.20 or above, including DRC/LVS/RCX.
2	**PDK Reference Manual**	*<pdk_install_directory>*/docs/ PDK_ReferenceManual_018EE_183350155.pdf
3	**Customization/ Special SPECs**	N/A
4	**Known problem & solutions**	1) The resistors is recommended to keep sq(Length/Width) >= 5. 2) For 2P3M ~2P5M design,if need simulate "top metal resistor", need modify device name in model card from "rm6" to "rm5"("rm4"..."rm2"). 3) For TIM resistor, the "MINUS" port is connected to the GT port. The volgate connected to "PLUS" port must lager than the voltage connected to "MINUS" port.
5	**Update design with new released PDK**	Apply utility by typing "PasFlexUpdateLib" in CIW. Please refer to PDK Reference Manual, part-19, "Update CDFs Utility" for details.

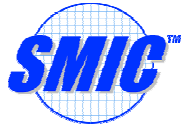|	**REFERENCE DOCUMENTS**		
Document NO.	**Doc Rev**	**tech rev**	**Document Title**
TD-EE18-DR-2002	10T	0.9	0.18um e-EEPROM 2P3M(4M/5M/6M) salicide 1.8V/3.3 V/5.0V/15.5V Process Layout Design Rule
TD-EE18-SP-2001	12R	1.8	0.18um EEPROM 2P4M Salicide 1.8/3.3/5/15.5V Spice Model (Version 1.8)

Design Service PDK group, Marketing & Sales,
Semiconductor Manufacturing International Corporation

REVISION HISTORY					
Doc Rev.	Date	Developer	Reference Documents	DocRev. /techRev.	PDK Revision Hisotry
1.6	2010-8-10	Xiurong Chen	TD-EE18-DR-2002 TD-EE18-SP-2001	10T/0.9 12R/1.8	1) Design rule updated to 10T. 2) Spice model updated to 12R 3) Add M6 option upon request 4) Update following model name based on new spice model: pip/pip_ckt/mim/mim_ckt/rtimsab_ckt/rtimsab/pvar18_ckt to pipe2r/pipe2r_ckt/mime2r/mime2r_ckt/rtimsabe2r_ckt/rtimsabe2r/pvar18e2r_ckt 5) Add guardring option for p155e2r. 6) Add metal Slot on large size diode 7) Fix bug of PIP layout. 8) Add option of "partial SAB cover" for PIP.

1.5	2009-3-6	Lucy Li	TD-EE18-DR-2002 TD-EE18-SP-2001	9T / 1.0 7R / 1.4	1) Update Spice model & Design rule 2) Update DRC/LVS/RCX deck 3) Add 1.8V native nmos nz18e2r 4) Add mos varactor pvar18_ckt 5) Update mim capacitor 6) Debug mim/pip ams netlist 7) Update techfile 8）add mim_ckt and pip_ckt 9) Change mos watermark to VISA (63:63) 10) remove tc1, tc2 from resistors HspiceD netlist
1.4	2007-12-21	Lucy Li	TD-EE18-DR-2002 TD-EE18-SP-2001	7T / 0.8 4R / 1.3	1) Update design rule TD-EE18-DR-2002 to 7T 2) Update DRC/LVS deck 3) Fix P155E2R device tap error 4) Fix mos tap error when abutment 5) Add dummy layer RESP1 for 3T poly resistors 6) Remove "c" parameter and add "w/l" in mim/pip simulator netlist

1.3	2006-6-15	Lucy Li	TD-EE18-DR-2002 TD-EE18-SP-2001	6T / 0.7 4R / 1.3	1) Update Spice model TD-EE18-SP-2001 to 4R 2) Update PIP bottom plate extension outside top plate 3) Update techfile with prRules 4) Add EEPROM cells NCG and NSG 5) Add pnp33 devices 6) Add subckt and _3t resistors
1.2	2006-8-31	Lucy Li	TD-EE18-DR-2002 TD-EE18-SP-2001	5T / 0.6 2R / 1.1	1) Update DR TD-EE18-DR-2002 version 5T-> 6T 2) Fix P155E2R device connect problem 3) Add MIM device according to customer's request.
1.1	2006-8-11	Lucy Li	TD-EE18-DR-2002 TD-EE18-SP-2001	5T / 0.6 2R / 1.1	1) Modify the techfile symbolic M4_M3, M4 enclosure V3 0.42->0.09. 2) Fix P155E2R device abutment problem. 3) Add dummy layer CGDUM, GPDUM for CG and GP. Change DUMGT to GTDUM, DUMAA to AADUM.
1.0	2006-7-28	Lucy Li	TD-EE18-DR-2002 TD-EE18-SP-2001	5T / 0.6 2R / 1.1	Initial release