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A 9 GHz Dual-Mode Digitally Controlled Oscillator for GSM/UMTS Transceivers in 65 nm CMOS

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***Abstract*— A 9 GHz fully digitally controlled oscillator implemented in 65 nm CMOS technology is presented. This is the first DCO implemented at 9 GHz which covers all transmitter (TX) and receiver (RX) bands of GSM/EDGE and UMTS except Band VII (Table I). It covers a coarse tuning range from 6.35 GHz to 9.15 GHz which is realized by binary weighted switchable capacitors. The phase noise performance meets the specifications of GSM/EDGE and UMTS with a low current consumption.**

I. Introduction

Due to the coexistence of multi-standards of radio frequency (RF) cellular communications in different countries, a multi-mode transceiver is required to realize global mobility and a wide range of services. In order to reduce cost, sharing of RF blocks between different systems and bands is necessary. However, sharing the oscillator for UMTS and GSM/EDGE is a big challenge due to the vastly different specifications. It has to cover all the frequency bands of GSM/EDGE and UMTS which are widely spread (see Table I). The stringent phase noise requirement of GSM and low power requirement of UMTS due to continuous transmission have to be fulfilled with the same oscillator.

Further improvements will be achieved by increasing the level of integration. It meets the key issues of modern communication systems namely lower power consumption and cost of production. Fully digital solutions show advantages especially with deep sub-micron CMOS technologies. Digital blocks are highly reconfigurable and allow more robust designs in terms of component mismatch and temperature drift. A digitally controlled oscillator (DCO) enables the use of all digital phase locked loops (ADPLL) function as either local oscillator (LO) or direct frequency modulator for wireless communication terminals.

A 4 GHz DCO with 1 GHz tuning range for GSM/UMTS applications in 0.13 um CMOS was reported in [1]. However this DCO is only applicable for transmitter and has no coverage of Band Japan (see Table I). This paper presents the first dual-mode DCO in 65 nm CMOS technology which is capable of covering all bands of GSM/EDGE and UMTS transceiver specifications except Band VII. This is in line with the described trend towards RF-CMOS.

In Section II, details of the DCO implementation are presented. Section III shows first measurement results. Finally, in Section IV the most important results are summarized in the conclusion part.

TABLE I
Frequency Requirement of Different Bands of GSM/EDGE and UMTS

Band	TX (MHz)	RX (MHz)	Mode
Band I	1920-1980	2110-2170	UMTS(W)
Band II	1850-1910	1930-1990	Cobanded(GW)
Band III	1710-1785	1805-1880	Cobanded(GW)
Band IV	1710-1755	2110-2155	UMTS(W)
Band V	824-849	869-894	Cobanded(GW)
Band VI	830-840	875-885	Subband of band V
Band VII	2500-2570	2620-2690	UMTS(W)
Band VIII	880-915	925-960	Cobanded(GW)
Band IX	1749.9-1784.9	1844.9-1879.9	Subband of band III
Band X	1710-1770	2110-2170	Extended band IV
Band Japan	1428-1448	1476-1496	UMTS(W)

II. Implementation

The block diagram of the implemented DCO is shown in Fig. 1. A complementary differential LC oscillator core is chosen because of its high phase noise performance while consuming less power compared with NMOS only or PMOS only cores. As analyzed in [2], the $1/f^2$ phase noise of complementary differential LC oscillator is

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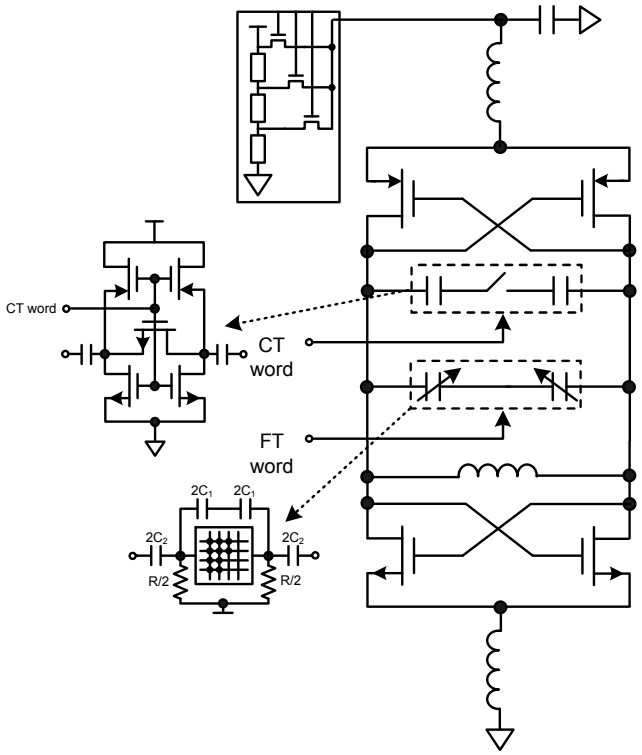

Fig. 1. DCO Block Diagram

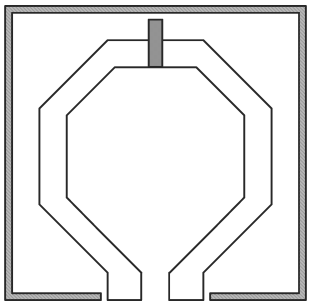

Fig. 2. Single-Winged Center-Tapped 400pH On-Chip Inductor

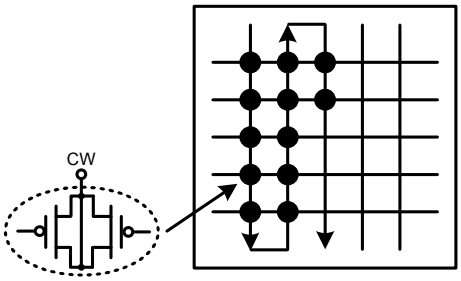

Fig. 3. Thermometer Coded Varactor Tank with Serpentine Switching Scheme

$$\mathcal{L}_{DS}(\Delta\omega) = 10\log\left[\frac{k_B T}{C^2 A_{DS}^2 R\Delta\omega^2}\left(1+\frac{\gamma_n+\gamma_p}{2}\right)^2\right] \quad (1)$$

The $1/f^2$ phase noise of NMOS only differential LC oscillator is

$$\mathcal{L}_{SS}(\Delta\omega) = 10\log\left[\frac{k_B T}{C^2 A_{SS}^2 R\Delta\omega^2}\left(1+\gamma_n\right)^2\right] \quad (2)$$

where γ_n and γ_p are the channel noise factor for nMOS and pMOS transistors, C and R are the equivalent capacitance and resistance of the LC tank. For the same current consumption, the oscillation amplitude

$$A_{DS} = 2A_{SS} \quad (3)$$

Therefore, for the same current consumption, the complementary differential oscillator has about 6dB better phase noise performance compared to NMOS only differential LC oscillator.

The noise filtering technique is used to enhance the phase noise performance [3]. A big MIM-cap is connected to the DCO top biasing to bypass high frequency noise. The top inductor and bottom inductor resonates with the parasitic capacitance on the top biasing and bottom biasing nodes at $2\omega_0$. Thus improves the efficiency of DC power converted to fundamental RF power by suppressing the second order harmonics in the LC oscillator.

As shown in Fig. 2, a 400 pH single-winged on chip inductor with center tap is used as the main coil in the LC tank. A 4-bit programmable DCO top biasing voltage is used to switch the DCO operation between different phase noise and power consumption requirements of different modes.

The coarse tuning range 6.35 GHz - 9.15 GHz is realized by a 10-bit binary weighted switchable capacitor tank. By dividing the DCO frequency by 4, 6 and 8, this DCO is able to cover frequency ranges of 1588 MHz - 2288 MHz, 1058 MHz - 1525 MHz and 794 MHz - 1144 MHz respectively. This frequency coverage contains all the TX and RX bands in Table I except Band VII. In [1], the reported DCO covers a frequency range of 3 GHz - 4 GHz, which is divided by 2 or 4 to a LO frequency range of 1500 MHz - 2000 MHz and 750 MHz - 1000 MHz. Compared to the DCO in [1], this DCO covers a much wider frequency range and is applicable for more applications.

Fine tuning of the presented DCO is realized using a combination of 9-bit thermometer coded varactor tank and 4-bit binary weighted switchable capacitor. The thermometer coded varactor tank is shown in Fig. 3 where "CW" is the control word. A PMOS pair is used as a unit cell in the tank because of its well-defined "high" and "low" capacitance levels. A serpentine switching scheme is used to improve the matching of fine tuning step sizes.

In order to achieve finer tuning step size, capacitance division technique is used to scale down the ΔC each PMOS pair provides. As shown in Fig. 1, the fine tuning part is composed of the fine tuning varactor tank, capacitors in parallel with the varactor tank and AC coupling capacitors C_2. The capacitance change from the varactor is converted to the LC tank with

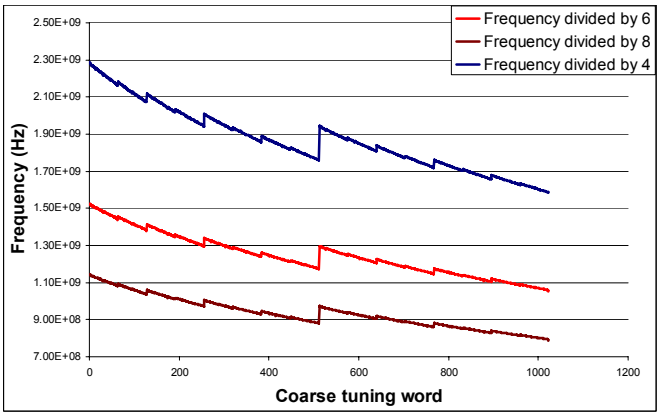

Fig. 4. Coarse tuning curves (DCO frequency divided by 4, 6 and 8) versus coarse tuning words

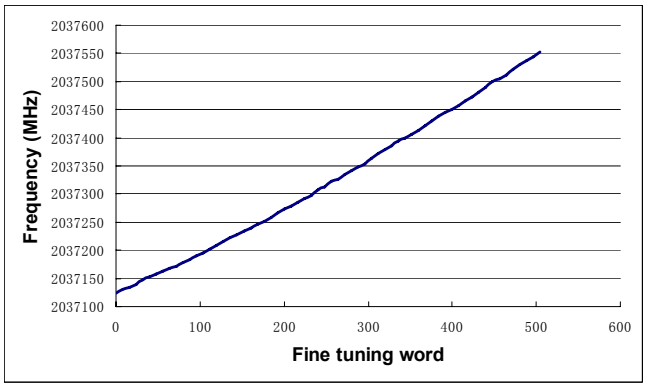

Fig. 5. DCO frequency versus fine tuning word

ΔC_{eq} equals to

$$\Delta C_{eq} = \left(\frac{C_2}{C_0 + C_1 + C_2}\right)^2 \Delta C \tag{4}$$

where C_0 is the intrinsic capacitance of the varactor tank and ΔC is the capacitance change when a unit varactor cell is switched. The resistor R in Fig. 1 has to be big enough so as not to influence the equivalent capacitance severely. Using this technique with the DCO fine tuning tank as shown in Fig. 1, we can achieve finer tuning step size by a capacitor divider with carefully chosen division ratios.

III. Measurement Results

Fig. 4 shows the DCO coarse tuning frequency curves versus coarse tuning words with DCO frequency divided by 4, 6 and 8. Measured at room temperature, a 31% coarse tuning range covers frequency ranges of 1588 MHz - 2288 MHz, 1058 MHz - 1525 MHz, 794 MHz - 1144 MHz respectively. Overlaps are added in order to ensure complete frequency coverage. The nonlinearity of the coarse tuning curves is due to that

$$\Delta f = \frac{1}{2\pi\sqrt{LC_0}} - \frac{1}{2\pi\sqrt{L(C_0 + \Delta C)}} \tag{5}$$

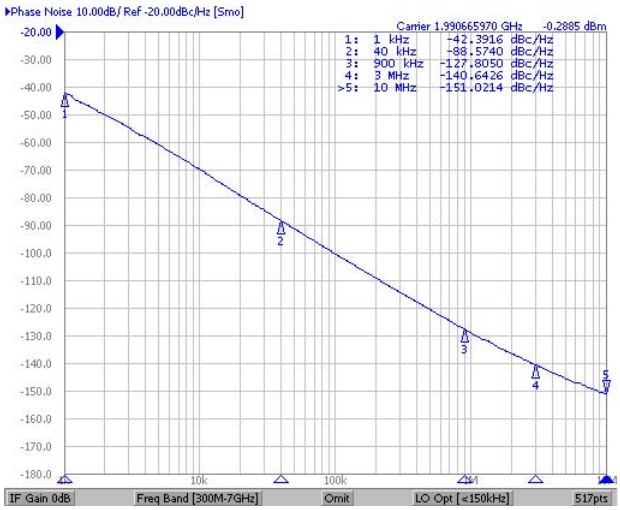

Fig. 6. Measured phase noise profiles at 1.99GHz carrier (DCO frequency divided by 4)

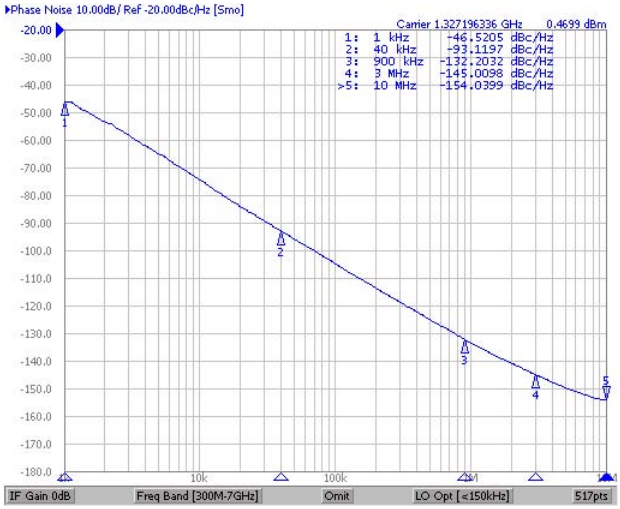

Fig. 7. Measured phase noise profiles at 1.33GHz carrier (DCO frequency divided by 6)

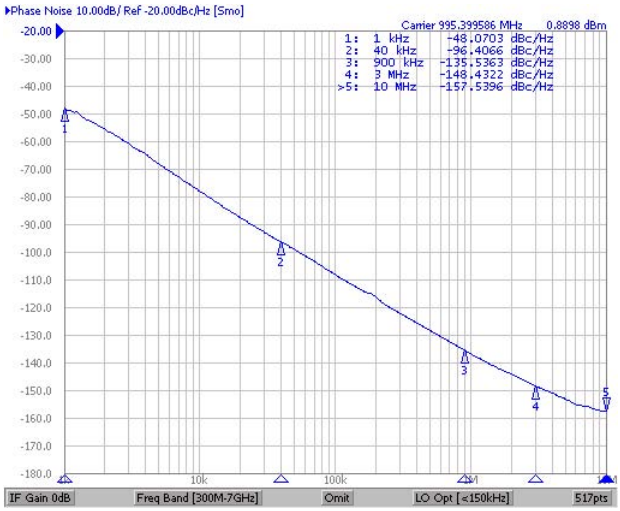

Fig. 8. Measured phase noise profiles at 995MHz carrier (DCO frequency divided by 8)

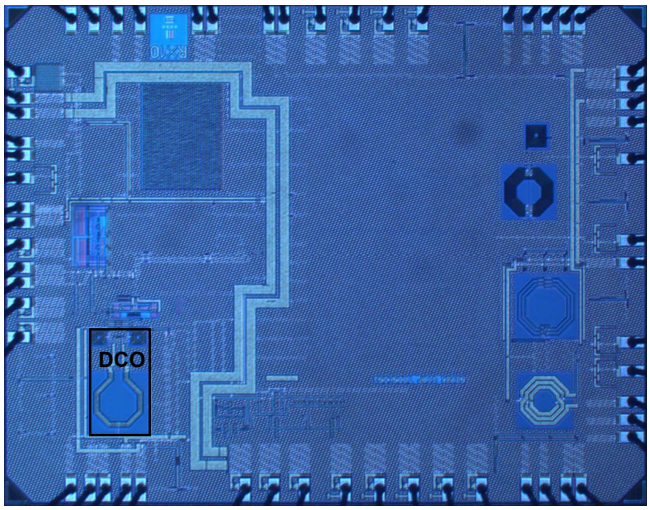

Fig. 9. Chip Microphoto

The design target of DCO fine tuning is to have a step size of 1.5 kHz at 2 GHz domain. However, due to underestimation of the parasitic capacitance of the capacitance divider, a higher division ratio gives a fine tuning step size of 0.8 kHz. Fig. 5 shows the fine tuning curve versus fine tuning words. This problem can be easily corrected by resizing the AC coupling capacitor size.

Fig. 6, Fig. 7 and Fig. 8 show the free running phase noise of the DCO output frequency divided by 4, 6 and 8 between 1 kHz and 20 MHz offset. The DCO phase noise performance meets the stringent requirement of GSM at a current consumption of 16 mA. Only 8 mA is needed to achieve UMTS requirement. Calculating the FOM of this DCO using the following equation [4]

$$FOM = \left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1}{\mathcal{L}(\omega)P} \tag{6}$$

we get a FOM of 183 for far-off thermal noise.

The die photo is shown in Fig. 9, where the DCO is indicated.

IV. Conclusion

A 9 GHz GSM/EDGE and UMTS multi-mode DCO has been implemented in 65 nm CMOS technology. A programmable DCO bias voltage is used to achieve the different phase noise and power consumption required for GSM/EDGE and UMTS. A 10-bit binary weighted coarse tuning tank is used to realize a frequency range of 6.35 GHz - 9.15 GHz. A 9-bit thermometer coded varactor tank is used to realize a minimum fine tuning step size of 0.8 kHz. The DCO phase noise performance meets GSM/EDGE and UMTS requirement with a low current consumption.

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