5V VSB

ATX Power Supply Control Circuit

CPU

File: CPU.kicad_sch

SRAM-EPROM

File: SRAM-EPROM.kicad_sch

DRAM

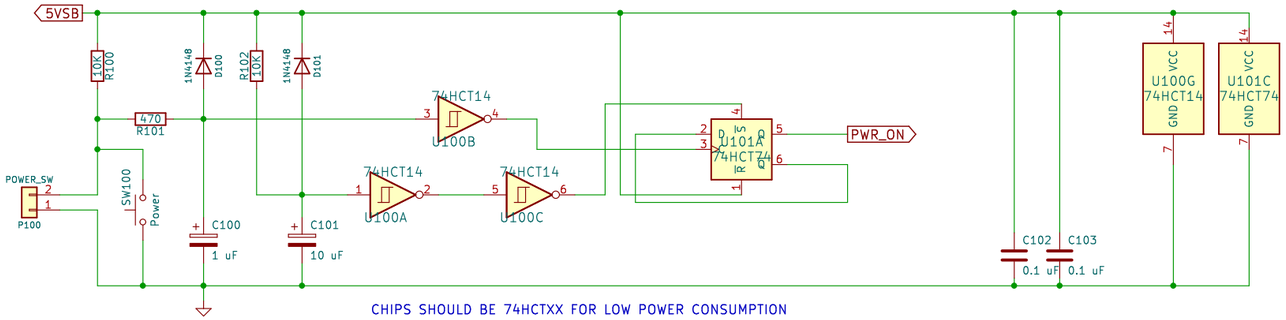
File: DRAM.kicad_sch

IO

File: IO.kicad_sch

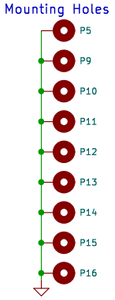
Decoders

File: Decoders.kicad_sch

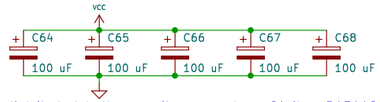


CHIPS SHOULD BE 74HCTXX FOR LOW POWER CONSUMPTION

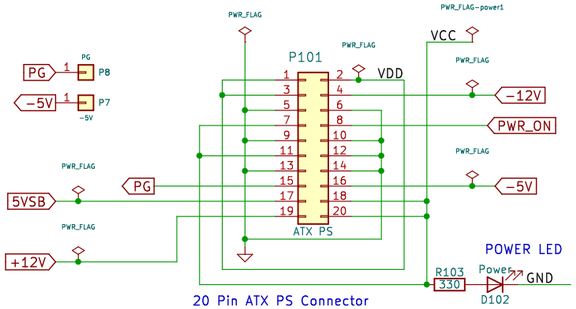
Mounting Holes

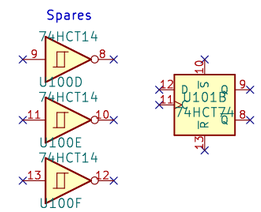


Prototyping Area



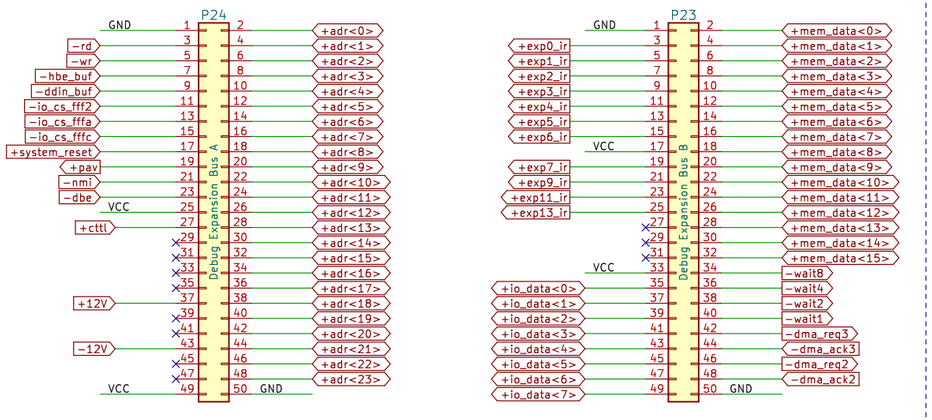
Note: distributed bulk capacitance such as Digikey P15112-ND





Based on Bruce Culbertson NS32016 project
https://ftp.funet.fi/pub/misc/pc532/Culbertson

CPU local debug expansion bus (deb) connectors



Sheet: /
File: NS32016-BC.kicad_sch

Title:

Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 1/6

NOTE: KiCAD DIODE PINS 1 & 2
REVERSED AGAINST ORIGINAL SCHEMATIC
DUE TO SPICE COMPATIBILITY. DIODE
REVERSED AGAINST ORIGINAL NETLIST
FOR FUNCTIONALITY.

VCC
1N4148
D1
10K
R1
-rst_sw
SW1
Reset
C3
10 uF
GND

RR8
4700
-wait8
-wait4
-wait2
-wait1
-dma_breq
-dma_req2
-dma_req3
io_decode1
io_decode2

X1
20 MHz
+tcu_clk_in
tcu_osc

U1
NS32016
+st0
+st1
+st2
+st3
-supervisor
-pfs
+bbg
1000 pF
C1
1 uF
C2
GND
VCC
+phi1
+phi2
+rdy
-int
-nmi
ST0
ST1
ST2
ST3
U/S
PFS
BBG
GNDL
GNDB
VCC
PHI1
PHI2
RDY
INT
NMI
A23
A22
A21
A20
A19
A18
A17
A16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
DS/FLT
RST/ABT
ADS
HLDA
AT/SPC
HOLD
DDIN
ILO
HBE
-flt
-abt
-ads
-hlda_mmu
-spc
-hold
-ddin
-hbe
CPU

U2
NS32082
MMU
A24/HBF
HLDAI
HLDAO
INT
PAV
+mmu_a24
-pav

U5
NS32201
-io_cs_fff0
-cwait
P21
-wait8
-wait4
-wait2
-wait1
-ddin
-pav
RSTI
RWEN/SYNC
XIN
XOUT
PER
CWAIT
FCLK
WAIT8
WAIT4
WAIT2
WAIT1
RSTO
TSO
CTTL
DBE
RD
WR
+fclk
-system_reset
-tso
+cttl
-dbe
-rd
-wr
TCU

U29A
74LS07
-eprom_cs
U29G
C4
25 pF
C5
25 pF

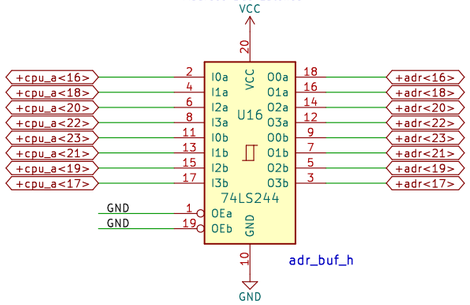
U3
NS32081
FPU
-spc
-system_reset
+cttl
SPC
RST
CLK
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0

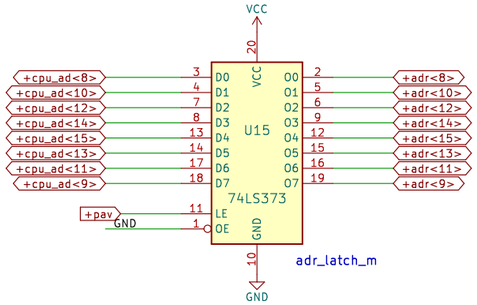
U4
NS32202
ICU
+uart1_ir
-int
+st1
+uart2_ir
+fdc_ir
+scsi_ir
-dma_ir
+exp6_ir
+exp4_ir
+exp2_ir
+exp0_ir
+io_data<7>
+io_data<6>
+io_data<5>
+io_data<4>
+io_data<3>
+io_data<2>
+io_data<1>
+io_data<0>
IR15
INT
ST1
G7/IR14
G6/IR12
G5/IR10
G4/IR8
G3/IR6
G2/IR4
G1/IR2
G0/IR0
D7
D6
D5
D4
D3
D2
D1
D0
Cout/SCin
IR13
IR11
IR9
IR7
IR5
IR3
IR1
CLK
WR
RD
A4
A3
A2
A1
A0
CS
+exp13_ir
+exp11_ir
+exp9_ir
+exp7_ir
+exp5_ir
+exp3_ir
+exp1_ir
+cttl
-wr
-rd
-system_reset
+adr<5>
+adr<4>
+adr<3>
+adr<2>
+adr<1>
-io_cs_fffe

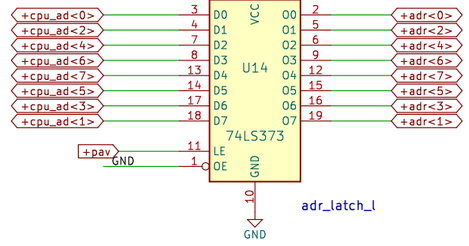
U33
NS32203
DMA
dma_ctl
-dma_cs
cs = 0xffecxx
-dma_breq
tied high RR8 pin 6
-dma_req3
tied high RR8 pin 8
-dma_req2
tied high RR8 pin 7
-dma_req1
-dma_req0
-dma_ack3
-dma_ack2
-dma_ack0
-hbe_buf
-ddin
-dma_ir
-hold
-hlda
tied high RR6 pin 9

Sheet: /CPU/
File: CPU.kicad_sch
Title:
Size: B
Date: 4 feb 2016
Rev:
KiCad E.D.A. kicad (6.0.11)
Id: 2/6

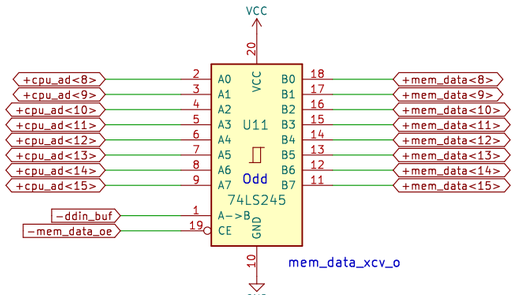
Address Bus Latches

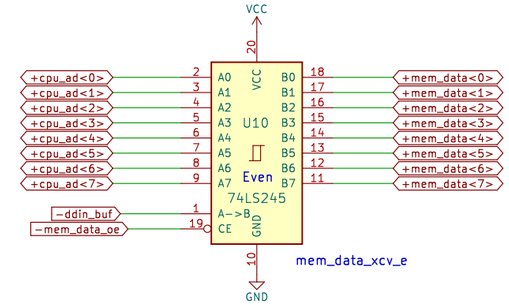




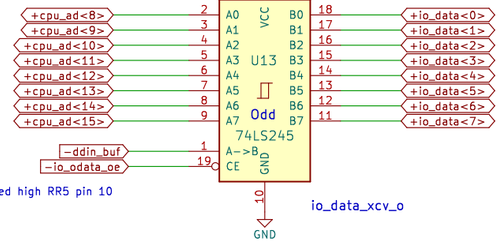


Memory Data Bus Latches

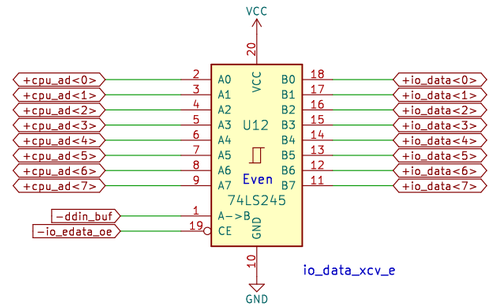




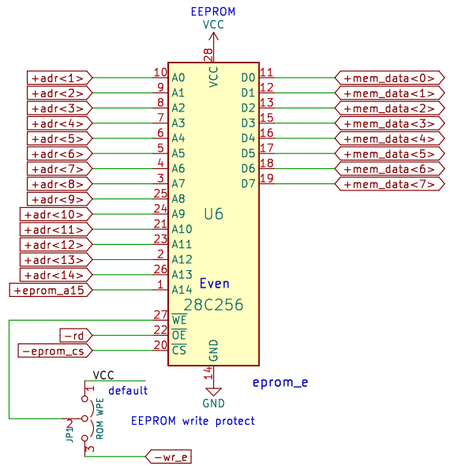
IO Data Bus Latches

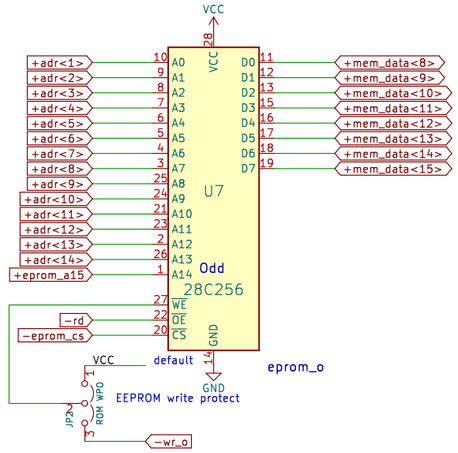


tied high RR5 pin 10



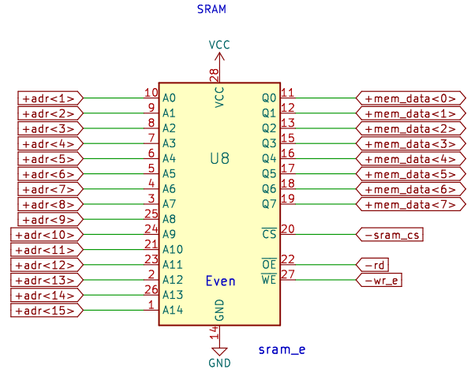
EEPROM

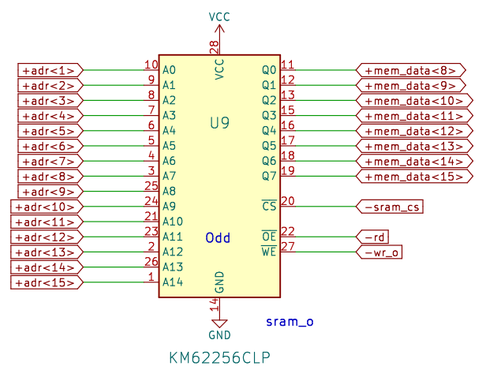


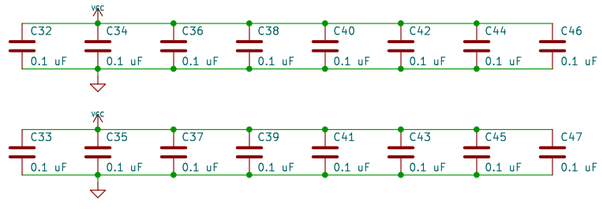


Note: orginal design specified 27C256 EPROMs but substituted 28C256 EEPROMs with slightly different pin-out (1=A14, 27=WR#)

SRAM







Sheet: /SRAM-EPROM/	
File: SRAM-EPROM.kicad_sch	
Title:	
Size: B	Date: 4 feb 2016
KiCad E.D.A. kicad (6.0.11)	Id: 3/6

U37
GAL16V8
VCC
+cttl
+rfshclk
GND
rfshpal

U38
GAL16V8
VCC
+fclk
-tso
+rfsh
-par
-ddln_buf
+dramcpal1
+cttl
-dram_cs
+dramcpal2
-rasin
-mode
-cwait
tied high RR7 pin 7
tied high RR7 pin 8
GND
dramcpal

DS1010-50
P3
U35
TAP1
TAP2
TAP3
TAP4
TAP5
TAP6
TAP7
TAP8
TAP9
TAP10
DELAY
VCC
NC
IN
GND
+ras_dly100
<-- Default
-rasin
Delay Line
dram_delay0
Note: use jumper
to select delay setting.
Default is TAP4
(jumper connector P3 7 to 8)

Note: due to non-availability of originally specified
DDU-7-20 delay line, Maxim DS1010-50 used instead.
Output was pin 8 (20 ns), now is pin 4 (20 ns).

Note: +ras_dly100 refers to the 100% tap
delay of DDU-7-20 or 20 ns. Net name is
reused for consistency with original design
notes but is misleading with DS1010-50 circuit.

DS1010-50
P4
U36
P6
RELAY 2
Delay Line
dram_delay1
Note: U36 is unused. It is kept
for compatibility with original
design notes. Do not populate.

U39
74AS157
dram_mux

U40
74AS244
dram_drv

4700
RR7
+m0
+rahs
+a09
-win
+dramcpal1
+dramcpal2
3st_buf
C8
1 uF
ceramic
C9
1 uF
tantalum
Note: C8 and C9 must be
close to U34 pins 36 and 38

U34
DP8419
DRAM Controller
dramc
VCC
RGCK
ADS
tied high RR7 pin 4
RASIN#
RFCK
WIN#
RFSH#
CS#
M0
RAHS
RFI/O
RAS3#
RAS2#
RAS1#
RAS0#
CAS#
WE#
-rasin
+rfshclk
-win
-mode
-dram_cs
+m0
+rahs
+rfsh
-ras31
-ras21
-ras11
-ras01
-cas1
-we_l1
-we_h1

dram_term1
dram_term2
dram_term3
RP1
RP2
RP3

TC514400_ZIP-20
U41
U42
U43
U44
U45
U46
U47
U48
U49
U50
U51
U52
U53
U54
U55
U56
-ras02
-ras12
-ras22
-ras32
-cas2
-we_l2
-we_h2
-rd
RAS#
CAS#
WRITE#
OE#
VCC
GND

C6 C11 C14 C17 C20 C23 C26 C29
C7 C12 C15 C18 C21 C24 C27 C30
C10 C13 C16 C19 C22 C25 C28 C31
0.1 uF
0.47 uF
Note: use 0.47 uF Monolithic Ceramic capacitors such as Digikey 490-8852-ND

Sheet: /DRAM/
File: DRAM.kicad_sch
Title:
Size: C
Date: 4 feb 2016
Rev:
KiCad E.D.A. kicad (6.0.11)
Id: 4/6

Floppy controller

U57
P82072
Floppy Controller
Analog GND
Separate connection
to ground plane.
tied high RR5 pin 8
U58A 74LS38
U58B 74LS38
U58C 74LS38
U58D 74LS38
fd_drv1
X3
24MHz
fd_osc
4700
RR5
fd_pullup
P2
FLOPPY
fd_conn
U60A 74LS14
U60B 74LS14
U60C 74LS14
U60D 74LS14
U60E 74LS14
U60F 74LS14
fd_rcv
U59A 7406
U59B 7406
U59C 7406
U59D 7406
U59E 7406
U59F 7406
fd_drv2

RS232 Serial Controllers

U17
NS16450
Serial UART
UART 1
!cs = 0xfff08x
J1
DE9 Male
U19
MC1489
rs232_rcv
U20
MC1488
rs232_drv
X2
1.8432MHz
Note: TTL oscillator substituted
for crystal and resistor network
Note: +uart_xtal2 signal deleted
P25
UART HEADER
uart_header
U18
NS16450
Serial UART
UART 2
!cs = 0xfff0cx
J2
DE9 Male
Note: uart_header replaced with X2 TTL
oscillator and J1 and J2 DE-9 connectors

SCSI Controller

VCC
GND
220R
330R
RR1
RR2
RR3
RR4
P1
SCSI BUS
sc_term
D2
1N5820
NOTE: KICAD DIODE PINS 1 & 2
REVERSED AGAINST ORIGINAL SCHEMATIC
DUE TO SPICE COMPATIBILITY. DIODE
REVERSED AGAINST ORIGINAL NETLIST
FOR FUNCTIONALITY.
U32
NCR5380
SCSI Controller
tied high RR5 pin 9
-dack
ZuluSCSI Compact RP2040 – a SCSI-1 and
SCSI-2 hard drive emulator
https://www.ebay.com/itm/195663613492

Notes:–

1) SCSI Terminator Resistor Packs
   Some swapping of resistor positions against original netlist for schematic neatness.

2) Serial Controller Clock
   Original circuit swapped out for a 14pin DIL oscillator

3) Serial Controller Output Header
   Havs been swapped out for 2 x DE-9 male connectors

U58E 74LS38
U60G 74LS14
U59G 7406
C69 C70 C71 C72 C73 C74 C75 C76
C56 C57 C58 C59 C60 C61 C62 C63
0.1 uF

Sheet: /IO/
File: IO.kicad_sch
Title:
Size: A2 | Date: 25 jun 2017 | **Rev:**
KiCad E.D.A. kicad (6.0.11) | Id: 5/6

I/O Decode

+adr<23> 1
+adr<22> 2
+adr<21> 3
+adr<20> 4
+adr<19> 5
+adr<18> 6
+adr<17> 7
+adr<16> 10
+adr<15> 11
+adr<14> 12
+adr<13> 13
+adr<12> 14
io_decode1 15

U21A 74ALS133 9 → −io_cs

low for 0xfffxxx

tied high RR8 pin 9

io_decode1

DMA Decode

+adr<23> 1
+adr<22> 2
+adr<21> 3
+adr<20> 4
+adr<19> 5
+adr<18> 6
+adr<17> 7
+adr<16> 10
+adr<15> 11
+adr<14> 12
+adr<13> 13
+adr<11> 14
+adr<10> 15

U22A 74ALS133 9 → −dma_cs1

low for 0xffecxx

dma_decode

P22

SW HEADER

−nmi_up 1 | 2 VCC
−nmi_down 3 | 4
−rst_sw 5 | 6
GND 7 | 8
9 | 10
11 | 12
GND 13 | 14 +swap_jumper

Note: P22 13 & 14 (+swap_jumper) toggles location of EEPROM in memory for dual boot strap option

Note: was U29 sw_header

SW2

GND 2
1 −nmi_up
3 −nmi_down
NMI SEL

nmi_sw

U28

GAL16V8

+cttl 1
−nmi_up 2
−nmi_down 3
−tso 4
5
6
7
8
9
11

I1/CLK VCC I01 19
I2 I02 18
I3 I03 17
I4 I04 16
I5 I05 15
I6 I06 14
I7 I07 13
I8 I08 12
I9
I10/OE GND

VCC 20
GND 10

−nmi 12

nmipal

U27

GAL16V8

+adr<15> 1
+adr<16> 2
+adr<17> 3
+adr<18> 4
+adr<19> 5
+adr<20> 6
+adr<21> 7
+adr<22> 8
+adr<23> 9
+swap_jumper 11

I1/CLK VCC I01 19
I2 I02 18
I3 I03 17
I4 I04 16
I5 I05 15
I6 I06 14
I7 I07 13
I8 I08 12
I9
I10/OE GND

VCC 20
GND 10

−dram_cs
−sram_cs
+eprom_a15
−eprom_cs

memcspal

U23

74ALS138

A0 VCC O0 15 → −io_cs_fff0 uarts
A1 O1 14 → −io_cs_fff2 expansion
A2 O2 13 → −io_cs_fff4 floppy controller
E3 O3 12 → −io_cs_fff6 scsi −cs
E2 O4 11 → −io_cs_fff8 scsi −dack
E1 O5 10 → −io_cs_fffa expansion
GND O6 9 → −io_cs_fffc expansion
O7 7 → −io_cs_fffe icu

tied high RR8 pin 10
io_decode2 6
+adr<8> 5
−io_cs 4

8

io_decode2

Unused Gates

U26D 74LS126 12 11 13
U26C 74LS126 9 8 10
U31B 74ALS32 4 5 6

U29B 74LS07 3 4
U29C 74LS07 5 6
U29D 74LS07 9 8
U29E 74LS07 11 10
U29F 74LS07 13 12

RR6

1000

+spc 2
−int 3
−hold 4
+mmu_a24 5
−nmi_up 6
−nmi_down 7
+swap_jumper 8
−pav 9
−cwait 10

C48 C49 C50 C51 C52 C55

0.1 uF

U21B U22B U24E U31E U25G U26E

74ALS133 / 74ALS32 / 74ALS04 / 74LS126

VCC 16 / 16 / 14 / 14 / 14 / 14
GND 8 / 8 / 7 / 7 / 7 / 7

or_1

U24A 74ALS32 1 2 3
−wr
+adr<0>
−wr_e

U24B 74ALS32 4 5 6
−dbe
−io_cs
−io_edata_oe

U24C 74ALS32 9 10 8
+adr<23>
−dbe
−mem_data_oe

U24D 74ALS32 12 13 11
−hbe_buf
−wr
−wr_o

U31A 74ALS32 1 2 3
−dma_cs1
+adr<12>
−dma_cs

or_2

U31C 74ALS32 9 10 8
+ddin_buf
−hbe_buf
−we_h0

U31D 74ALS32 12 13 11
+ddin_buf
+adr<0>
−we_l0

invert_1

U25A 74ALS04 1 2
+adr<6> → −adr<6>

U25B 74ALS04 3 4
−pav → +pav

U25C 74ALS04 5 6
−system_reset → +system_reset

U25D 74ALS04 9 8
−ddin → +ddin_buf

U25E 74ALS04 11 10
+dma_req1 → −dma_req1

U25F 74ALS04 13 12
+dma_req0 → −dma_req0

3st_buf1

U26A 74LS126 2 3 1
−hbe → −hbe_buf
−hida

U26B 74LS126 5 6 4
−ddin → −ddin_buf
3st_buf

tied high RR7 pin8

Sheet: /Decoders/		
File: Decoders.kicad_sch		
Title:		
Size: A3	Date: 25 jun 2017	**Rev:**
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