

# Course Information

Logic Design Lab. <sup>텍스트</sup>

Fall 2019

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TA. Hyunyoung Jung

([gusdud1500@gmail.com](mailto:gusdud1500@gmail.com))

# Notification

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- **For the report**

- No sample form

- Put today's results and homework altogether and make it as **one file pdf**

- Submit your report on eTL assignment

- **Lab computer account**

- Use designated lab account on lab class

- **Contact**

- Check your e-mail address on eTL

- Feel free to contact TA

- About lectures, labs, schedule, etc.

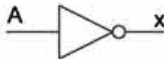



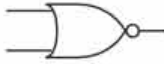

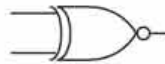
# Contents

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- **Combinational logic practice**
  - Lab 1 review
  - Tactile switches
  - LEDs
  - Pull-up & pull-down resistors
  - Practice: Half-adder implementation
- **Homework**

# Lab 1 review

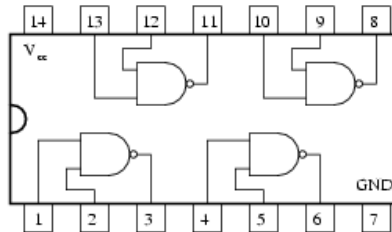
## Logic Gates

Name	NOT	AND	NAND	OR	NOR	XOR	XNOR																																																																																																
Alg. Expr.	$\overline{A}$	$AB$	$\overline{AB}$	$A+B$	$\overline{A+B}$	$A\oplus B$	$\overline{A\oplus B}$																																																																																																
Symbol																																																																																																							
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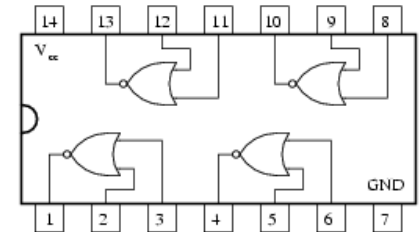
# Lab 1 review

- Logic Gates on IC chip

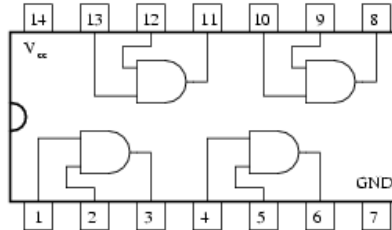
5400/7400  
Quad NAND gate



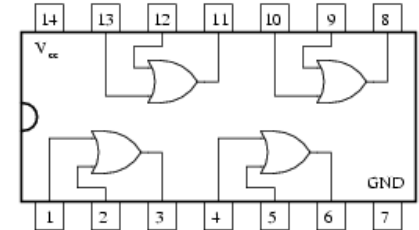
5402/7402  
Quad NOR gate



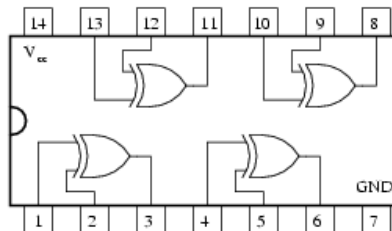
5408/7408  
Quad AND gate



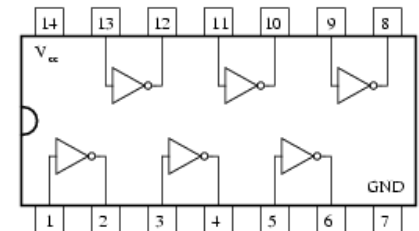
5432/7432  
Quad OR gate



5486/7486  
Quad XOR gate



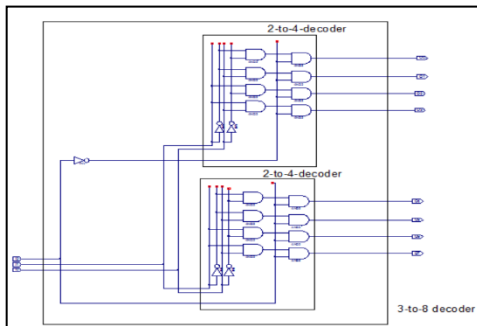
5404/7404  
Hex inverter



# Lab 1 review

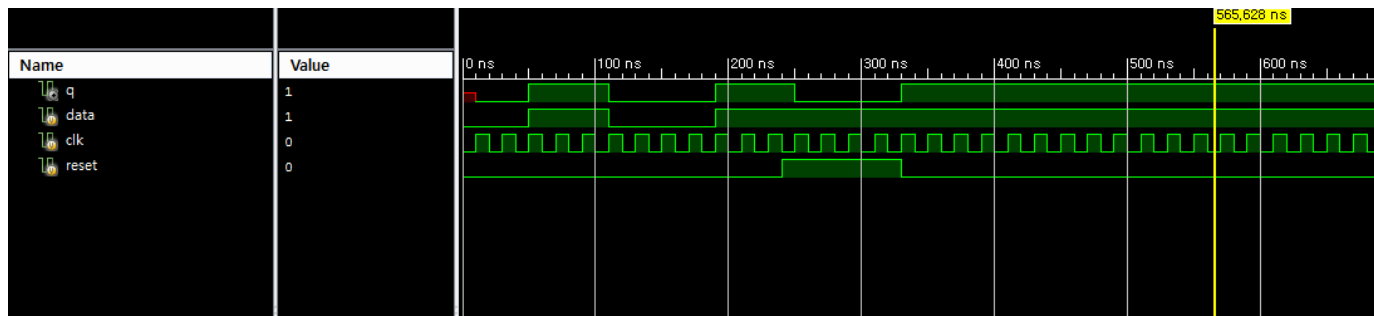
## ■ Computer Simulation

Schematic Design



Hardware Description Language

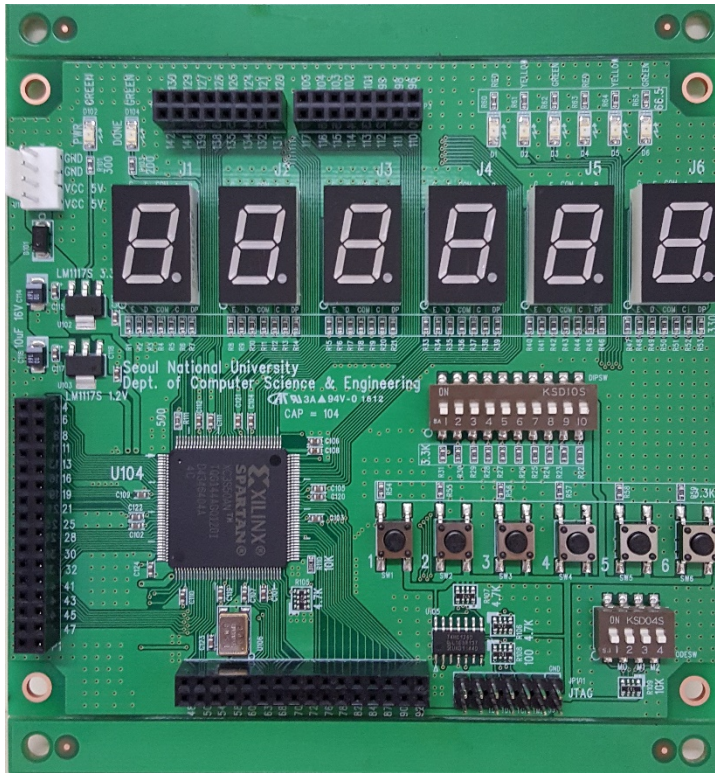
```
module seq_test_module(data, clk, reset, q);  
    input data, clk, reset;  
    output q;  
    reg q;  
  
    always @ (posedge clk)  
    begin  
        if (reset == 1)  
            q <= 0;  
        else  
            q <= data;  
        end  
    endmodule
```



## ■ Prototyping

# Lab 1 review

## ■ Prototyping

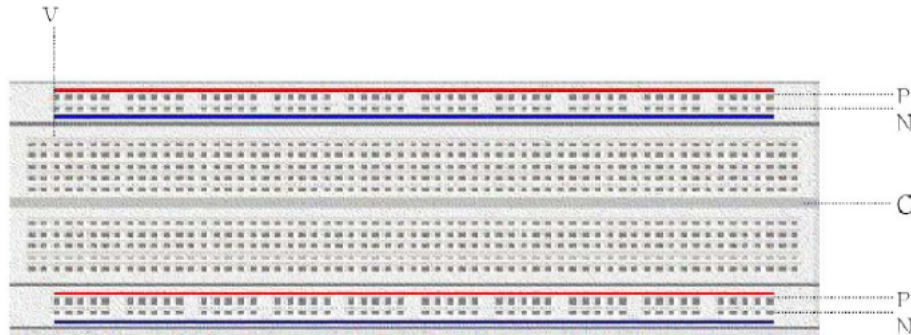


Evaluation Circuit Board

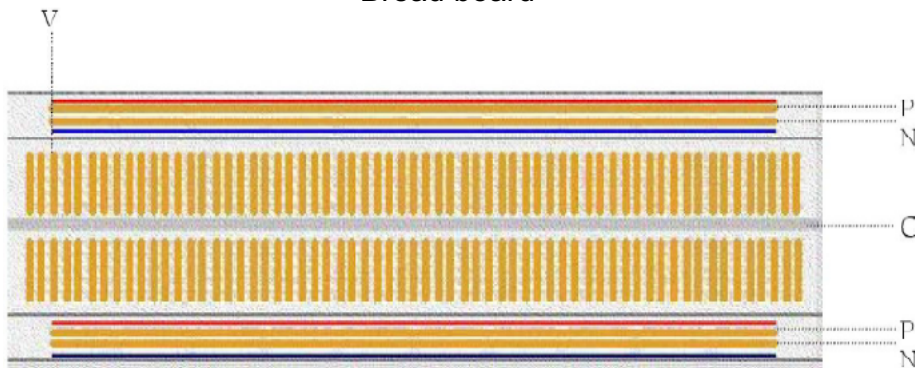
You can build your own board of your logic design with logic gates and electronic parts.

This is SNU's logic design evaluation circuit board. You will make a computer with this for the term project.

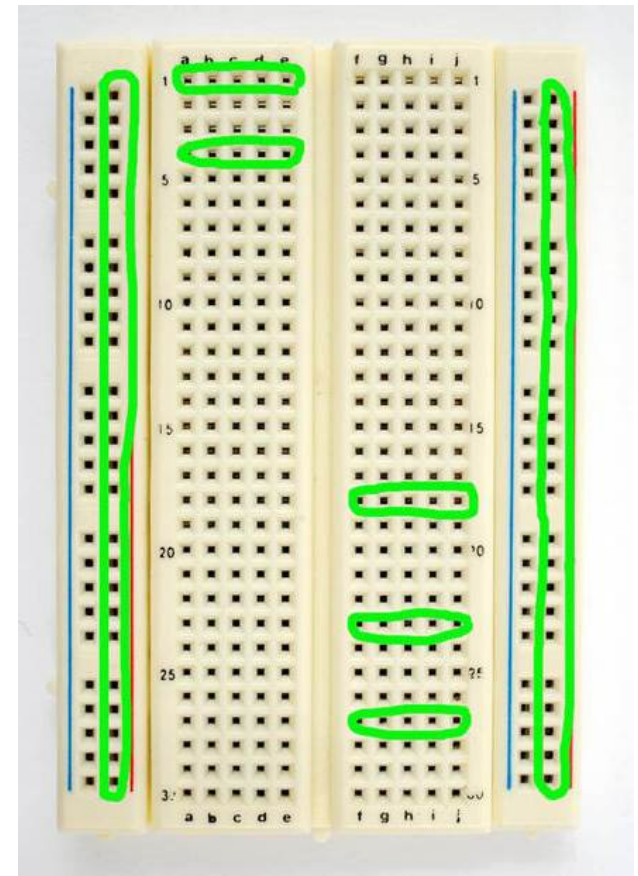
# Lab 1 review



✓ Bread board



✓ Internal wiring of Bread board

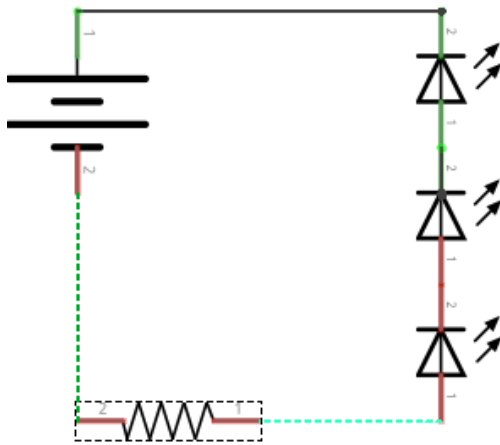


- You can construct testing the circuit using the bread board, before soldering or wrapping.



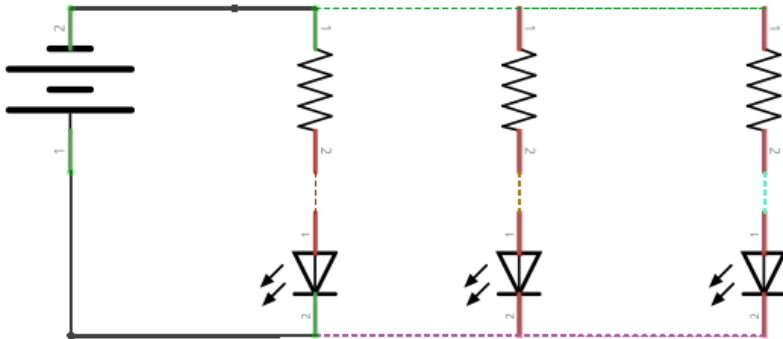
# Lab 1 review

**LED SERIES CIRCUIT**



**SYSRECON.COM**

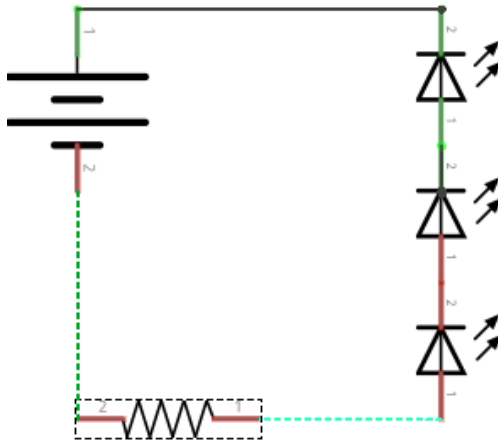
**LED PARALLEL CIRCUIT**



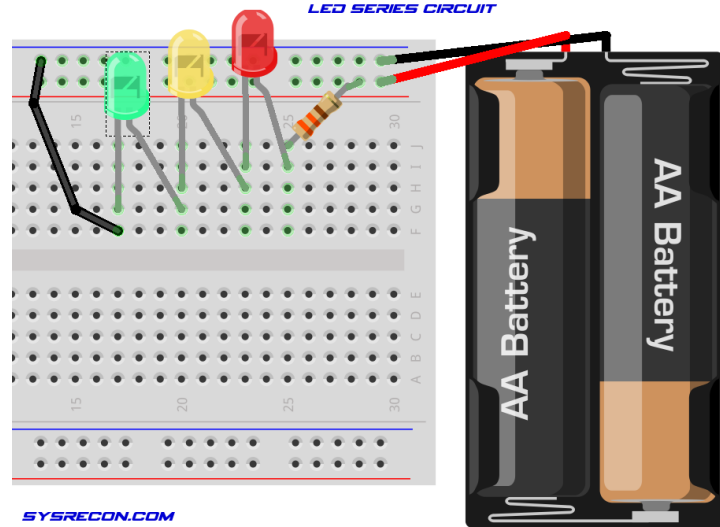
**SYSRECON.COM**

# Lab 1 review

**LED SERIES CIRCUIT**

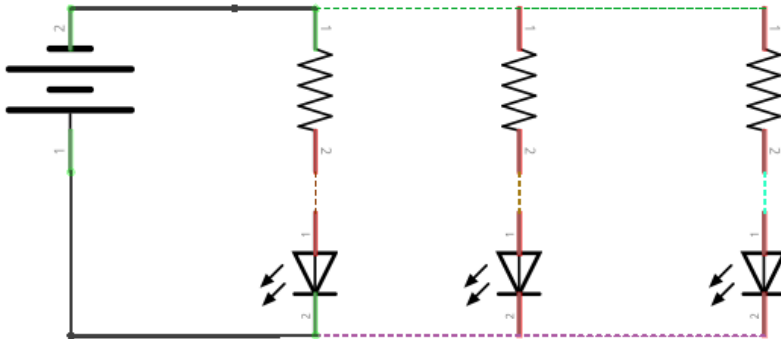


**SYSRECON.COM**

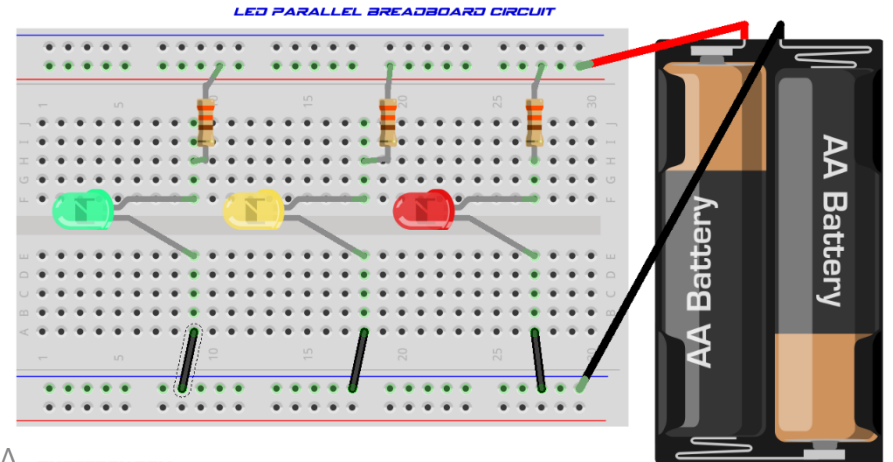


**SYSRECON.COM**

**LED PARALLEL CIRCUIT**



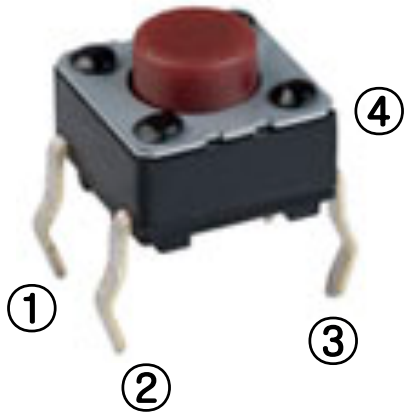
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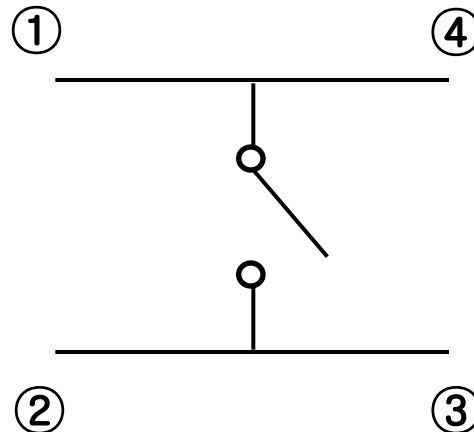
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# Combinational Logic Practice

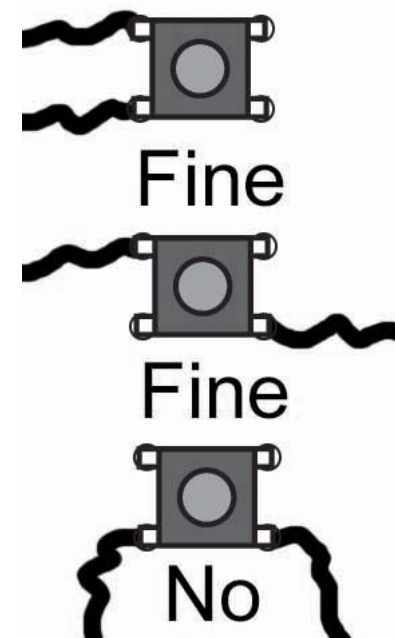
- Tactile switches



Tactile Switch



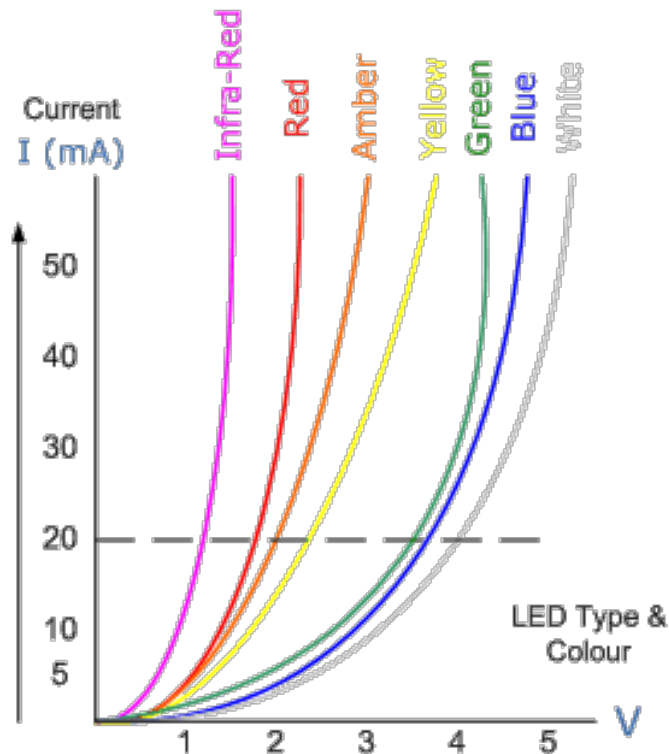
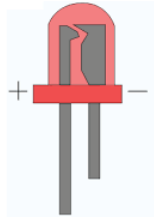
Circuit Diagram



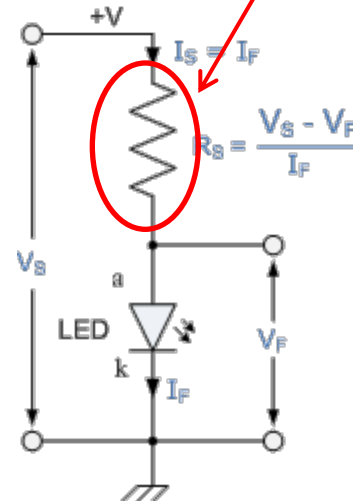
Usage

# Combinational Logic Practice

## ■ LEDs

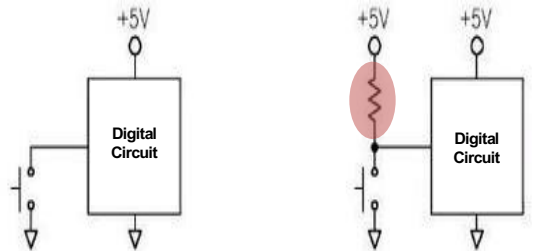


- LEDs emit colored light when passed through by forward current
- To protect LED from excessive current flow, using an appropriate resistor (around  $3 \sim 400 \Omega$ ) is necessary



# Combinational Logic Practice

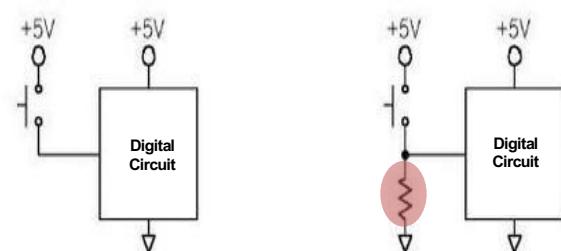
## ■ Pull-up & pull-down resistors



(a) Switch Only (b) Pull-up resistor  
<Pic 1> L switch & Pull-up resistor

switch	ON	OFF
(a)그림	0V(Low)	Floating
(b)그림	0V(Low)	+5V(High)

**Pull-up Resistor**



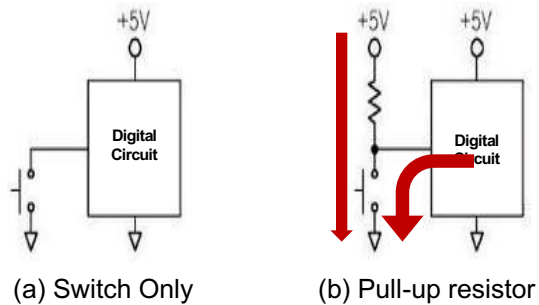
(a) Switch Only (b) Pull-down resistor  
<Pic 2> H switch & Pull-down resistor

switch	ON	OFF
(a)그림	+5V(High)	Floating
(b)그림	+5V(High)	0V(Low)

**Pull-down Resistor**

# Combinational Logic Practice

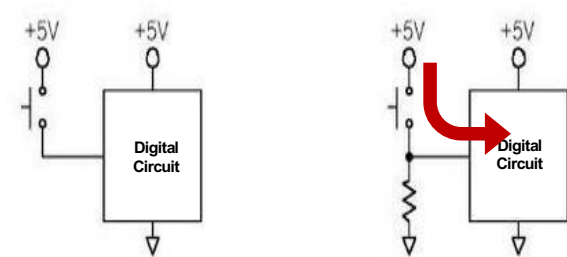
## ■ Pull-up & pull-down resistors



<Pic 1> L switch & Pull-up resistor

switch	ON	OFF
(a)그림	0V(Low)	Floating
(b)그림	0V(Low)	+5V(High)

**Pull-up Resistor**



(a) Switch Only (b) Pull-down resistor

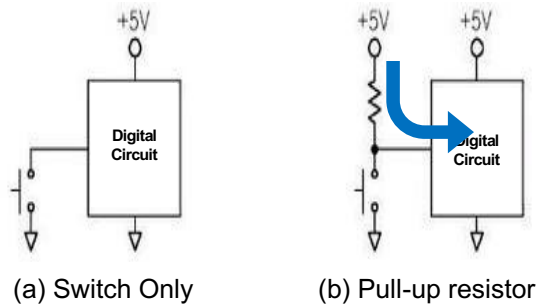
<Pic 2> H switch & Pull-down resistor

switch	ON	OFF
(a)그림	+5V(High)	Floating
(b)그림	+5V(High)	0V(Low)

**Pull-down Resistor**

# Combinational Logic Practice

## ■ Pull-up & pull-down resistors



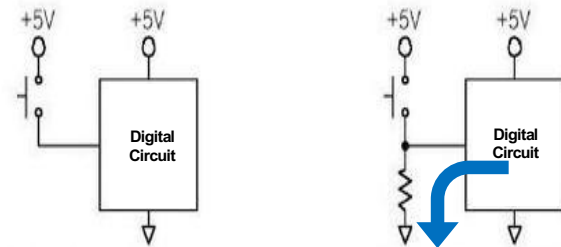
(a) Switch Only

(b) Pull-up resistor

<Pic 1> L switch & Pull-up resistor

switch	ON	OFF
(a)그림	0V(Low)	Floating
(b)그림	0V(Low)	+5V(High)

**Pull-up Resistor**



(a) Switch Only

(b) Pull-down resistor

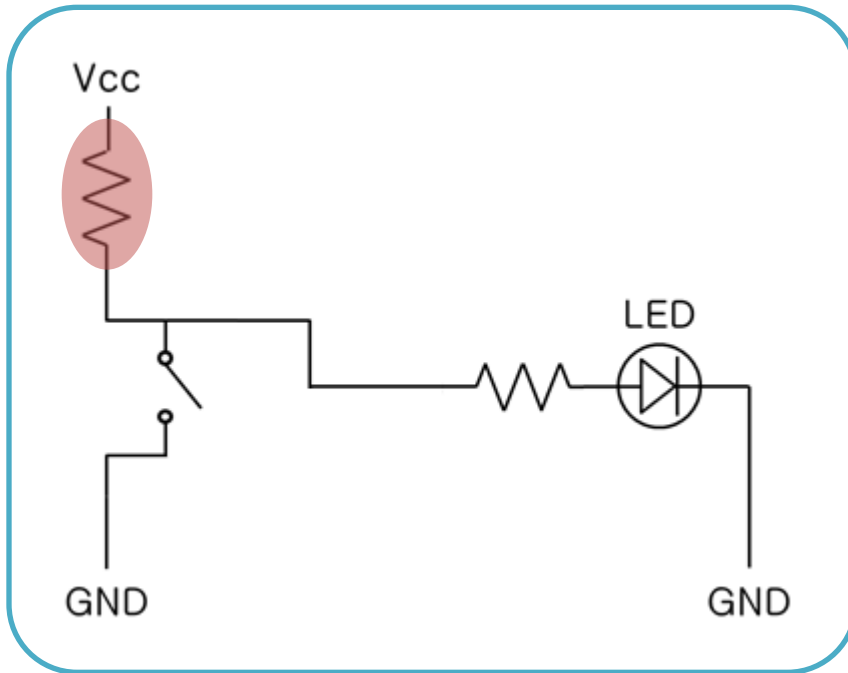
<Pic 2> H switch & Pull-down resistor

switch	ON	OFF
(a)그림	+5V(High)	Floating
(b)그림	+5V(High)	0V(Low)

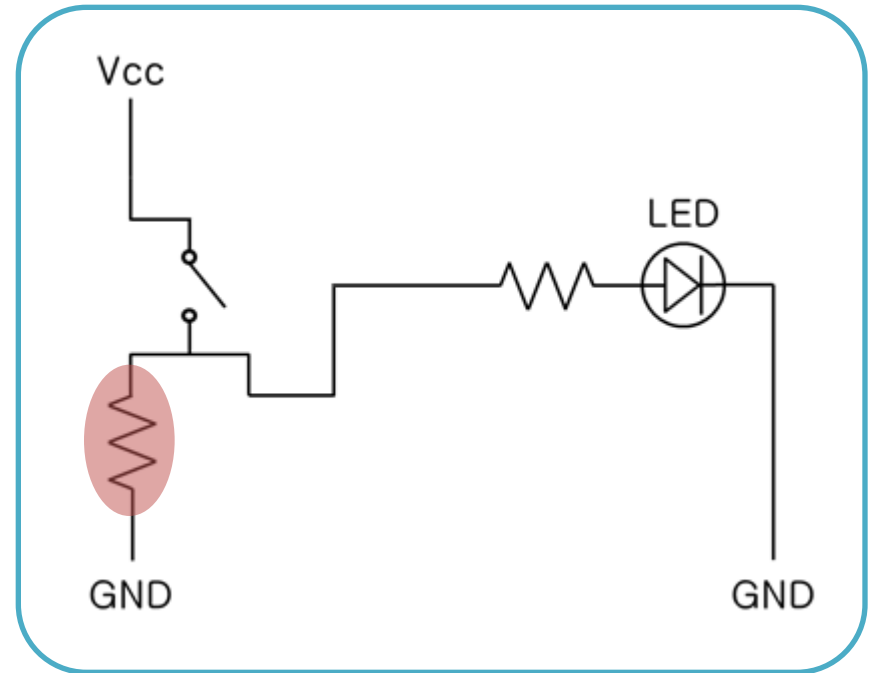
**Pull-down Resistor**

# Combinational Logic Practice

- Pull-up & pull-down resistors



**Pull-Up Resistor**



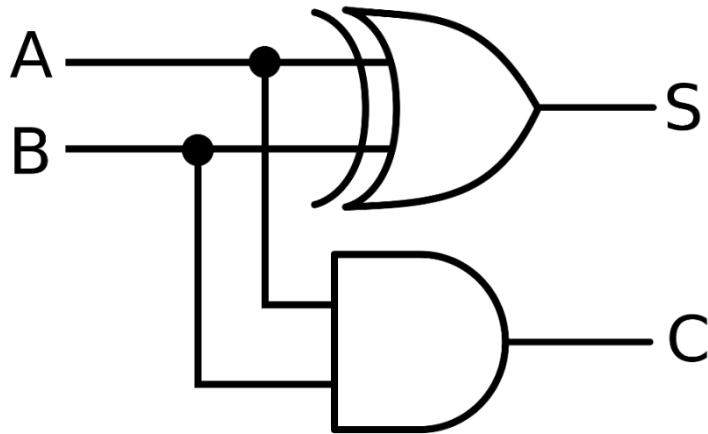
**Pull-Down Resistor**



# Combinational Logic Practice

- **Practice: Half-adder implementation**

- Let's implement half-adder on breadboard.



Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

# Homework

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1. Draw a circuit schematic for the below formula using ONLY NOR gates and NOT gates. You can draw it by hand or using any of a computer program.
  - $Y = A(B+CD)$
  
2.  $Y = AB + ABC + A'B + AB'C$ 
  - (1) Make a truth table
  - (2) Minimize # of gates
  - (3) Draw a circuit schematic

# Homework

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3.

Implement simple combinational logic circuits **1-1** and **1-2** using breadboard. (Take pictures to prove it's working)

- **3-1.** Implement a full adder using 2-input NAND gates only
- **3-2.** Implement LM1 & RM1 using NOR gates only
  - 4-bit input, 2-bit LM1 output, 2-bit RM1 output

Position (2-bit) : 00 01 10 11

Input (4-bit) : ☐ ☐ ☐ ☐

- LM1 (RM1) outputs position of leftmost (rightmost) 1 in input
- E.g. LM1(1010) = 00, RM1(1010) = 10  
LM1(0100) = 01, RM1(0100) = 01  
LM1(0000) = XX, RM1(0000) = XX (don't care)

# Homework

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- Write a report
  - Either in Korean or in English
  - Must include the result and discussion of the practice
  - # of pages doesn't matter
  - **Due : 23 Sep., 7:00 pm (Before class, on eTL)**