E-learning week self-study materials

Please go through these materials on your own during the e-learning/recess week

You may post questions on the edventure discussion board or email Dr Chan if you have questions regarding these contents

- **IEEE logic symbols**
- **CMOS transmission gate**
- **CMOS 2-input multiplexer**

IEEE/ANSI Standard Logic Symbols

- use rectangular symbols
- bubbles replaced by small triangles or wedges (think 0)
- Students are required to recognise these symbols but not required to draw these symbols

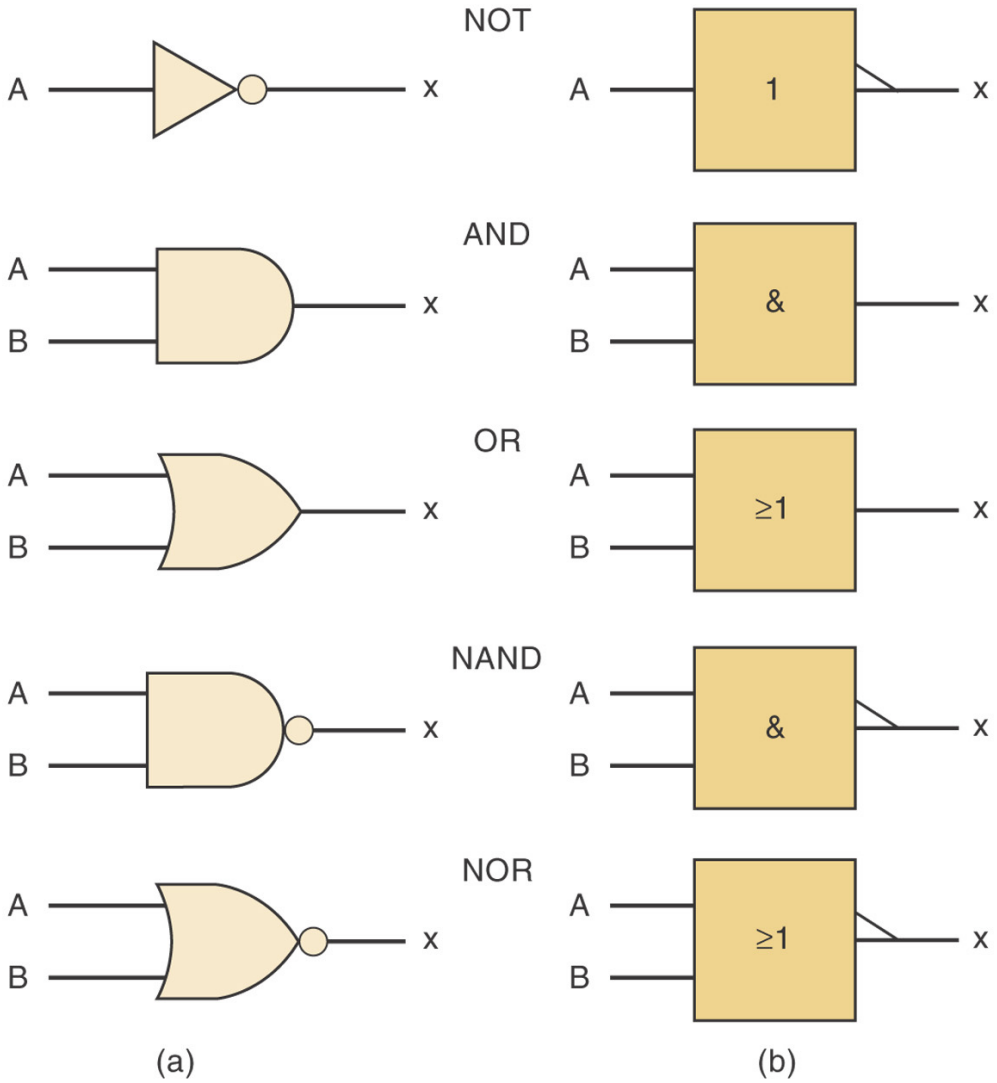
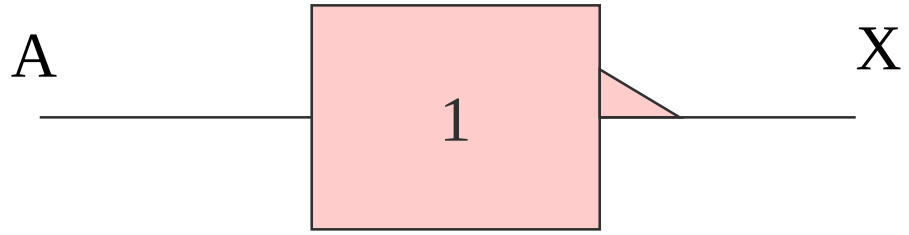


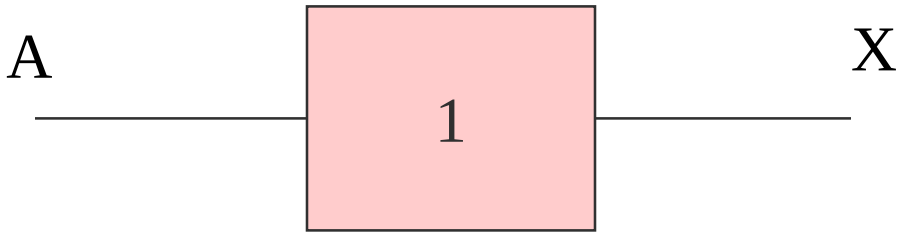
Fig. 3-41: Traditional and IEEE logic symbols (Tocci 10th ed)

Output is 0 when “the single input” is 1



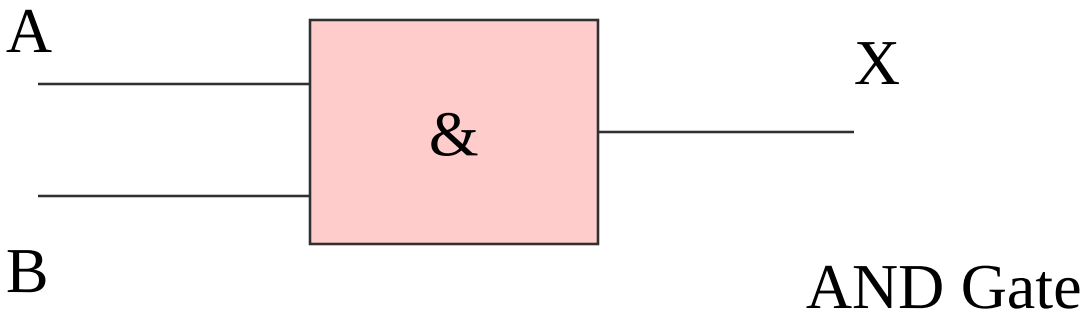
NOT Gate

Output is 1 when “the single input” is 1

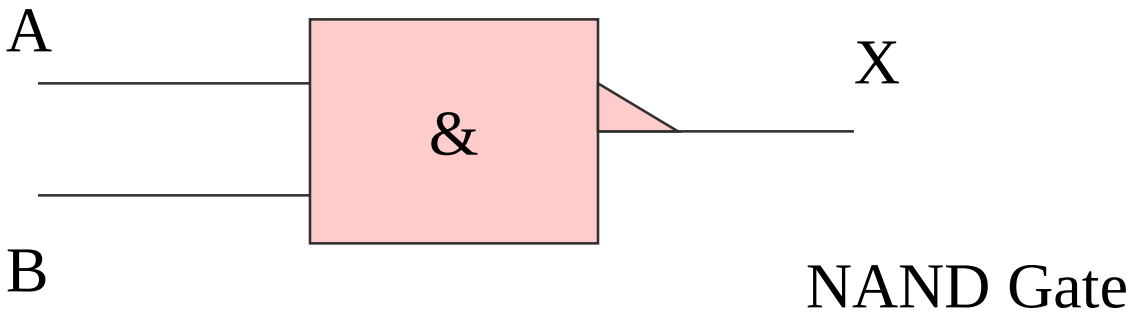


Buffer

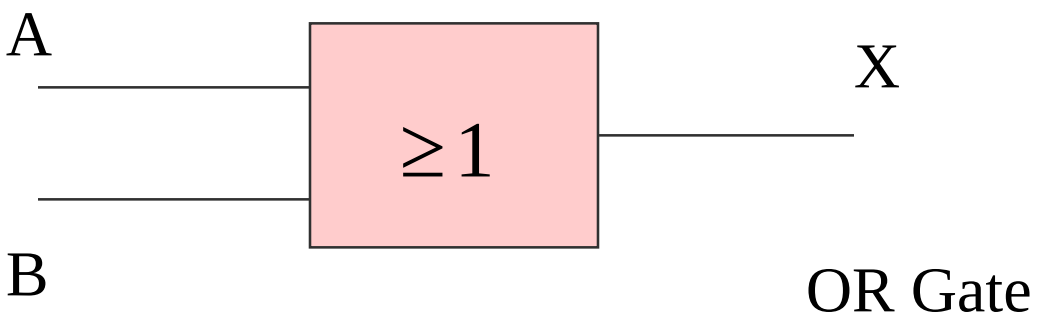
Output is 1 when “all the inputs” are 1



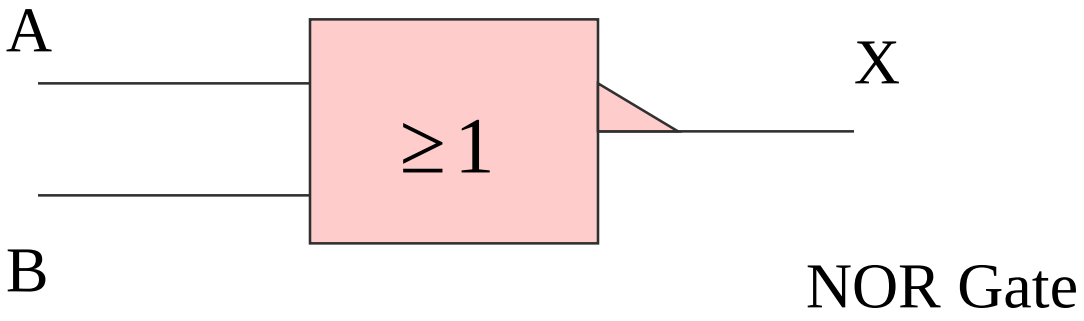
Output is 0 when “all the inputs” are 1



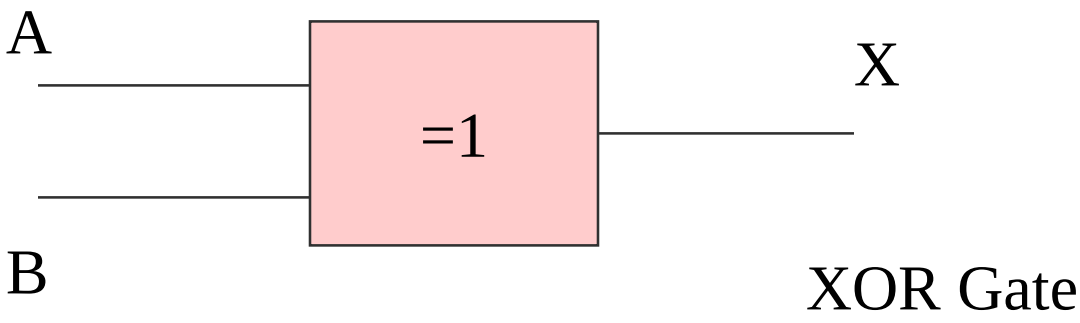
Output is 1 when “at least one input is” 1



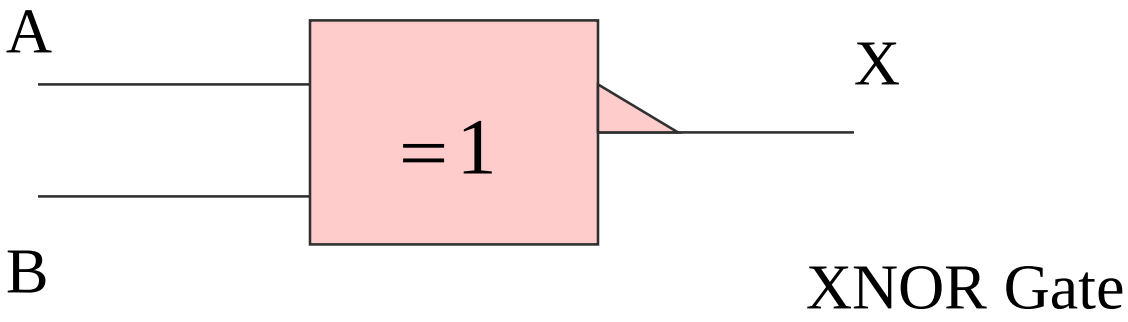
Output is 0 when “at least one input” is 1



Output is 1 when “exactly one input” is 1



Output is 0 when “exactly one input” is 1



IEEE/ANSI Standard Logic Symbols

How to interprete

- **The symbol inside the rectangle specifies the requirement on the inputs**
- **& : “all the inputs”**
- **1 : “the single input” – only true for a buffer or an inverter**
- **≥ 1 : “at least one input”**
- **=1 : “exactly one input” – e.g. on a 2-input XOR gate**

Example 1: CMOS transmission gate

- Section 3.7.1 of textbook by Wakerly
- 1 PMOS and 1 NMOS transistors can be connected in parallel to form a logic-controlled switch.
- When S=0 (S'=1), both transistors are off. Output f is effectively disconnected from input X. f is at high impedance.
- When S=1 (S'=0), both transistors are on. Output f is effectively connected to input X.

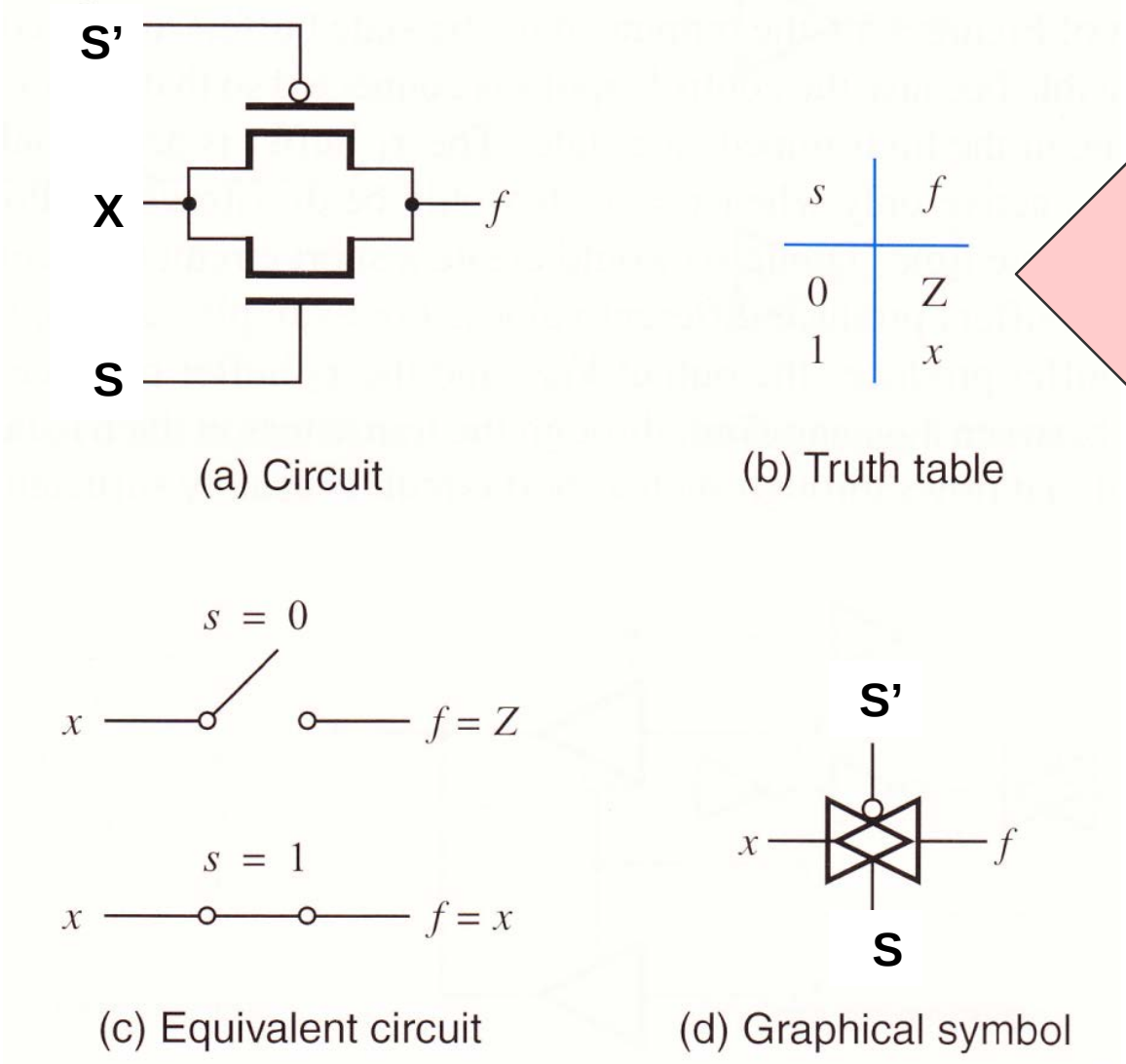
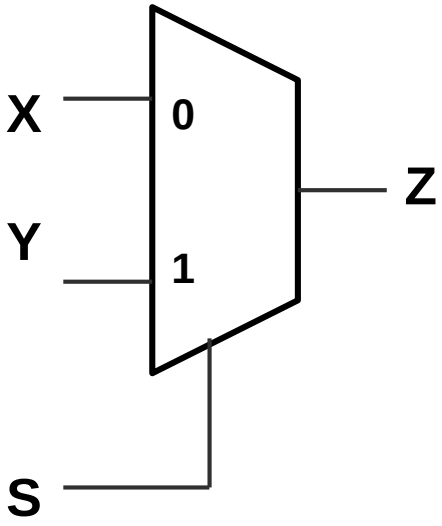
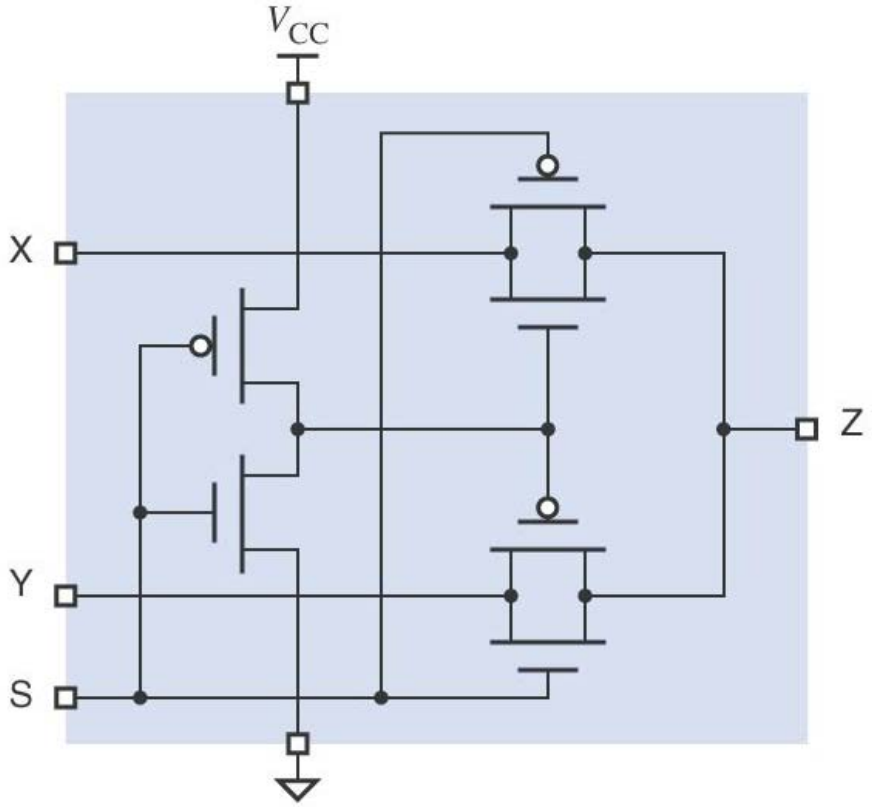


Fig. 3-45: CMOS transmission gate

Example 2: Two-input multiplexer using CMOS transmission gates

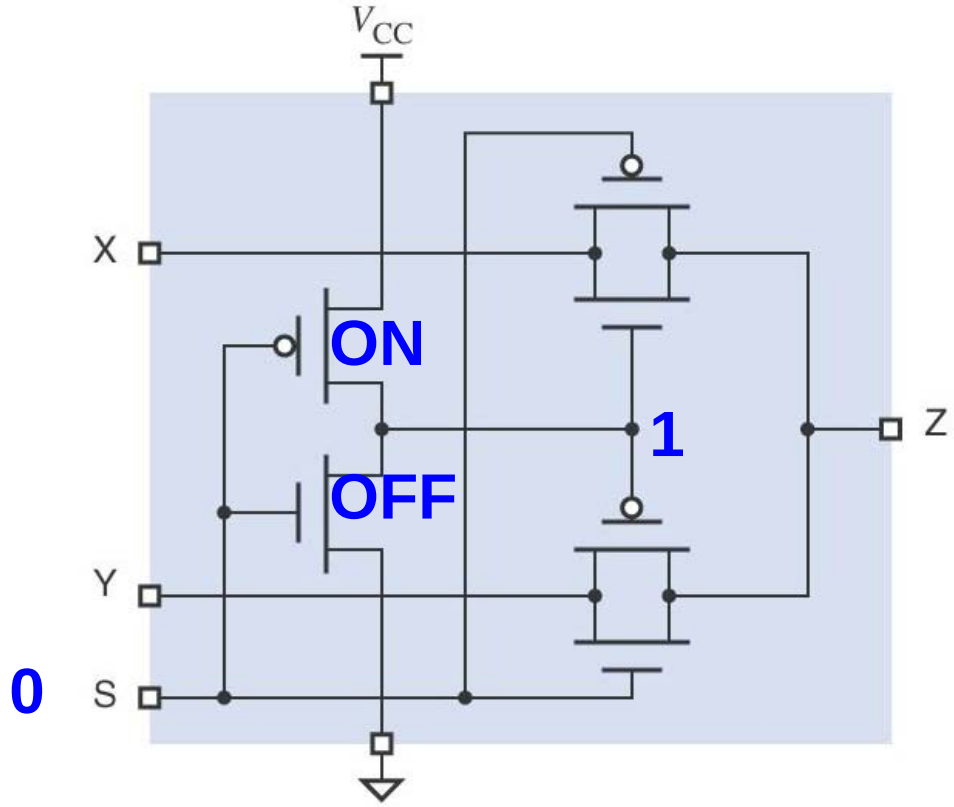


Logic symbol



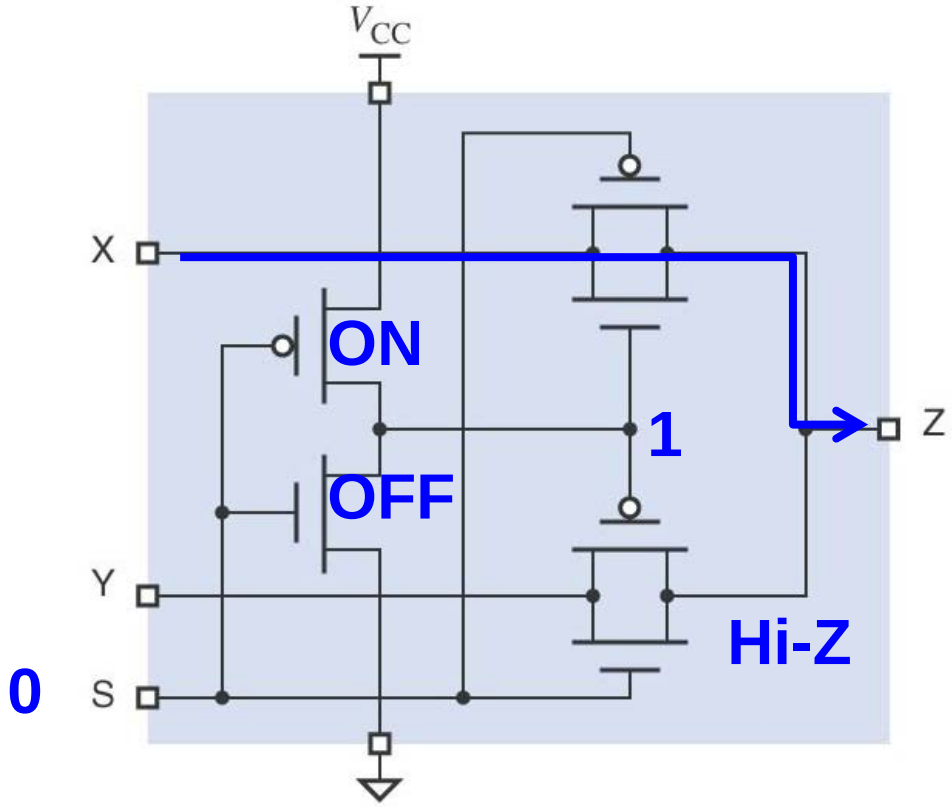
Circuit analysis: when S=0

- **When S=0**



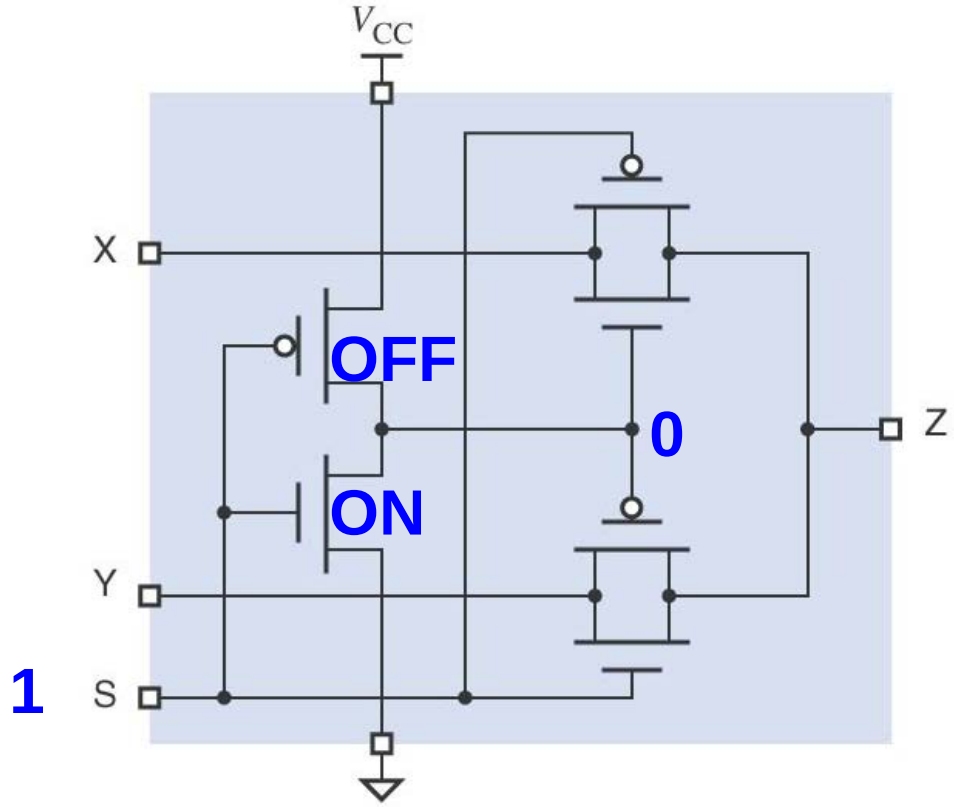
Circuit analysis: when S=0, only upper transmission gate conducts.

- When S=0,
- Output Z=X



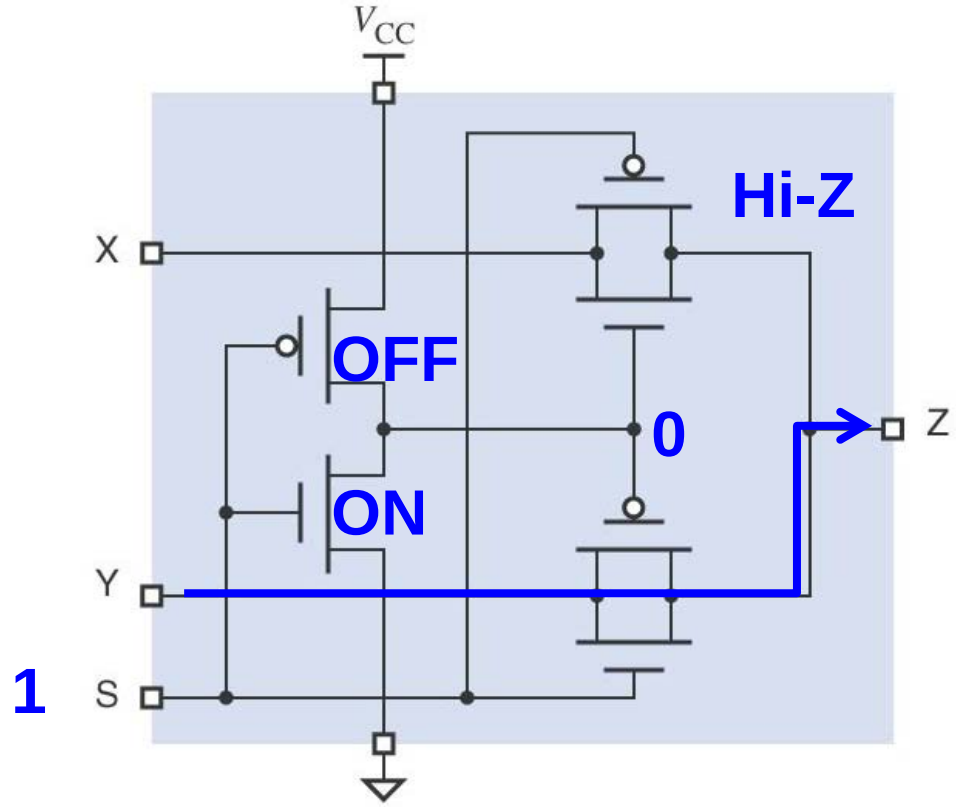
Circuit analysis: when S=1

- **When S=1**

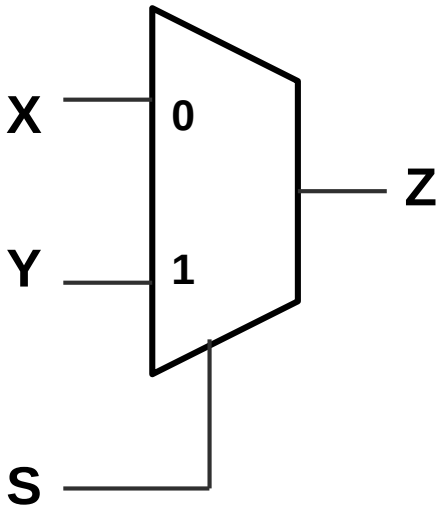


Circuit analysis: when S=1, only lower transmission gate conducts.

- When S=1,
- Output Z=Y



Two-input multiplexer using CMOS transmission gates: truth table



Logic symbol

Input S	Ouput Z
0	X
1	Y

Truth Table