Note: Do not refer to the case study notes for this tutorial. A smaller system will be used instead.

7.1 Cache

1. Given a processor system with the following characteristics
   - Processor has a direct-mapped cache with 32 cache blocks and a cache size of 512 bytes.
   - Cache Memory Access time = 5ns.
   - Cache Hit rate = 0.9
   - 64Kbyte DRAM used as the main memory.
   - DRAM Memory access time = 200ns

   a. In doing cache mapping analysis, how many **blocks** would the main memory be partitioned to?

   b. What is the format of a memory address as seen by the cache (i.e. determine the sizes of the tag, block and offset fields)?

   c. CPU needs to read a byte from main memory address 0x0DB63.

      i. Which cache block would CPU looked at to search for the required data?
      ii. How many main memory blocks could potentially be mapped to the same cache block as that of 0x0DB63?
      iii. How does the CPU knows if the cache block identified in (i) above contains the data that it needs?
      iv. What is the purpose of the 'offset' field in the cache mapping?

   d. What is the effective access time of the memory in this system?

2. In a system with 8 bit Main Memory address, given that it has a fully associative cache with 4 blocks and block size of 16 words,
   a. Would the following address access sequence allow the user to see if LRU or FIFO replacement policy is used? Why?

      0x00, 0x10, 0x20, 0x30, 0x40, 0x50, 0x60, 0x70

   b. How would you modify the address access sequence so that user can tell whether LRU or FIFO is used?

7.2 Virtual Memory

3. In a processor system with the following characteristics,
   - 1 MByte Virtual memory space
   - 64 Kbyte DRAM as main memory
   - Paging scheme used for virtual memory management, Page Table as shown in Table 7.2
   - Virtual Page size = 1 KByte
   - TLB with 4 entries

Table 7.2 – Page Table

Virtual Page Number	Valid Bit	Page Frame Number
0	1	1
1	1	2
2	0	-
3	1	16
4	1	9

a. How many bits are required for each virtual address?

b. How many bits are required for each physical address?

c. What is the maximum number of entries in the page table in Table 7.2?

d. What is the maximum number of valid entries in the page table in Table 7.2?

e. With reference to Table 7.2, answer the following. Indicate when a page fault occurs.

   (i) The compiler mapped the UART routine to virtual address 0x005F0 – 0x006FF, where in the DRAM would you be able to find the UART routine?

   (ii) The compiler mapped the I2C routine to virtual address 0x009C0 - 0x009DF, where in the DRAM would you be able to find the I2C routine?

   (iii)What happens when there is a page fault?

f. What memory are the Page Table and TLB resided?

g. What is the function and effect of a TLB?