CE1006/CZ1006
Computer Organisation and Architecture

Computer Memory

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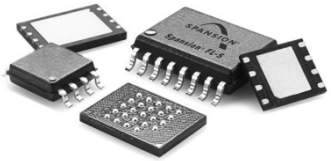
Computer Memory

Semiconductor-based

Solid-State HDD

SODIMM

CF, SD, miniSD, microSD, MMC



NAND Flash Memory Chip

Thumb Drive

Magnetic-based

Magnetic HD

- Which is (are) volatile?
- Which is (are) non-volatile?

Optical-based

CD, DVD, BluRay

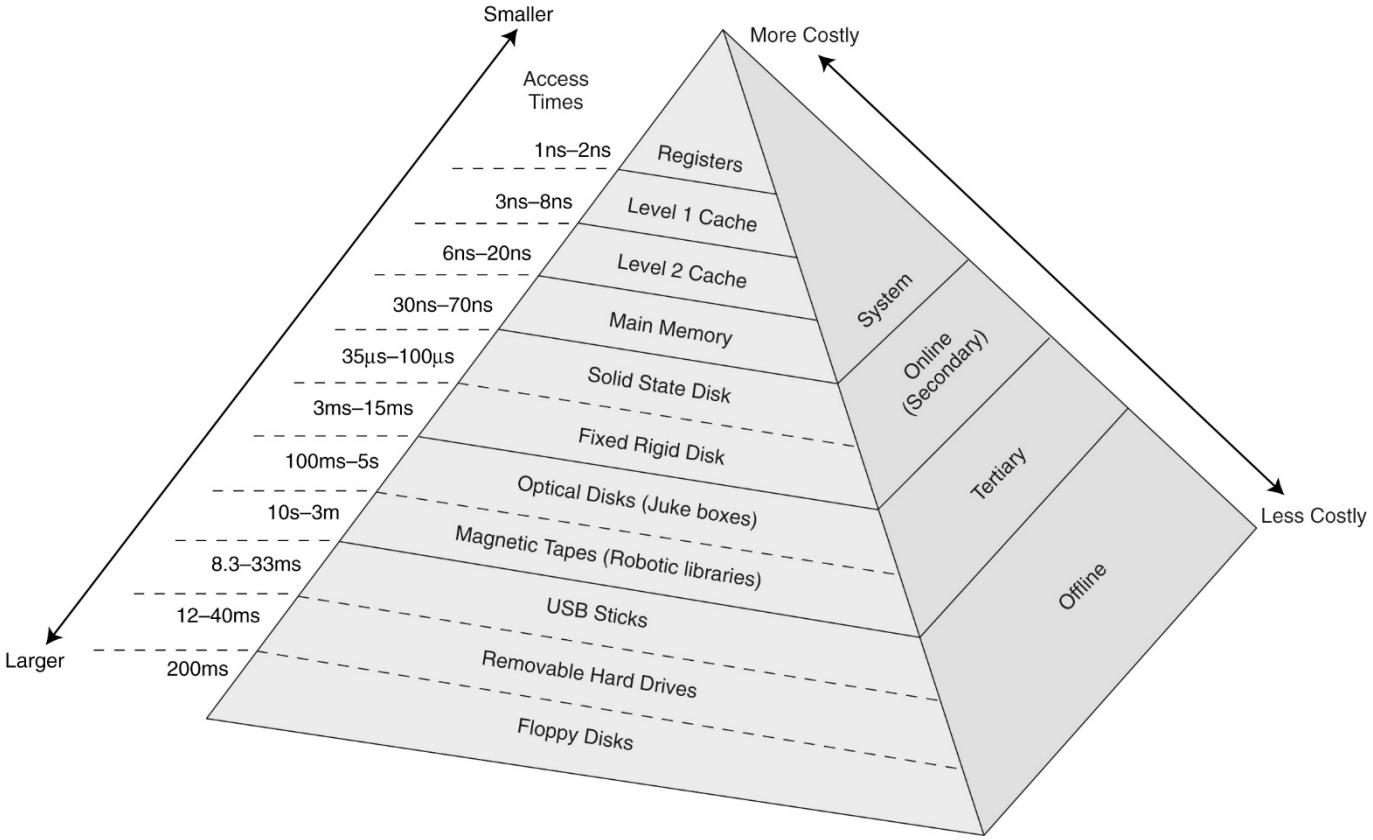
Volatile and Non-Volatile Memory

- Volatile
  - Data is **lost** when electric power is **removed**.
  - Temporary storage.
  - Typically used as system memory.
  - We will look at Random Access Memories such as Static-RAM (SRAM) and Dynamic-RAM (DRAM).

- Non-volatile
  - Data is **retained** even if electric power is **removed**.
  - Permanent storage.
  - Typically used as main storage.
  - We will look at FLASH, magnetic hard-disk and optical compact disc specifically.

Memory – Cost vs Function Trade Off

- The memory and storage devices may be organised like a pyramid.
- The pinnacle has the fastest access time, but is also more costly.
- Memory Access Time below are only for illustration. These changes with improvement in technology.



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Computer Memory
Volatile Memory

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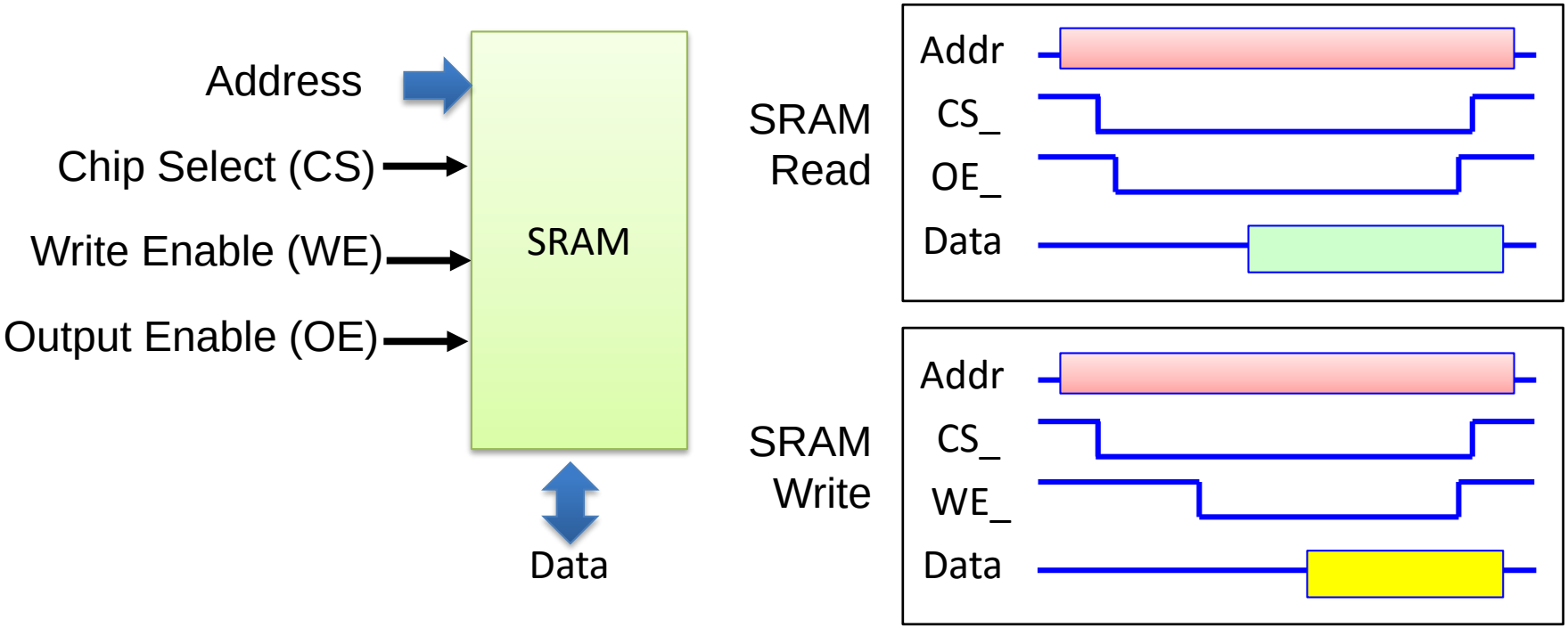
Random Access Memory (RAM)

- Static RAM (SRAM)
  - Static Random Access Memory
  - **Data stored as long as supply is applied**.
  - Large (4 to 6 transistors per cell).
  - Fast.
  - Differential.
- Dynamic Random Access Memory (DRAM)
  - **Periodic refresh required**.
  - Small (1 to 3 transistors per cell).
  - Slower.
  - Single-ended.

Static RAM (SRAM) Access



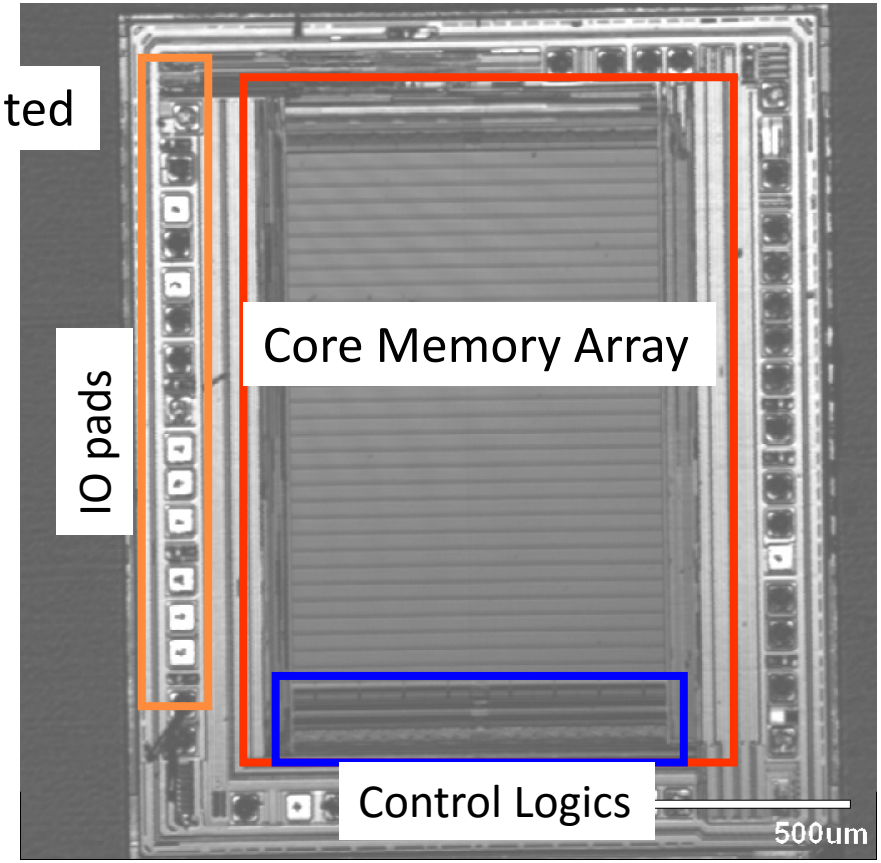
Addr	Specifies Address of memory location.	
Data	Data to be read/written.	Typically 8,16 or 32 bits.
CS	Control signals	Chip Select (Enables or disables the chip).
WE		Write Enable (Allows data to to be written)
OE		Output Enable (Allows SRAM to output data)

SRAM Chip DeCap

Commercial SRAM Chip
Cypress CY62128, 1 Mbit

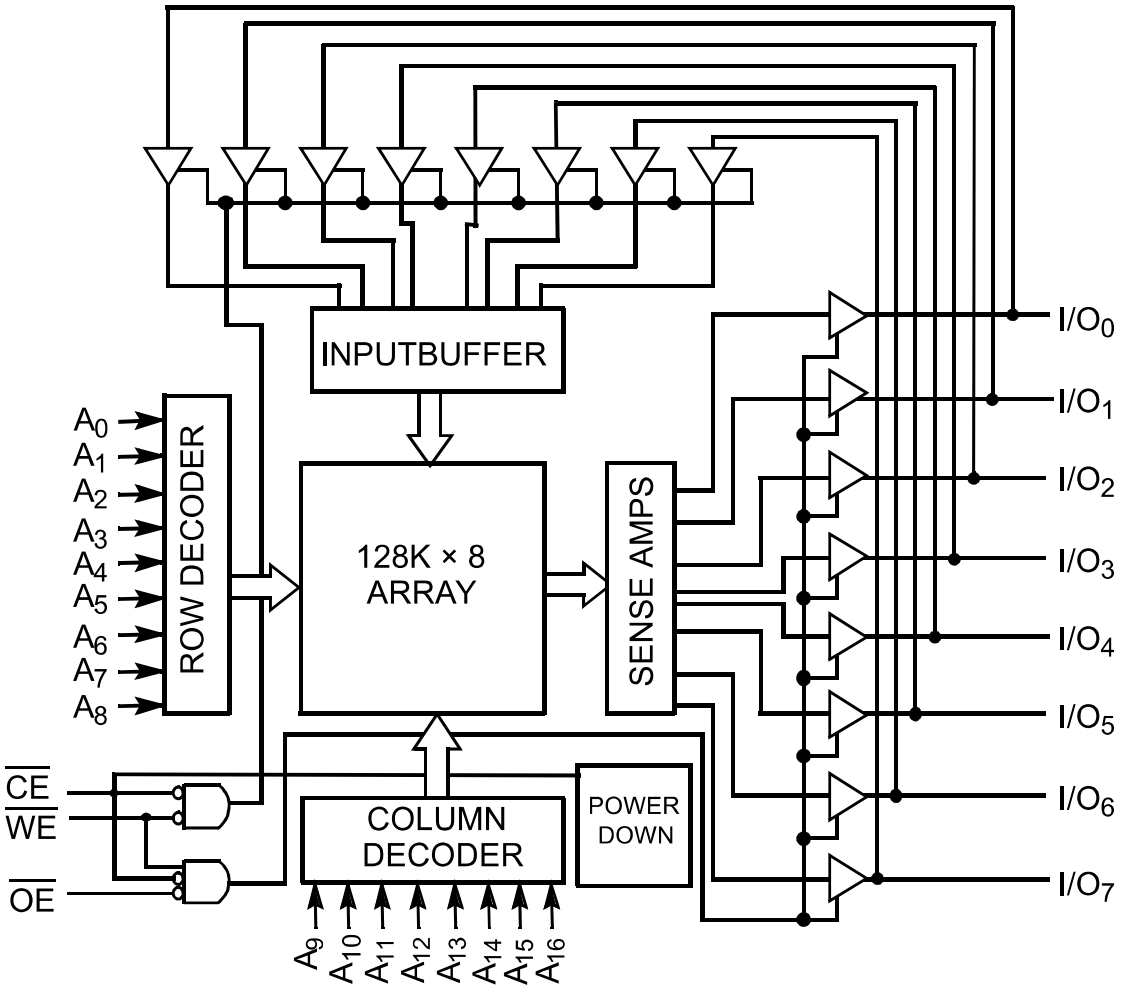
Decapsulated

Decapsulated silicon die
Laser scanned image, 5x magnification



- **Memory** array takes up **most** of the **real estate**.
- Leading Edge Semiconductor Process is usually first tested with Memory Design.

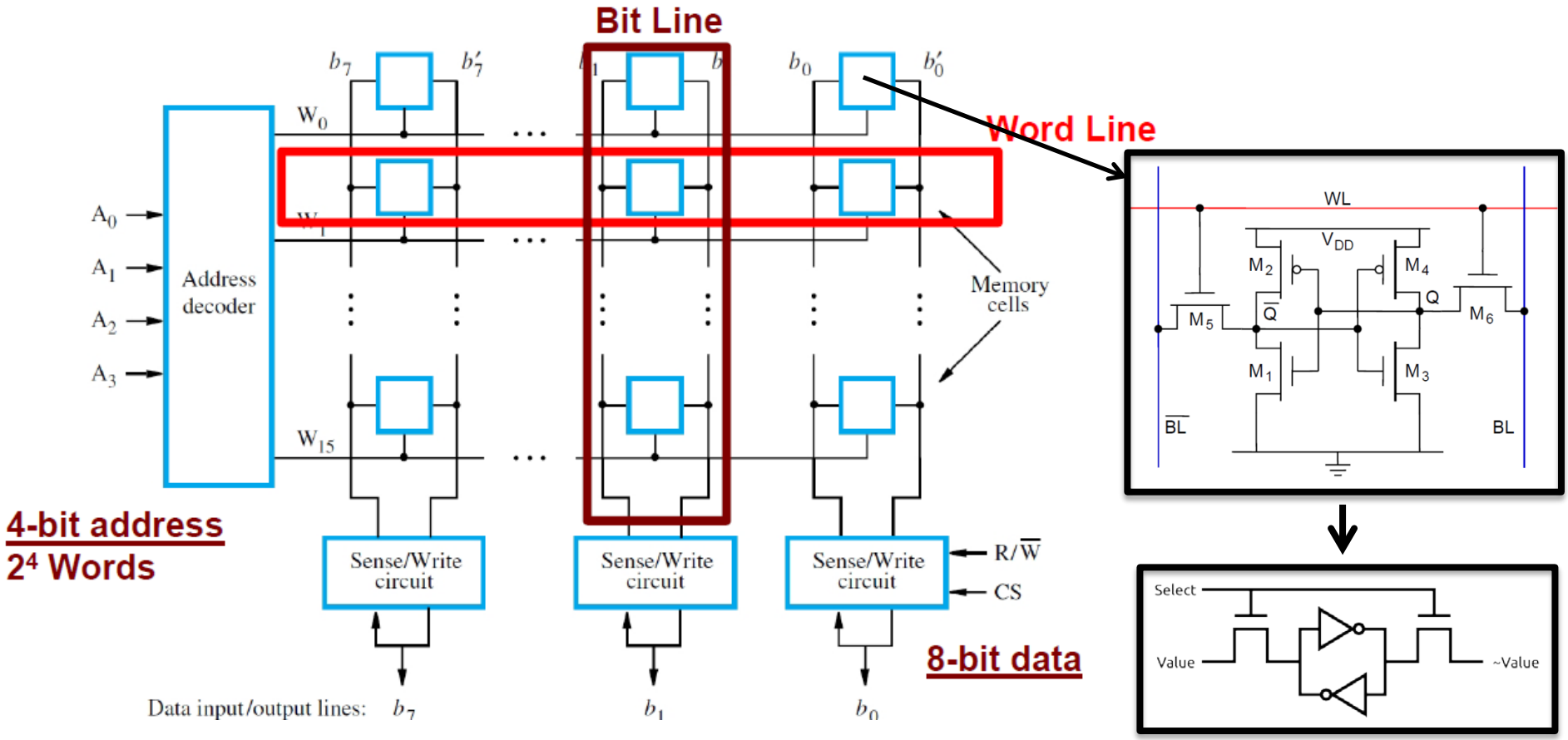
SRAM Internal Circuitry



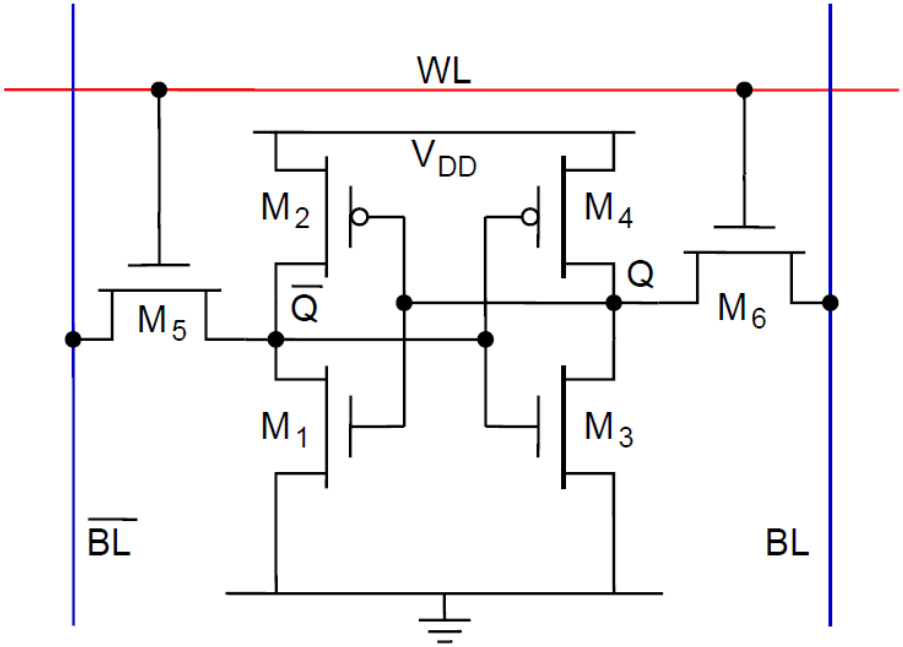
- Memory array
- 1M SRAM cells for the chip shown.
- Control circuitry
- Decoders
- Sense amplifiers
- Input/Output multiplexers

SRAM Cell

- Memory cells are organised in arrays (rows), and are accessed via the **word lines** and **bit lines**.
- Each individual SRAM Bit consist of 6 Transistors (typical design).

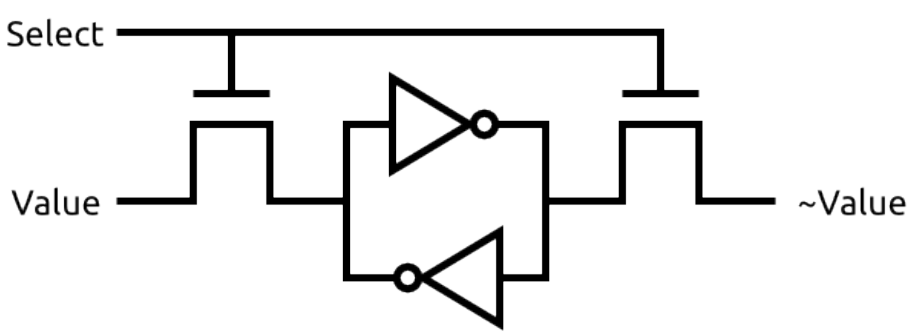


SRAM Cell

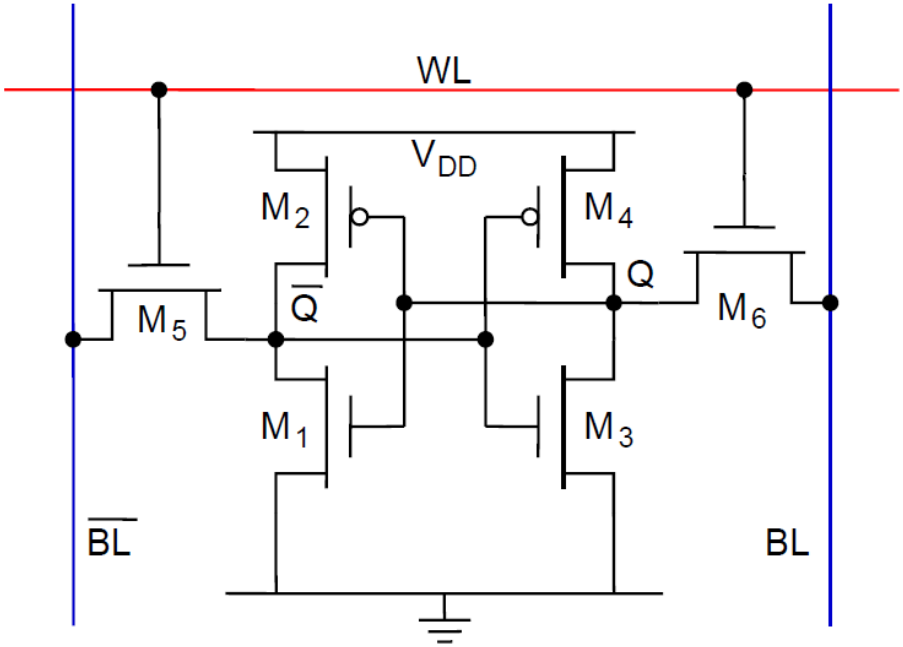


- There are six transistors
- M1, M2, M3, M4, M5 and M6
- Word line (**WL**) is derived from Address Decoder Output. It **controls the Read/Write process**
- The actual data are placed on the differential bit lines (**BL** and BLB). This is **connected to the Data Bus**.

- The **data bit is stored in M1, M2, M3 and M4** (which is equivalent to two invertors connected as shown on the right).
- M5 and M6 are **pass transistors**.



SRAM Cell



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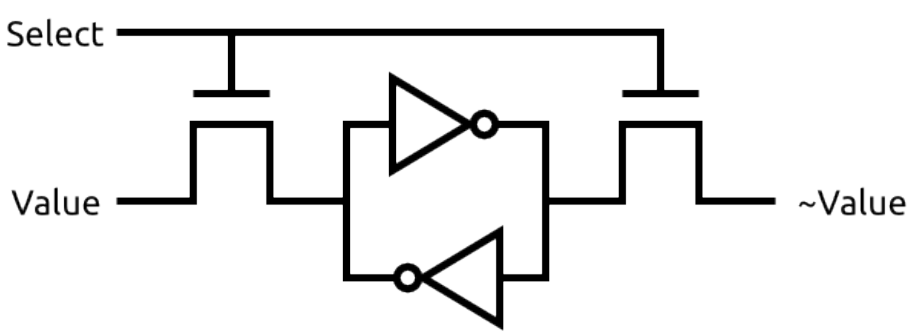

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Computer Memory
Dynamic RAM (DRAM)

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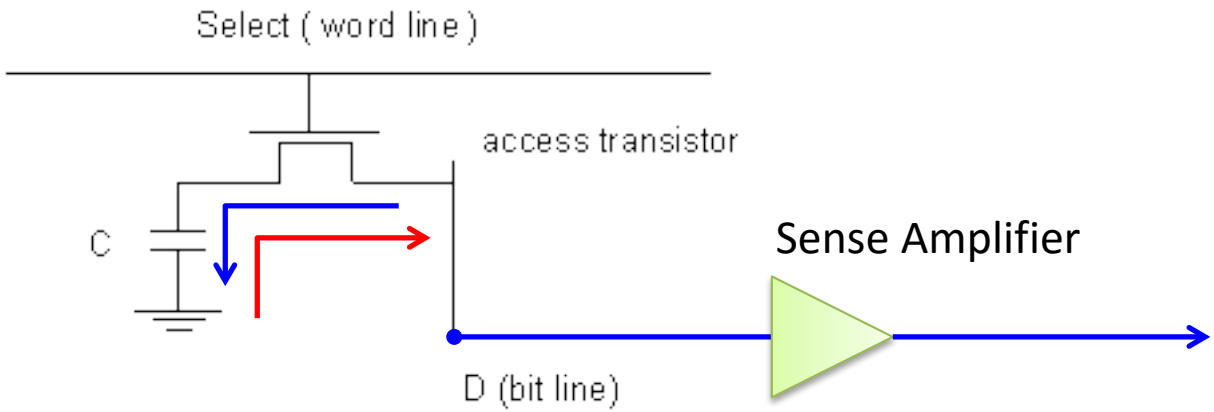
Dynamic RAM (DRAM)



- Single Transistor Design
- DRAM uses a **capacitor** as its **storage** element.
- The Transistor is used to control charges flowing in and out of the capacitor during the Read and Write process.
- Write Process
  - **To store a Logic '1': Enable the Transistor, transfer charge into capacitor.**
  - **To store a Logic '0': Enable the Transistor, discharge the capacitor.**
- Read Process
  - Enable the Transistor. Measure the capacitor charge using a sense amplifier.

DRAM – Read and Refresh

- DRAM **Read** Process **destroys** information stored on capacitor
- The process of measuring charges on a capacitor also effectively discharged it i.e. data is destroyed.
- Hence, the original data has to be re-written back after every read
- **Periodic refresh** is needed as the stored charge “leaks” with time.
- The basic DRAM is more or less obsolete in the market today. It is replaced by its synchronous version called **Synchronous DRAM (SDRAM)**.
- Difference between SDRAM and DRAM is that the former make use of a clock signal from the host to synchronise data transfer, enabling **faster transfer rate**.
- Other enhancements of SDRAM includes its double date rate versions DDR, DDR2, DDR3 SDRAM, which could reach transfer speed of more than 2G transfers per second.

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Computer Memory
Non Volatile Semiconductor Memory

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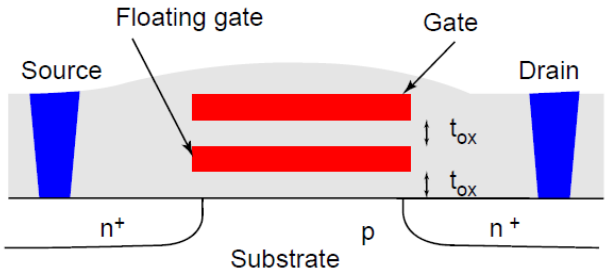
EPROM and EEPROM

- EPROM (Erasable Programmable ROM)
  - Earliest floating gate transistors are implemented as Erasable Programmable ROM (EPROM) devices.
  - Need to put device under ultra-violet (**UV**) light to **erase** the stored program.

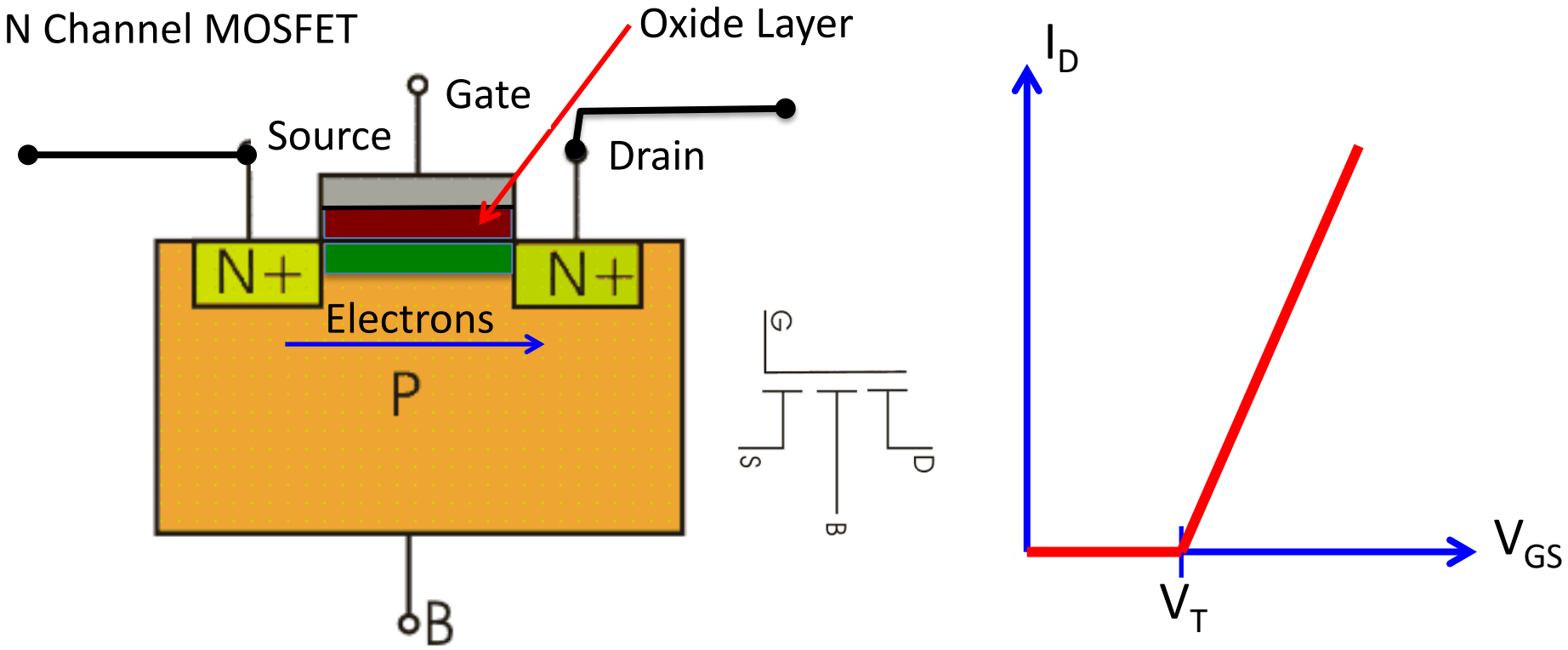
[Source] www.old-computers.com



Device cross-section

- EEPROM (Electrically Erasable PROM)
  - Advancement in process technologies make it possible to **reduce** the **oxide thickness** (t_{ox}).
  - Can **electrically program or erase device**.
  - Hence, named Electrically Erasable Programmable ROM (E^2PROM).

MOSFET



- MOSFET (**M**etal-**O**xide-**S**emiconductor **F**ield **E**ffect **T**ransistor)
- For N-Channel MOSFET, if **Gate-Source Voltage (Vgs) > Threshold Voltage** (Vt), a **conductive** channel of electrons (inversion layer) will be formed and current will flow if a positive voltage is applied across Drain and Source.

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Floating Gate Transistor

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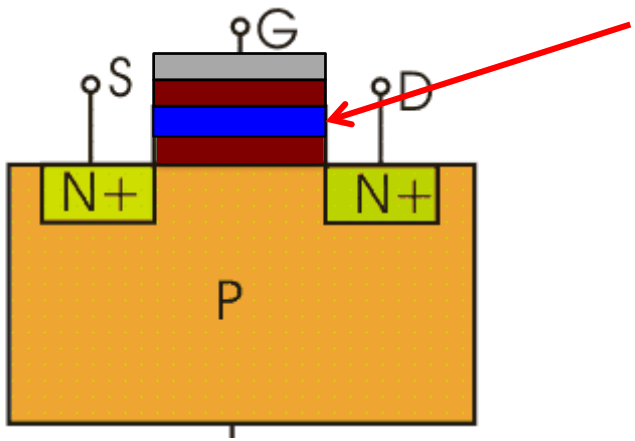
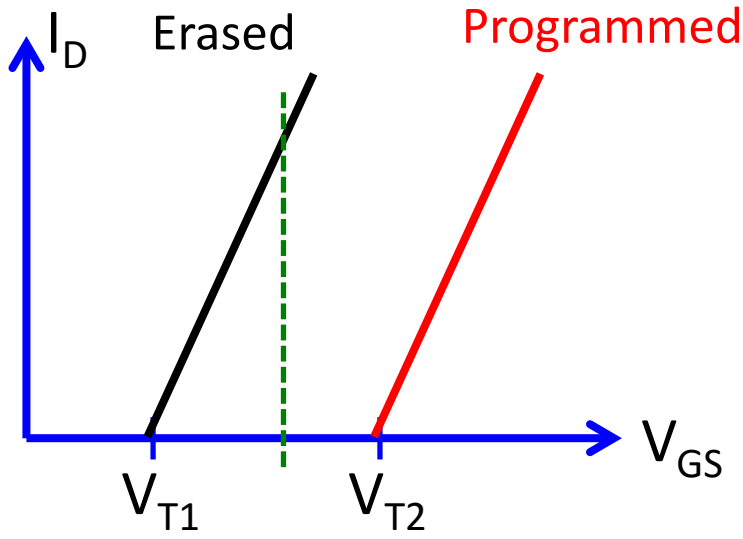
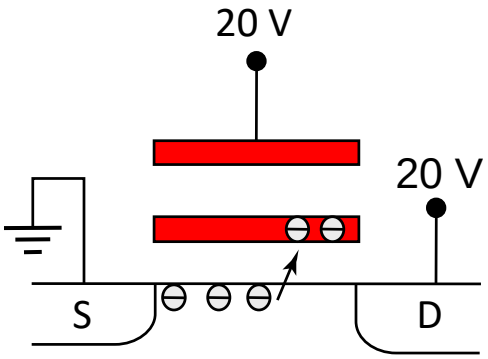
Floating Gate Transistor

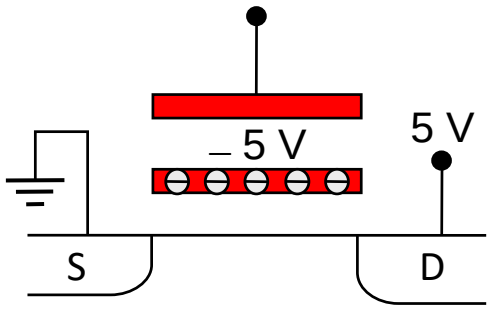




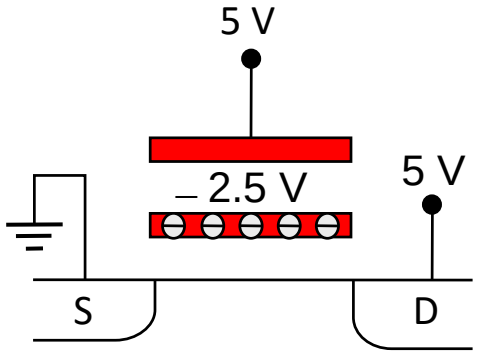
"Programming" results in altered threshold voltage of Floating Gate Transistor



Avalanche injection



Removing programming voltage leaves charge trapped

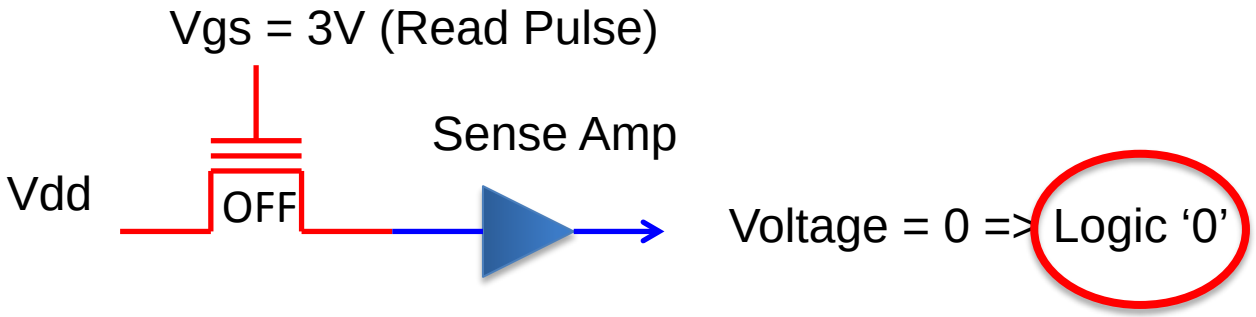


Programming results in higher V_T.

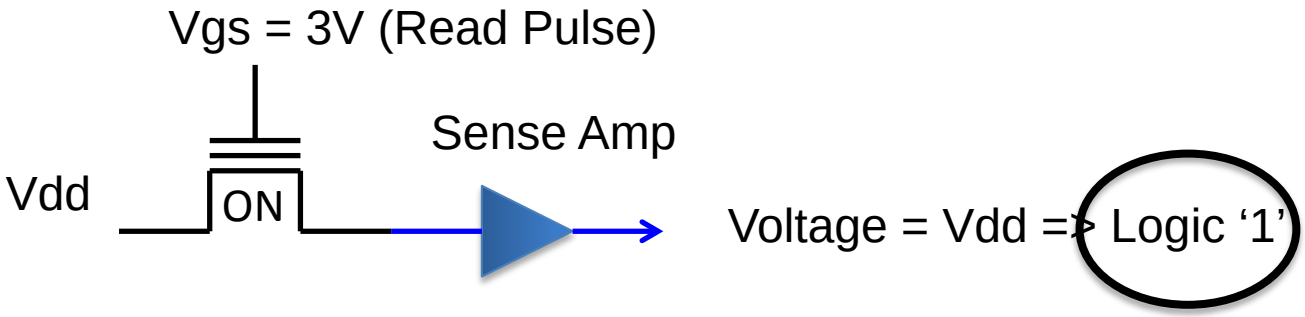
Storing Data using Floating Gate

- With a positive Gate Voltage (Vgs)
  - Transistor **OFF** if floating gate is **programmed** (contains charges).
  - Transistor **ON** if floating gate is **erased** (no charges).
- 3V value below is for **illustration only**. Actual Vt value in real world may varies depending on the doping of the transistors.

Programmed State
Transistor OFF
(Vt > 3V)



Erased State
Transistor ON
(Vt < 3V)



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Computer Memory
Flash Memory (NAND and NOR Flash)

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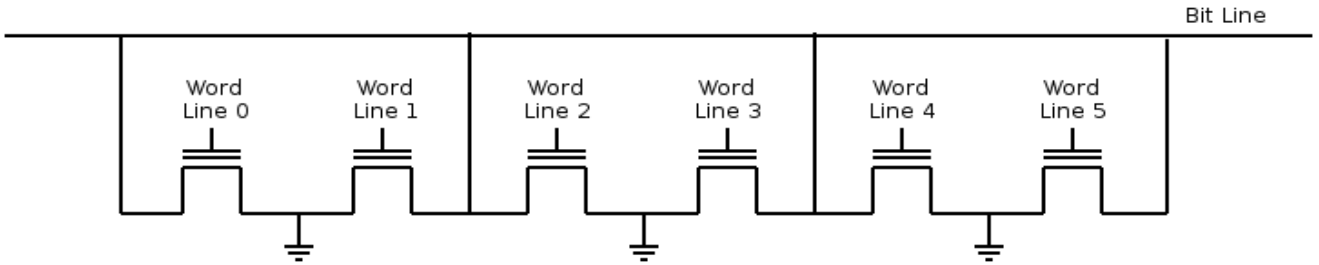
Flash

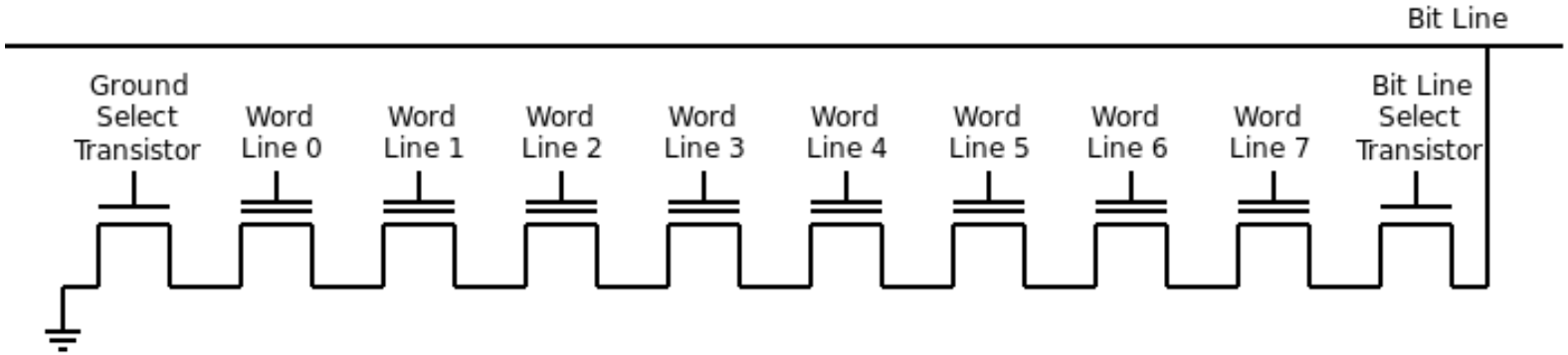
- Based on same floating gate technology as EEPROM.
- Can be **erased in larger blocks size** compared to EEPROM (which typically erase at **smaller bytes level**).
- **Erase cycle** is comparatively **slower** than other operation (Read/Write) so Flash has a faster speed than EEPROM when performing write operations for large block of data.
- Flash also **cost less** than EEPROM.
- Suitable for system requiring large amount of non-volatile memory.
- Two main types of Flash in the market
  - **NAND Flash**
  - **NOR Flash**

NOR Flash



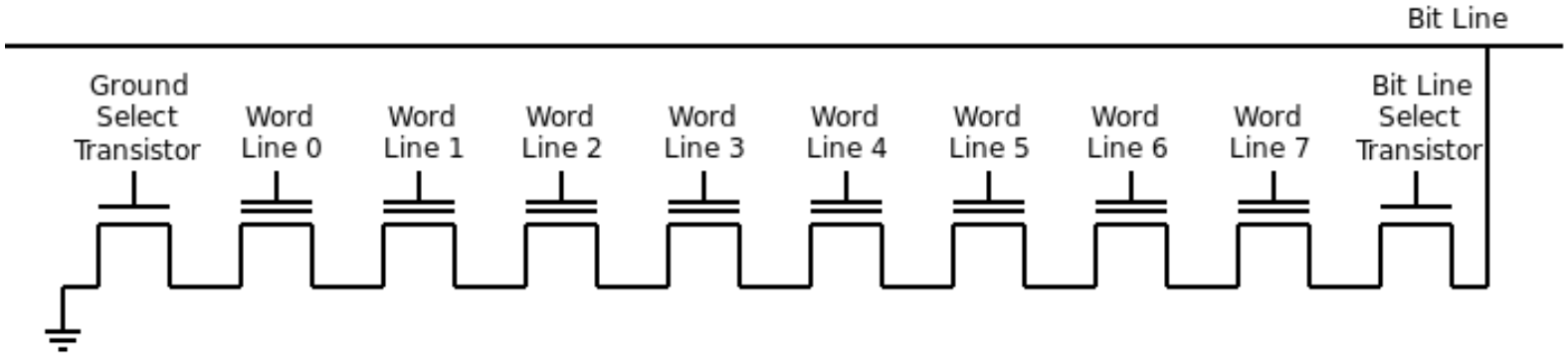
- Cell behaves like a NOR gate.
  When **any** one of the **Word Line > Vt(Prog), Bit Line output = 0**.
- Supports **Execute in Place**, i.e. Program code stored in NOR Flash can be executed directly without the need to transfer to RAM first.
  - Allows Random Reading of memory data using only Address information (no additional Commands needed).
- The Parallel NOR Flash **behaves like SRAM** during **read** operation.
- Need **Special Commands** (issue in **Write** mode) in order to perform operations other than Data Read. E.g. Program, Erase etc.
- Allows **random word/byte programming**. But **erasure** has to be done **at block level**. Typical Block size: 64KByte, 128KByte, 256KByte
- Use mainly as system memory to store program code.

NAND Flash



- Cell behaves like NAND gate.
  - **Bit line output = '0'** only when **ALL Word Line > Vt(Prog)**.
- **Does not support execute in place** operation.
  - Data has to be accessed one page at a time.
  - Command issued to open a particular page, followed by which byte(s) is/are needed in the page.
  - NAND chips uses a single bus to carry Address and Data.
- **Lower Cost per Bit than NOR**. Used mainly as Main Storage.
  - On Board Main Storage, USB Flash Drive, SSD etc

NAND Flash



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NOR and NAND Flash chip pin-out