TUTORIAL #6 Interrupts and DMA (CE/CZ1006)

6.1 Interrupts

1) Consider the system diagram in Figure 1 of case study notes.
   - The processor UART peripheral in its Serial I/O module is configured to receive data with format of 1 start-bit, 7 data-bits, 1 parity-bit and 1 stop-bit.
   - Each time the UART peripheral receives a character, it'll store the data into a buffer.
   - It will then interrupt the CPU to notify CPU that there is data available.
   - The CPU will then execute the Interrupt Service Routine (ISR) to read the character received.
   - Interrupt Latency is the term used to describe the time between interrupt request and entrance to ISR.
   - The minimum interrupt latency for the CPU is 10 μs and it takes 90 μs for the CPU to execute the instructions in the ISR (read the received data from the buffer).
   - Assume that the UART data is transferred back to back i.e. no delays between each UART packets.

   What is the maximum baud rate that can be supported with this UART interface?

2) The specifications of the system in Figure 1 (case study notes) requires the buttons to be asserted 400 times over a 24-hour period. Given that the processor consumes 0.1mA current when it is idling and 50mA when it is in active mode i.e. running code, answer the following.

   (a) Supposed polled IO technique is used to sample the button status. Given that the processor poll the buttons every 100ms, each poll requires the processor to be active for 10ms, what is the average current consumed over the 24-hour period?

   (b) If interrupt-driven I/O is used to sample the button status, what is the average current consumed in the same 24-hour period? Given that it takes 20ms to service each interrupt, including interrupt latency and ISR execution.

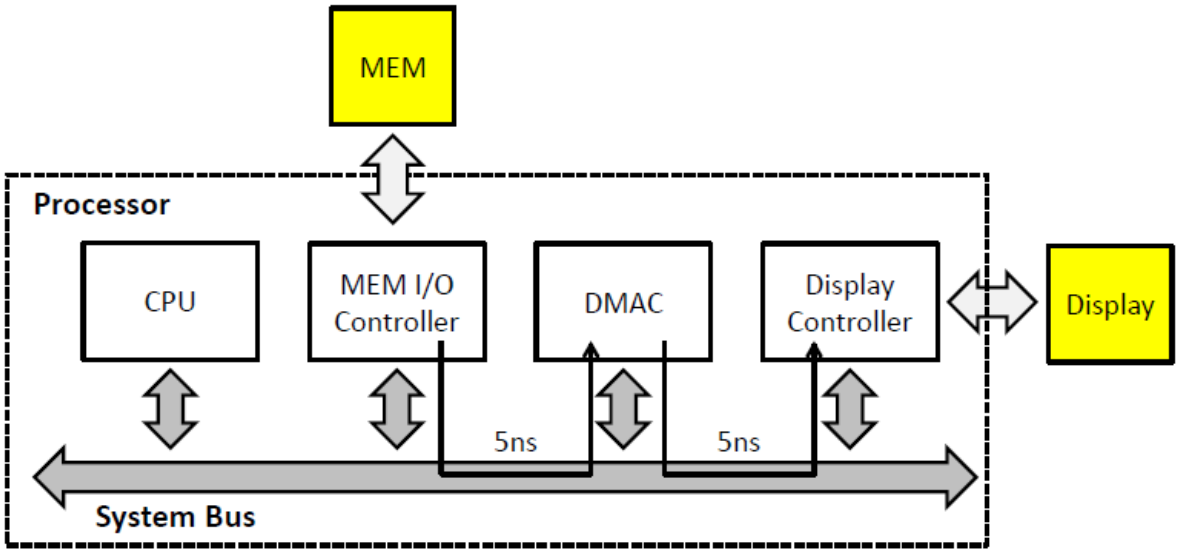
   (c) Comment on the results obtained above.

6.2 Direct Memory Access (DMA)

3) Although DMA does not use the CPU, the maximum transfer rate is limited by other factors. Name three possible factors that might limit the transfer rate of a block of data from the memory.

4) Consider the system in Figure 1 (Case study notes). Given that

- The processor's system bus is capable of supporting simultaneous transfer of up to 3 bytes of data at one time.
- DMA is used to transfer video data from Memory to Display Controller module.
- Each video pixel data consist of three bytes (Red, Green, Blue) and are transferred simultaneously on the system bus on each bus cycle.
- Each transfer on the system bus takes 5ns and transfer of the bus control between the CPU and the DMAC takes 100ns.
- Assume that DMAC is using Fetch-and-Deposit DMA.
- Note that 1Kbyte = 1024 Byte.



(a) Given that the video is output at a rate of 30 frames per second and each video frame has a resolution of 1920x1080 pixels. If burst-mode was used by the DMAC to burst one frame of video data at a time, would the DMAC be able to transfer each video frame completely?

(b) Repeat the calculation if the DMAC is using cycle-stealing mode, assume that DMAC needs to wait at least 5 instructions before it could request for control of the system bus again.