9.1 Number Representation

1. Figure 9.1 shows a 32-bit binary number (the top row shows the bit numbers and the bottom row shows the corresponding binary values). Find the decimal value of the 32-bit number if it is represented as:
   a. Unsigned Integer
   b. Signed-Magnitude
   c. Two's Complement
   d. IEEE 754 Single Precision

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 9.1 – 32-bit number

9.2 Integer Arithmetic

2. An array consisting of the length of 256 wires is given by L[0], L[1], … , L[255]. Describe a scheme to compute the average length of the 256 wires that will yield a result with the highest precision based on the following specifications:

   - 16-bit registers are used for storing the data and result.
   - Only Single-Precision and Fixed-Point arithmetic is used.
   - Maximum possible length of each wire is 0x3FF and is an integer.

   Illustrate your answer in the form of a mathematical expression and justify your answer.

9.3 Pipelines

3. Consider a processor (not VIP) with 4 pipeline stages: Fetch Instruction (F), Decode (D), Execute (E) and Store (S). Assume that

    - Branch target address is calculated at the execute stage
    - Instruction length for every instruction is one word long
    - Each pipeline stage take 1 cycle to complete

    How many cycles does the code in Figure 9.2 take? Assume delay branching is not enabled.

```
      MOV   AR, #5      ; I1
      MOV   R0, #0x800  ; I2
      MOV   R1, #0x300  ; I3
Loop  SUB   [R0],[R1]   ; I4
      INC   R1          ; I5
      JDAR  Loop        ; I6
      ADD   R3, [R0]    ; I7
      MOV   [R1], R3    ; I8
```

Figure 9.2

4. Consider a processor (not VIP) with 4 pipeline stages: Fetch Instruction (F), Decode (D), Execute (E) and Store (S). Assume that

    - Branch target address is calculated at the execute stage
    - Instruction length for every instruction is one word long
    - Each pipeline stage takes 1 cycle to complete
    - No Resource Conflicts
    - Delayed Branching is enabled

    Identify and describe ALL pipeline conflicts the code in Figure 9.3 has when run in the pipeline processor above. Suggest workaround for pipeline conflicts identified.

```
      MOV   R3, #300    ; I1
      MOV   AR, #10     ; I2
Loop  JDAR  Loop        ; I3
      ADD   R1, [R3]    ; I4
      INC   R3          ; I5
      MOV   R1, R3      ; I6
      MOV   R0, R2      ; I7
```

Figure 9.3

(Not necessary to be covered during tutorial)

[Optional, but students are encouraged to attempt these questions]

9.4 Rounding Error

5. You have been tasked to write a program that calculates the actual time based on a counter that is incremented once every 0.10 seconds. For example, if the counter value is 3,600,000, you would expect the actual time to be 100 hours ((3,600,000 x 0.1) / (60 x 60)).

   Suppose you have decided to use a 24-bit fixed point representation as shown in Figure 8.4 to store the value of 0.10 seconds ($2^{-4} + 2^{-5} + 2^{-8} + 2^{-9} + 2^{-12} + 2^{-13} + \ldots$).

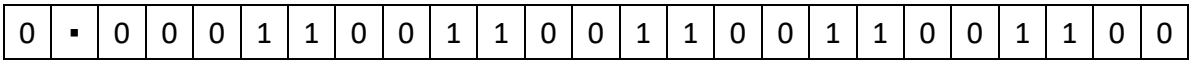

Figure 9.4 – Fixed point representation of 0.1010

   a. Approximate the round-off error (in decimal) of 0.10_{10} due to the fixed-point representation.
   b. What is the effect of this round-off error on the time calculated if the counter value is 3,600,000?