General Description

The DS28E05 is a 112-byte user-programmable EEPROM organized as 7 pages of 16 bytes each. Memory pages can be individually set to write protected or EPROM emulation mode through protection byte settings. Each part has its own guaranteed unique 64-bit ROM identification number (ROM ID) that is factory programmed into the chip. The DS28E05 communicates over Maxim Integrated's single contact 1-Wire® interface at overdrive speed with the ROM ID acting as node address in the case of a multiple-device 1-Wire network.

Applications

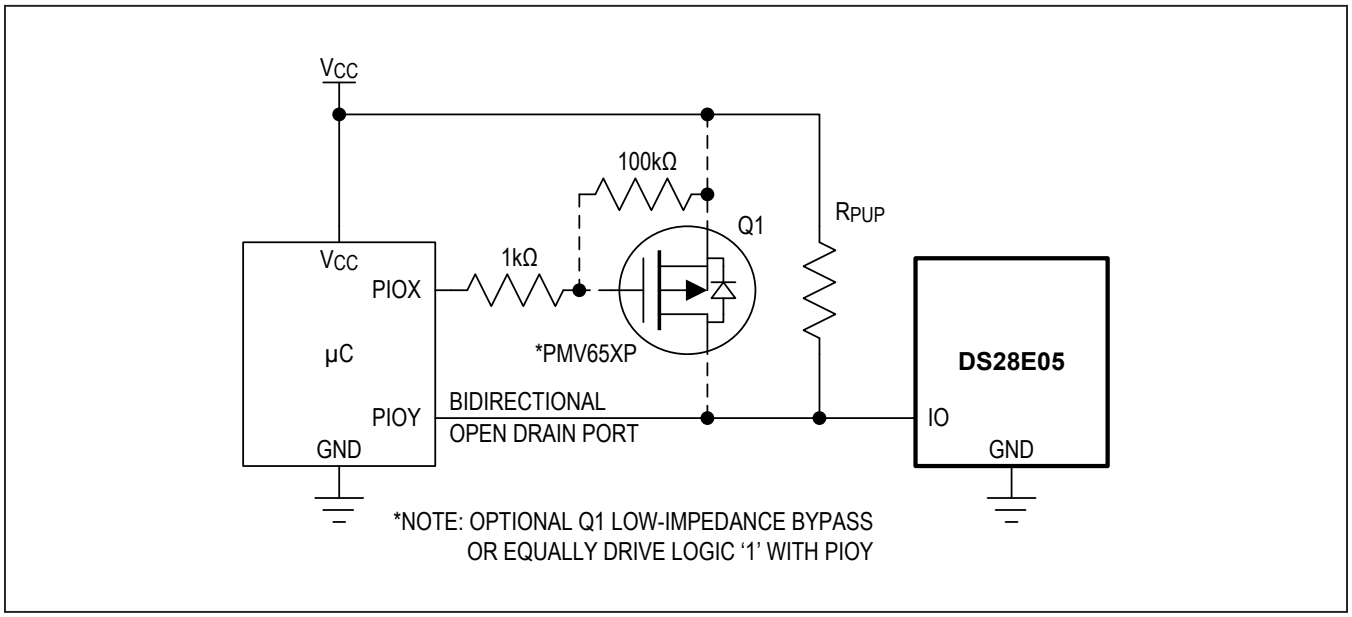
- Accessory/PCB Identification
- Medical Sensor Calibration Data Storage
- Analog Sensor Calibration
- Aftermarket Management of Consumables

Features

- Single-Contact 1-Wire Interface
- 112 Bytes User EEPROM with 1K Write Cycles
- Programmable Write Protection and OTP EPROM Emulation Modes for User Memory
- Unique Factory-Programmed 64-Bit ROM ID Number
- Communicates with Host at Up to 76.9kbps (Overdrive Only)
- Operating Range: 1.71V to 3.63V, -40°C to +85°C
- ±8kV HBM ESD Protection (typ) on IO Pin
- 4-Ball UCSP, 2-Pad SFN, 3-Pin SOT23 and 6-Pin TSOC Packages

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit



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maxim integrated™

Absolute Maximum Ratings

IO Voltage Range to GND.....-0.5V to 3.63V
IO Sink Current.....±20mA
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: GENERAL DATA						
1-Wire Pullup Voltage	V_{PUP}	(Note 2)	1.71		3.63	V
1-Wire Pullup Resistance	R_{PUP}	V_{PUP} = 2.75V to 3.63V (Note 3)	300		1500	Ω
		V_{PUP} = 1.71V to 2.75V (Note 3)	300		750	
Input Capacitance	C_{IO}	(Notes 4, 5)		1500		pF
Input Load Current	I_L	IO pin at V_{PUP}		5	20	µA
		IO pin at V_{PUP} = 1.8V+5%		2	8	
High-to-Low Switching Threshold	V_{TL}	(Notes 6, 7)		0.65 x V_{PUP}		V
Input Low Voltage	V_{IL}	V_{PUP} = 2.75V to 3.63V (Notes 2, 8)			0.5	V
		V_{PUP} = 1.71V to 2.75V (Notes 2, 8)			0.3	
Low-to-High Switching Threshold	V_{TH}	(Notes 6, 9)		0.75 x V_{PUP}		V
Switching Hysteresis	V_{HY}	V_{PUP} = 2.75V to 3.63V (Notes 6, 10)		0.3		V
		V_{PUP} = 1.71V to 2.75V (Notes 6, 10)		0.17		
Output Low Voltage	V_{OL}	V_{PUP} = 1.89V to 3.63V, I_{OL} = 4mA (Note 11)			0.4	V
		V_{PUP} = 1.71V to 1.89V, I_{OL} = 2mA (Note 11)			0.4	
Recovery Time	t_{REC}	(Notes 2, 12)	5			µs
Time Slot Duration	t_{SLOT}	(Notes 2, 13)	13			µs
IO PIN: 1-Wire RESET, PRESENCE DETECT CYCLE						
Reset Low Time	t_{RSTL}	(Note 2)	48		80	µs
Reset High Time	t_{RSTH}	(Note 14)	48			µs
Presence Detect Sample Time	t_{MSP}	(Notes 2, 15)	8		10	µs
IO PIN: 1-Wire WRITE						
Write-Zero Low Time	t_{W0L}	(Notes 2, 16)	8		16	µs
Write-One Low Time	t_{W1L}	(Notes 2, 16)	0.25		2	µs
IO PIN: 1-Wire READ						
Read Low Time	t_{RL}	(Notes 2, 17)	0.25		2 - δ	µs
Read Sample Time	t_{MSR}	(Notes 2, 17)	t_{RL} + δ		2	µs

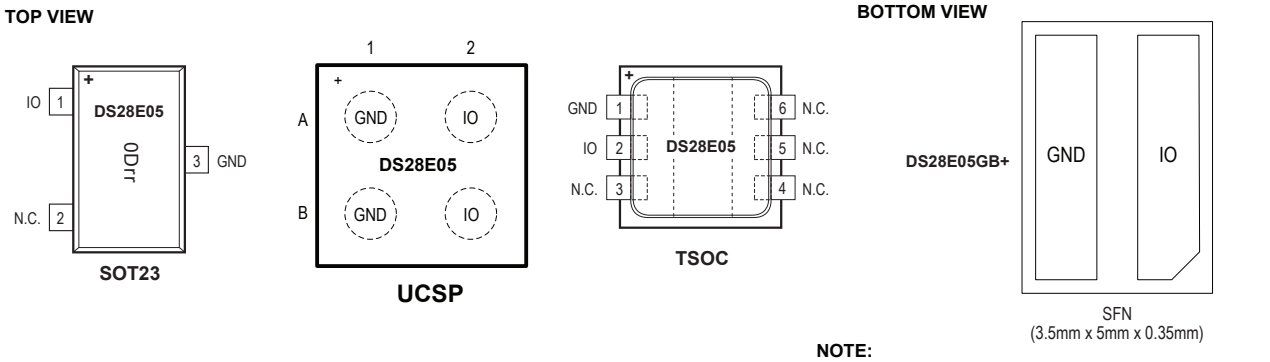
Electrical Characteristics (continued)

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM						
Programming Current	I_{PROG}	(Notes 5, 18)			400	µA
Programming Time for a 16-Bit Segment	t_{PROG}	(Note 19)			16	ms
Write/Erase Cycling Endurance	N_{CY}	T_A = +85°C (Notes 20, 21)	1000			—
Data Retention	t_{DR}	T_A = +85°C (Notes 22, 23, 24)	10			Years

Note 1: Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.
Note 2: System requirement.
Note 3: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times.
Note 4: Typical value represents the internal parasite capacitance when V_{PUP} is first applied. Once the parasite capacitance is charged, it does not affect normal communication.
Note 5: Guaranteed by design and/or characterization only. Not production tested.
Note 6: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage, which is a function of V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on IO. Lower V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.
Note 7: Voltage below which, during a falling edge on IO, a logic 0 is detected.
Note 8: The voltage on IO must be less than or equal to V_{ILMAX} at all times the master is driving IO to a logic 0 level.
Note 9: Voltage above which, during a rising edge on IO, a logic 1 is detected.
Note 10: After V_{TH} is crossed during a rising edge on IO, the voltage on IO must drop by at least V_{HY} to be detected as logic 0.
Note 11: The I-V characteristic is linear for voltages less than 1V.
Note 12: Applies to a single device attached to a 1-Wire line.
Note 13: Defines maximum possible bit rate. Equal to $1/(t_{W0LMIN} + t_{RECMIN})$.
Note 14: An additional reset or communication sequence cannot begin until the reset high time has expired.
Note 15: Interval after t_{RSTL} during which a bus master can read a logic 0 on IO if there is a DS28E05 present. The power-up presence detect pulse could be outside this interval but will be complete within 2ms for a 3.3V V_{PUP} or 20ms for a 1.8V V_{PUP} after power-up.
Note 16: ε in Figure 10 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F - \varepsilon$ and $t_{W0LMAX} + t_F - \varepsilon$, respectively.
Note 17: δ in Figure 10 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input-high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.
Note 18: Current drawn from IO during the EEPROM programming interval, during which the voltage at IO must not drop below 1.69V.
Note 19: The t_{PROG} interval begins immediately after the trailing rising edge on IO for the last time slot of the Release byte for a valid Write Memory sequence. Interval ends once the device's self-timed EEPROM programming cycle is complete and the current drawn by the device has returned from I_{PROG} to I_L.
Note 20: Write-cycle endurance is tested in compliance with JESD47G.
Note 21: Not 100% production tested; guaranteed by reliability monitor sampling.
Note 22: Data retention is tested in compliance with JESD47G.
Note 23: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to the data sheet limit at operating temperature range is established by reliability testing.
Note 24: EEPROM writes can become nonfunctional after the data-retention time is exceeded. Long-term storage at elevated temperatures is not recommended.

Pin Configurations



NOTE:
THE SFN PACKAGE IS QUALIFIED FOR ELECTRO-MECHANICAL CONTACT USE CASES ONLY. NOT FOR SOLDERING.

Pin Descriptions

PIN				NAME	FUNCTION
SFN	BUMP	SOT23	TSOC		
—	—	2	3–6	N.C.	Not Connected
1	A2, B2	1	2	IO	1-Wire Bus Interface. Open-drain signal that requires an external pullup resistor.
2	A1, B1	3	1	GND	Ground Reference

Detailed Description

The DS28E05 combines 896 bits of user EEPROM organized as seven 128-bit pages, 64 bits of administrative data memory, and a 64-bit ROM ID in a single chip. Data is transferred serially through the 1-Wire protocol, which requires only a single data lead and a ground return.

The user memory can have unrestricted write access (factory default), or can be write protected or put in EPROM emulation mode. Write protection prevents changes to the memory data. EPROM emulation mode logically ANDs memory data with incoming new data, which allows changing bits from 1 to 0, but not vice versa. By changing one bit at a time this mode could be used to create nonvolatile nonresettable counters. For more details refer to Application Note 5042: *Implementing Nonvolatile, Nonresettable Counters for Embedded Systems*.

The device's 64-bit ROM ID can be used to electronically identify the equipment in which the DS28E05 is used. The ROM ID guarantees unique identification and is also used to address the device in a multidrop 1-Wire network environment, where multiple devices reside on a common 1-Wire bus and operate independently of each other. Applications include accessory/PCB identification, medical sensor calibration data storage, analog sensor calibration, and after-market management of consumables.

Overview

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS28E05. The DS28E05 has three main data components: seven 128-bit pages of user EEPROM, 64 bits of administrative data memory, and a 64-bit ROM ID. Figure 2 shows the hierarchic structure of the 1-Wire protocol. The bus master must first provide one of the five ROM function commands: Read ROM, Match ROM, Search ROM, Skip ROM, or Resume Communication. The protocol required for these ROM function commands is described in Figure 8. After a ROM function command is successfully executed, the memory functions become accessible and the master can select one of the two memory function commands. The function protocols are described in Figure 6. **All data is read and written least significant bit first.**

64-Bit ROM ID

Each DS28E05 contains a unique ROM ID that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a cyclic redundancy check (CRC) of the first 56 bits. See Figure 3 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4.

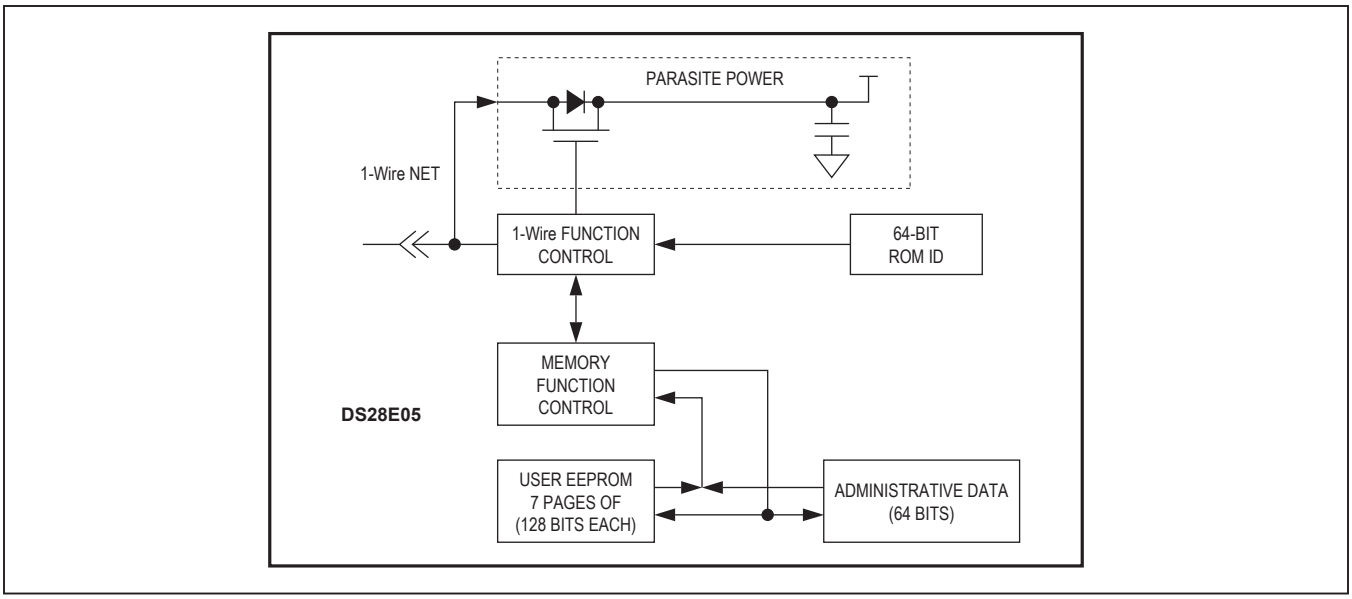


Figure 1. Block Diagram

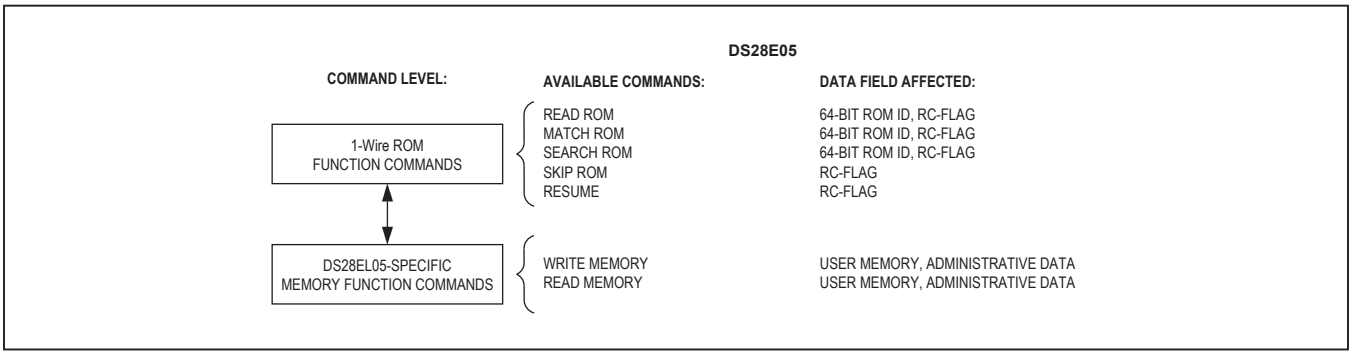


Figure 2. Hierarchical Structure for 1-Wire Protocol

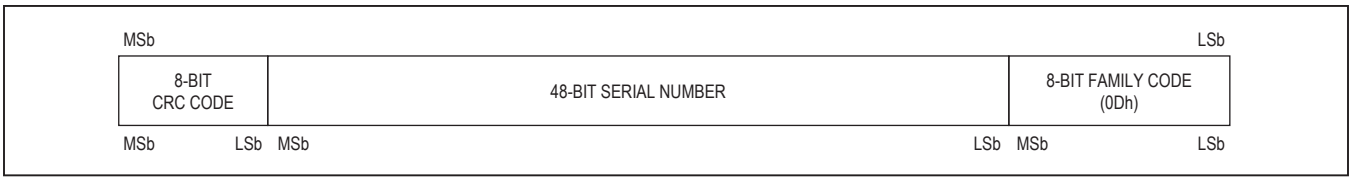


Figure 3. 64-Bit ROM ID

The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 1-Wire Cyclic Redundancy Check is available in Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton® Products*.

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The shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, the serial number is entered. After the last bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of the CRC returns the shift register to all 0s.

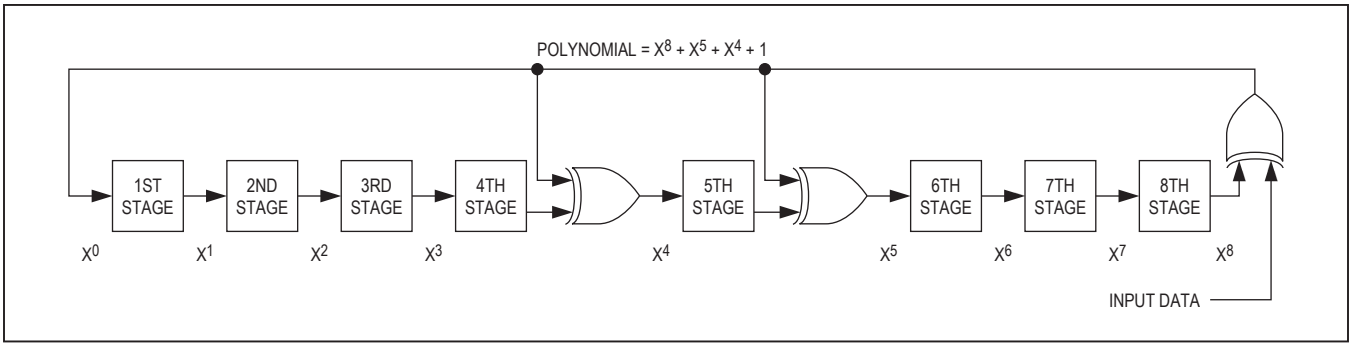

Figure 4. 1-Wire CRC Generator

Table 1. Memory Resources

NAME	SIZE (BYTES)	ACCESS MODE	PURPOSE
User memory (EEPROM)	112	Read, (Write)	Application-specific data storage
Administrative data	8	Read, (Write), Internal Read	Page protection settings, factory bytes, user bytes/manufacturer ID
ROM ID	8	Read, Internal Read	1-Wire network device address

Table 2. Address to Segment Mapping

	Segment 7		Segment 6		Segment 5		Segment 4		Segment 3		Segment 2		Segment 1		Segment 0	
	B1	B0	B1	B0	B1	B0	B1	B0	B1	B0	B1	B0	B1	B0	B1	B0
Page 0	(0Fh)							(08h)								(00h)
Page 1	(1Fh)							(18h)								(10h)
Page 2	(2Fh)							(28h)								(20h)
Page 3	(3Fh)							(38h)								(30h)
Page 4	(4Fh)							(48h)								(40h)
Page 5	(5Fh)							(58h)								(50h)
Page 6	(6Fh)							(68h)								(60h)
Page 7	ROM ID								Factory		MAN. ID/U.		PPD	PPC	PPB	PPA

Legend: (5Fh) → designates memory location 5Fh. Text without brackets refers to the register name.

Memory Resources

The memory of the DS28E05 consists of user memory, administrative data, and a ROM ID. Table 1 shows the size, access mode and purpose of the various memory areas. Brackets around an access mode indicate possible restrictions, such as write protection or read protection.

The memory is organized as 8 pages of 16 bytes each (Figure 5). Each page consists of 8 segments. Table 2 shows how the segments relate to a memory address. Pages 0 to 6 are the user memory. Page 7 contains the administrative data and the ROM ID. The function memory locations 0074h to 0075h depends on the code in the Factory Word (addresses 0076h to 0077h). The Manufacturer ID can be a customer-supplied identification code that assists the application software in identifying the product the DS28E05 is associated with. Contact the factory to set up and register a custom manufacturer ID.

Write protection or EPROM emulation mode is activated through the Write Memory command by writing to the corresponding locations (PPA to PPD) in the administrative data page. Once a protection is activated, it cannot

ADDRESS RANGE	TYPE	DESCRIPTION	PROTECTION CODES
0000h to 000Fh	R/(W)	User memory page 0	—
0010h to 001Fh	R/(W)	User memory page 1	—
0020h to 002Fh	R/(W)	User memory page 2	—
0030h to 003Fh	R/(W)	User memory page 3	—
0040h to 004Fh	R/(W)	User memory page 4	—
0050h to 005Fh	R/(W)	User memory page 5	—
0060h to 006Fh	R/(W)	User memory page 6	—
0070h*	R/(W)	Page protection PPA, lower nibble: page 0; upper nibble: page 1	0h: open (factory default); Ah: EPROM mode; all other codes: write protected
0071h*	R/(W)	Page protection PPB, lower nibble: page 2, upper nibble: page 3	0h: open (factory default); Ah: EPROM mode; all other codes: write protected
0072h*	R/(W)	Page protection PPC, lower nibble: page 4, upper nibble: page 5	0h: open (factory default); Ah: EPROM mode; all other codes: write protected
0073h*	R/(W)	Page protection PPD, lower nibble: page 6, upper nibble: copy lock	0h: open (factory default); Ah: EPROM mode; all other codes: write protected Copy lock 0h: open (factory default); all other codes: Page protection locations PPA,PPB,PPC,PPD write protected. Prevents changes to the page modes.
0074h to 0075h	R/(W)	Manufacturer ID/User bytes	—
0076h to 0077h	R	Factory Word. Set at factory.	C3A9h: addresses 0074h to 0075h are user bytes. 3C56h: addresses 0074h to 0075h are write protected and hold a Manufacturer ID.
0078h to 007Fh	R	ROM ID, alternate readout (family code at address 0078h)	—

*ONCE A NIBBLE IS PROGRAMMED TO ANYTHING OTHER THAN 0h, THE NIBBLE CANNOT BE CHANGED.

Figure 5. User Memory Map

be reversed. Once the page protections are finalized, the copy lock nibble (73h, upper) should be set to prevent changes. The protection settings are read-accessible through the Read Memory command. See the *Memory Function Commands* section for command flow details.

The ROM ID uniquely identifies each individual DS28E05 and serves as network address in a multidrop 1-Wire network. The ROM ID can be read through the ROM Function commands; it is also read-accessible as part of the 8th memory page. The family code is stored at the lower address (78h).

Memory Function Commands

The memory function flowchart (Figure 6) describes the protocols to access the memory of the DS28E05. The memory is written in segments of 2 bytes.

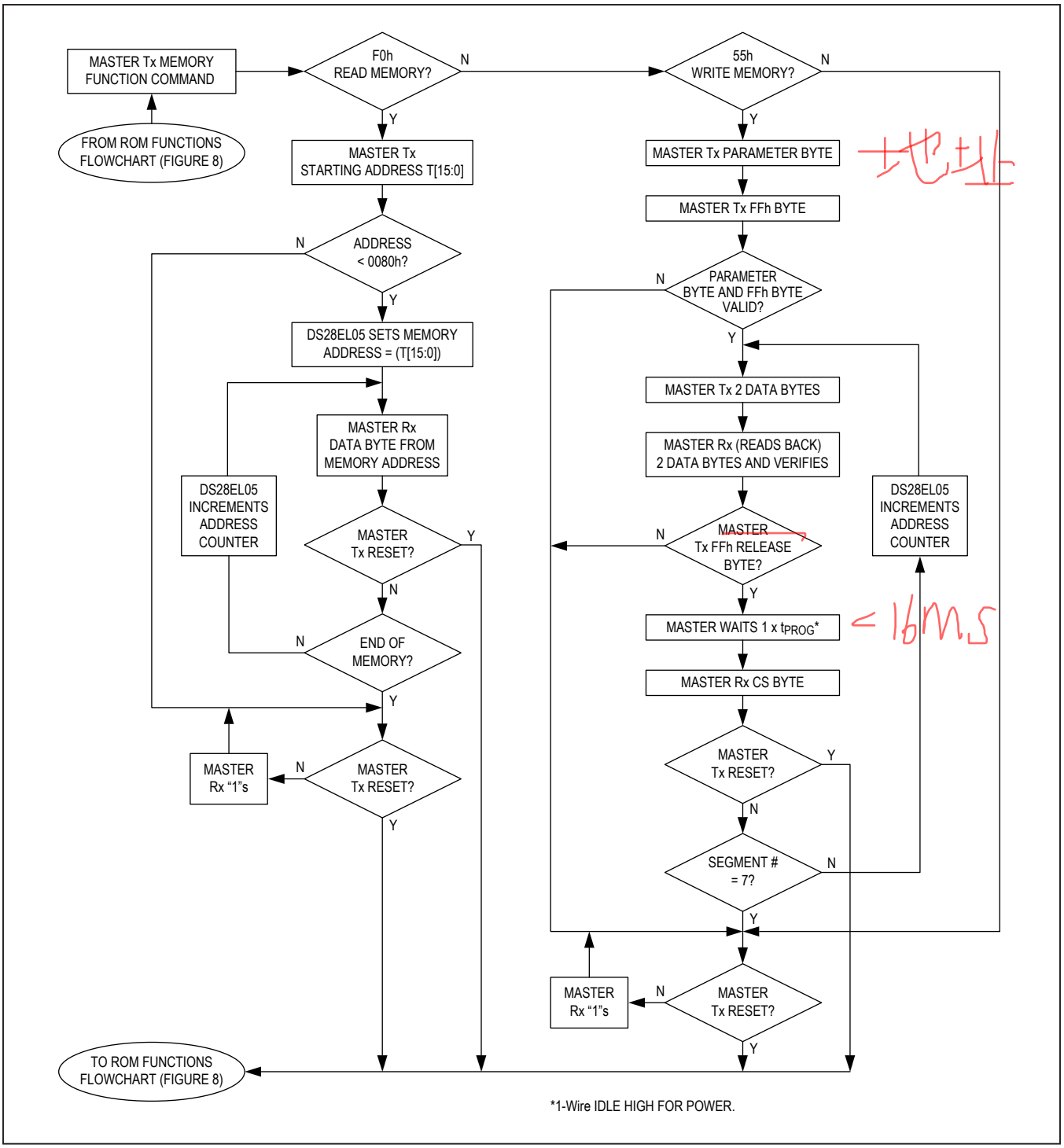

Figure 6. Memory Functions Flowchart

Write Memory [55h]

The Write Memory command is used to program one or more contiguous 2-byte segments of a memory page. This command is applicable only to memory locations that are not write protected. The parameter byte specifies the page and segment number where the writing begins. The new segment data is transmitted in the sequence B0, B1. Table 2 shows the how these bytes map to the addressed memory page. The command flow allows writing one or multiple adjacent segments within a page. To safeguard against transmission errors, the DS28E05 supports read-after-write verification. In case of data error, the master aborts the command by issuing a 1-Wire reset. To start the transfer to EEPROM the master must transmit a release byte (FFh). After the programming time is over, the DS28E05 transmits a CS byte. If a page is in EPROM emulation mode, the new segment data is the bitwise AND of the segment data in memory and the new data provided with the command.

Write Memory	
Command Code	55h
Parameter Byte	Target page selection, starting segment number (Table 3).
Restrictions	The memory page must not be write protected.
Protocol Variations	Writing within a page. Writing through the end of the page.
Error conditions	Invalid parameter byte. The memory page is write protected.
CS Byte	AAh = success. 33h = ~~The command failed because the page is write protect~~ed.

Table 3. Parameter Byte Bitmap

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	PAGE #			SEG #			0

Note: *The bits marked as 0 must be transmitted as 0 for the parameter byte to be valid.*

Bits 6:4: Memory Page Selection (PAGE #). These bits specify the memory page that is to be written to. Valid memory page numbers are 000b (page 0) to 111b (page 7).

Bits 3:1: Starting Segment Selection (SEG #). These bits specify the location within the selected memory page where the writing begins. For pages 0 to 6 valid segment numbers are 000b (start of memory page) to 111b (last segment of memory page). Valid segment numbers for page 7 are 000b, 001b, and 010b.

Read Memory [F0h]

The Read Memory command is used to read the memory. The command needs a 16-bit starting address TA1, TA2. The parameter byte specifies the lower address byte (TA1, T[6:0]) where the reading begins. After the parameter byte, the master transmits TA2 (T[15:8]), which must be 00 to be valid. The reading can start at any valid starting address and continue trough the end of the memory. If memory page 7 is read and the master continues reading, the resulting data is FFh. The master can end the Read Memory command at any time by issuing a reset pulse.

Read Memory	
Command Code	F0h
Parameter Byte	Starting memory address (Table 4).
Restrictions	None. This command can be issued at any time.
Protocol Variations	None.
Error conditions	Invalid parameter byte.
CS Byte	N/A

Table 4. Parameter Byte Bitmap

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	TA1						

Note: *The bit marked as 0 must be transmitted as 0 for the parameter byte to be valid.*

1-Wire Bus System

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances the DS28E05 is a slave device. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots, which are initiated on the falling edge of sync pulses from the bus master.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS28E05 is open drain with an internal circuit equivalent to that shown in Figure 7.

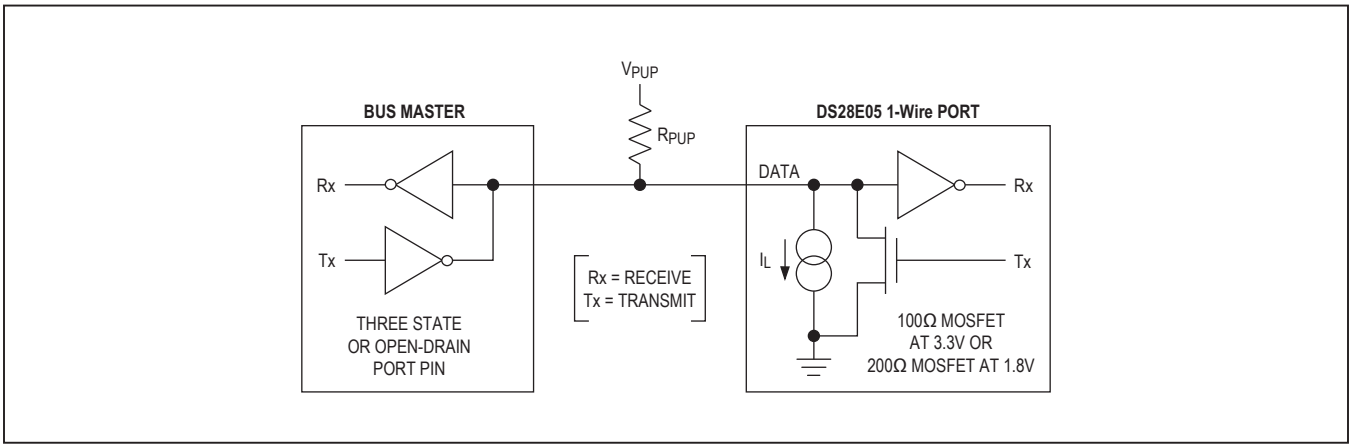

Figure 7. Hardware Configuration

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The DS28E05 supports overdrive speed of 76.9kbps (max) only and cannot be used together with standard speed or dual-speed 1-Wire slaves on the bus. The value of the pullup resistor primarily depends on the 1-Wire pullup voltage, network size and load conditions. The DS28E05 requires a pullup resistor of maximum 1.5kΩ for 3.3V operation or a pullup resistor of maximum 750Ω for 1.8V operation.

The idle state for the 1-Wire bus is high. If for any reason a transaction must be suspended, the bus must be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs, one or more devices on the bus could be reset.

Transaction Sequence

The protocol for accessing the DS28E05 through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction Data

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS28E05 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

1-Wire ROM Function Commands

Once the bus master has detected a presence, it can issue one of the five ROM function commands that the DS28E05 supports. All ROM function commands are 8 bits long. A list of these commands follows (see the flowchart in Figure 8).

Read ROM [33h]

The Read ROM command allows the bus master to read the DS28E05's ROM ID (8-bit family code, unique 48-bit serial number, and 8-bit CRC). This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The family code and 48-bit serial number as read by the master are unlikely to match the CRC.

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM ID, allows the bus master to address a specific DS28E05 on a multidrop bus. Only the DS28E05 that exactly matches the 64-bit ROM ID responds to the following memory function command. All other slaves wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their ROM ID numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the ID of all slave devices. For each bit of the ID number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its ID number bit. On the second slot, each slave device participating in the search outputs the complemented value of its ID number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the search tree. After one complete pass, the bus master knows the ROM ID number of a single device. Additional passes identify the ID numbers of the remaining devices. Refer to Application Note 187: *1-Wire Search Algorithm* for a detailed discussion, including an example.

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM ID. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

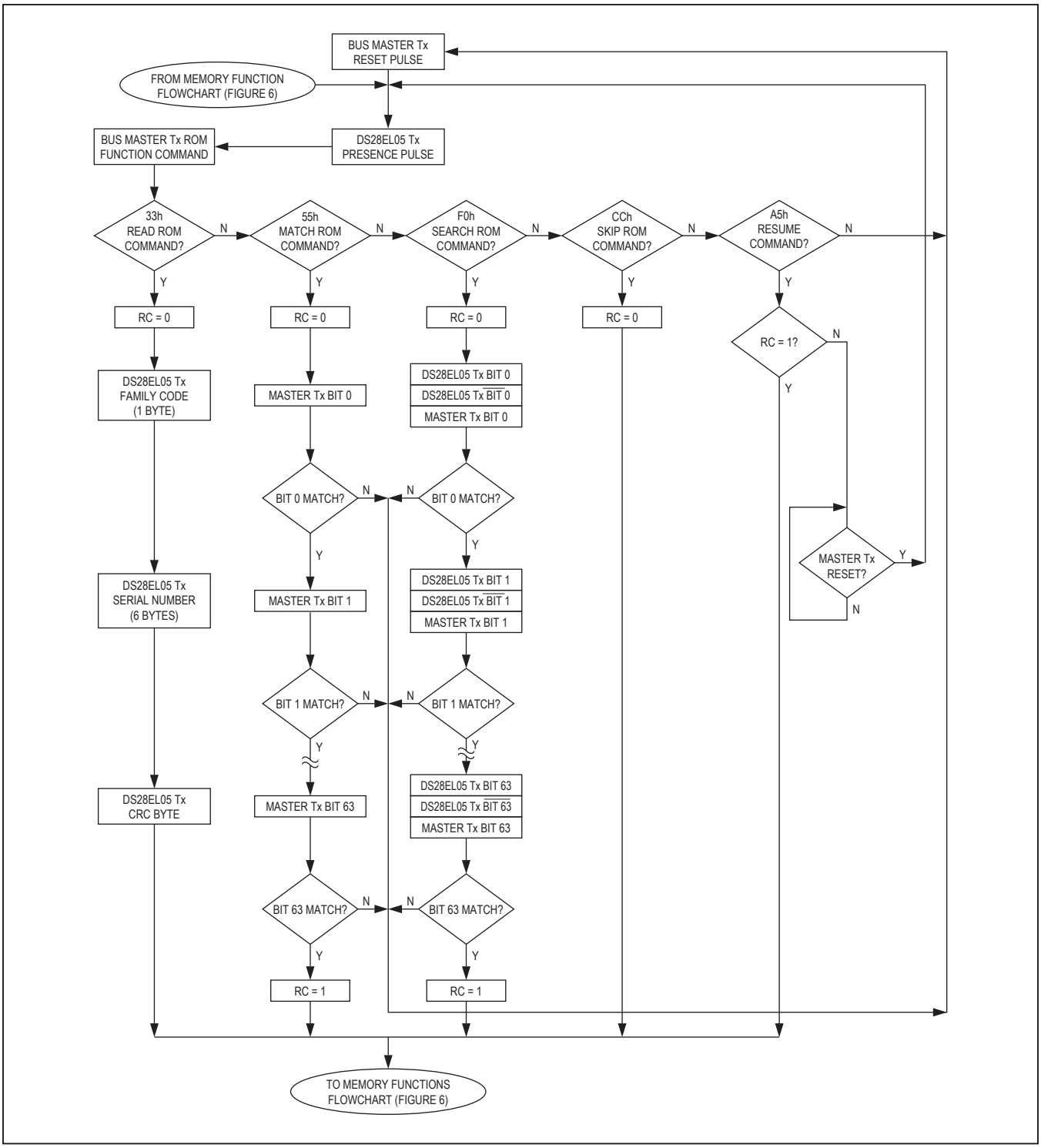

Figure 8. ROM Functions Flowchart

Resume Command [A5h]

To maximize the data throughput in a multidrop environment, the Resume command is available. This command checks the status of the RC bit and, if it is set, directly transfers control to the memory functions, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM or Search ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command.

1-Wire Signaling

The DS28E05 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus master initiates all falling edges. The DS28E05 communicates at overdrive speed only.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from $V_{IL(MAX)}$ past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 9 as ε, and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage $V_{IL(MAX)}$ is relevant for the DS28E05 when determining a logical level, not triggering any events.

Figure 9 shows the initialization sequence required to begin any communication with the DS28E05. A reset pulse followed by a presence pulse indicates that the DS28E05 is ready to receive data, given the correct ROM and memory function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge.

After the bus master has released the line it goes into receive mode. Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor. When the threshold V_{TH} is crossed, the DS28E05 waits and then transmits a presence pulse by pulling the line low. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

Read-/Write-Time Slots

Data communication with the DS28E05 takes place in time slots that carry a single bit each. Write time slots transport data from bus master to slave. Read time slots transfer data from slave to master. Figure 10 illustrates the definitions of the write- and read-time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS28E05 starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

Master-to-Slave

For a write-one time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time $t_{W1L(MAX)}$ is expired. For a write-zero time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time $t_{W0L(MIN)}$ is expired. For the most reliable communication, the voltage on the data line should not exceed $V_{IL(MAX)}$ during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS28E05 needs a recovery time t_{REC} before it is ready for the next time slot.

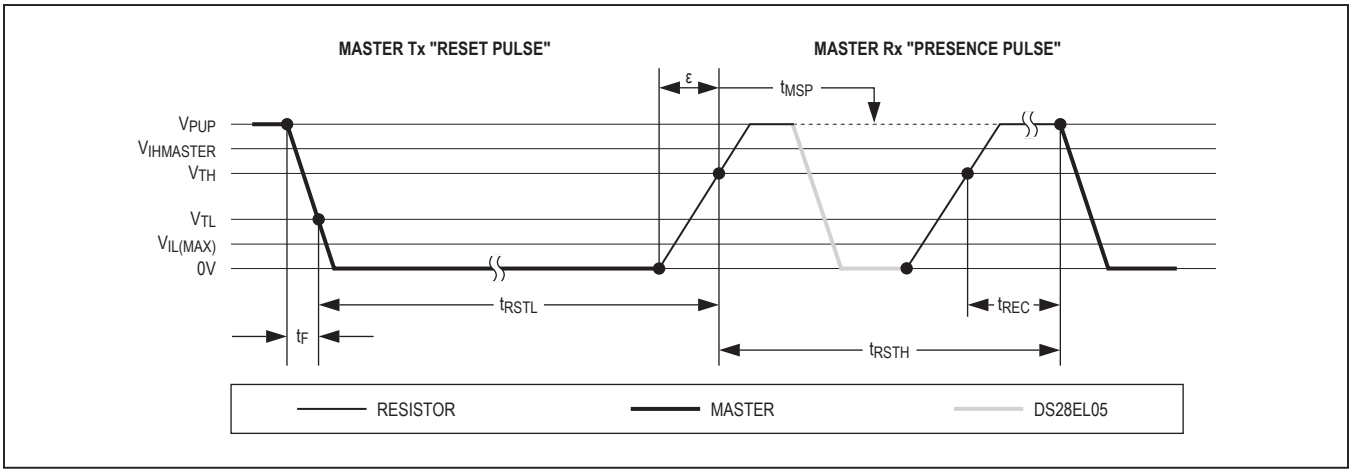

Figure 9. Initialization Procedure: Reset and Presence Pulse

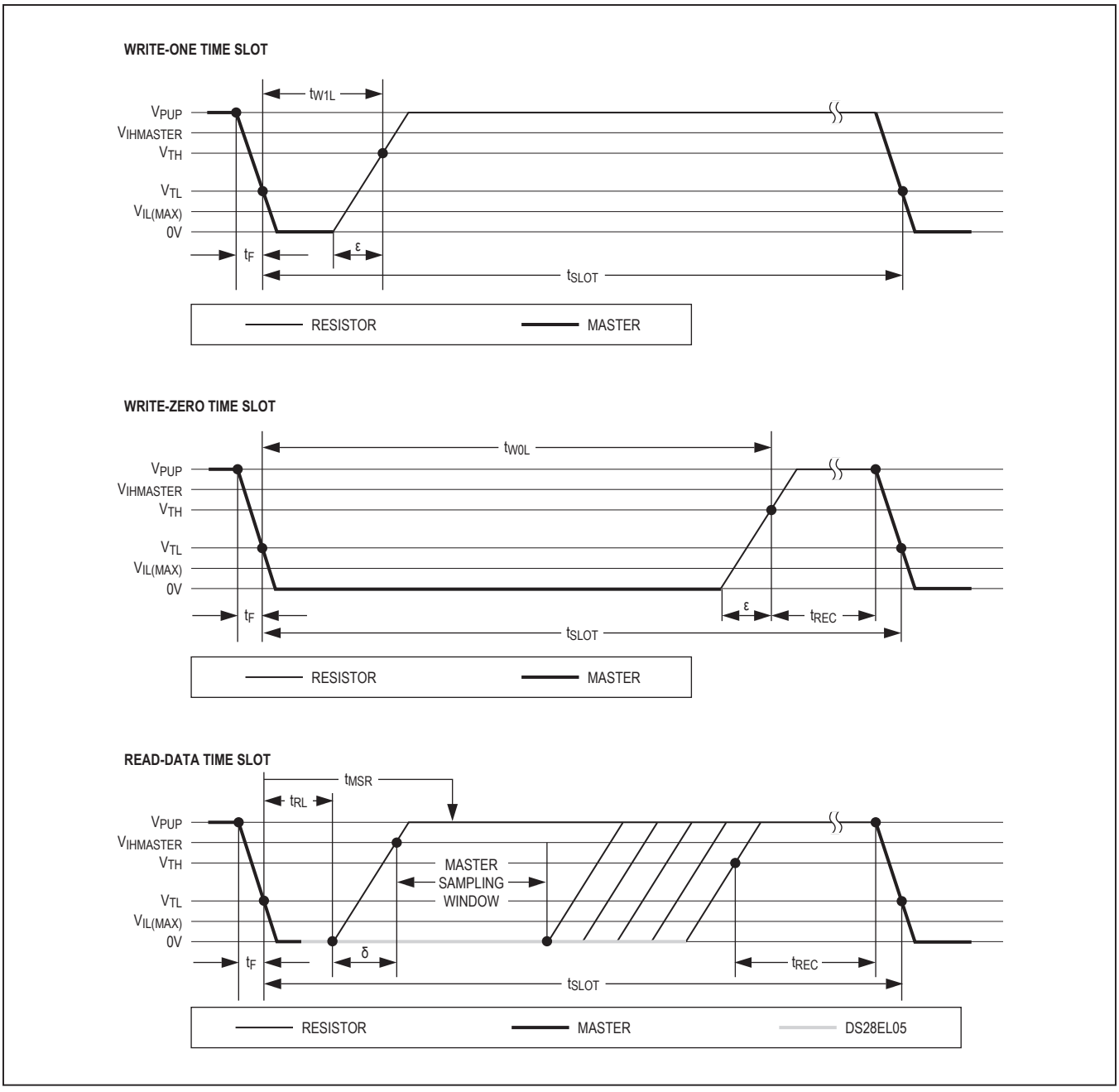

Figure 10. Read/Write Timing Diagrams

Slave-to-Master

A read-data time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS28E05 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS28E05 does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of t_{RL} + δ (rise time) on one side and the internal timing generator of the DS28E05 on the other side define the master sampling window ($t_{MSR(MIN)}$ to $t_{MSR(MAX)}$), in which the master must perform a read from the data line. For the most reliable communication, t_{RL} should be as short as permissible, and the master should read close to but no later than $t_{MSR(MAX)}$. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS28E05 to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS28E05 attached to a 1-Wire line. For multidevice configurations, t_{REC} must be extended to accommodate the additional 1-Wire device input capacitance.

Improved Network Behavior (Switchpoint Hysteresis)

In a 1-Wire environment, line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, consequently, result in a Search ROM command coming to a dead end or cause a device-specific function command to abort. The DS28E05 uses a 1-Wire front-end with built-in hysteresis at the low-to-high switching threshold V_{TH}. If a negative glitch crosses V_{TH} but does not go below V_{TL}, it is not recognized (Figure 11).

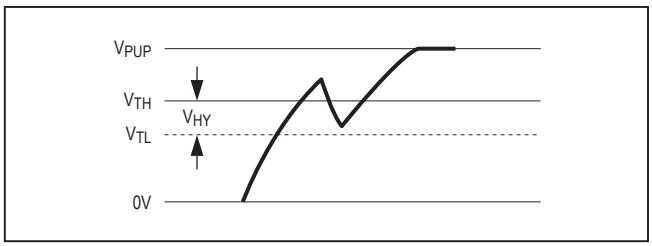

Figure 11. Noise Suppression Scheme

1-Wire Communication Examples

See Table 5 and Table 6 for the 1-Wire communication legend and data direction codes.

Table 5. 1-Wire Communication Legend

SYMBOL	DESCRIPTION
RST	1-Wire reset pulse generated by master
PD	1-Wire presence detect pulse generated by slave
Select	Command and data to satisfy the ROM function protocol
PB	Parameter byte
CS	Command Success indicator
Release	FFh byte sent by the master to start a write activity in the slave
WM	Command “Write Memory”
RM	Command “Read Memory”
<n bytes>	Transfer of n bytes
<data to EOP>	Transfer of as many bytes as are needed to reach the end of the page
Data	Transfer of 2 bytes segment data
FF loop	Indefinite loop where the bus master reads FFh bytes

Table 6. Data Direction Codes

Master-to-Slave	Slave-to-Master	Master waits (1-Wire idle high)

1-Wire Communication Examples (continued)

Write Memory

Writing within a page, not reaching the end of the page.

RST	PD	Select	WM	PB	FFh	Data	Data	Release	Wait t_{PROG}	CS = AAh	RST

Repeat

Writing through the end of the page.

RST	PD	Select	WM	PB	FFh	Data	Data	Release	Wait t_{PROG}	CS = AAh	FF Loop

Repeat

Writing fails with protection error

RST	PD	Select	WM	PB	FFh	Data	Data	Release	Wait t_{PROG}	CS = 33h	RST

Invalid parameter byte

RST	PD	Select	WM	PB = 7Eh	FFh	FF Loop

Read Memory

Starting at address 33h, reading 6 bytes

RST	PD	Select	RM	PB = 33h	00h	<6 bytes>	RST

Starting at the manufacturer ID, reading beyond the end of memory

RST	PD	Select	RM	PB = 76h	00h	<10 bytes>	FF Loop

Invalid parameter byte

RST	PD	Select	RM	PB = 80h	00h	FF Loop

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS28E05X+T	-40ºC to +85ºC	4 UCSP (2.5k pcs)
DS28E05R+T	-40ºC to +85ºC	3 SOT23 (3k pcs)
DS28E05P+T	-40ºC to +85ºC	6 TSOC (4k pcs)
DS28E05P+	-40ºC to +85ºC	6 TSOC
DS28E05GB+T	-40ºC to +85ºC	2 SFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
4 UCSP	Z40B0+1	**21-100035**	Refer to **Application Note 1891**
3 SOT23	U3+2	**21-0051**	**90-0179**
6 TSOC	D6+1	**21-0382**	**90-0321**
2 SFN	S23A5N+1	**21-0661**	Refer to **Application Note 4132**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/12	Initial release	—
1	1/14	Expanded V_{PUP} (min) to 2.75V and V_{IL} (max) to 0.5V	1, 2
2	1/17	Added SFN package, updated *Features*, *Electrical Characteristics* table, *Pin Configurations*, *Pin Descriptions*, *Ordering Information*, and *Package Information*	1–16

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