
HH EU194

Design and Implementation of Vectorized Pseudorandom Number Generators

Master's Thesis Defense and Presentation

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Outline

Introduction

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What do we need random numbers for?

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- Physical Simulations, based on Monte-Carlo Methods

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- create a software library and design a good API
- apply library to physical problems
- compare performance to other implementations

Pseudorandom Number Generators

True Randomness

What is a random sequence?

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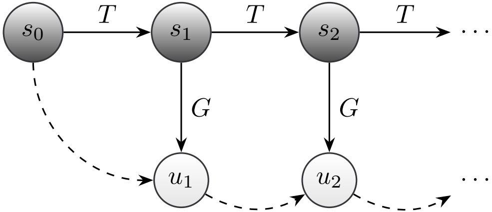
Disadvantages:

- Unreproducibility
- Speed Limitations

Pseudorandom Number Generator Definition



S . . . Set of States

T . . . Transition Function

U . . . Set of Possible Outputs

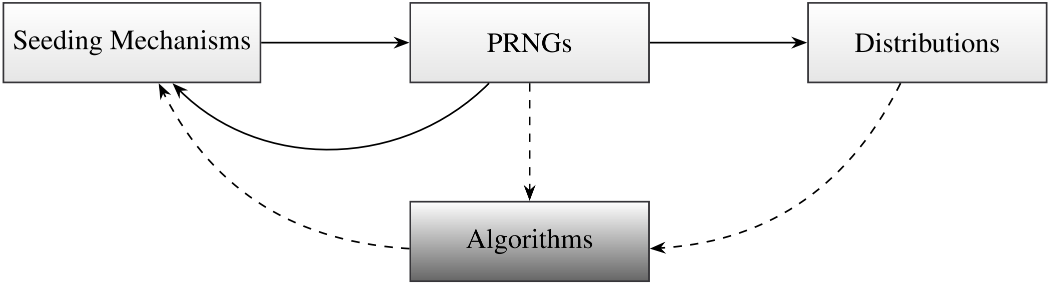
G . . . Generator Function

$$\mathcal{G} := (S, T, U, G), \qquad T\colon S \to S, \qquad G\colon S \to U$$

$$s_0 \in S, \qquad s_{n+1} := T(s_n), \qquad u_n := G(s_n)$$

Design of the Library

Design Components



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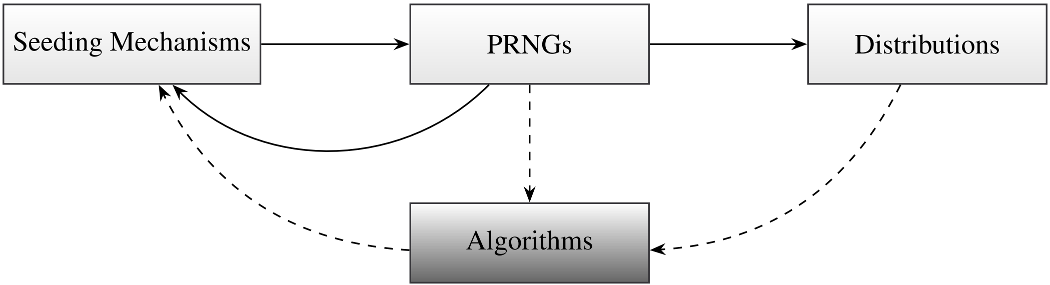

- pXart: header-only library written in C++

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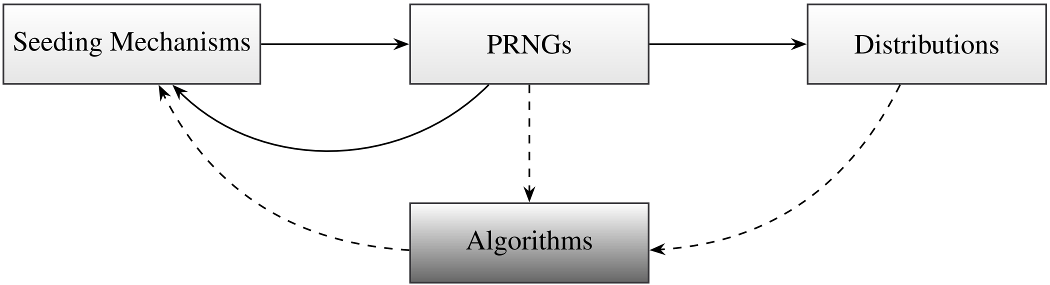

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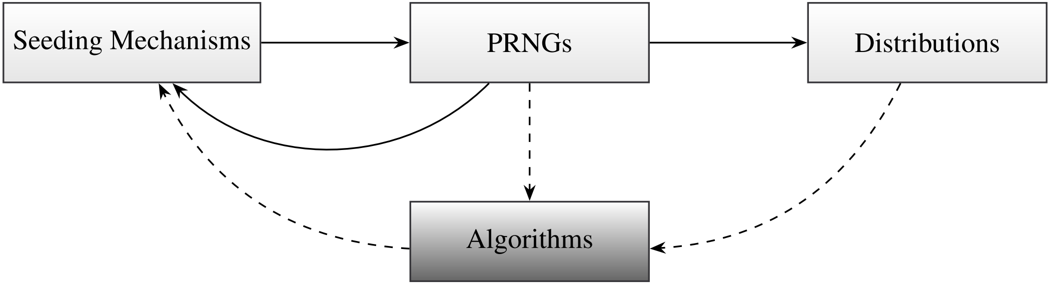

- pXart: header-only library written in C++
- support for CMake and build2
- providing online documentation

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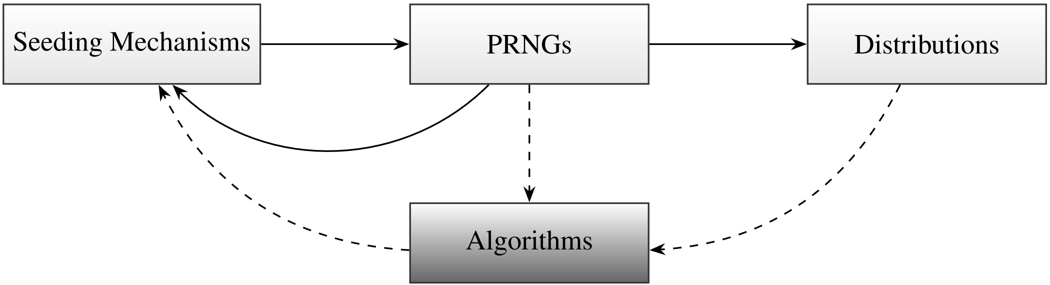

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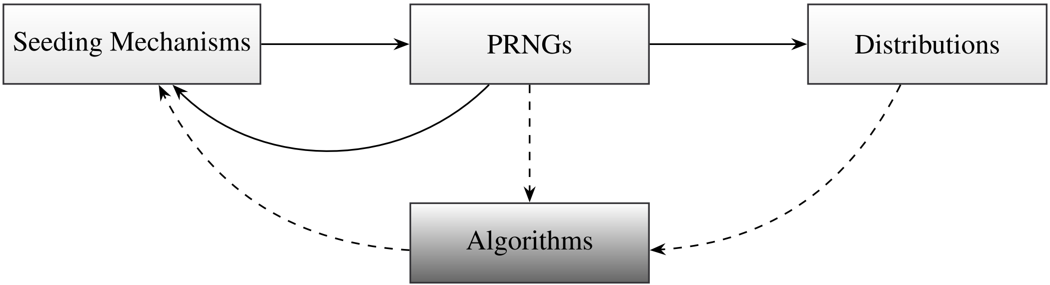

- PRNGs: MT19937, Xoroshiro128+, MSWS

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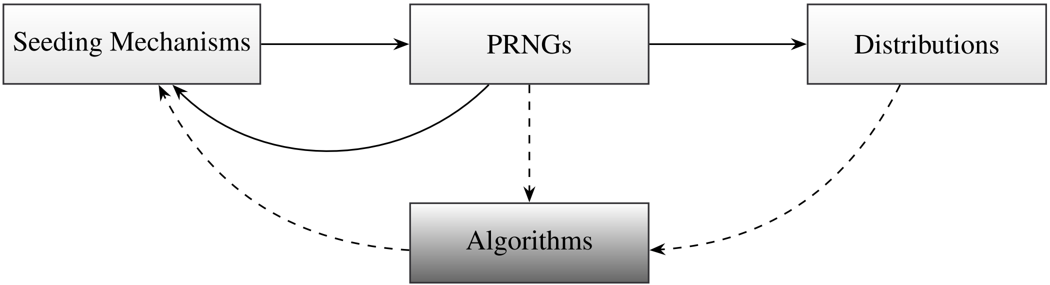

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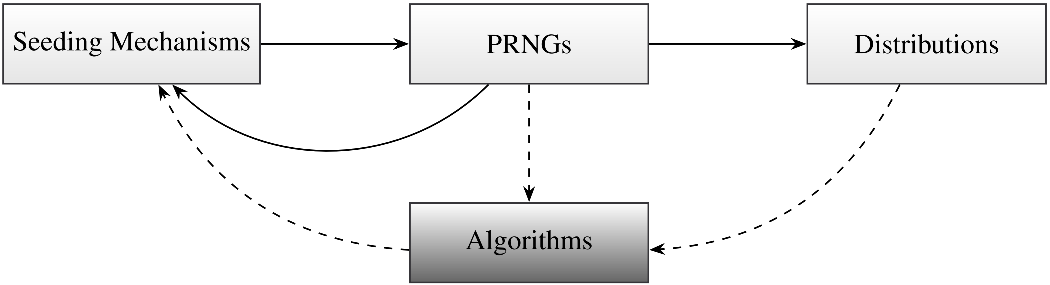

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- real and integer uniform distributions
- different seeding facilities

Vectorization and SIMD Architectures

SIMD Architecture

x_7	x_6	x_5	x_4	x_3	x_2	x_1	x_0

$$+$$

y_7	y_6	y_5	y_4	y_3	y_2	y_1	y_0

$$=$$

$x_7 + y_7$	$x_6 + y_6$	$x_5 + y_5$	$x_4 + y_4$	$x_3 + y_3$	$x_2 + y_2$	$x_1 + y_1$	$x_0 + y_0$

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- Single Instruction Multiple Data
- processor contains vector registers multiple elements

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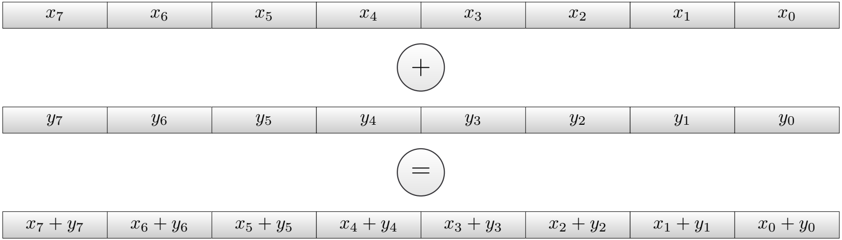

- Single Instruction Multiple Data
- processor contains vector registers multiple elements
- processor operates on all values simultaneously

SIMD Implementations

Actual Hardware:

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- SSE, AVX and AVX512 instruction sets by Intel

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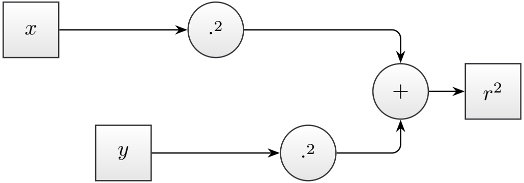
Why should we vectorize PRNGs manually?

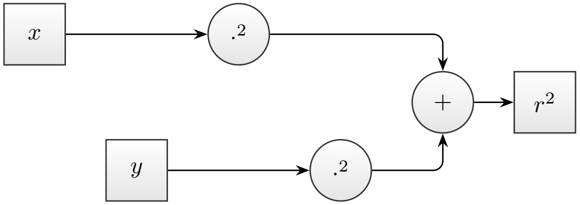
- performance and speed
- use full functionality of today's processors
- no automatic vectorization possible
- external vectorized code needs random numbers

SIMD Example



$$x, y \in \mathbb{R}, \qquad r^2 = x^2 + y^2$$

SIMD Example



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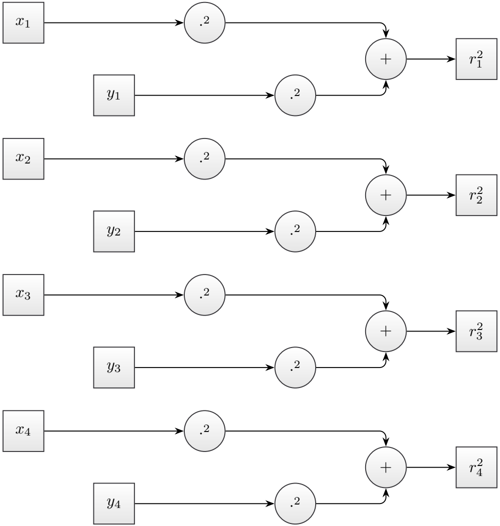

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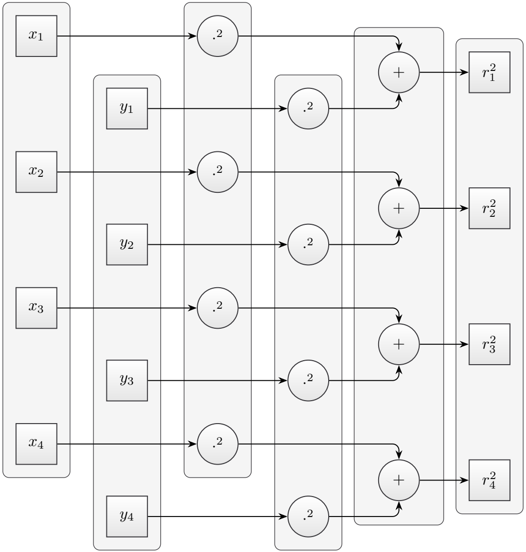
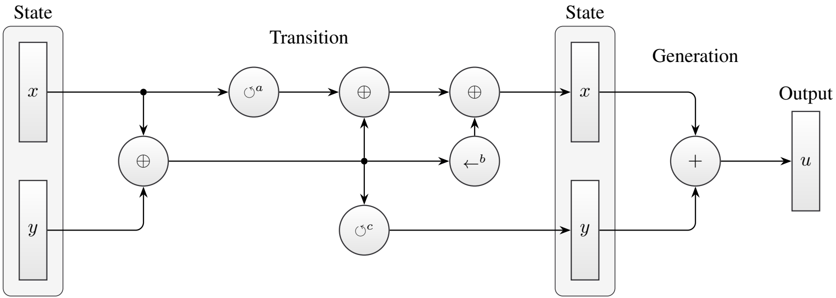


Xoroshiro128+

Xoroshiro128+ Scheme



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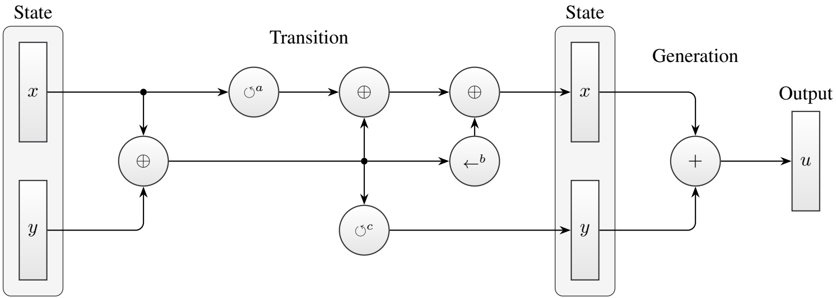

- scrambled linear PRNG

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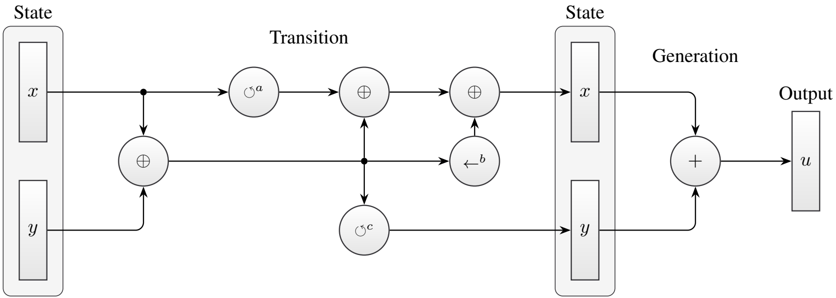

- scrambled linear PRNG
- 128-bit state, 64-bit output

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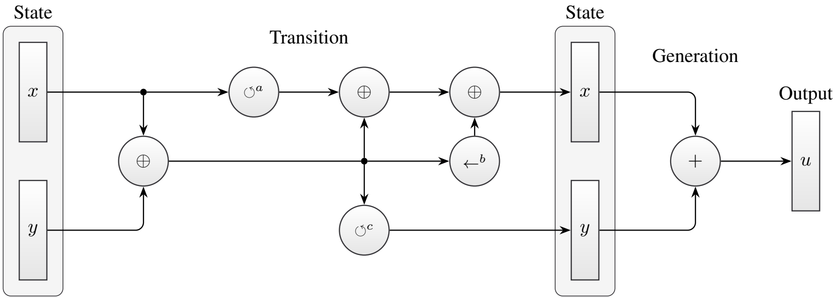

- scrambled linear PRNG
- 128-bit state, 64-bit output
- period: $2^{128} - 1$

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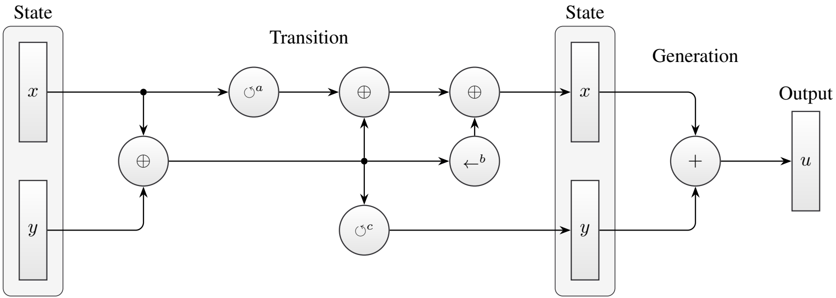

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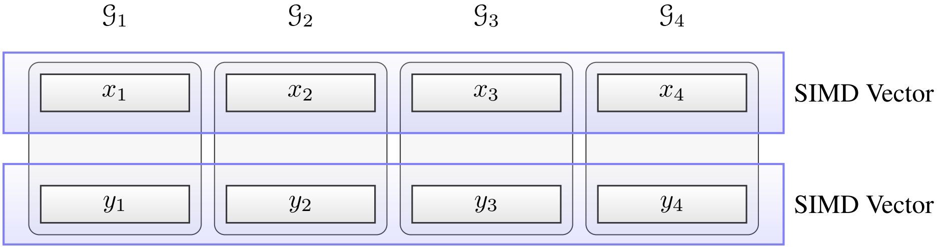
- period: $2^{128} - 1$
- jump operations

Xoroshiro128+ SIMD Scheme



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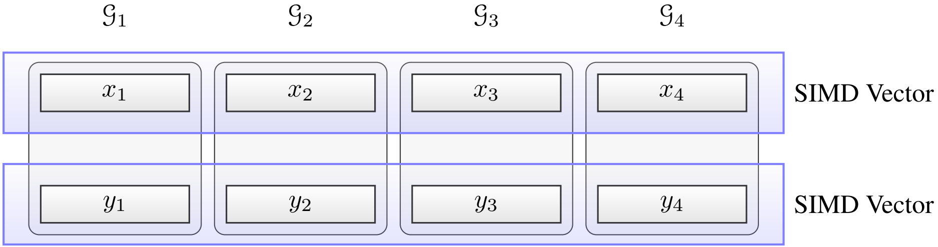

- several parallelization techniques for multiple streams

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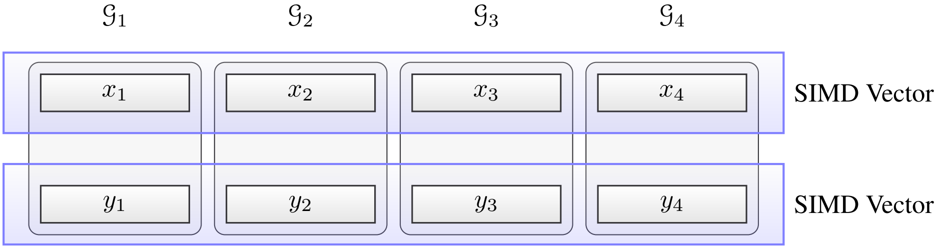

- several parallelization techniques for multiple streams
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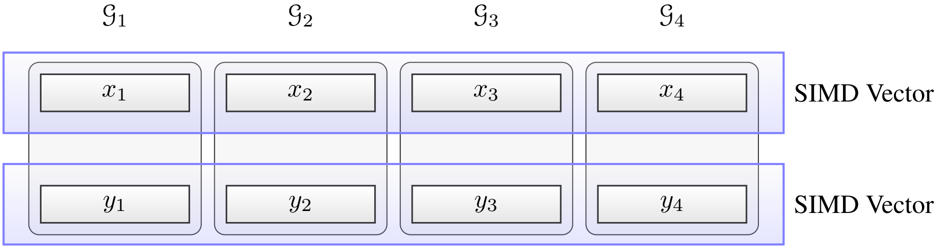
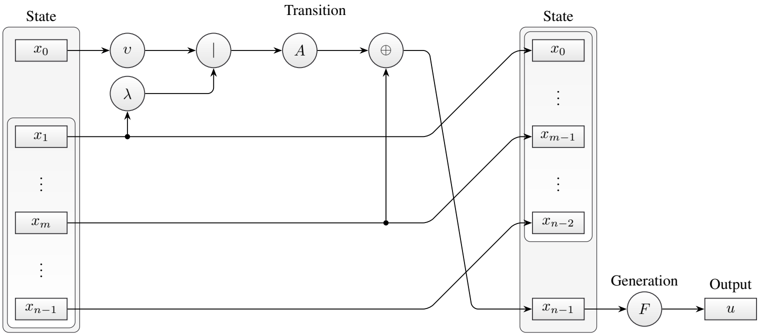


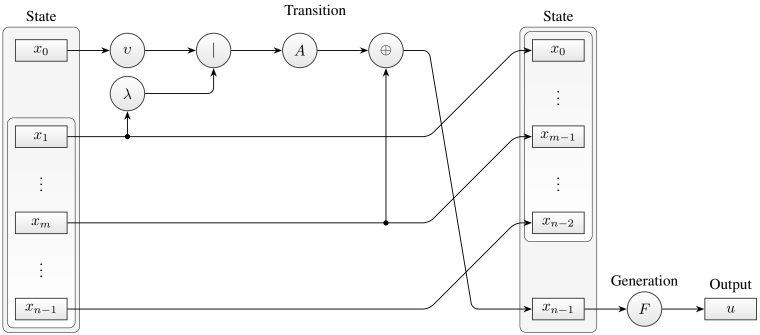
- several parallelization techniques for multiple streams
- here: multiple instances of the same generator
- seeding and parameter variations for multiple streams

Mersenne Twister MT19937

MT19937

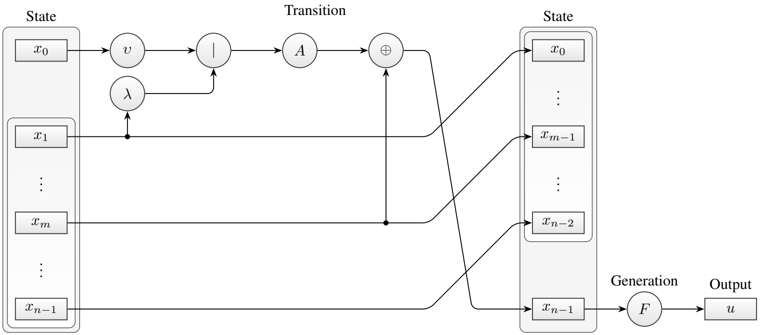

State
Transition
State
Generation
Output
x_0
x_1
x_m
x_{n-1}
υ
λ
$|$
A
$\oplus$
x_0
x_{m-1}
x_{n-2}
x_{n-1}
F
u

MT19937



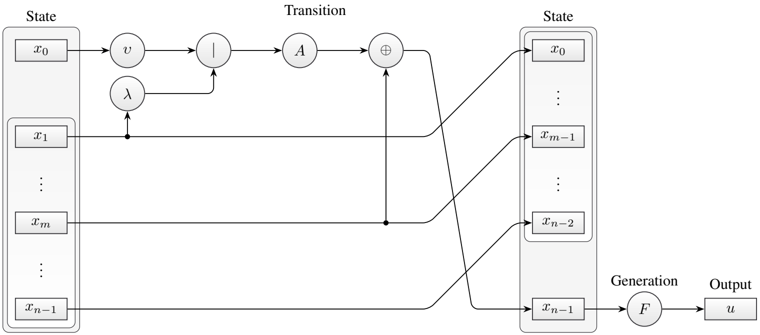
- de-facto standard

MT19937



- de-facto standard
- linear PRNG

MT19937



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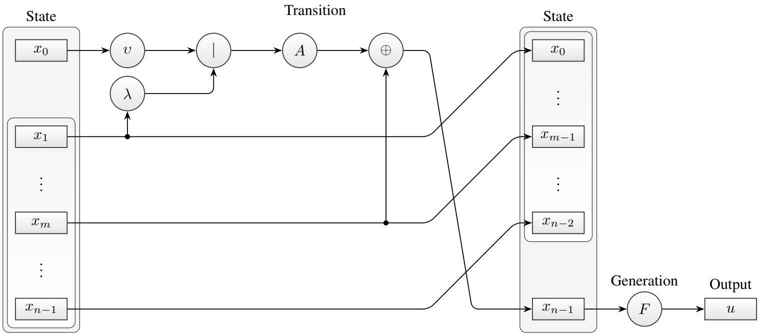
MT19937



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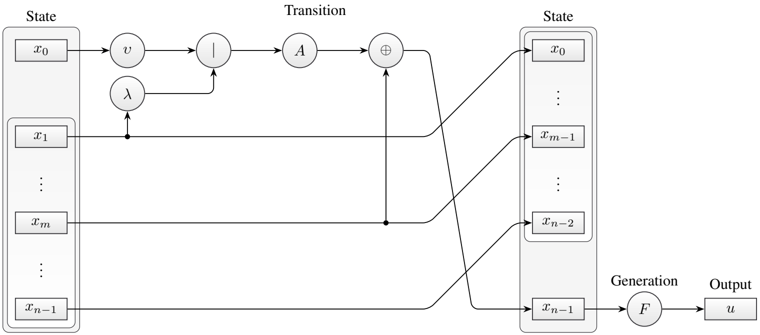
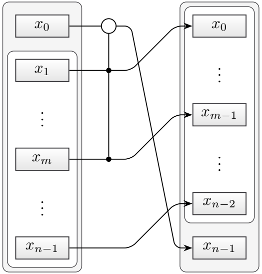
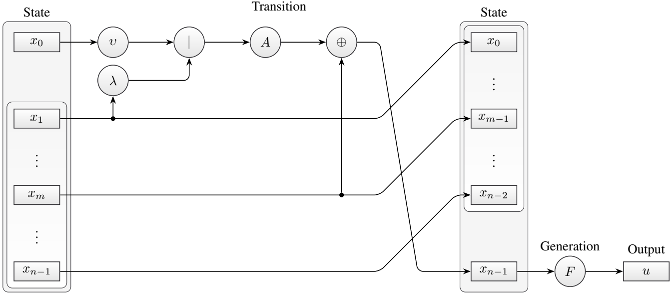


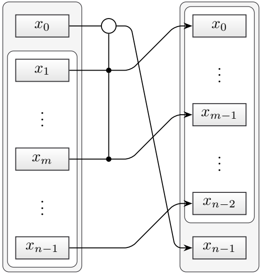
- de-facto standard
- linear PRNG
- 19937-bit state, 32-bit output
- period: $2^{19937} - 1$
- 623-dimensional equidistributed

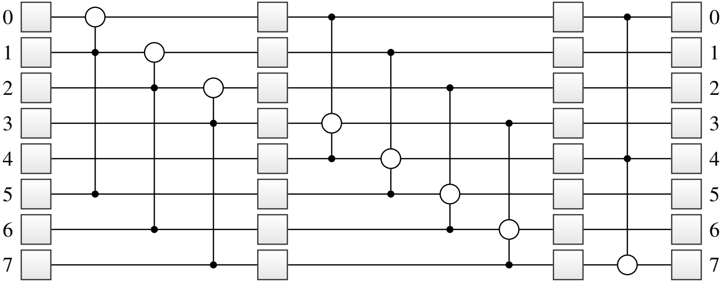
MT19937 Abbreviation





MT19937 Scalar Loop Scheme





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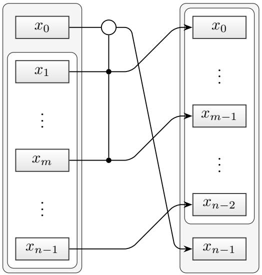

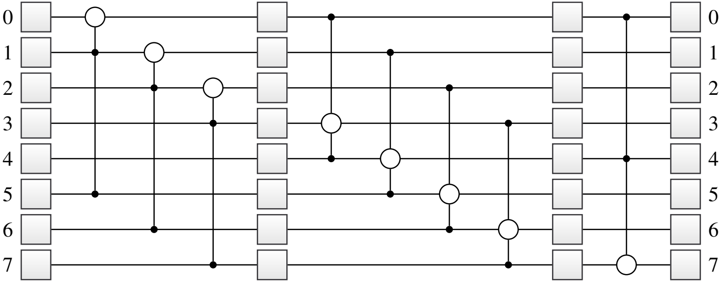

- moving all elements with one transition is inefficient

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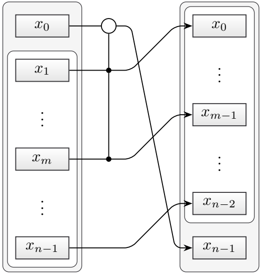

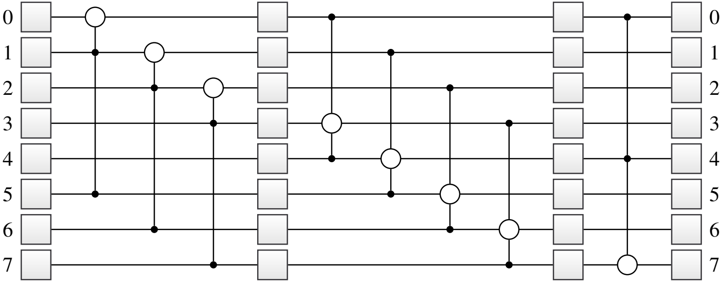

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- instead do n transitions at once

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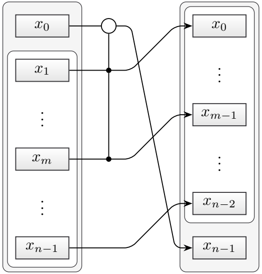

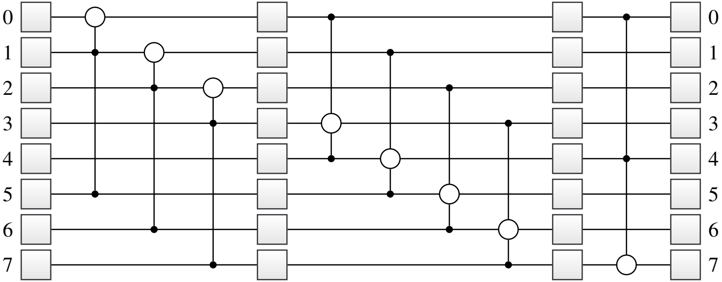

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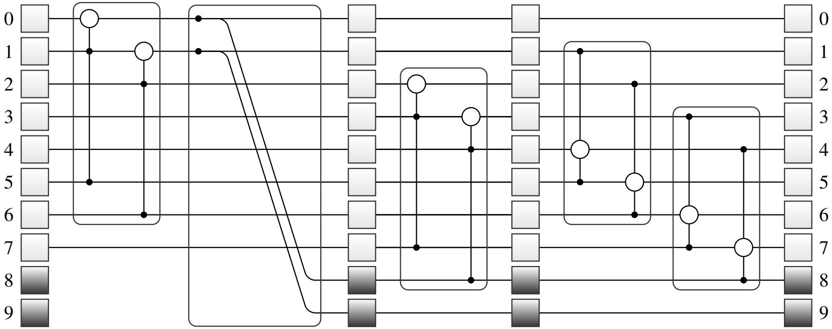
- instead do n transitions at once
- example with $n = 8$ and $m = 5$; reality with $n = 624$ and $m = 397$

MT19937 SIMD Loop Scheme



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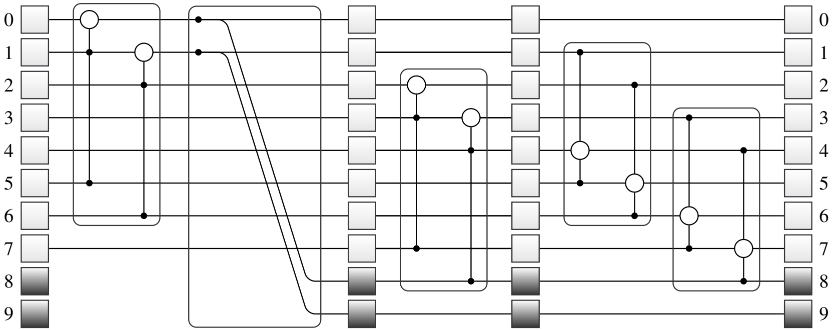

- example: two-element-vector; reality: up to eight-element-vector

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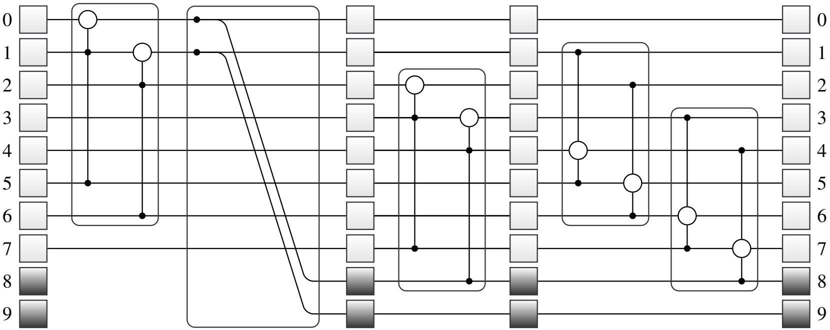

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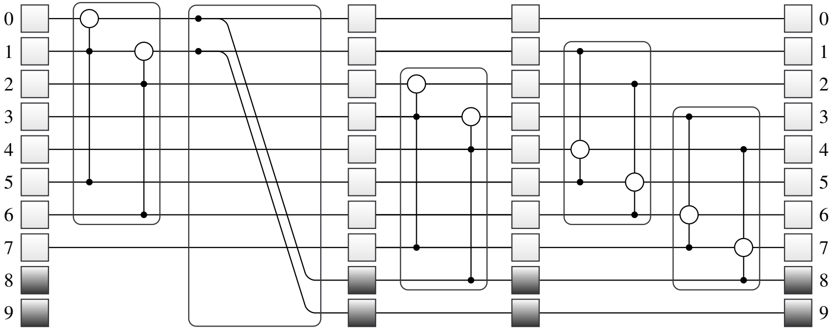
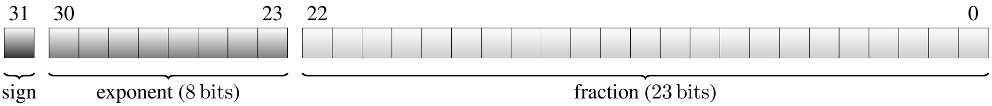


- example: two-element-vector; reality: up to eight-element-vector
- add vector-register-sized buffer at the end
- copy generated head to the end and do the vectorized loop

Uniform Distribution Functions

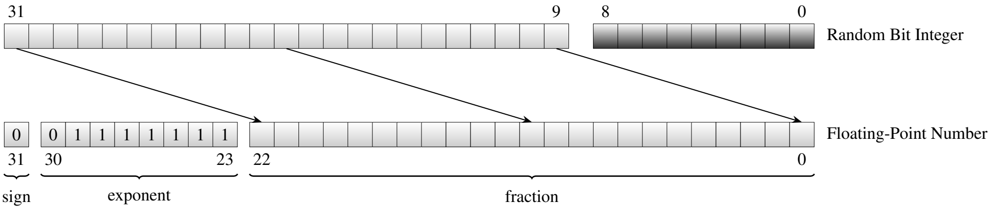
Real Uniform Distribution: Floating-Point Encoding



$$x = (-1)^s \cdot m \cdot 2^{e-o}$$

- IEEE 754
- we use only normalized numbers

Real Uniform Distribution



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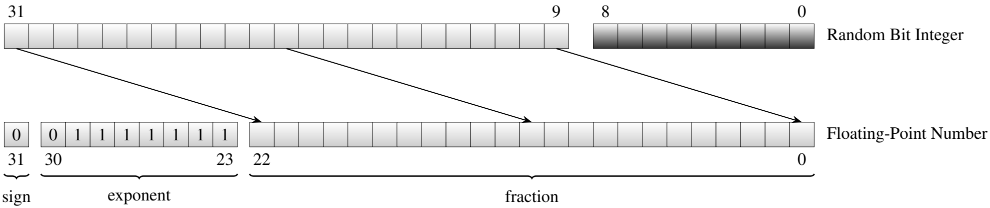
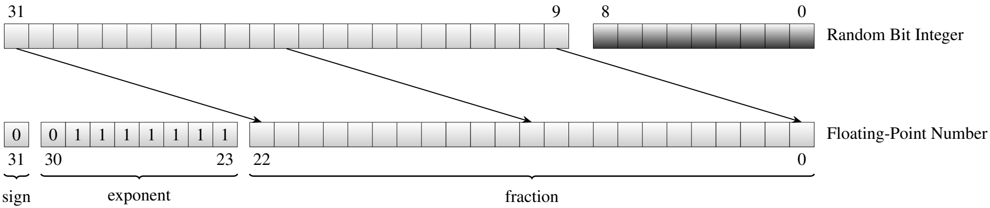


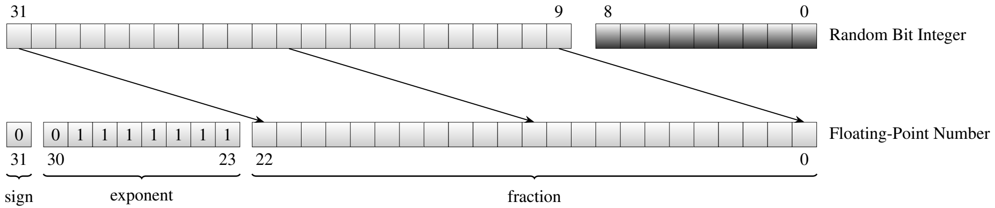
- get random integer

Real Uniform Distribution



- get random integer
- shift bits with highest entropy into fraction part

Real Uniform Distribution



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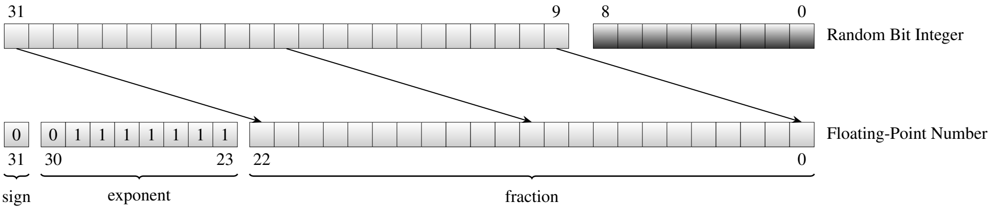

- get random integer
- shift bits with highest entropy into fraction part
- set sign and exponent to put floating-point value in range $[1, 2)$
- subtract one from result

Integer Uniform Distribution

Integer Uniform Distribution

- unbiased uniform integer algorithms should not be vectorized

Integer Uniform Distribution

- unbiased uniform integer algorithms should not be vectorized
- use simple multiplication-based approximation

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- use 64-bit multiplication for 32-bit integers
- bias can be neglected for typical simulations

Evaluation and Results

Tests and Performance

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- Consistency and Correctness: Unit Tests, API Tests, Examples

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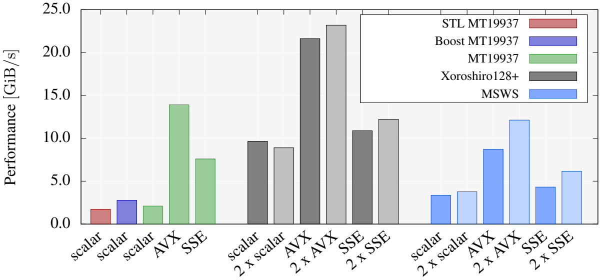
- Performance: Filling a Cache, Monte Carlo π



Comparison to Intel MKL VSL and RNGAVXLIB

Table: MT19937 Monte Carlo π Benchmark for 10^8 Samples

RNGAVXLIB	Intel MKL VSL	Cached AVX	Pure AVX
$0.38\,\mathrm{s}$	$0.10\,\mathrm{s}$	$0.09\,\mathrm{s}$	$0.08\,\mathrm{s}$

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- scalar interface of RNGAVXLIB reduces performance
- Intel MKL VSL always fills vector of data
- benchmarks are biased

Comparison to Intel MKL VSL and RNGAVXLIB

	pXart	RNGAVXLIB	Intel MKL VSL
Portable	✔	✘	✘
Good API	✔	✘	✘
Open Source	✔	✔	✘
Documentation	✔	✘	✔
Alternative Distributions	✘	✔	✔
AVX512 Support	✘	✘	✔
Header-Only	✔	✘	✘
Build System Support	✔	✘	✘

Conclusions and Future Work

Conclusions

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- photon simulation and path tracing

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- vectorized PRNGs speedup code even with caches

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- photon simulation and path tracing
- vectorized PRNGs speedup code even with caches
- MT19937 or Xoroshiro128+?

Future Work

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- seeding mechanisms for thread support

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Future Work

- alternative distributions
- seeding mechanisms for thread support
- AVX512 support
- latency optimizations
- application to real-world problems

Thank you for Your Attention!

References

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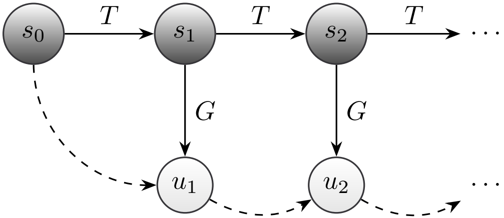
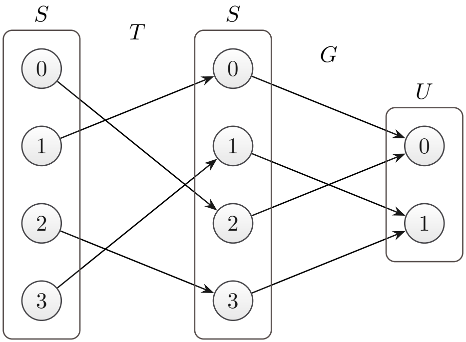
Appendix: Pseudorandom Number Generator Concept



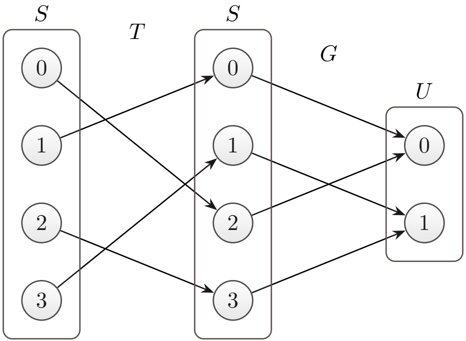
$$s_0 \sim \mathcal{U}_S, \qquad u_1 \leftarrow \mathcal{G}(), \qquad u_2 \leftarrow \mathcal{G}(), \qquad u_3 \leftarrow \mathcal{G}(), \qquad \ldots$$

Appendix: Pseudorandom Number Generator Example



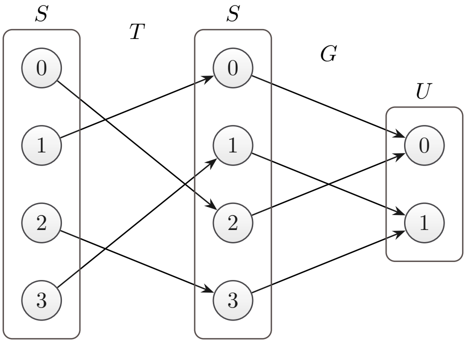
$$s_0 := 0, \qquad (s_n) = \overline{2310}, \qquad (u_n) = \overline{0110}$$

Appendix: Pseudorandom Number Generator Example



- construction of “good” PRNG is difficult

Appendix: Pseudorandom Number Generator Example

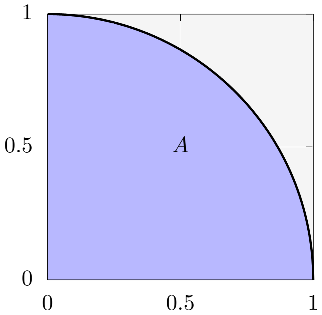


- construction of "good" PRNG is difficult
- pseudorandom number sequences will be periodic

Appendix: pXart Usage in C++

```
#include <pxart/pxart.hpp>
//
std::random_device rd{};
//
pxart::mt19937 rng1{};
pxart::mt19937 rng1{rd};
pxart::mt19937 rng1{pxart::mt19937::default_seeder{rd()}};
//
pxart::xrsr128p rng2{rng1};
//
const auto x = pxart::uniform<float>(rng1);
//
const auto y = pxart::uniform(rng2, -1.0f, 1.0f);
```

Appendix: Computation of π



$$A = \frac{\pi}{4}, \qquad \hat{\pi} = \frac{4N_A}{N}$$

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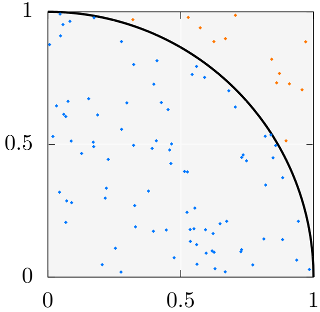
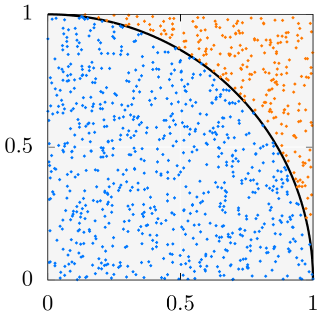


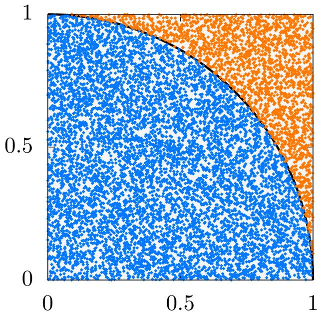
$$A = \frac{\pi}{4}, \qquad \hat{\pi} = \frac{4N_A}{N} = \frac{4 \cdot 87}{100} = 3.48$$

Appendix: Computation of π



$$A = \frac{\pi}{4}, \qquad \hat{\pi} = \frac{4N_A}{N} = \frac{4 \cdot 765}{1000} = 3.06$$

Appendix: Computation of π



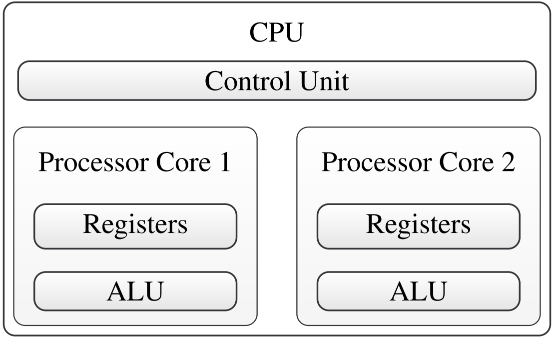
$$A = \frac{\pi}{4}, \qquad \hat{\pi} = \frac{4N_A}{N} = \frac{4 \cdot 7856}{10000} = 3.1424$$

Appendix: Example Usage

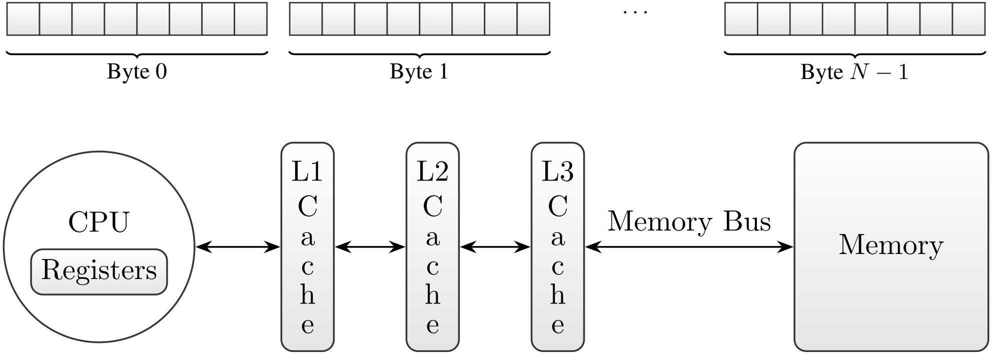
```cpp
// ...
#include <pxart/pxart.hpp>
// ...
pxart::mt19937 rng{};
const int samples = 100000000;
int pi = 0;
for (auto i = samples; i > 0; --i) {
  const auto x = pxart::uniform<float>(rng);
  const auto y = pxart::uniform<float>(rng);
  pi += (x * x + y * y <= 1);
}
pi = 4.0f * pi / samples;

// ...
```

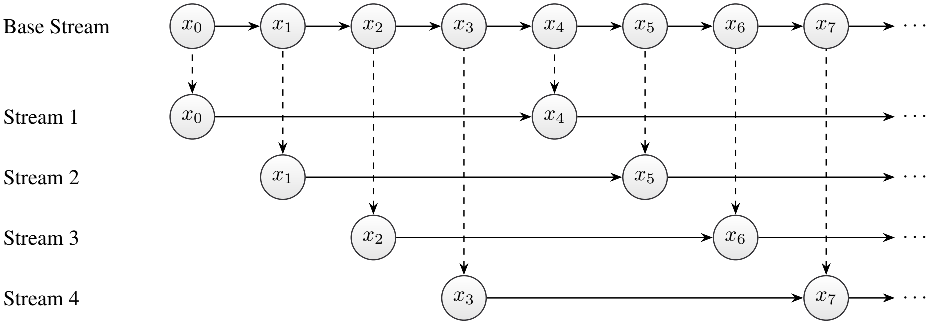
Appendix: Processor



Appendix: Memory Hierarchy

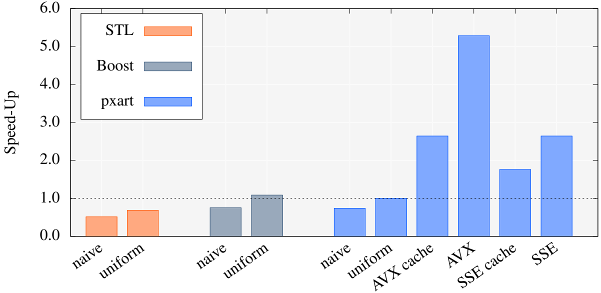


Appendix: MT19937 SIMD Leap Frogging



- vectorized generator will give same output as scalar one, only faster

Appendix: MT19937 Speed-Up Monte Carlo π



Appendix: Xoroshiro128+ Speed-Up Monte Carlo π