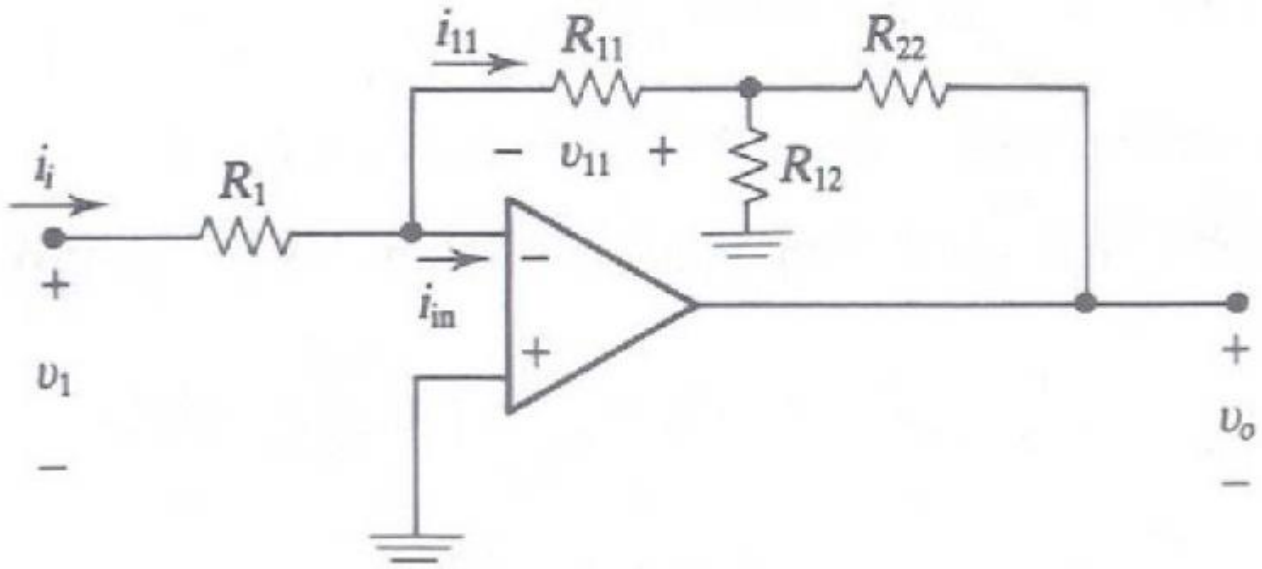
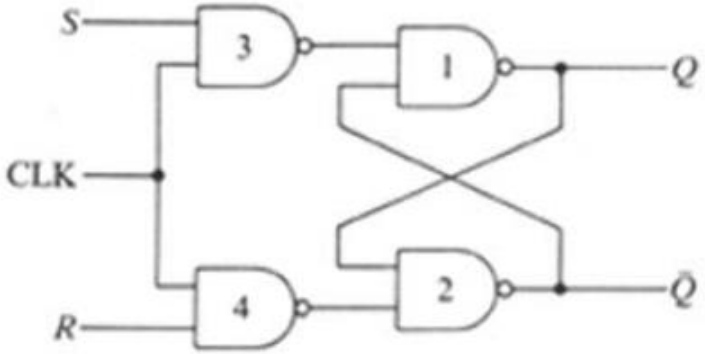
Problem (Time to solve - 10 min)

Find the gain of the circuits. Assume ideal op-amp.



Design an OpAmp circuit. Input voltage range 0.3V-1.0V output voltage 0.5 V to 4.5 V.

Clocked RS Flip-flop

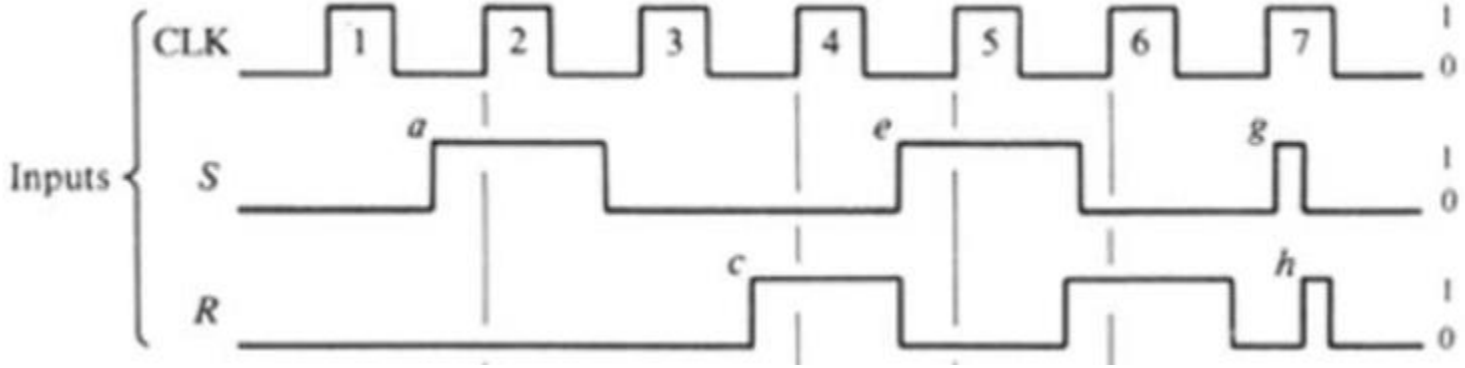


(a) Wired using NAND gates

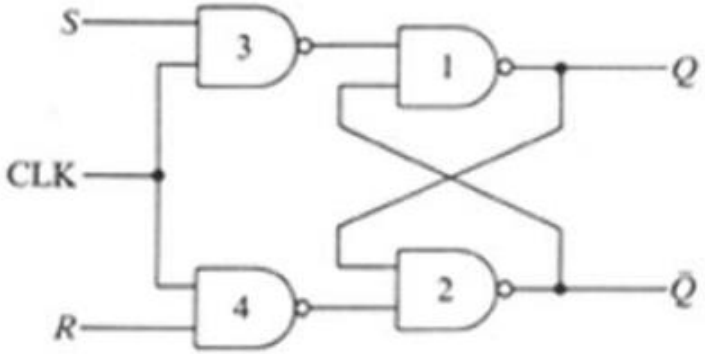
Mode of operation	Inputs			Outputs	
	CLK	S	R	Q	$\bar{Q}$
Hold	⎍	0	0	no change	
Reset	⎍	0	1	0	1
Set	⎍	1	0	1	0
Prohibited	⎍	1	1	1	1

⎍ = positive clock pulse

(b) Truth table



Clocked RS Flip-flop



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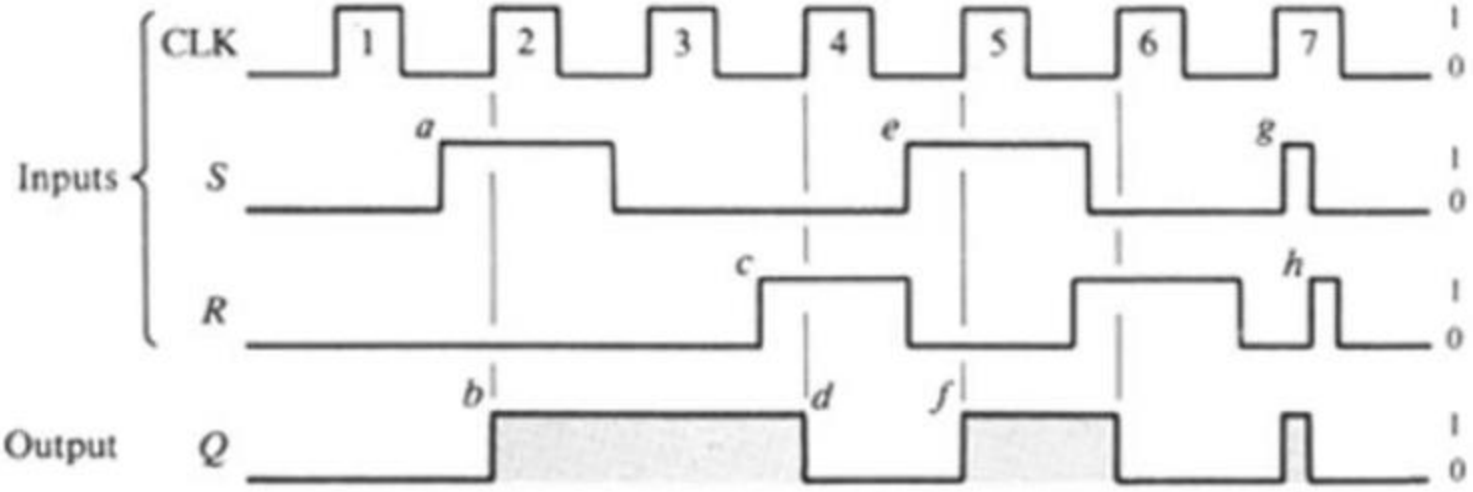
(b) Truth table



Clocked JK Flip-flop