

AE 242
Aerospace Measurements
Laboratory

Analog to Digital Conversion - ADC

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Analog voltage to Digital (integers)

Infinite to discrete

Digital to Analog Conversion - DAC

Digital (integers) to Analog voltage

Discrete to discrete

What is ADC?

Most of the sensors output is analog. Computers, micro-controller etc understands digital. ADC is a system which converts the analog voltage into equivalent digital number. Analog to digital converter (ADC) is an interface between analog world (voltages) and digital world (computer). The digital data can be stored, manipulated for further use. Less storage space compared to mechanical data storage devices - strip charts. High speed data acquisition possible.

These are available as 8-bit, 12-bit, 24-bit etc. also called as resolution. Data available at discrete steps.

8 bit - 255 (2^8-1)

12 bit - 4095 ($2^{12}-1$)

16 bit - 65535 ($2^{16}-1$)

Input range will be divided in above number of steps.

ADC

8 bit – 0 to 255 (2^8-1)

12 bit - 0 to 4095 ($2^{12}-1$)

16 bit - 0 to 65535 ($2^{16}-1$)

Input range will be divided in above number of steps.

Example: 8 bit ADC, 255 steps

Input voltage range 0-5 V.

ADC output 0 for 0 volt and ADC output 255 for 5 V

Input Voltage 2.5 V, ADC output will be 128 (Decimal)

1 increment = 0.0195 V

ADC

8 bit – 0 to 255 (2^8-1)

12 bit - 0 to 4095 ($2^{12}-1$)

16 bit - 0 to 65535 ($2^{16}-1$)

Input range will be divided in above number of steps.

Example: 8 bit ADC, 255 steps

Input voltage range 0-5 V.

ADC output 0 for 0 volt and ADC output 255 for 5 V

Input Voltage 2.5 V, ADC output will be 128 (Decimal)

1 bit = 0.0195 V

Input voltage range ± 5 V. ADC output 0 = -5 V

ADC output 255 = 5 V

Input voltage = 0V, ADC output will be 128 (Decimal)

1 increment = 0.039 V

Quantization error

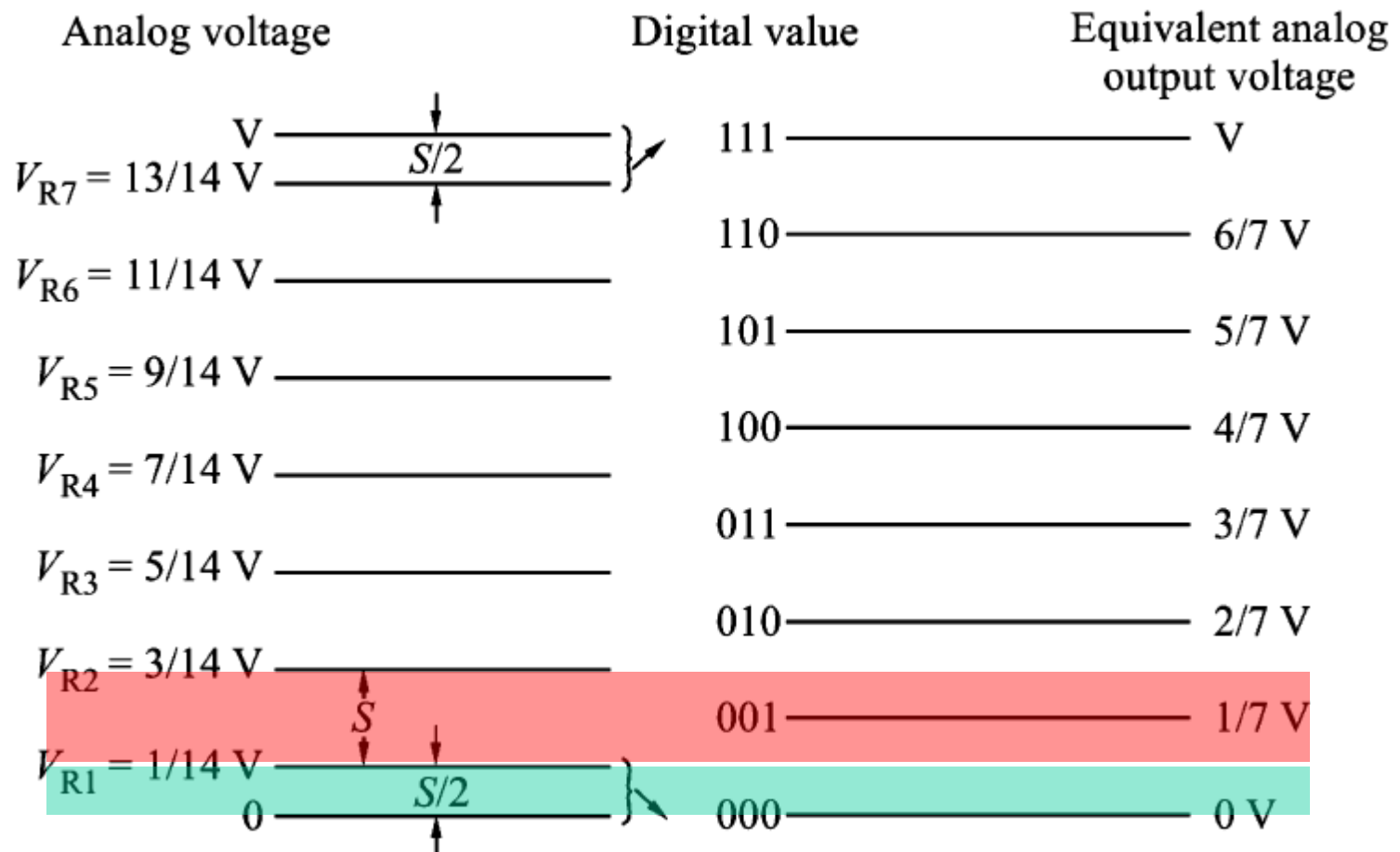
During ADC the difference between the input analog voltage and the obtained digital value is quantization error. This error is due to the discrete digital values. It can be maximum of $V/2^N$ Where V is the input range and N is number of bits in conversion. Input voltage infinite resolution, Output only discrete value

Analog voltage	Equivalent digital value
V	
$7/8 V$	111
$6/8 V$	110
$5/8 V$	101
$4/8 V$	100
$3/8 V$	011
$2/8 V$	010
$1/8 V$	001
0	000

Quantisation process

Quantization error

Quantisation error can be reduced by choosing the middle value. Error will be $S/2$, where S is voltage interval between two subsequent digital values.



Quantisation process

ADC Conversion steps

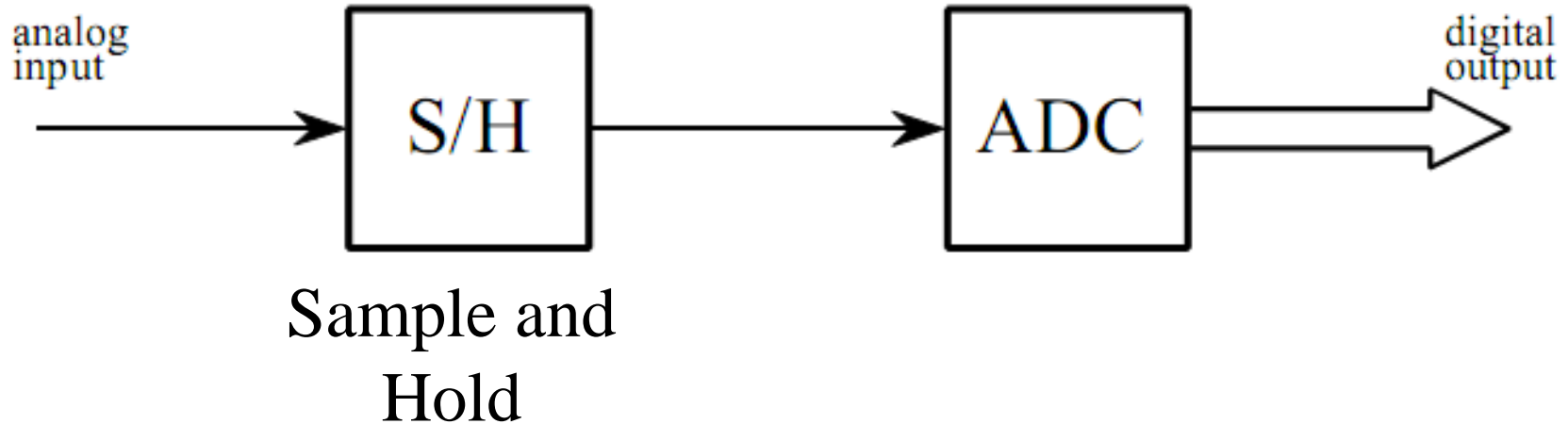
Following steps are involved in ADC:

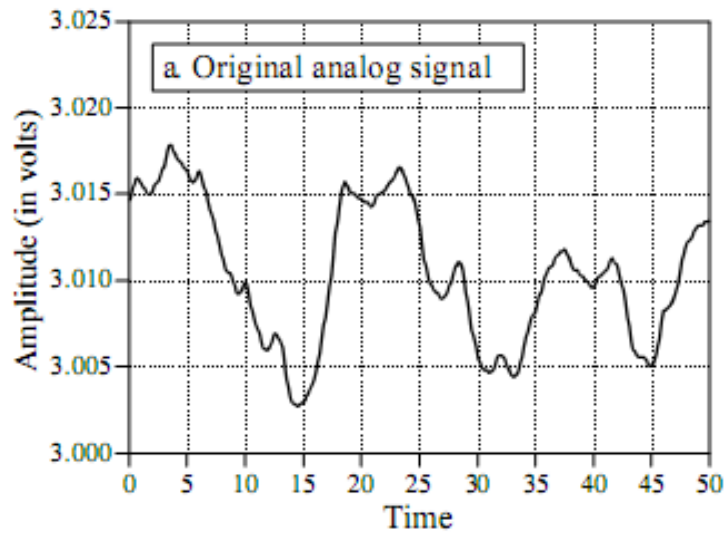
- 1) Sampling - Multiplexing
- 2) Holding - Hold the value till conversion is over
- 3) Quantizing - Converting the analog voltage to digital value
- 4) Encoding - Digital output may not be straight binary number

12 bit ADC: 0 – 4095

Input voltage 0 – 4.095

1 mV = 1 bit





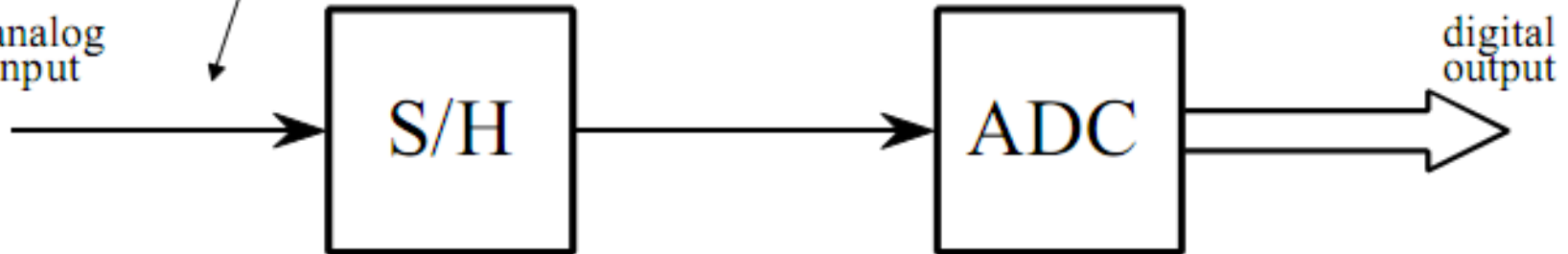
12 bit ADC: 0 – 4095

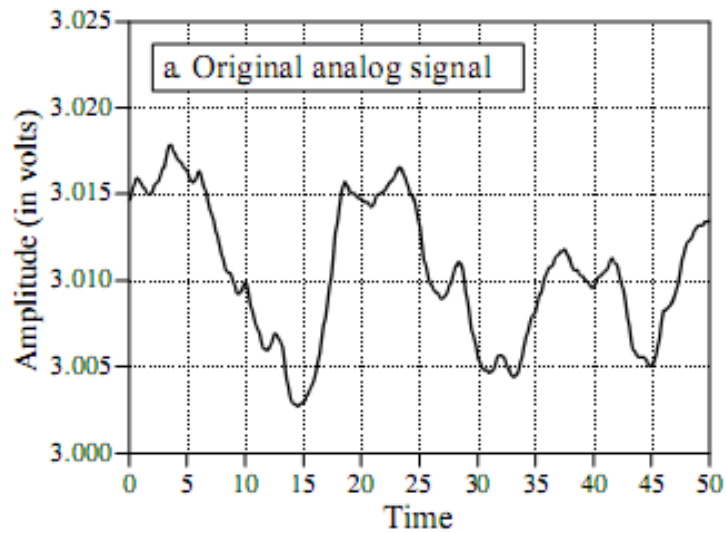
Input voltage 0 – 4.095

1 mV = 1 bit

Continuous

analog
input





12 bit ADC: 0 – 4095

Input voltage 0 – 4.095

1 mV = 1 bit

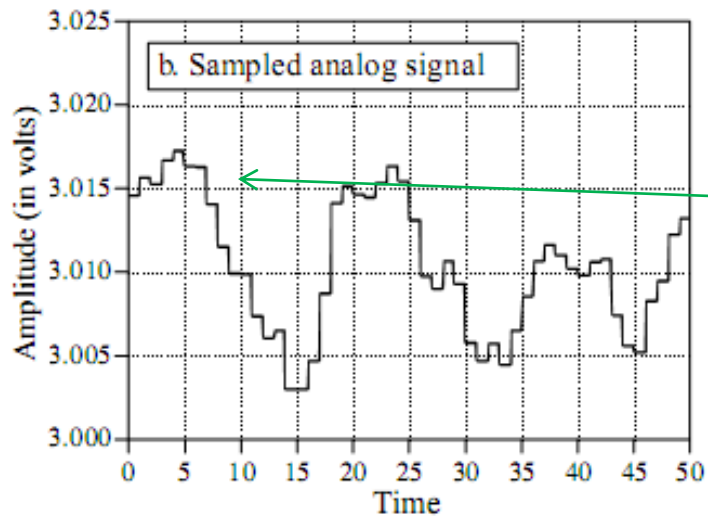
Continuous

analog
input

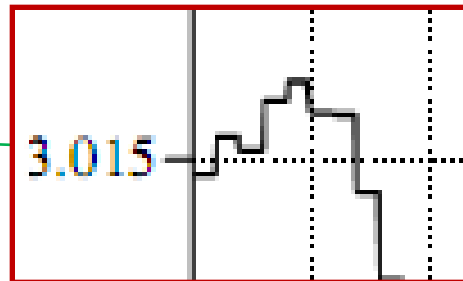
S/H

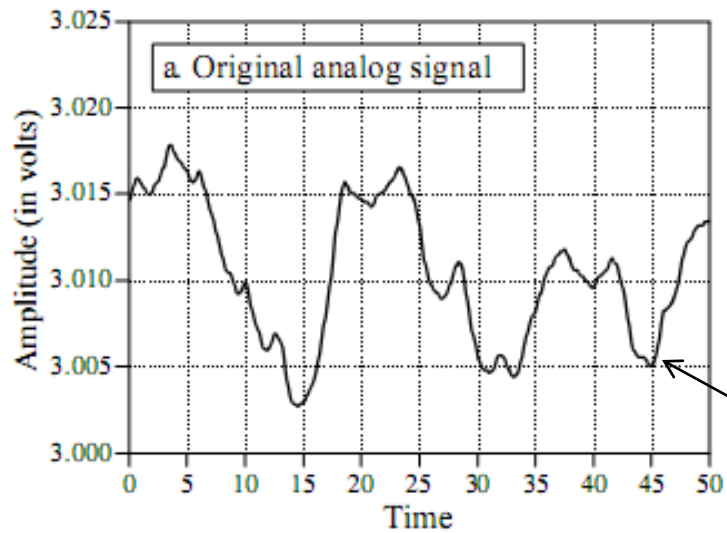
ADC

digital
output



Sampling





12 bit ADC: 0 – 4095

Input voltage 0 – 4.095

1 mV = 1 bit

Infinite to discrete

Continuous

analog input

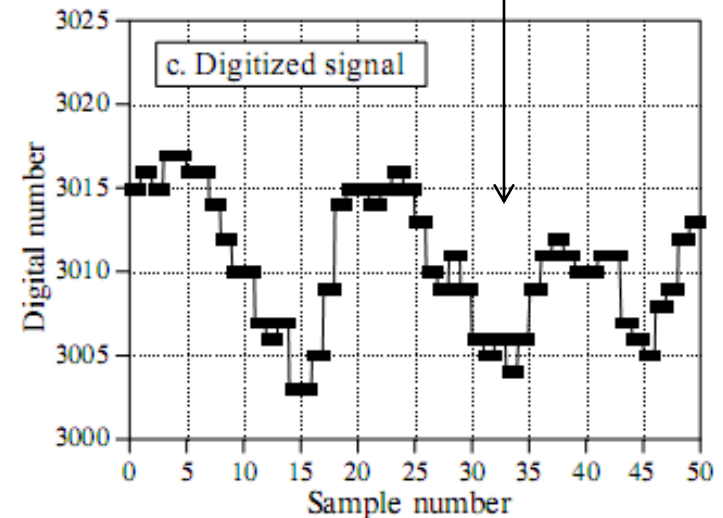
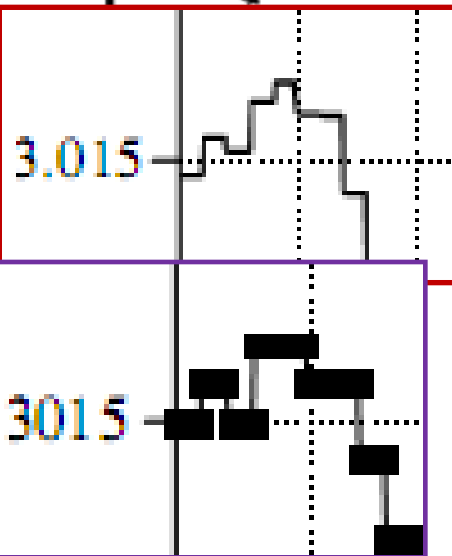
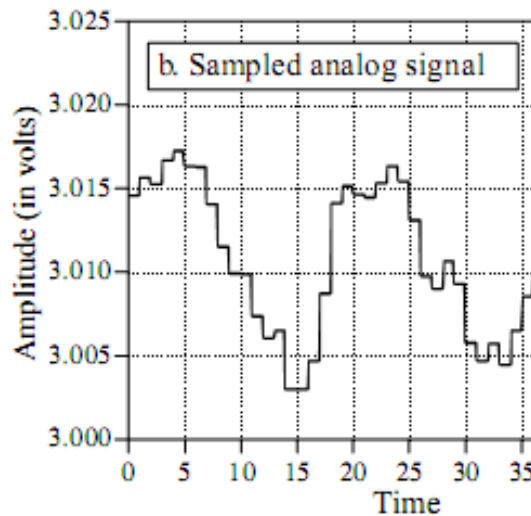
S/H

Sampling

ADC

digital output

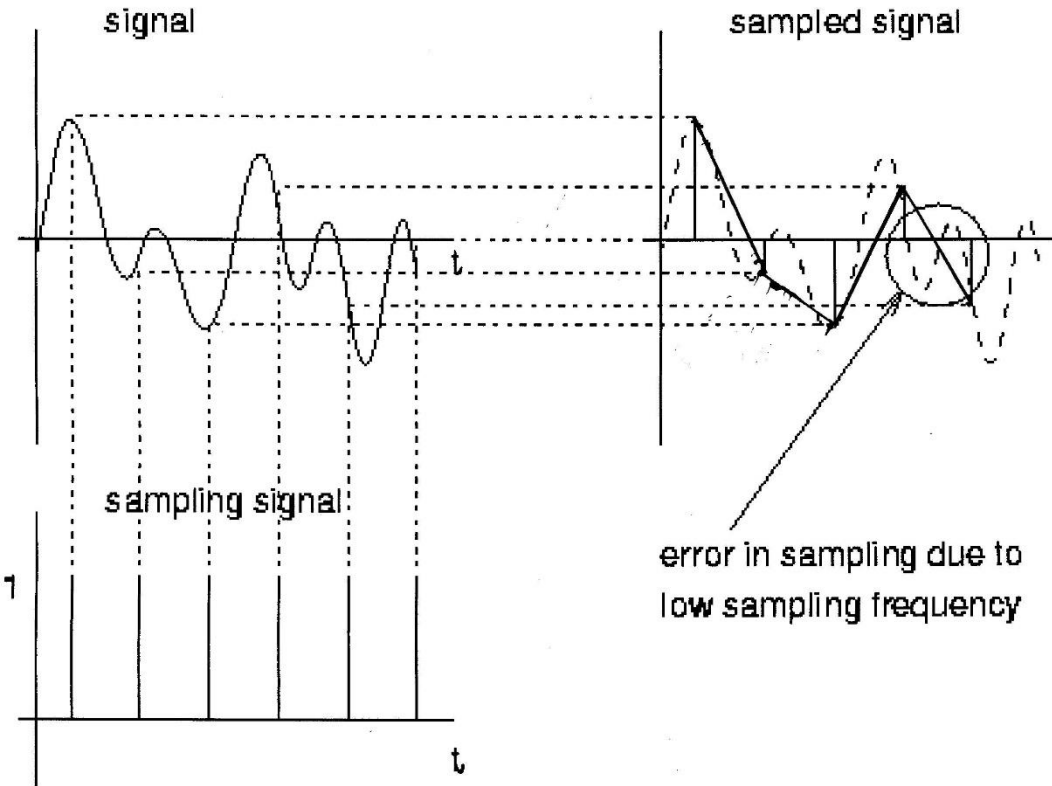
Quantisation



ADC

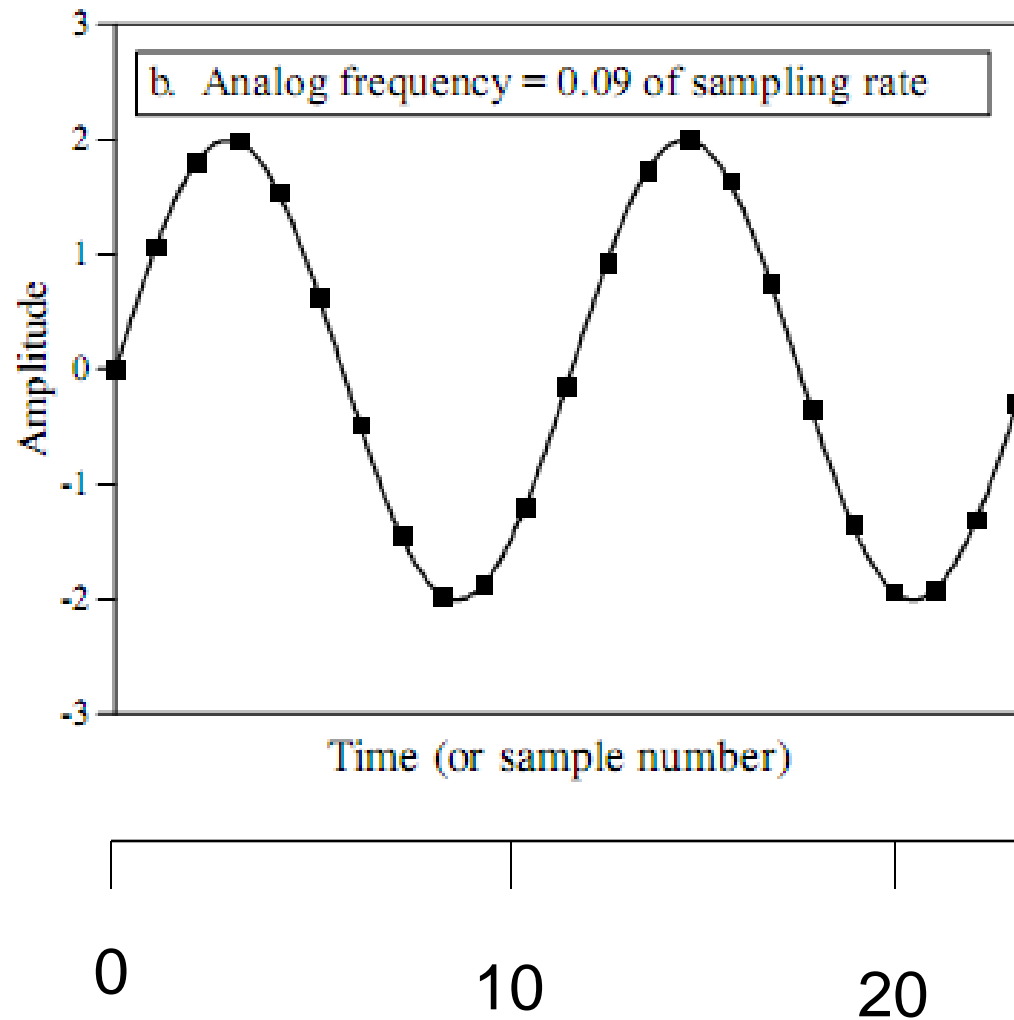
Accuracy and sampling interval

Accuracy is lost in sampling. Wave form distorts. Wave form can be captured with high resolution and sampling rate. For practical purpose 8-10 data required in one cycle of highest frequency to represent waveform correctly.



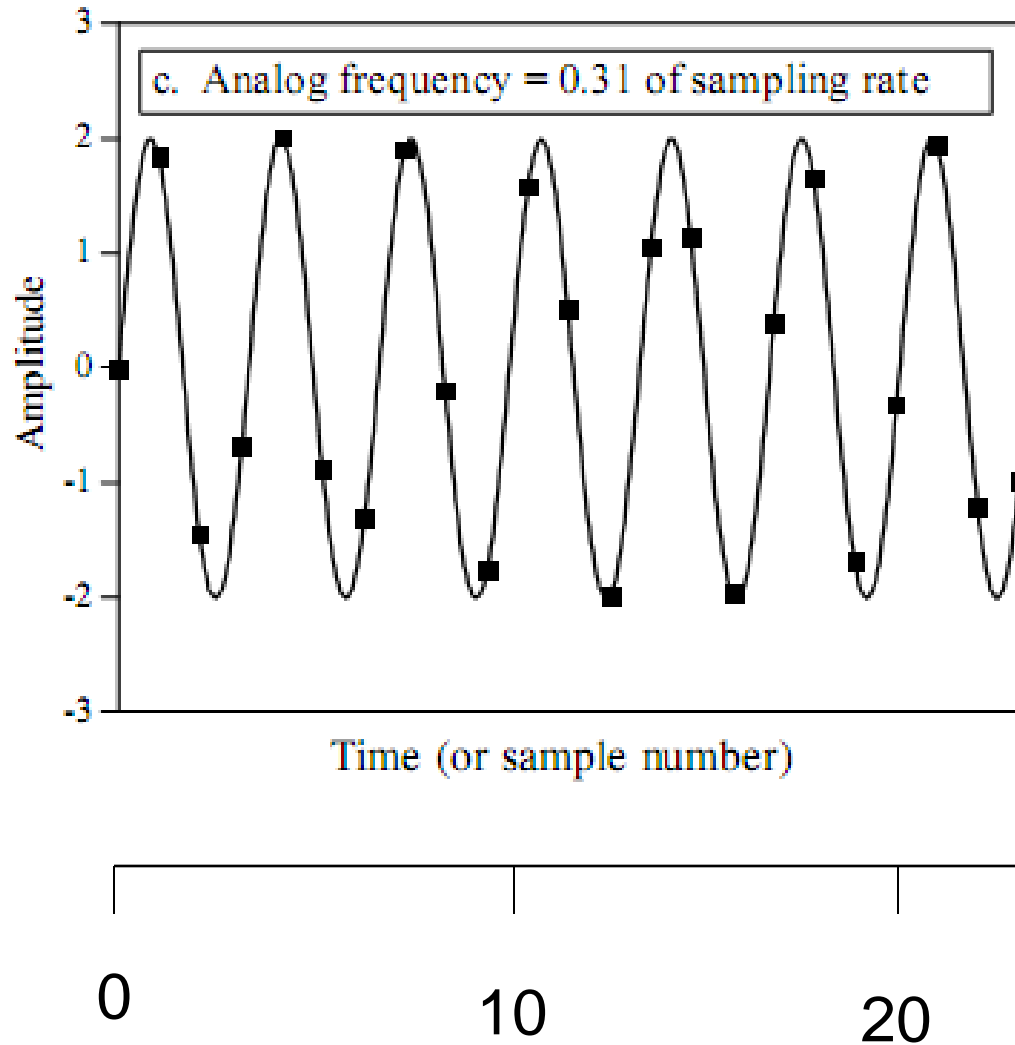
ADC

Accuracy and sampling interval



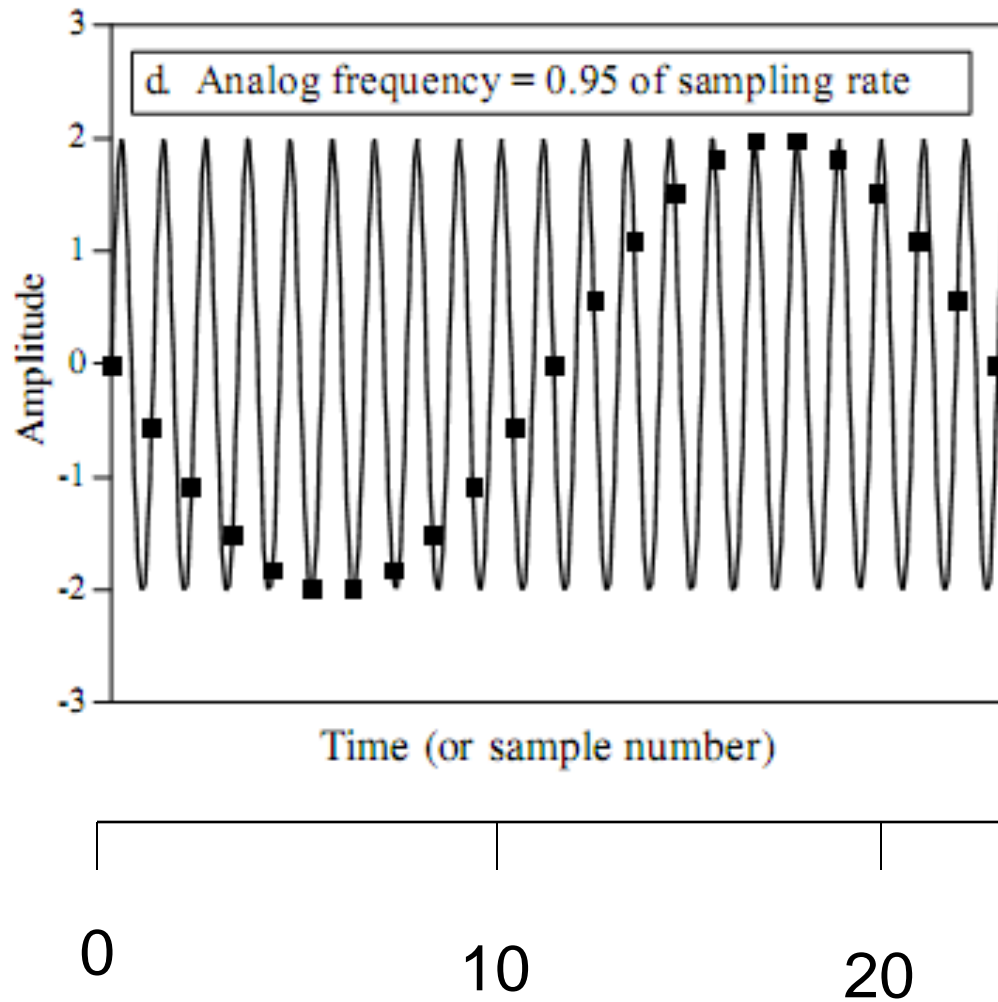
ADC

Accuracy and sampling interval

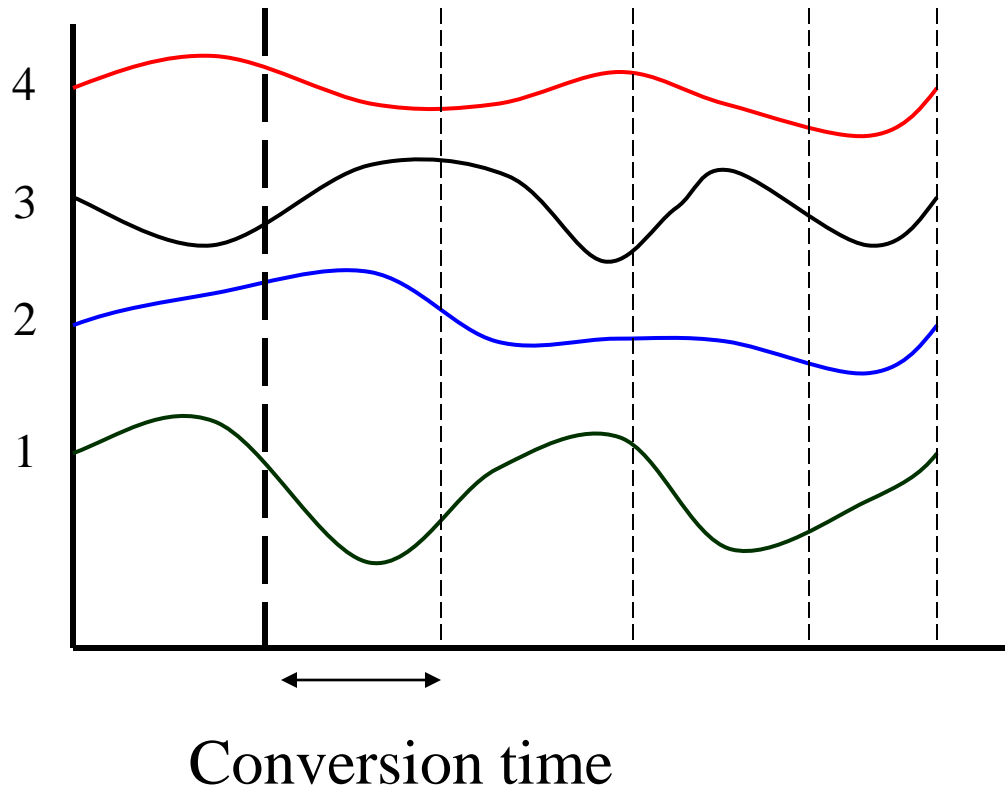


ADC

Accuracy and sampling interval



Output for various ADC configuration



Combination of sample and hold, multiplexer and ADC

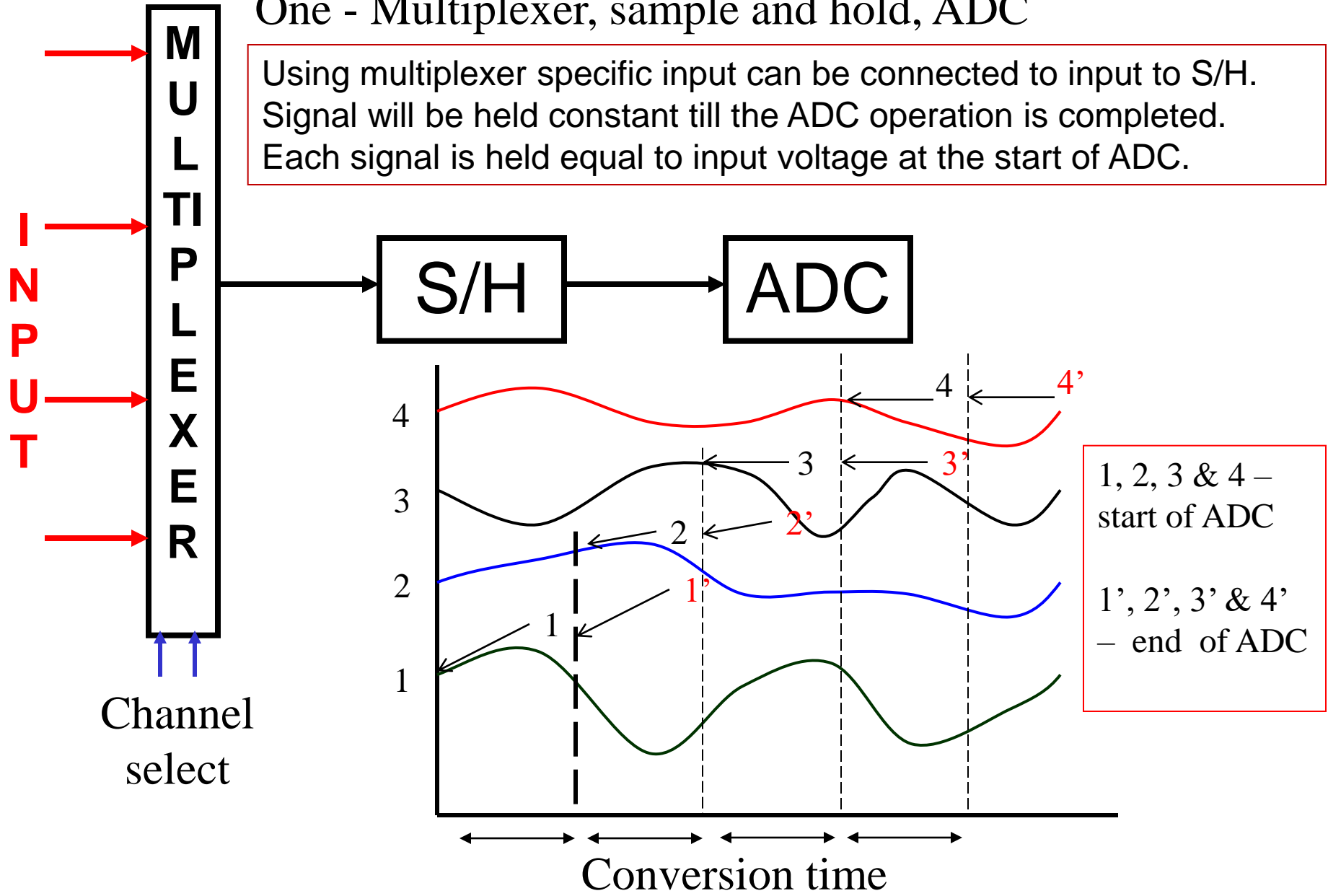
Sample and hold – it will sample and hold the signal for required time

Multiplexer - also called as mux. It is a data selector

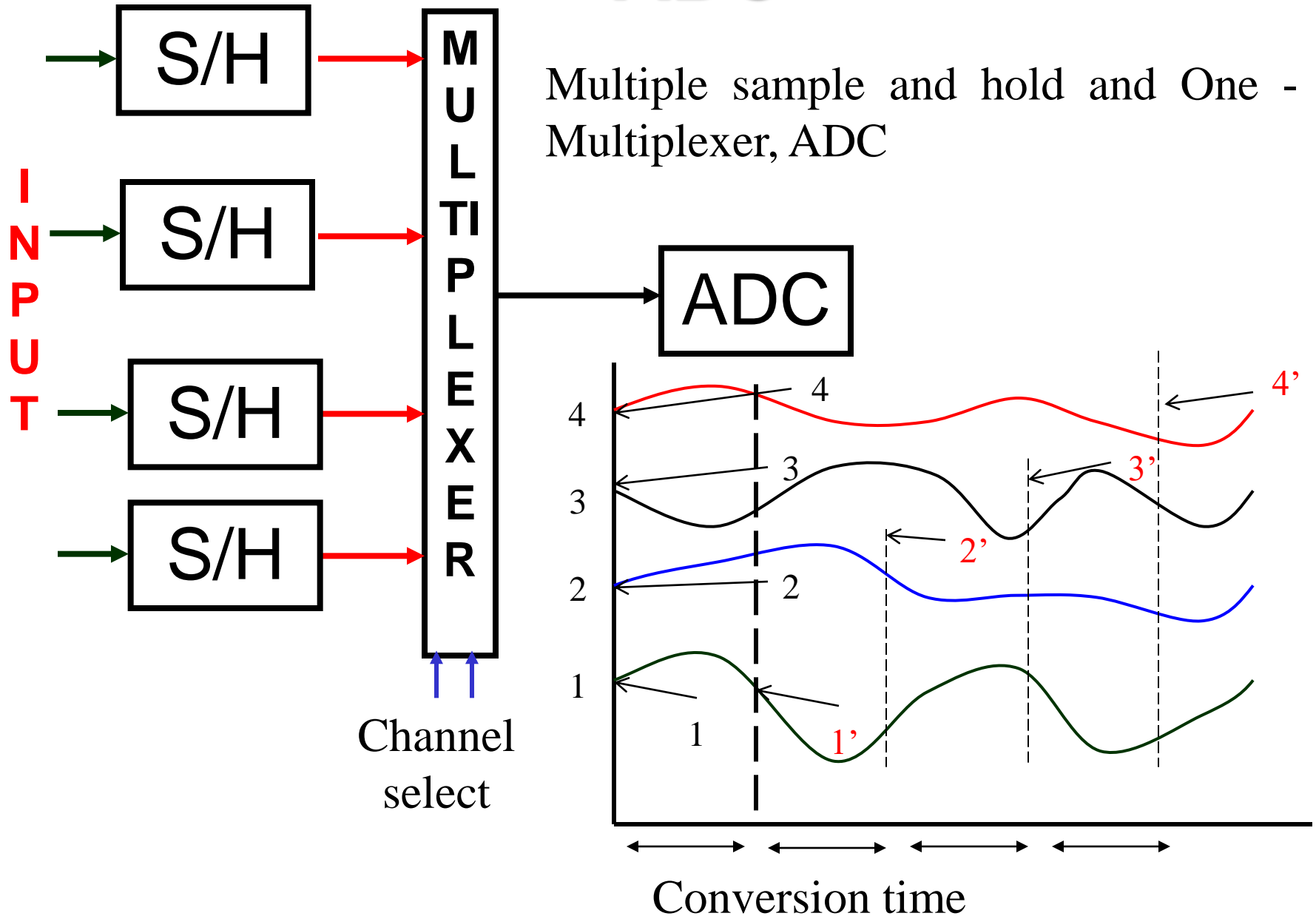
ADC

One - Multiplexer, sample and hold, ADC

Using multiplexer specific input can be connected to input to S/H. Signal will be held constant till the ADC operation is completed. Each signal is held equal to input voltage at the start of ADC.

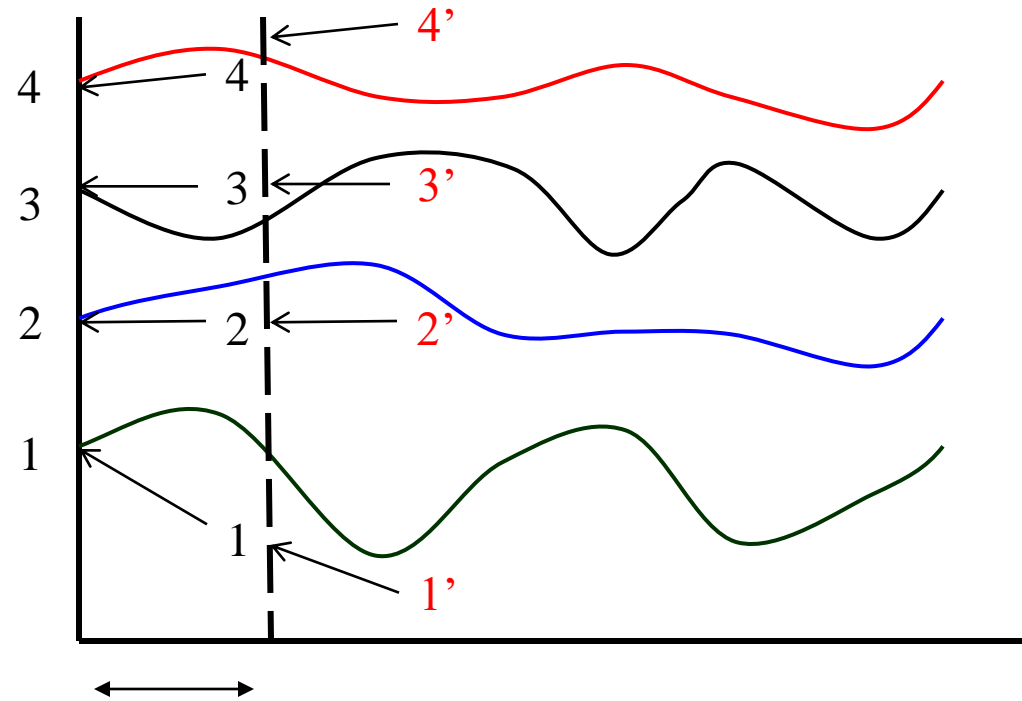
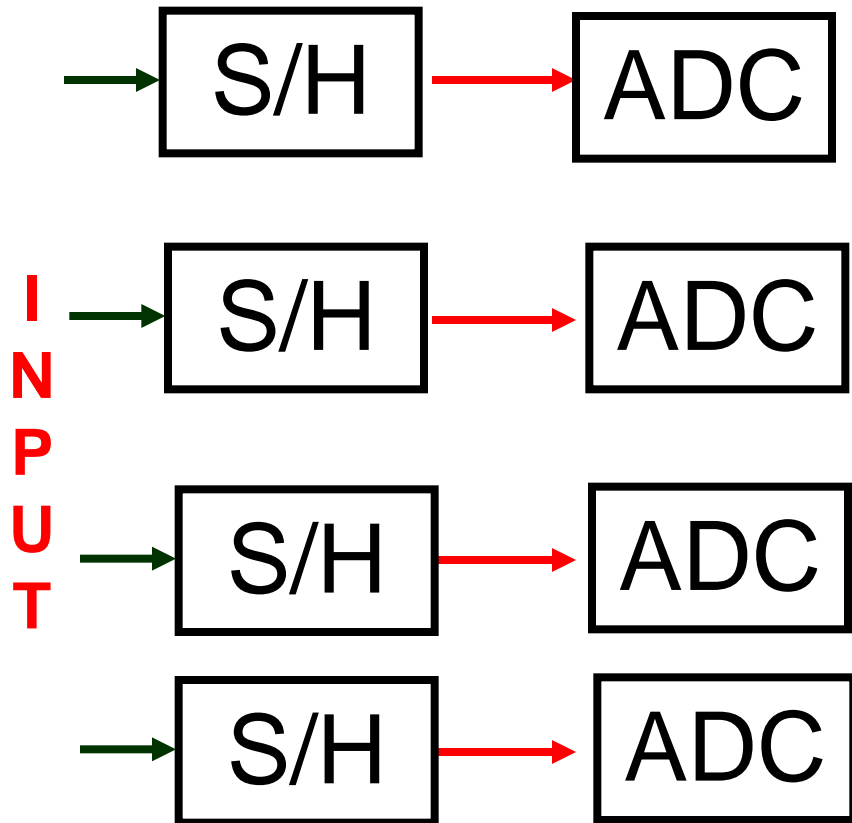


ADC



ADC

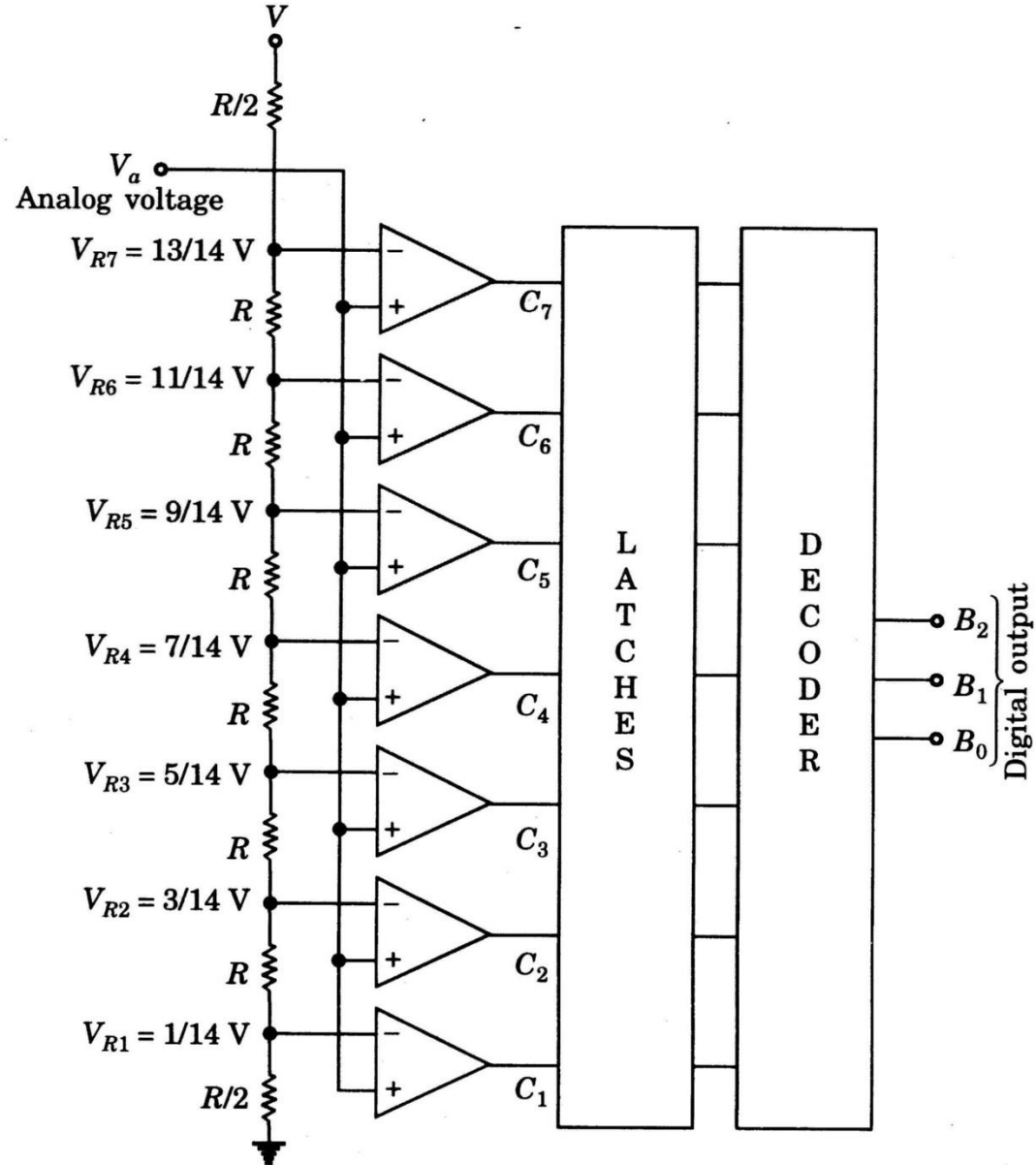
Multiple sample and hold and ADCs



Conversion time

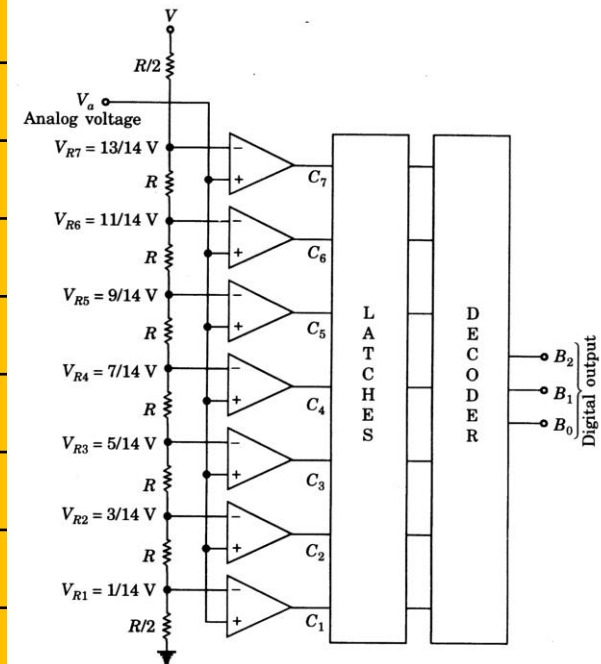
Parallel-comparator ADC

In this the input voltage is compared against the known voltages using comparators set at different voltage levels. The output of these comparators set the logic 1 or 0 and it is decoded using decoder. This ADC will require $(2^n - 1)$ comparators for conversion. This makes it very costly. This is the fastest ADC, also known as parallel ADC or flash ADC.



Parallel-comparator ADC

Analog Input	Comparator Output							Digital Output		
V_a	C_7	C_6	C_5	C_4	C_3	C_2	C_1	B_1	B_2	B_3
$0 \leq V_a < V_{R1}$	0	0	0	0	0	0	0	0	0	0
$V_{R1} < V_a < V_{R2}$	0	0	0	0	0	0	1	0	0	1
$V_{R2} < V_a < V_{R3}$	0	0	0	0	0	1	1	0	1	0
$V_{R3} < V_a < V_{R4}$	0	0	0	0	1	1	1	0	1	1
$V_{R4} < V_a < V_{R5}$	0	0	0	1	1	1	1	1	0	0
$V_{R5} < V_a < V_{R6}$	0	0	1	1	1	1	1	1	0	1
$V_{R6} < V_a < V_{R7}$	0	1	1	1	1	1	1	1	1	0
$V_{R7} < V_a \leq V$	1	1	1	1	1	1	1	1	1	1

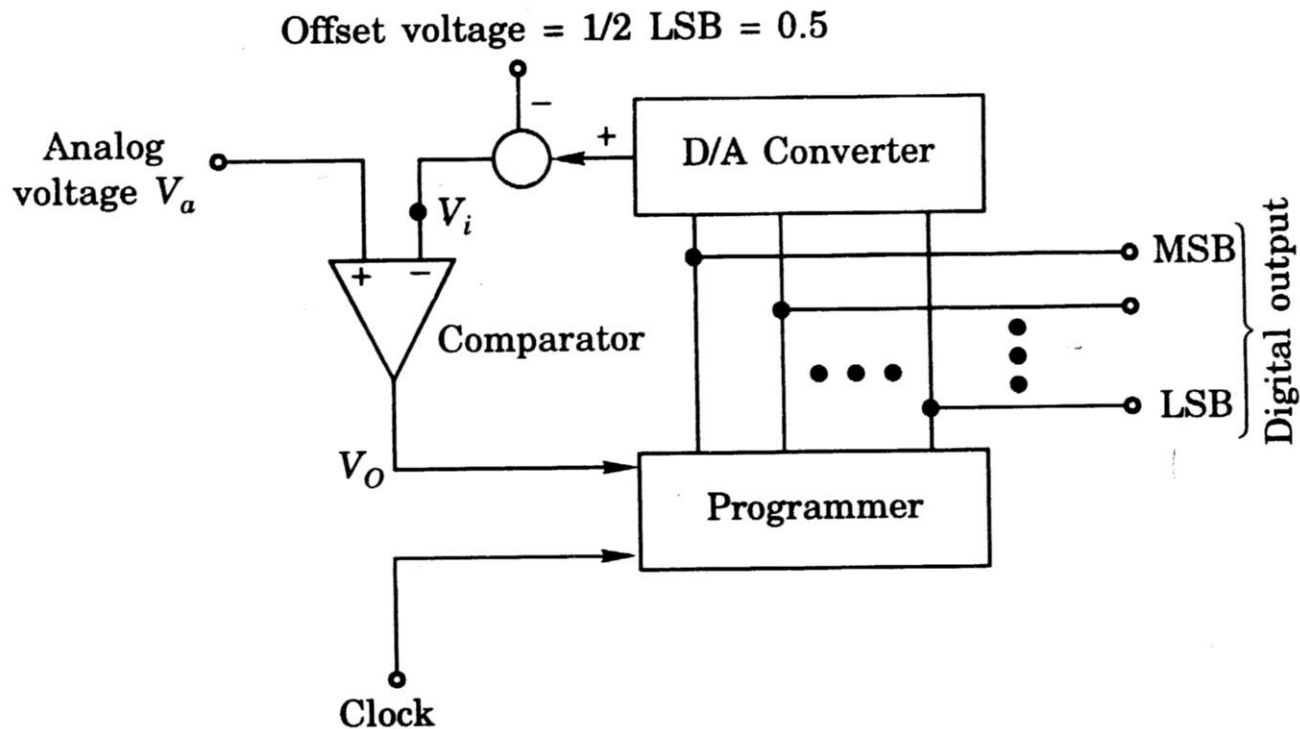


Latch holds the comparator output till it is required.

Decoder converts comparator output (Binary) to digital output (e.g. Straight Binary)

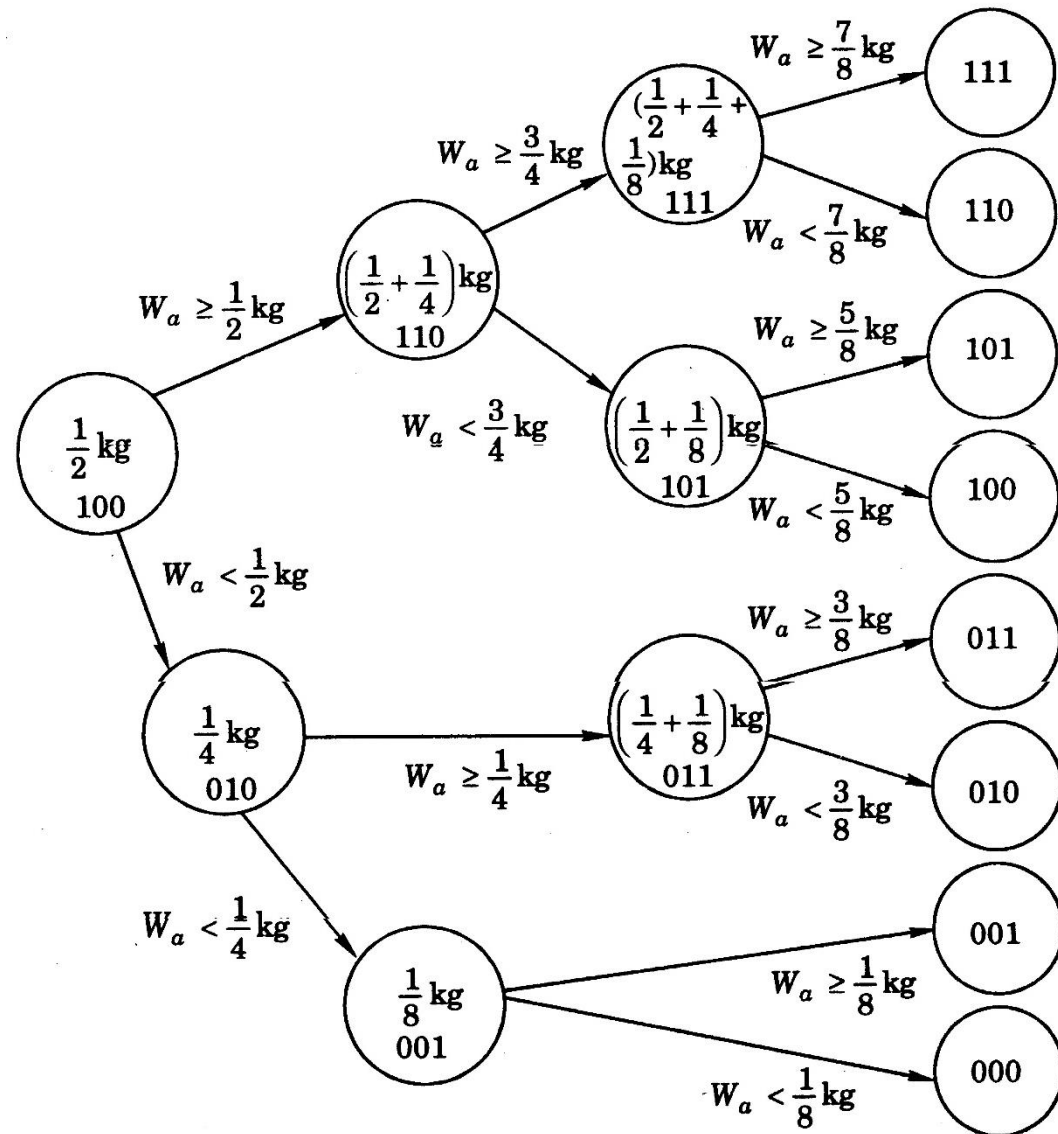
Successive-Approximation ADC

Output of the programmer sets the voltage level for the comparator. Programmer starts comparing input and half the voltage range. Depending on the comparator output it will add/subtract further smaller ($1/4$, $1/8$...) voltage and find out the result. Generally for N bit converter, N steps are required for ADC. Each step is a clock pulse.



Successive-Approximation ADC

Comparing the unknown quantity with half of the quantity which can be measured. If measured unknown quantity is more than the half, then add one fourth and again compare. Repeat the procedure by reducing the successive weight by half till the minimum denomination reached.



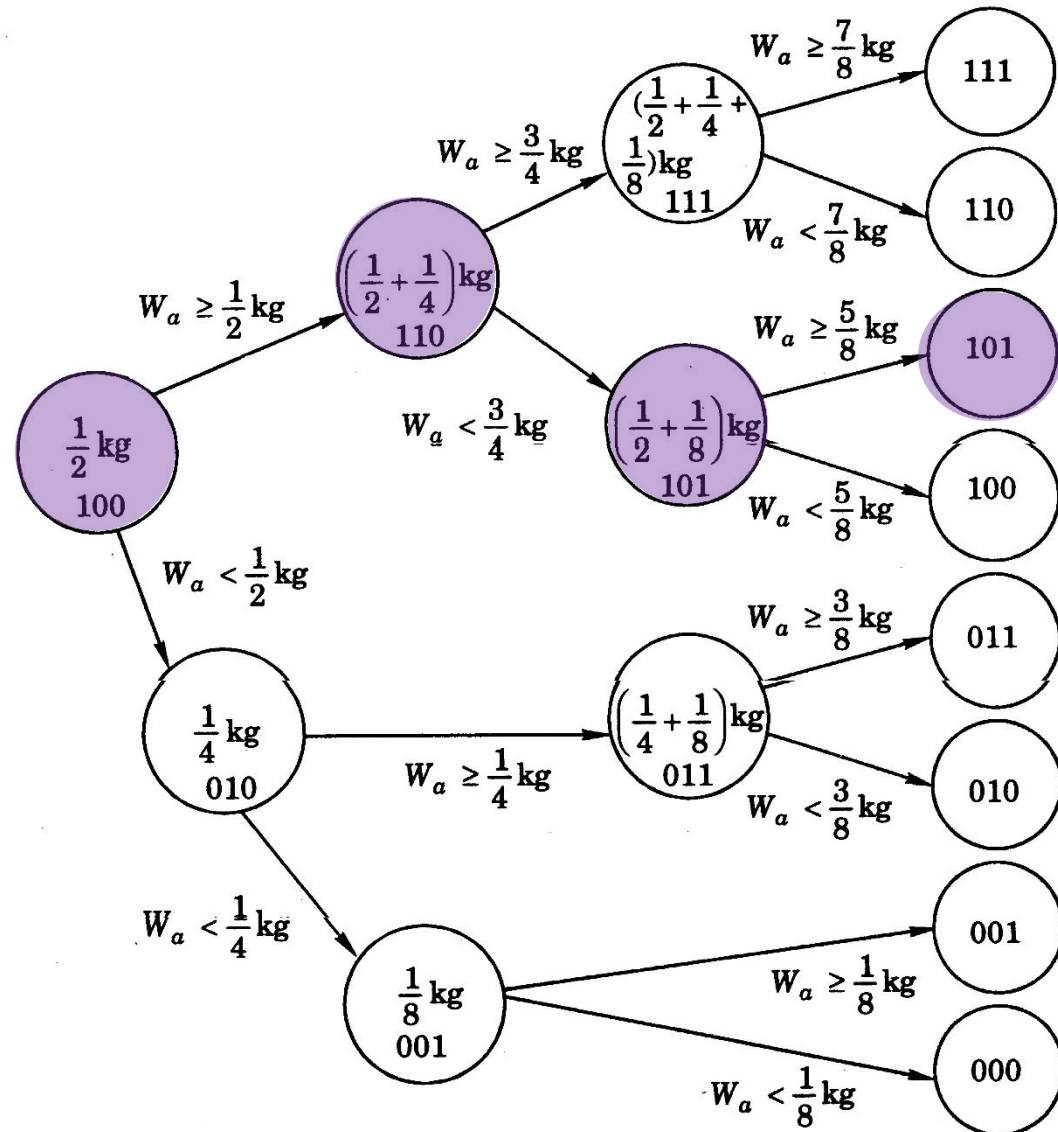
Successive-Approximation ADC

We wish to measure $6/8$ kg.

$$6/8 > 1/2$$

$$6/8 < 3/4$$

$$6/8 > 5/8$$



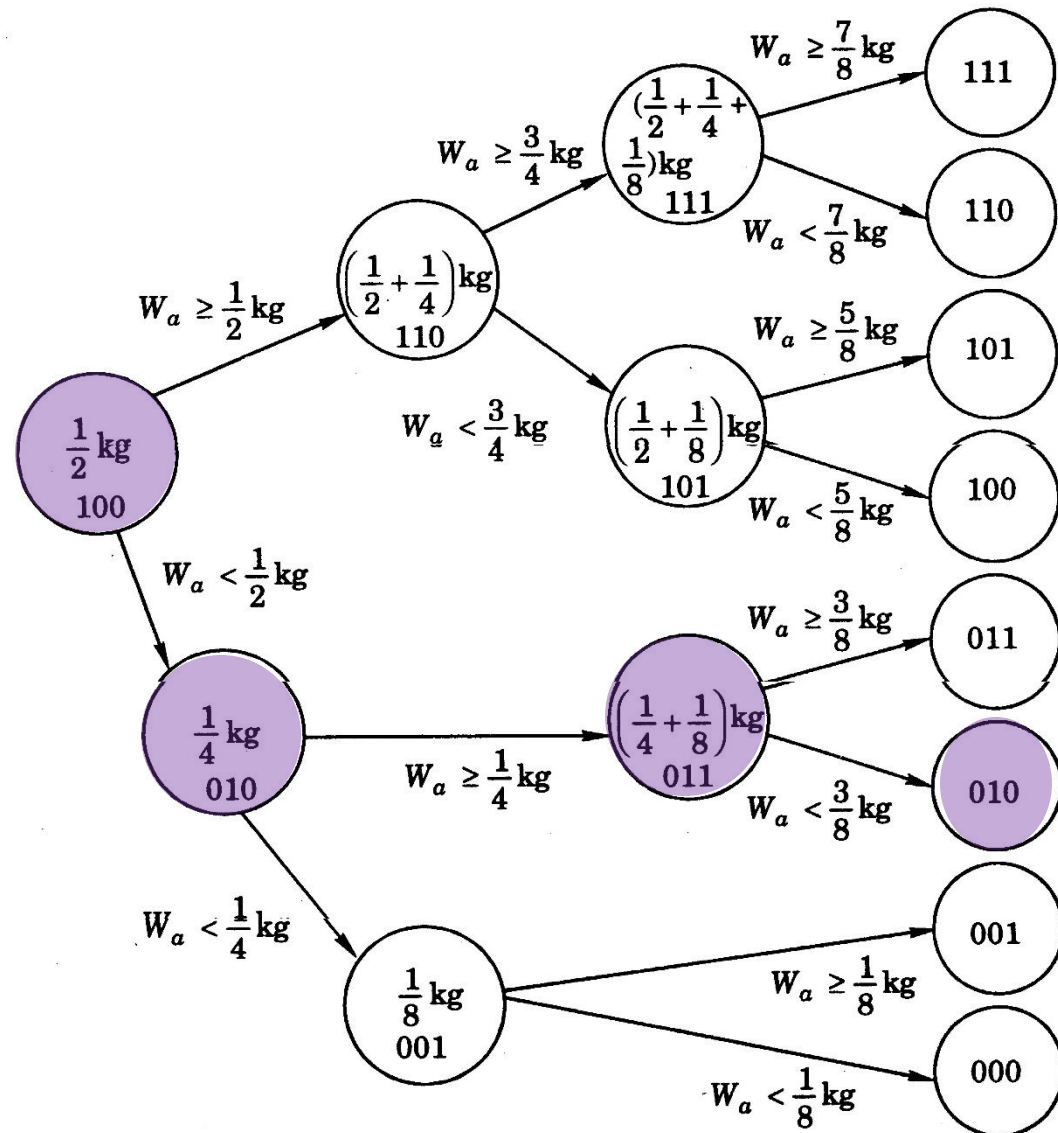
Successive-Approximation ADC

We wish to measure $2/8$ kg.

$$2/8 < 1/2$$

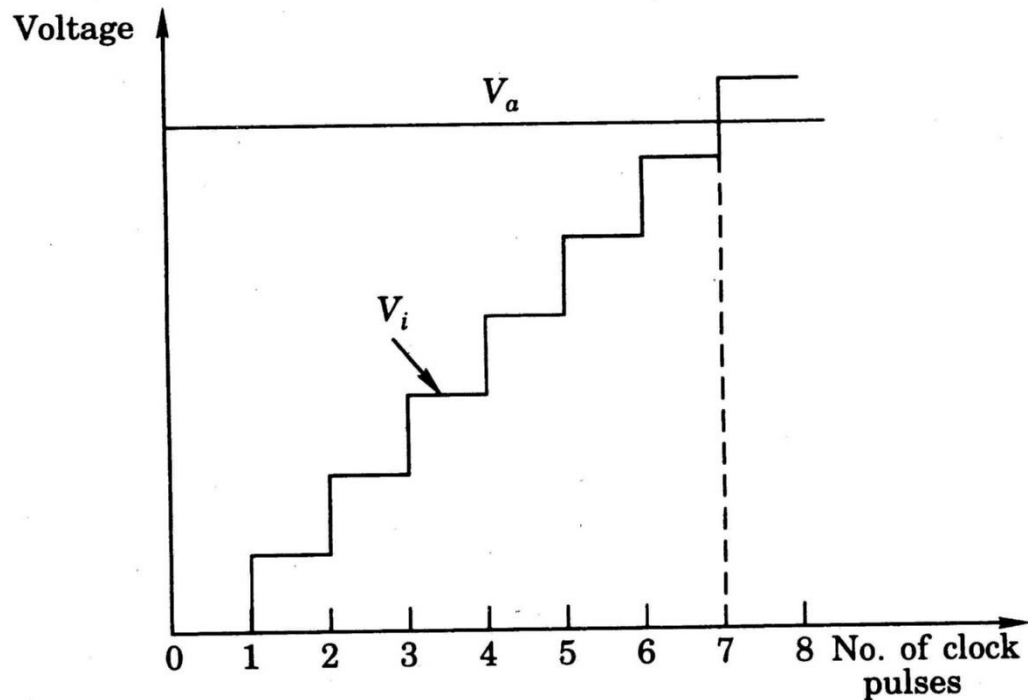
$$2/8 \geq 2/8$$

$$2/8 < 3/8$$



Counting ADC

A counter output is given to a DAC and the output of DAC is compared with input voltage. When the output of the comparator changes the counter value is ADC value. Maximum of 2^n cycles are required for N bit converter.



Specifications for ADC

1. Range of input voltage - 0-5 V, 0-10 V, ± 2.5 V, ± 5 V etc
2. Input impedance - k Ω to M Ω
3. Accuracy - $1/2$ LSB or ± 0.02 % FS
4. Conversion time - 50 μ s to 50 ns
5. Format of digital output - straight binary, two's complement etc