



杭州电子科技大学
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Vivado建工程注意事项



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- ❖ 1. 使用Vivado新建工程时，选择的FPGA型号不能选错，正确的型号为，Device: XC7A100T，Package: FGG484，Speed: -2L；

New Project

Default Part

Choose a default Xilinx part or board for your project.

Parts | Boards

[Reset All Filters](#)

Category: All Package: fgg484 Temperature: All Remaining

Family: Artix-7 Speed: -2L

Search: Q-

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Tran
xc7a15tfgg484-2L	484	250	10400	20800	25	0	45	4
xc7a35tfgg484-2L	484	250	20800	41600	50	0	90	4
xc7a50tfgg484-2L	484	250	32600	65200	75	0	120	4
xc7a75tfgg484-2L	484	285	47200	94400	105	0	180	4
xc7a100tfgg484-2L	484	285	63400	126800	135	0	240	4

< >

? < Back Next > Finish Cancel

Sources x Netlist | **Device Constraints** ? _ □ □

constrs_1 (1)
CLAA.xdc (target)
Simulation Sources (1)
sim_1 (1)

Hierarchy Libraries Compile Order

Source File Properties x Clock Regions ? _ □ □

CLAA.xdc

☒ Enabled

General Properties

Package x **Device** x CLAA.v x CLAA_Test.v ? _ □ □

Tcl Console Messages Log Reports Design Runs Package Pins **I/O Ports** x ? _ □ □

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN_
▼ All ports (14)													
> A (4)	IN			✓	34	LVC MOS18	1.800				PULLDOWN	▼ NONE	▼
▼ B (4)	IN			✓	34	LVC MOS18	1.800				PULLDOWN	▼ NONE	▼
B[3]	IN		V4	✓	34	LVC MOS18	1.800				PULLDOWN	▼ NONE	▼
B[2]	IN		W4	✓	34	LVC MOS18	1.800				PULLDOWN	▼ NONE	▼
B[1]	IN		Y4	✓	34	LVC MOS18	1.800				PULLDOWN	▼ NONE	▼
B[0]	IN		Y6	✓	34	LVC MOS18	1.800				PULLDOWN	▼ NONE	▼
> F (4)	OUT			✓	35	LVC MOS18	1.800		12	▼ SLOW	NONE	▼ FP_VTT_50	▼
▼ Scalar ports (2)													
C0	IN		AB8	✓	34	LVC MOS18	1.800				PULLDOWN	▼ NONE	▼
C4	OUT		G4	✓	35	LVC MOS18	1.800		12	▼ SLOW	NONE	▼ FP_VTT_50	▼

2. 管脚分配:

- (1) 所有输入输出信号必须分配Package Pin;
- (2) 所有输入输出信号的I/O Std设置为LVC MOS18;
- (3) 所有的输入信号, 要设置Pull Type为PULLDOWN。

I/O引脚约束文件 (.xdc) 例子:

```
set_property IOSTANDARD LVCMOS18 [get_ports {QN[3]}]
set_property IOSTANDARD LVCMOS18 [get_ports {QN[2]}]
set_property IOSTANDARD LVCMOS18 [get_ports {QN[1]}]
set_property IOSTANDARD LVCMOS18 [get_ports {QN[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports CLK]
set_property IOSTANDARD LVCMOS18 [get_ports CO]
set_property IOSTANDARD LVCMOS18 [get_ports EN]
```

```
set_property PACKAGE_PIN R1 [get_ports {QN[3]}]
set_property PACKAGE_PIN P2 [get_ports {QN[2]}]
set_property PACKAGE_PIN P1 [get_ports {QN[1]}]
set_property PACKAGE_PIN N2 [get_ports {QN[0]}]
set_property PACKAGE_PIN R4 [get_ports CLK]
set_property PACKAGE_PIN W7 [get_ports MR]
```

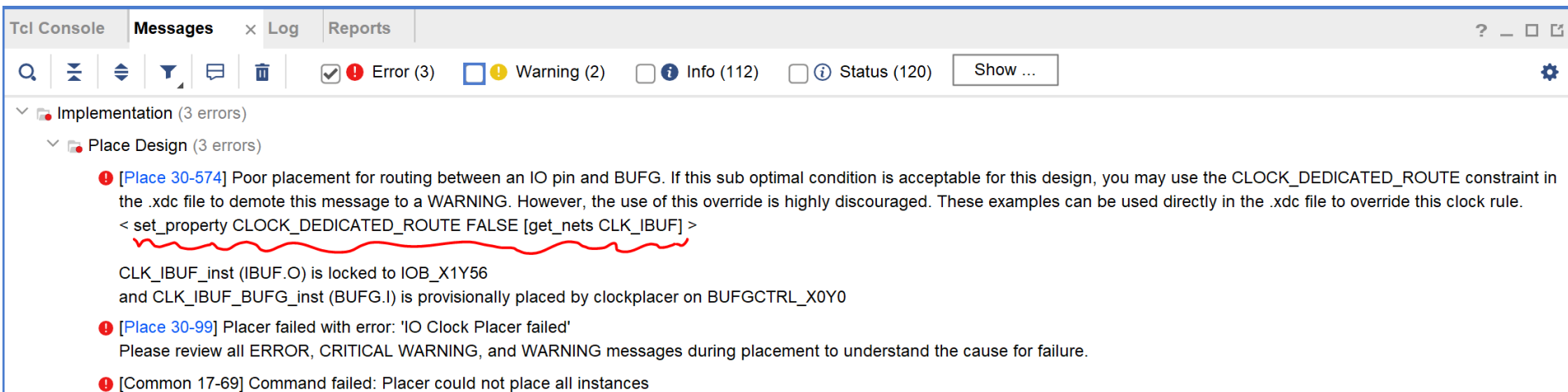
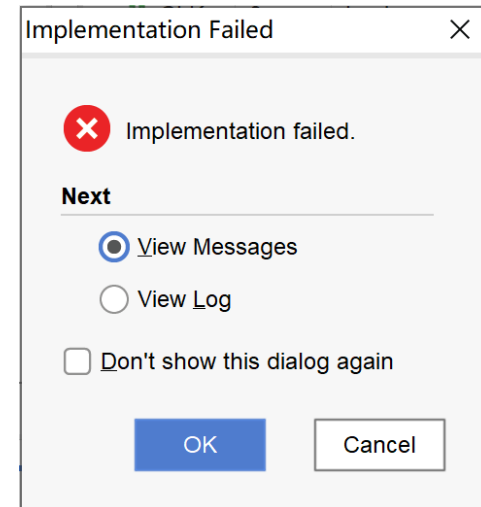
```
set_property PULLDOWN true [get_ports MR]
set_property PULLDOWN true [get_ports CLK]
```

```
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets MR]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets CLK]
```

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
```

在时序逻辑电路的实验中，运行Implementation时，可能会出现Implementation Failed。此时View Messages，在Messages信息栏，可能会出现下图所示的Error信息，如下图所示，则须将下图中红色曲线所指示的约束语句手动添加到.xdc约束文件中，也就是添加如下语句。

set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets CLK_IBUF]



Flow Navigator

Add Sources

Language Templates

IP Catalog

IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

RTL ANALYSIS

Open Elaborated Design

Report Methodology

Report DRC

Report Noise

Schematic

SYNTHESIS

IMPLEMENTATION

Run Implementation

Open Implemented Design

PROGRAM AND DEBUG

Generate Bitstream

Open Hardware

Bitstream Settings...

打开码流设置来更改码流文件格式设置

ELABORATED DESIGN - xc7a100tfgg484-2L (active)

Sources

Netlist

Device Constraints

CLAA

> Nets (17)

> CLA1 (CLA)

> FA0 (FA)

> FA1 (FA)

Source File Properties

Clock Regions

CLAA.xdc

☒ Enabled

General

Properties

Tcl Console

Messages

Log

Reports

Design Runs

Package Pins

I/O Ports

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength
All ports (14)									
> A (4)	IN			✓	34	LVC MOS18	1.800		
> B (4)	IN			✓	34	LVC MOS18	1.800		
> F (4)	OUT			✓	35	LVC MOS18	1.800	12	
Scalar ports (2)									

Package x Device x CLAA.v x CLAA_Test.v x CLAA.xdc

D:/sd_lab/sd_vivado/lab2_pc_adder/CLAA.srcs/constrs_1/new/CLAA.xdc

```

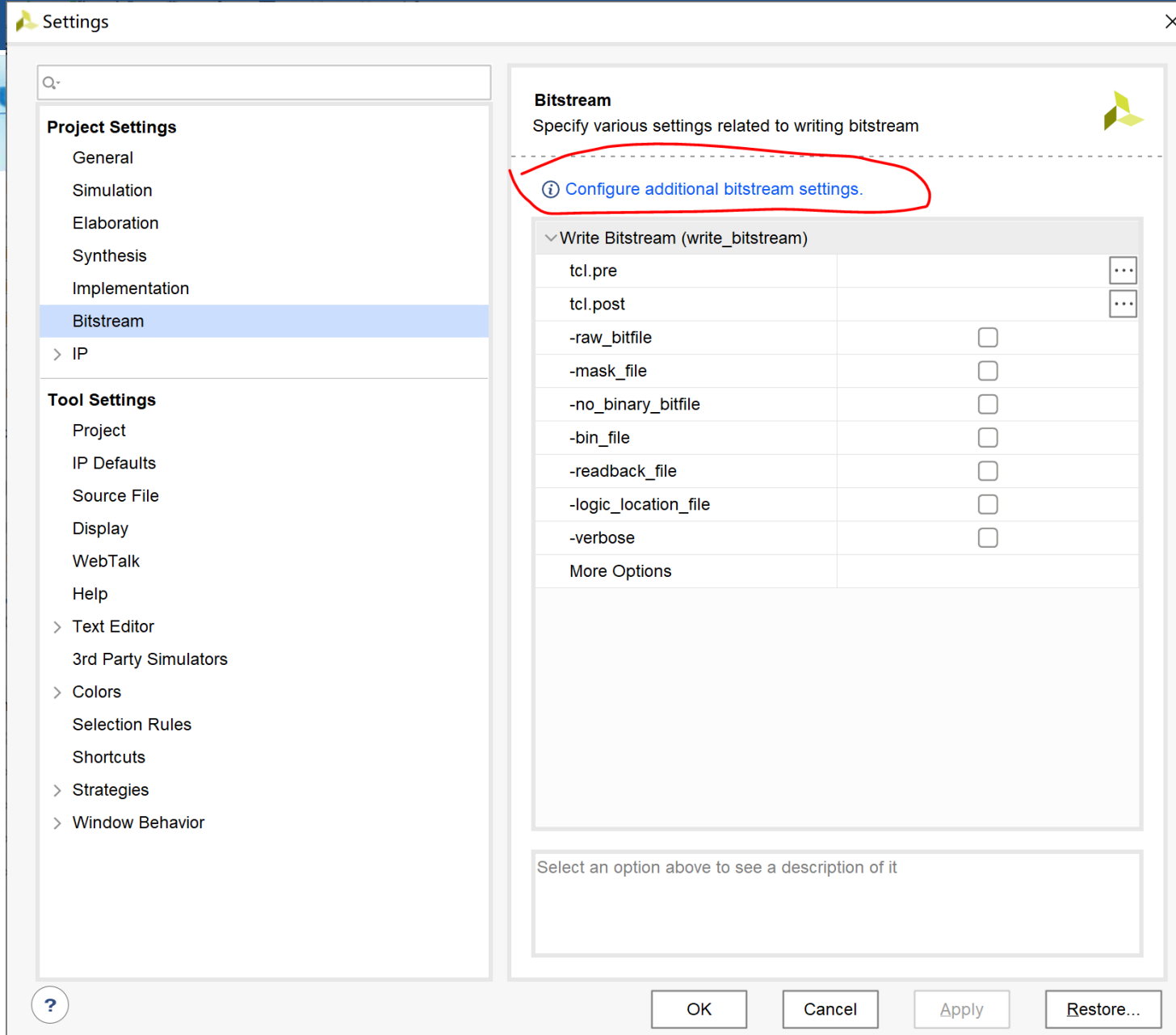
1  #左边8个开关，输入A和B
2  #最右边的开关输入C0
3  #最左边的4个显示灯显示F
4  #最右边的显示灯显示C4
5
6  set_property PACKAGE_PIN T3 [get_ports {A[3]}]
7  set_property PACKAGE_PIN U3 [get_ports {A[2]}]
8  set_property PACKAGE_PIN T4 [get_ports {A[1]}]
9  set_property PACKAGE_PIN V3 [get_ports {A[0]}]
10 set_property PACKAGE_PIN V4 [get_ports {B[3]}]
11 set_property PACKAGE_PIN W4 [get_ports {B[2]}]
12 set_property PACKAGE_PIN Y4 [get_ports {B[1]}]
13 set_property PACKAGE_PIN Y6 [get_ports {B[0]}]

```

❖ 3. 生成 bit 时，一定要先勾选压缩选项；

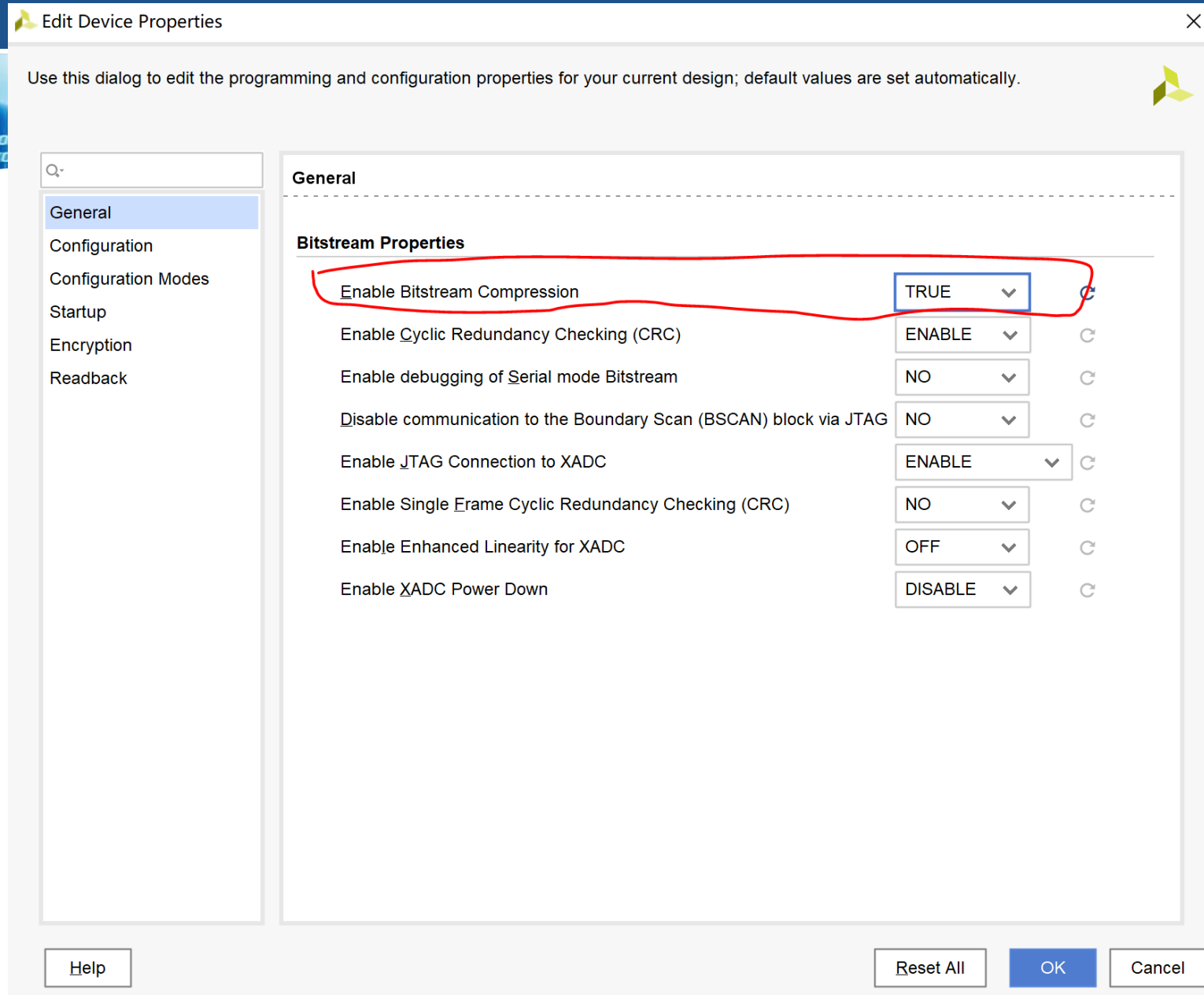
鼠标在 Generate Bitstream 上单击右键，出现 Bitstream Settings，然后单击左键。

❖ 3. 生成 bit 时，一定要先勾选压缩选项；



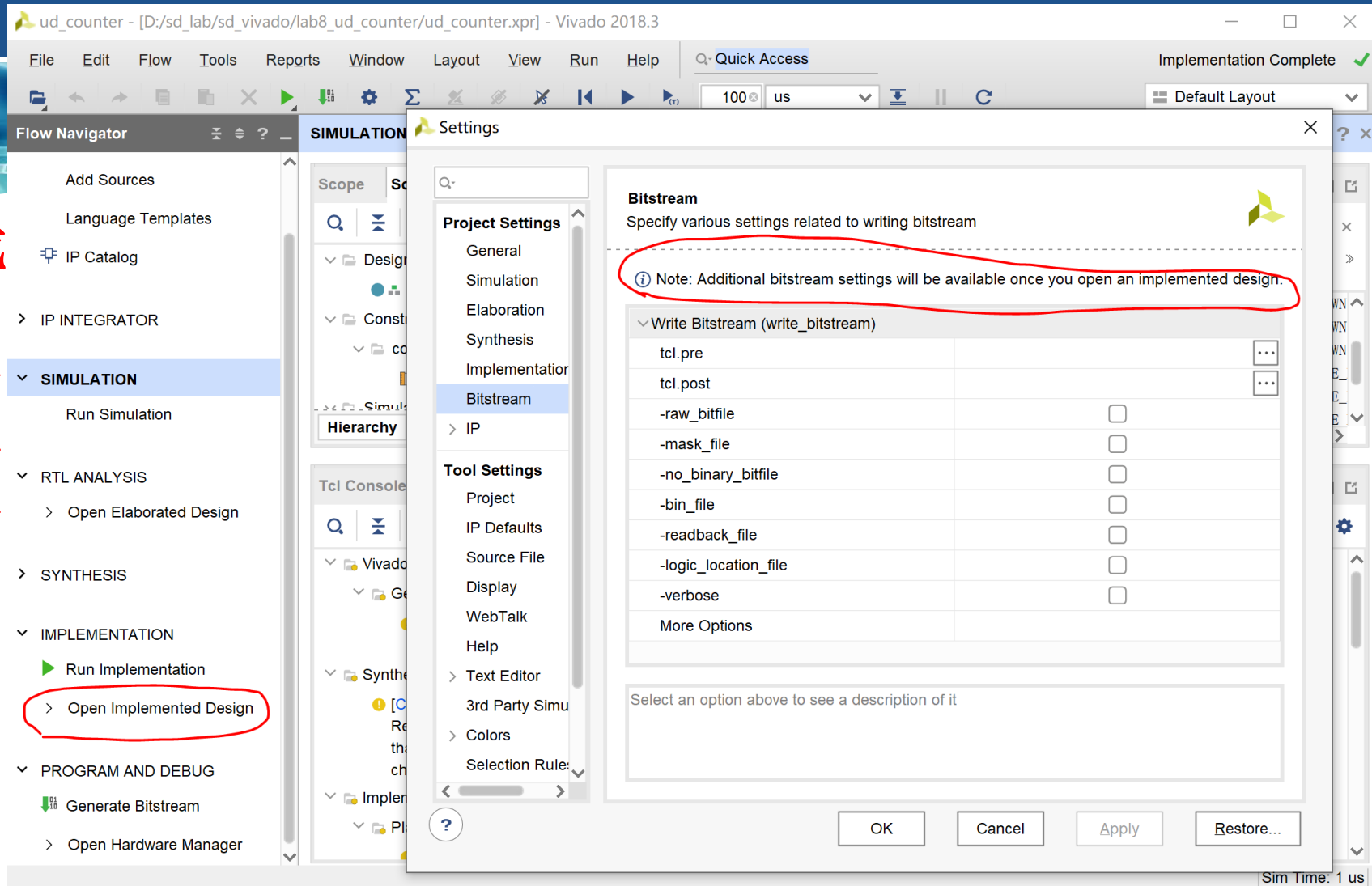
在Settings对话框里面，左键单击Configure additional bitstream settings.

❖ 3. 生成 bit 时，一定要先勾选压缩选项；




在新出现的Edit Device Properties对话框里面，设置Enable Bitstream Compression的属性为TRUE，之后点击OK。

3. 生成bit时，一定要先勾选压缩选项；



注意：如果在运行Implementation后，还没有左键单击执行Open Implemented Design，则在Settings对话框里面，不会出现可点击的Configure additional bitstream settings选项，根据提示，必须先执行Open Implemented design。



3. 生成 bit时， 一定要 先勾选 压缩选 项；

上述操作实际上是在.xdc约束文件中增加了下面的一条语句。

set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]

直接在.xdc约束文件中手工增加该条语句也是一样的效果。

同样前面通过**I/O Planning**图形化界面对**I/O**管脚进行的约束设置都可以在.xdc文件中根据语法要求手工添加。

有组合逻辑电路生成bit时的注意事项；

The screenshot shows the Vivado IDE interface. A dialog box titled "Bitstream Generation Failed" is open in the top right corner, displaying a red 'X' icon and the message "Bitstream Generation failed." Below the message, there are two options under the "Next" section: "View Log" (checked) and "Don't show this dialog again" (unchecked). "OK" and "Cancel" buttons are at the bottom of the dialog.

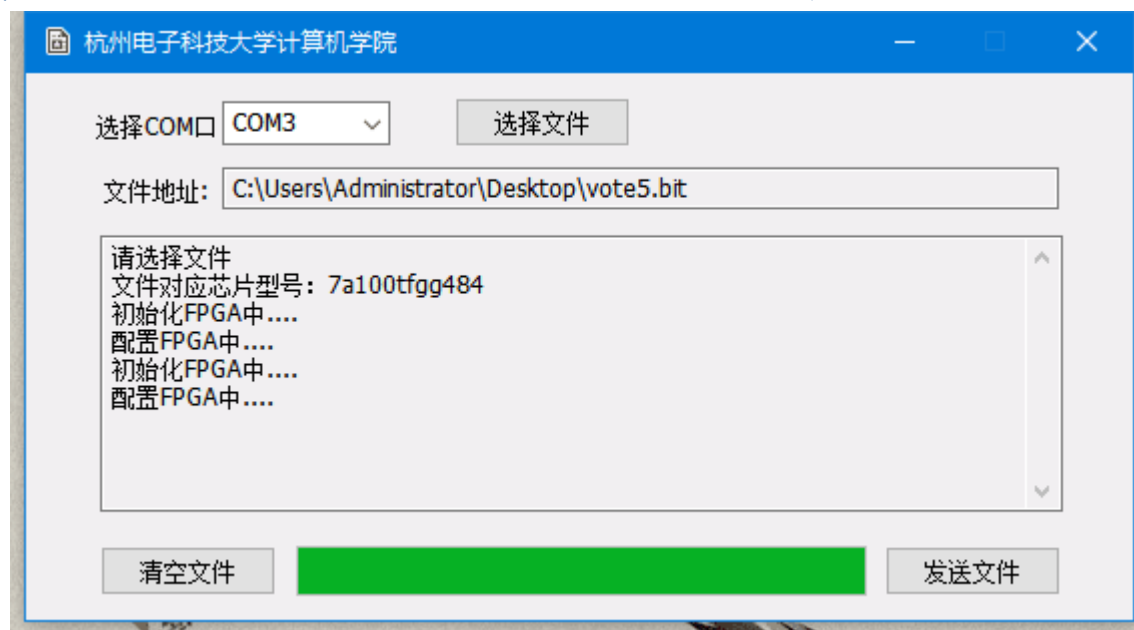
The Messages console in the bottom left shows the following error details:

- Synthesis (1 critical warning)
 - [Common 17-55] 'set_property' expects at least one object. [rs_triger.xdc:14]
- Implementation (2 errors)
 - Write Bitstream (2 errors)
 - DRC (1 error)
 - Netlist (1 error)
 - Design Level (1 error)
 - Combinatorial Loop (1 error)
 - [DRC LUTLP-1] Combinatorial Loop Alert: 1 LUT cells form a combinatorial loop. This can create a race condition. Timing analysis may not be accurate. The preferred resolution is to modify the design to remove combinatorial logic loops. If the loop is known and understood, this DRC can be bypassed by acknowledging the condition and setting the following XDC constraint on any one of the nets in the loop: 'set_property ALLOW_COMBINATORIAL_LOOPS TRUE [get_nets <myHier/myNet>]'. One net in the loop is Q_OBUF. Please evaluate your design. The cells in the loop are: Q_OBUF_inst_i_1.
 - [Vivado 12-1345] Error(s) found during DRC. Bitgen not run.

在有组合逻辑环路存在的电路实验中，最终在生成bit时，会出现上图所示的错误，此时需要按照错误提示在.xdc约束文件中增加下面的一条语句，从而允许组合逻辑环路的存在。

set_property ALLOW_COMBINATORIAL_LOOPS TRUE [get_nets Q_OBUF]

❖ 4. 烧录：打开自制程序（以管理员身份打开，不需要安装），再连接USB端子，如下图配



选择文件后，需要选择连接口COM，一般双USB接口的电脑其中一个COM3，其中一个COM4，选择好连接口后点击发送，发送成功后则可以在板卡上进行调试。若有无法识别板卡的情况，则可能是由于电脑的USB口供电不足造成的，可换一个电脑的USB口重新连接板卡。