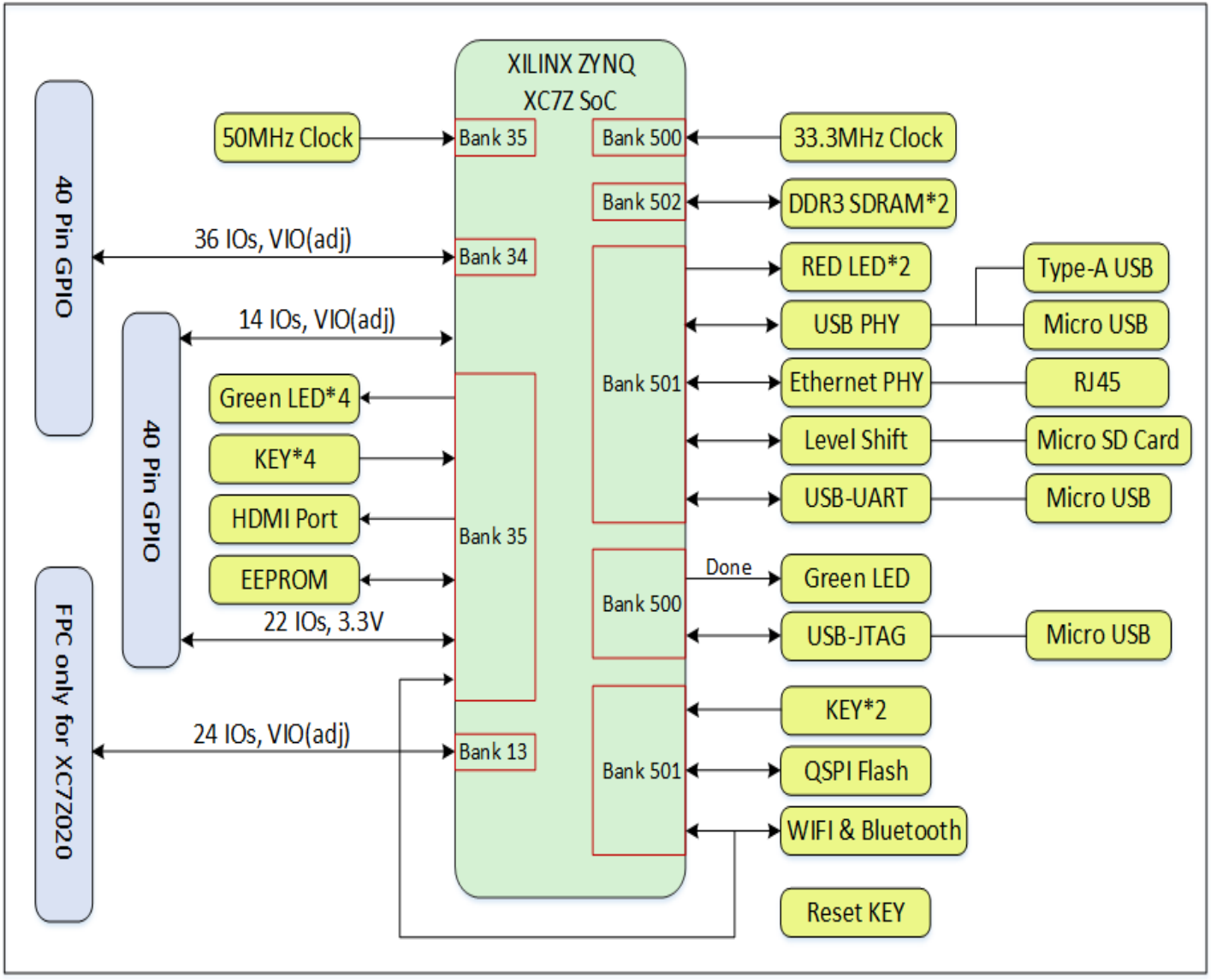
Xilinx Zynq-7000 FPGA Board (MicroZus)



Page Num	Description
Page00	Block
Page01	POWER
Page02	ZYNQ7010_POWER
Page03	ZYNQ7010_CONFIG
Page04	ZYNQ7010_PL
Page05	ZYNQ7010_PS
Page06	ZYNQ7010_DDR
Page07	DDR3
Page08	USB TO UART
Page09	USB OTG
Page10	GPHY
Page11	WIFI、 BT
Page12	HDMI_INTERFACE
Page13	CONNECTOR
Page14	EEPROM&QSPI FALSH&SD
Page15	KEY&LED
Page16	USB TO JTAG

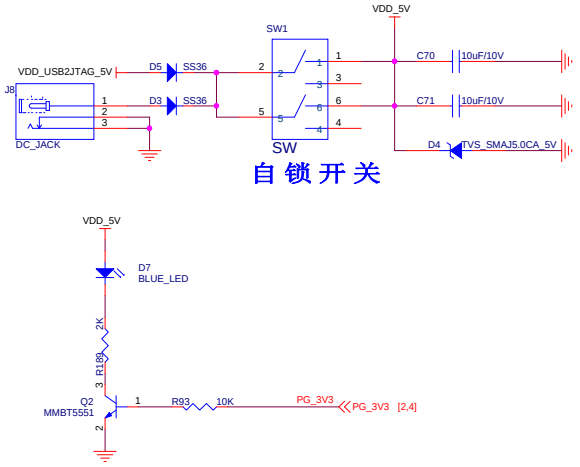
MicroPhase

Title: SCH_BLOCK

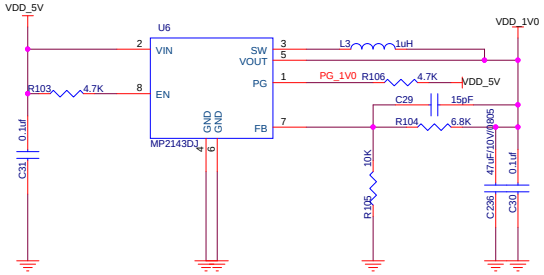
Size | Document Number: MicroZee Schematic | Rev: 1.2

Date: Thursday, December 21, 2017 | Sheet 1 of 17

POWER_INPUT

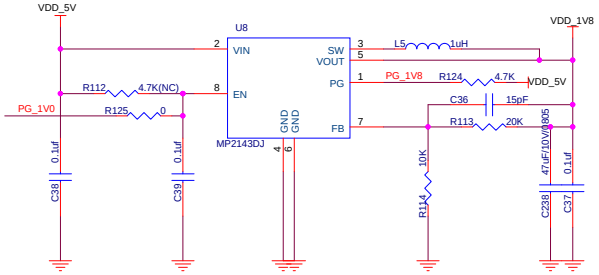


POWER_1V0



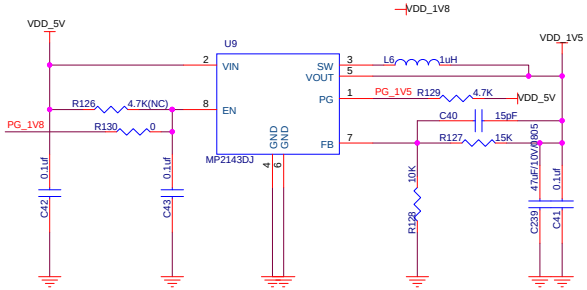
Vref = 0.6V VOUT = 1.0V

POWER_1V8



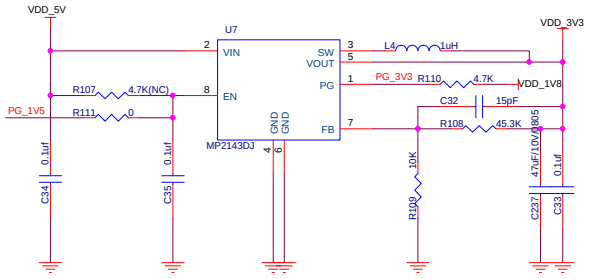
Vref = 0.6V VOUT = 1.8V

POWER_1V5



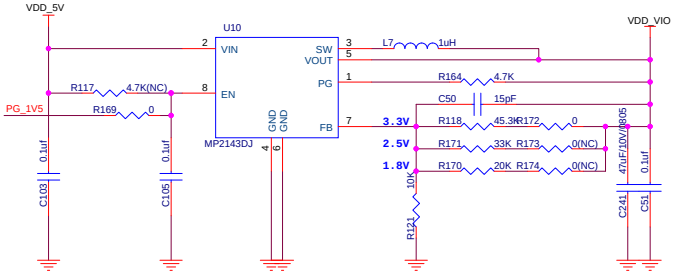
Vref = 0.6V VOUT = 1.5V

POWER_3V3



Vref = 0.6V VOUT = 3.3V

POWER_VIO

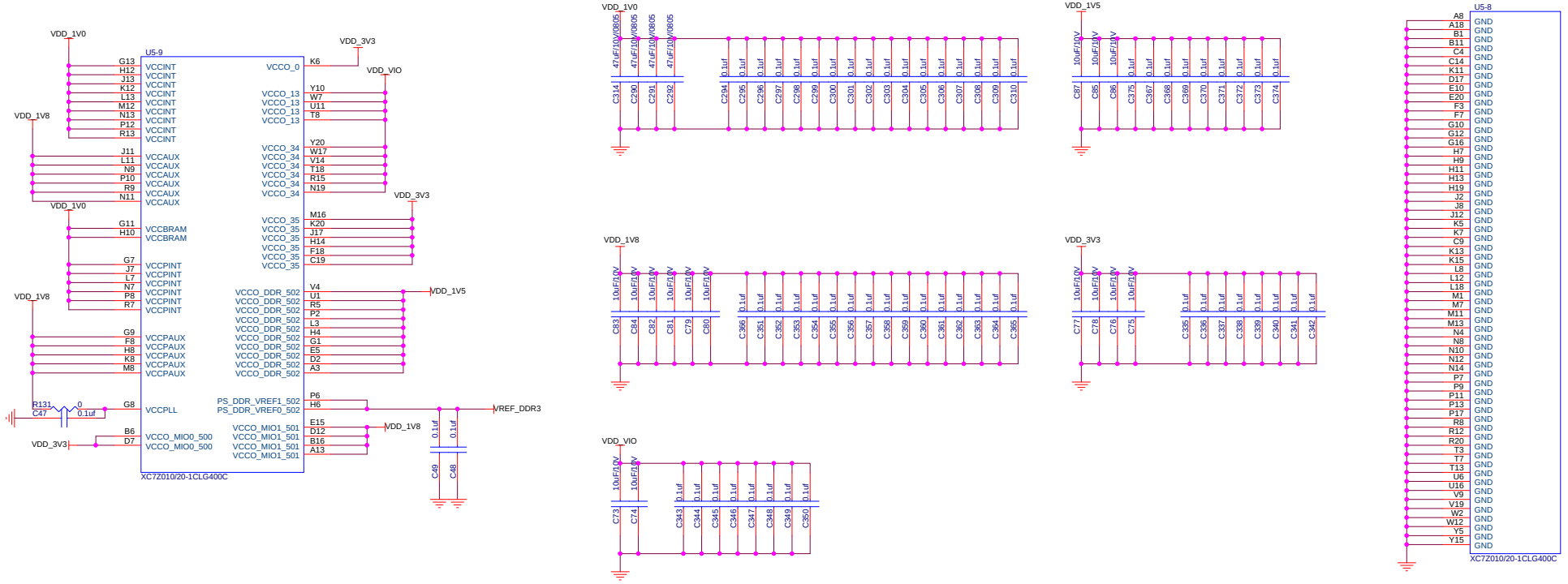


Vref = 0.6V VOUT = ADJ

MicroPhase Technology

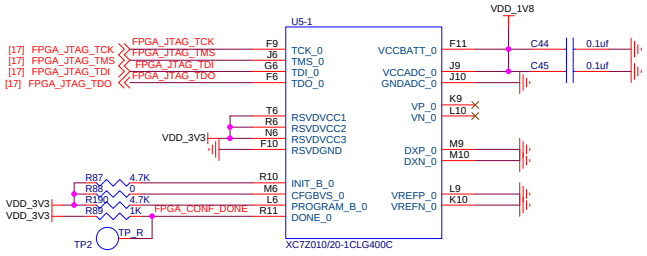
Title	ZYNQ7010 POWER
Size	Document Number: MicroZee Schematic
Rev	1.2
Date:	Thursday, December 21, 2017
Sheet	2 of 17

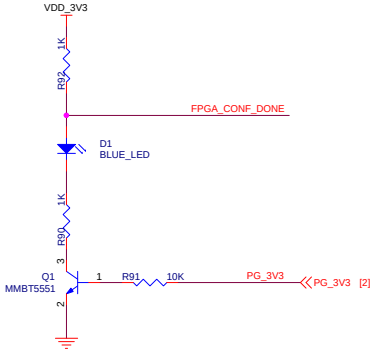
FPGA_POWER



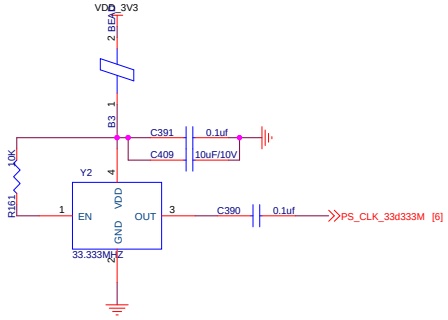
MicroPhase			
Title	ZYNQ7010 FPGA_POWER		
Size	Document Number MicroZee Schematic	1.2	Rev
Date: Thursday, December 21, 2017	Sheet 3 of 17		

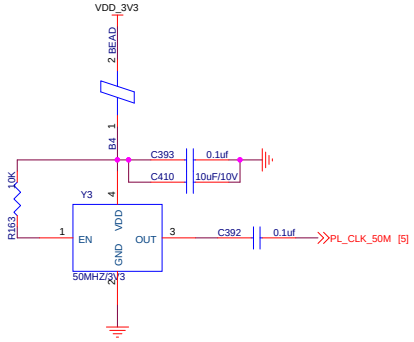
ZYNQ_CONFIG



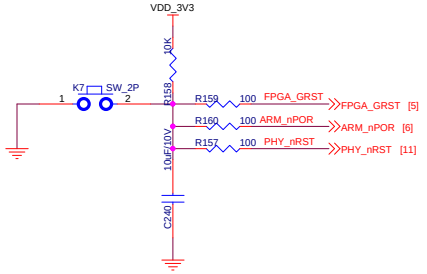


ZYNQ_CLK





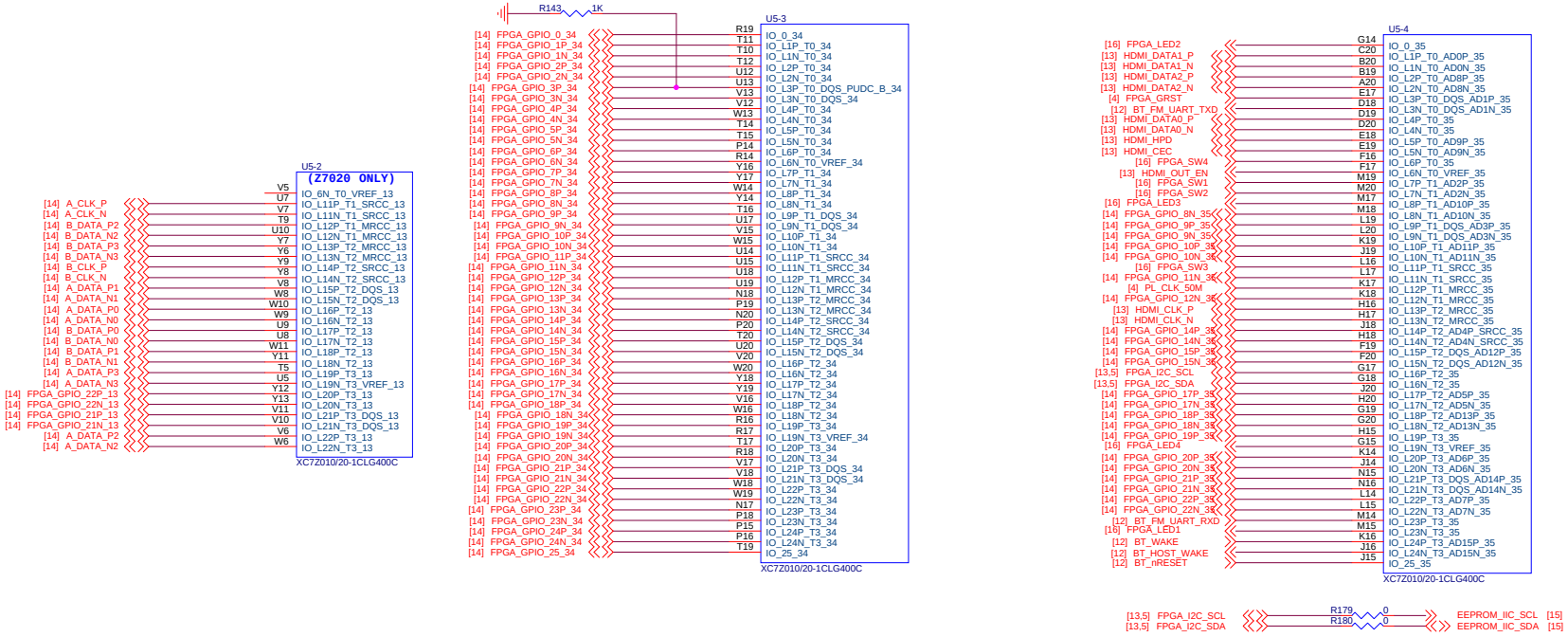
ZYNQ_RST



MicroPhase

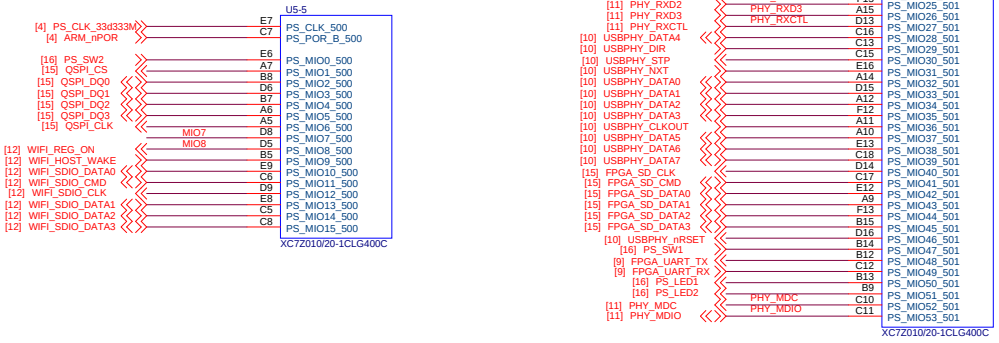
Title	ZYNQ7010 FPGA_CONFIG
Size	Document Number: MicroZee Schematic — Rev: 1.2
Date: Thursday, December 21, 2017	Sheet 4 of 17

FPGA_PL



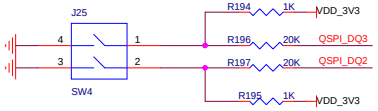
Title	ZYNQ7010 FPGA_PL
Size	Document Number: MicroZee Schematic
Rev	1.2
Date:	Thursday, December 21, 2017
Sheet	5 of 17

FPGA_PS



BOOT_OPTION


```
MIO[8] =1 ----MIO bank1 voltage=1.8V
MIO[2] =0 ----cascaded JTAG
MIO[3] =0 ----JTAG/NAND/Quad-SPI/SD
MIO[6] =0 ----PLL used
MIO[7] =0 ----MIO bank0 voltage=3.3V
```



Boot Mode	MIO[5] (QSPI_D3)	MIO[4] (QSPI_D2)
JTAG	0	0
NAND	0	1
QSPI-FLASH	1	0
SD Card	1	1

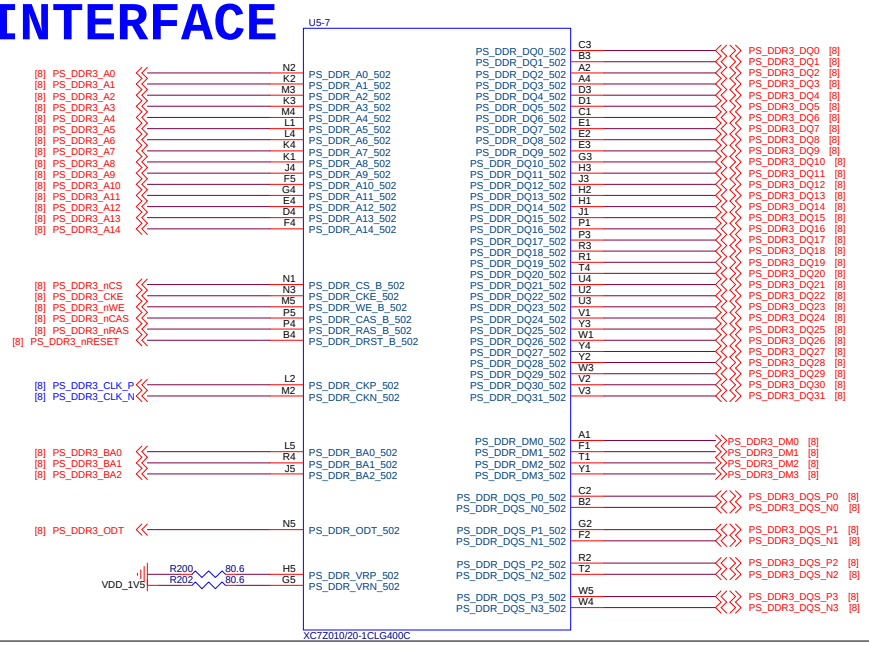
MicroPhase

Title: ZYNQ7010 FPGA_PS

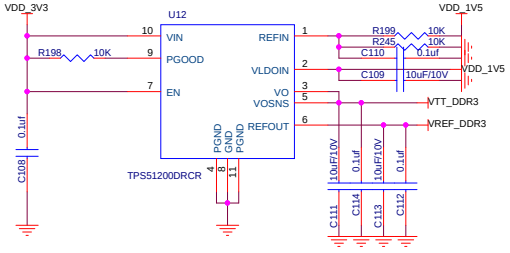
Size | Document Number: MicroZee Schematic | Rev: 1.2

Date: Thursday, December 21, 2017 | Sheet 6 of 17

DDR_INTERFACE

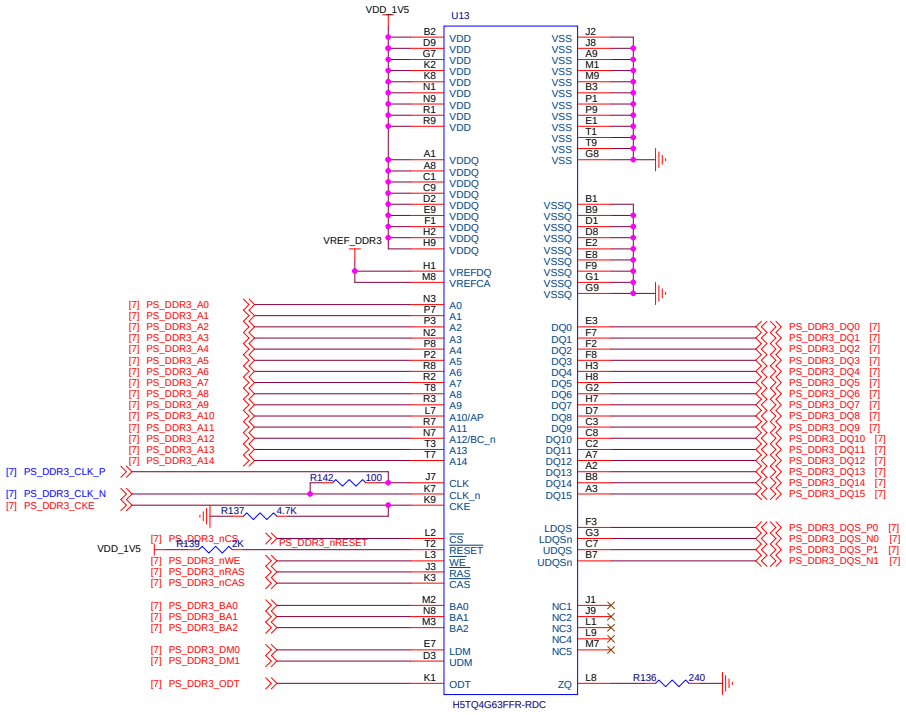


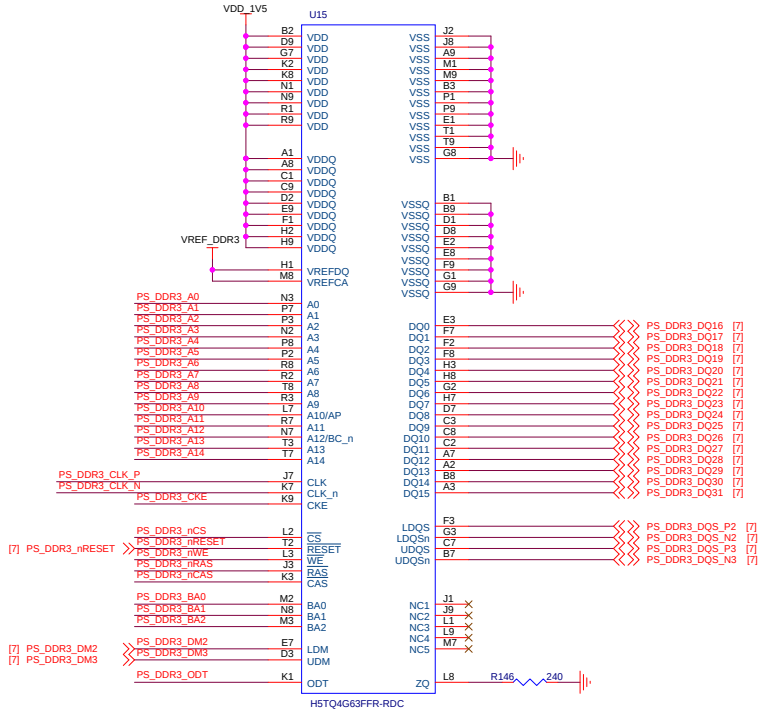
POWER_VTT&REF



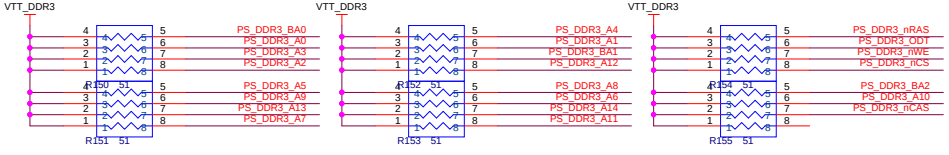
MicroPhase		
Title: ZYNQ7010 DDR INTERFACE		
Size	Document Number: MicroZee Schematic	Rev: 1.2
Date: Thursday, December 21, 2017	Sheet 7 of 17	

PS_DDR3

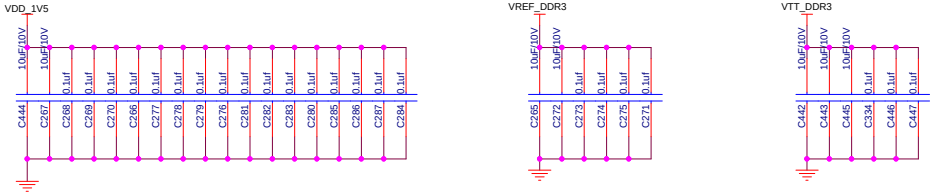




ODT

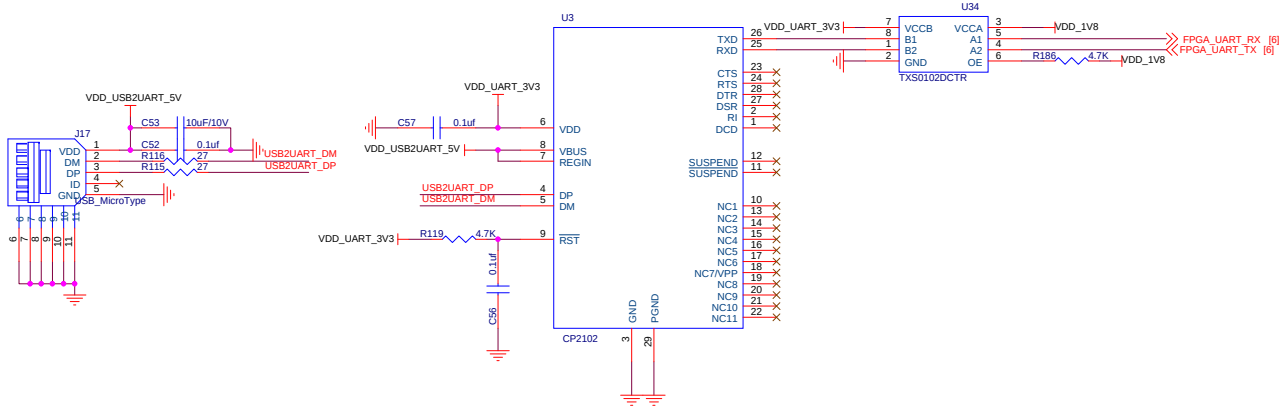


Discouple



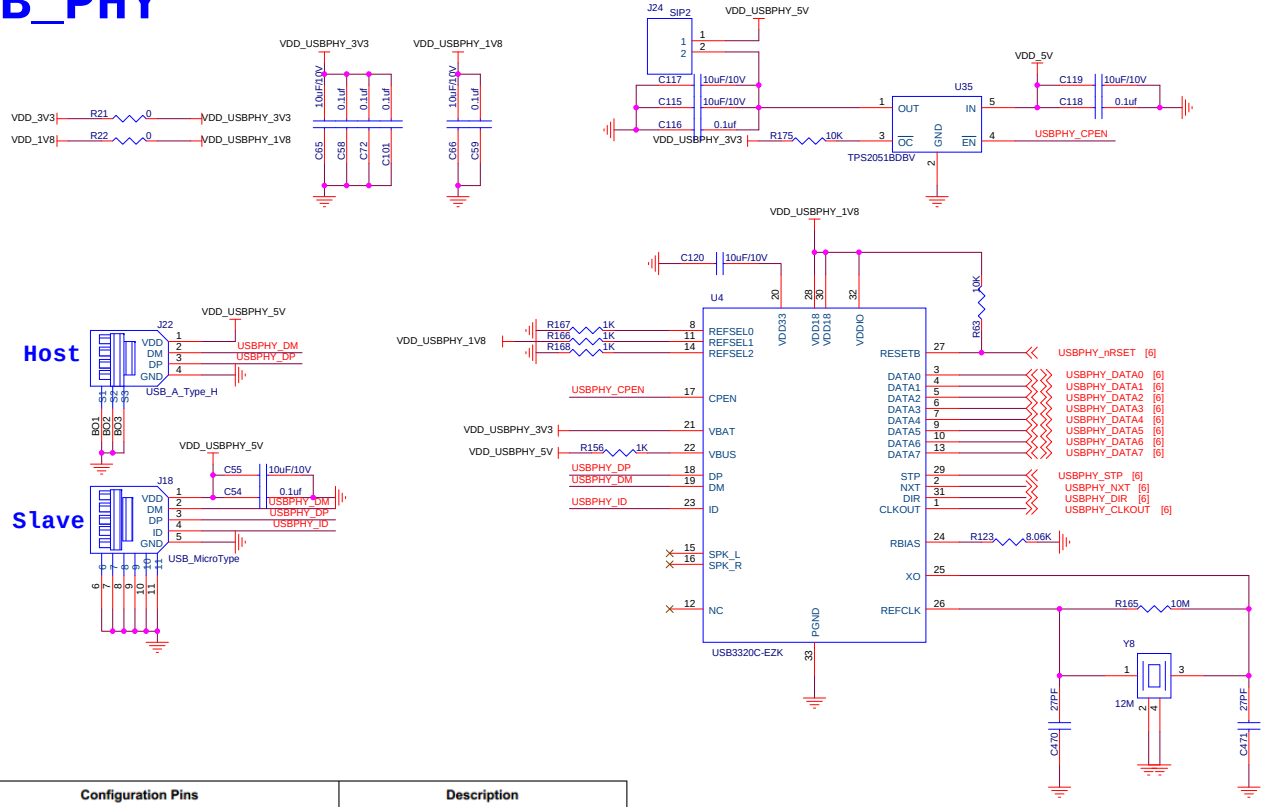
MicroPhase		
Title: ZYNQ7010 DDR		
Size	Document Number: MicroZee Schematic	Rev: 1.2
Date: Thursday, December 21, 2017	Sheet 8 of 17	

USB2UART



Title	ZYNQ7010 USB2UART		
Size	Document Number MicroZee Schematic		Rev 1.2
Date: Thursday, December 21, 2017	Sheet 9 of 17		

USB_PHY



Configuration Pins			Description
REFSEL[2]	REFSEL[1]	REFSEL[0]	Reference Frequency
0	0	0	52 MHz
0	0	1	38.4 MHz
0	1	0	12 MHz
0	1	1	27 MHz
1	0	0	13 MHz
1	0	1	19.2 MHz
1	1	0	26 MHz
1	1	1	24 MHz

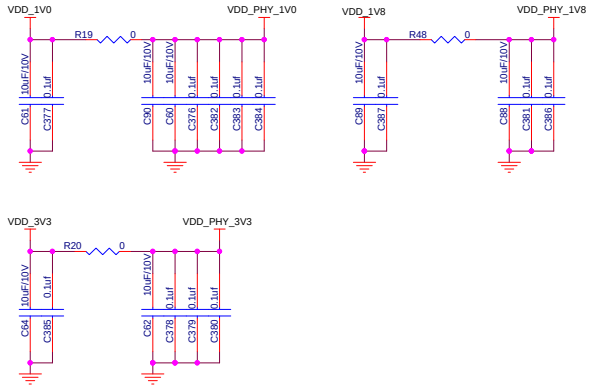
MicroPhase

Title: ZYNQ7010 USB_PHY

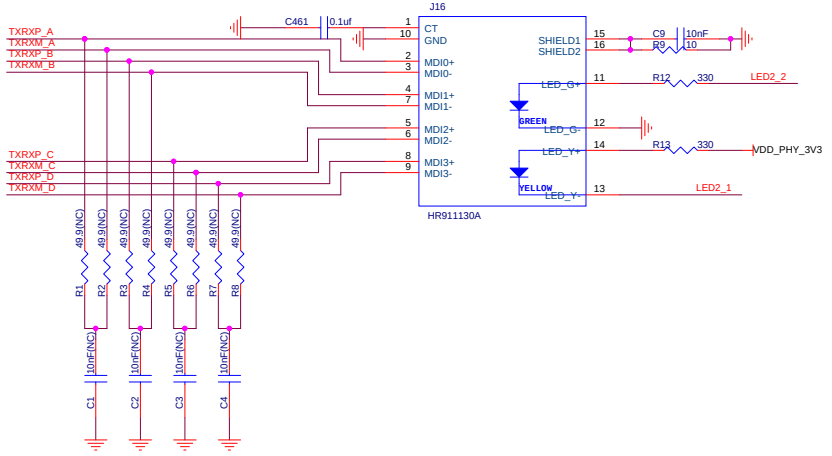
Size | Document Number: MicroZee Schematic | Rev: 1.2

Date: Thursday, December 21, 2017 | Sheet 10 of 17

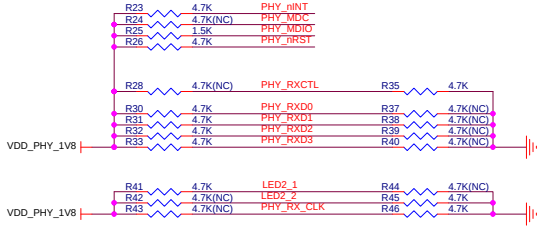
PHY POWER



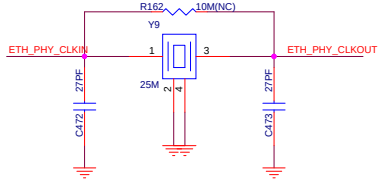
RJ45



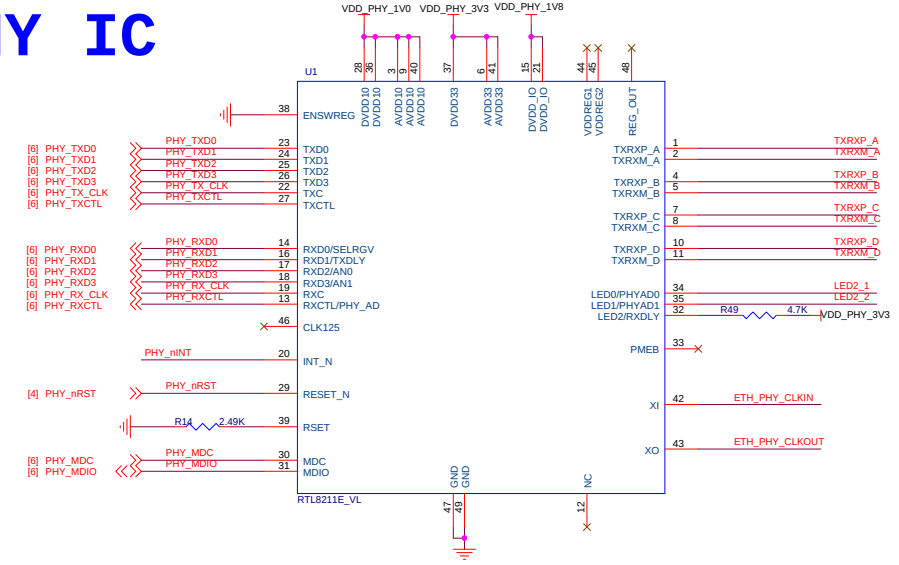
PHY CONFIG



PHY CLK

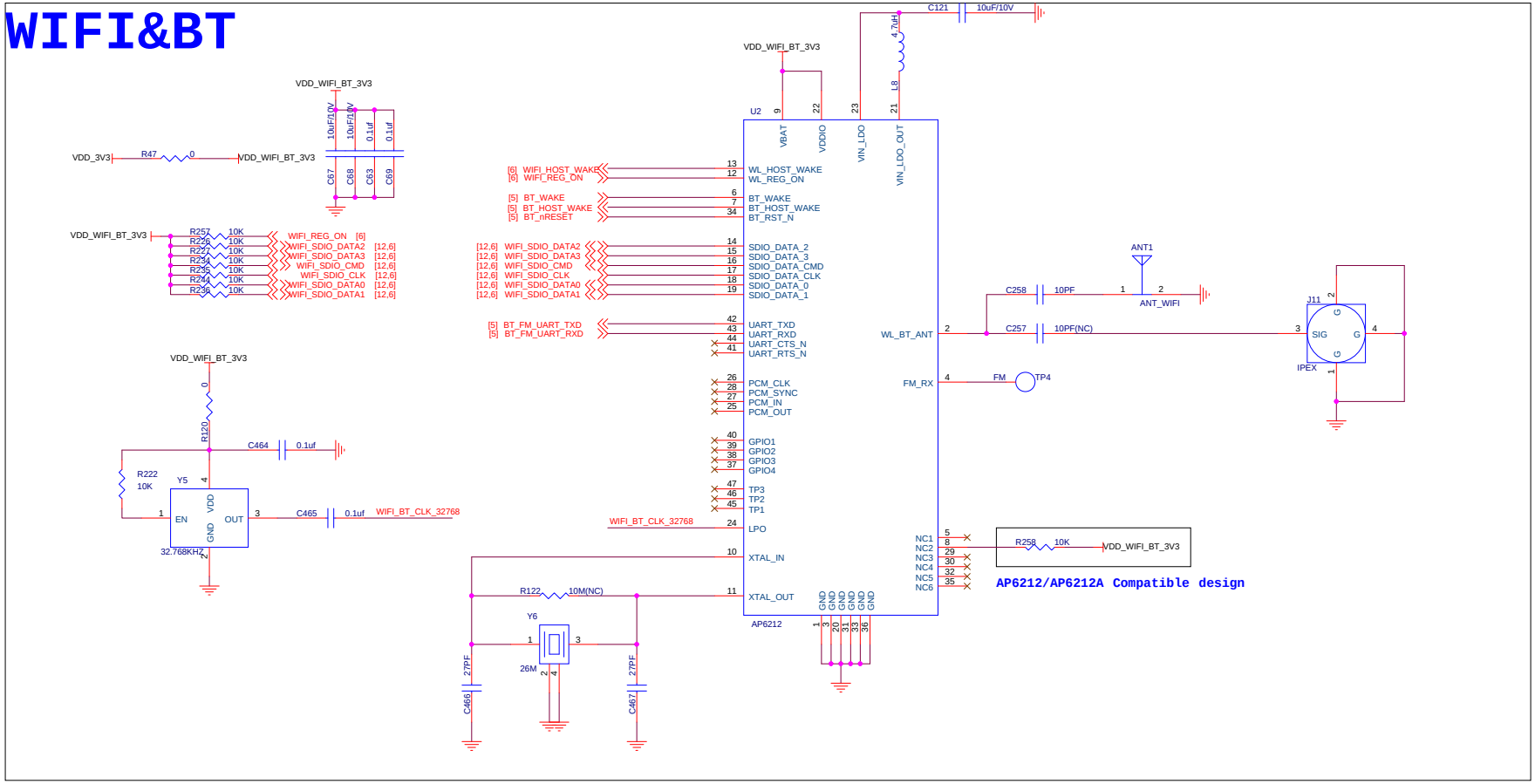


PHY IC



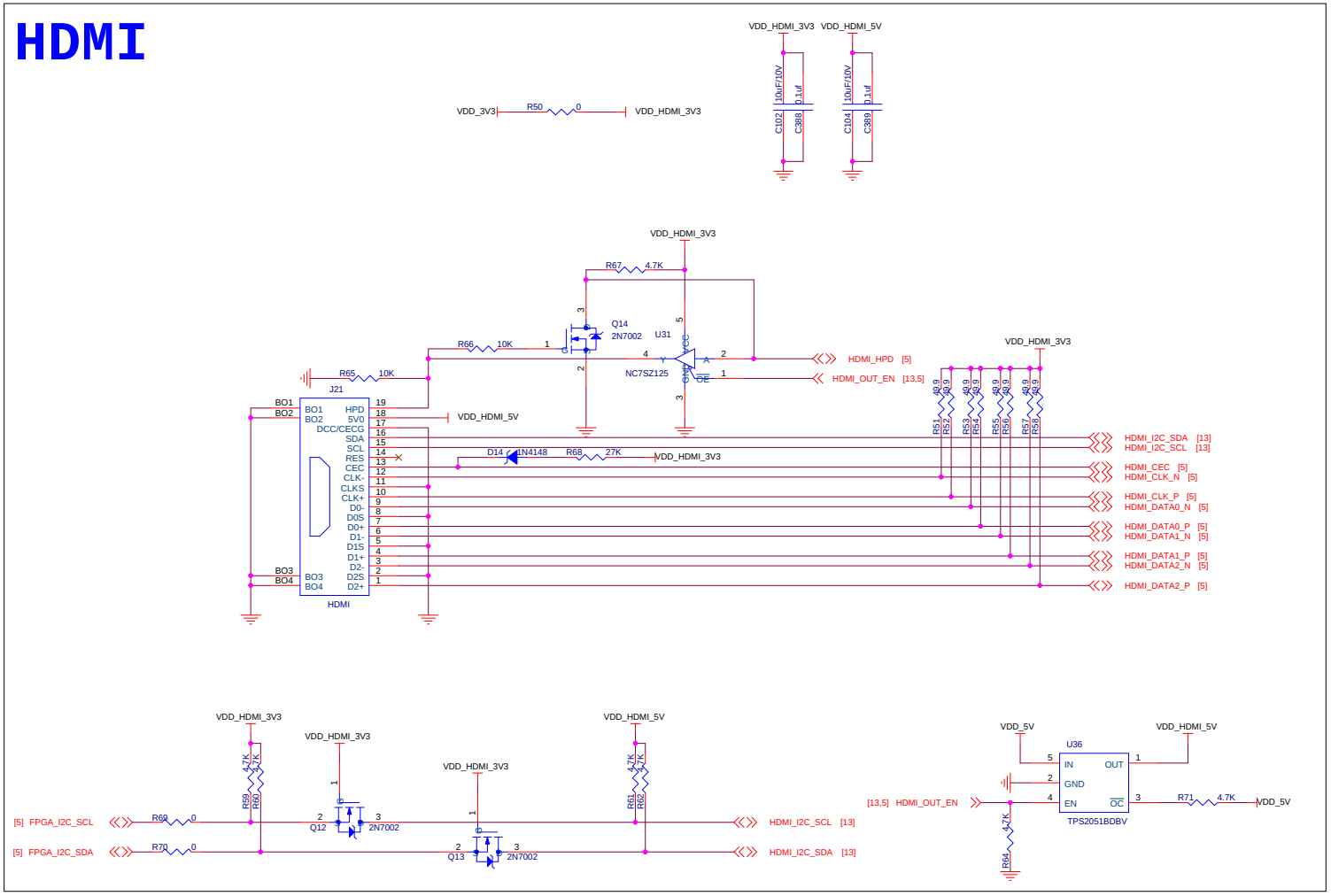
Title	ZYNQ7010 GPHY		
Size	Document Number MicroZee Schematic		Rev 1.2
Date: Thursday, December 21, 2017	Sheet 11 of 17		

WIFI&BT



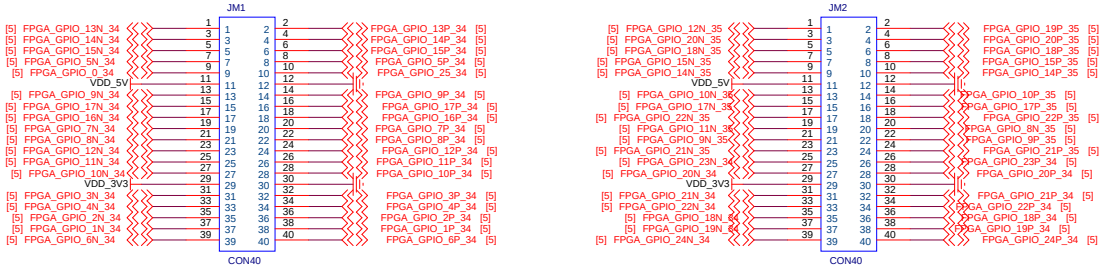
Title	ZYNQ7010 WIFI_BT		
Size	Document Number MicroZee Schematic		Rev 1.2
Date: Thursday, December 21, 2017	Sheet 12 of 17		

HDMI

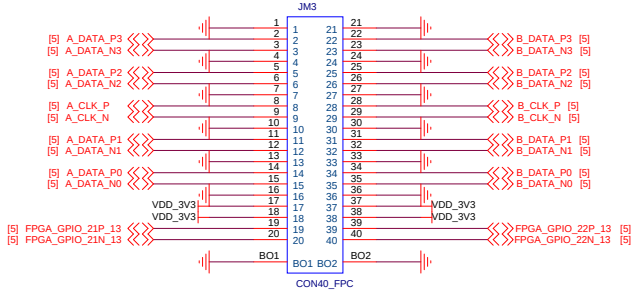


Title	ZYNQ7010 HDMI		
Size	Document Number MicroZee Schematic		Rev 1.2
Date: Thursday, December 21, 2017	Sheet 13 of 17		

DIP CONNECTOR

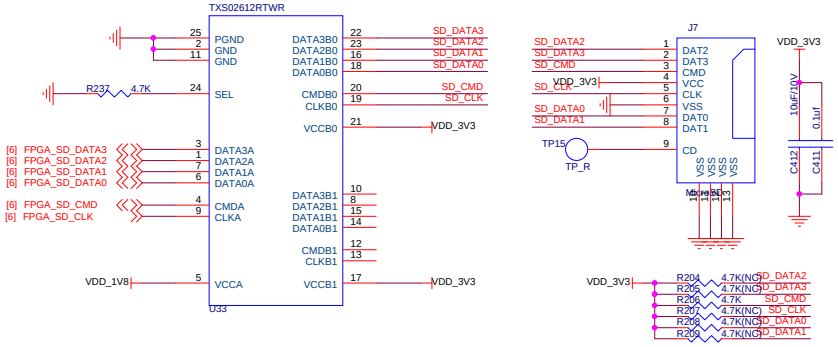


FPC CONNECTOR

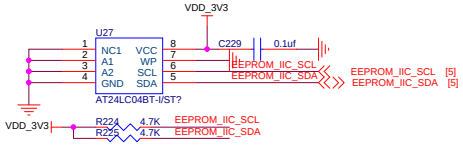


MicroPhase		
Title	ZYNQ7010 CONNECTOR	
Size	Document Number MicroZee Schematic	Rev 1.2
Date: Thursday, December 21, 2017	Sheet 14 of 17	

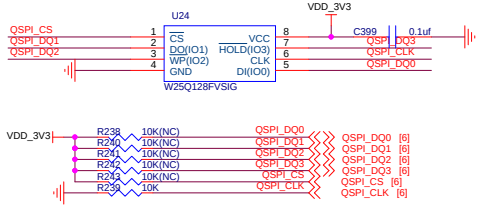
SD CARD



EEPROM

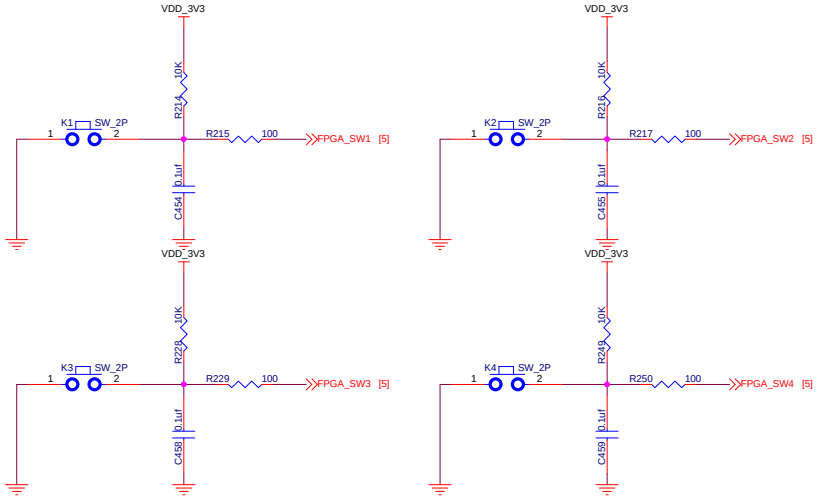


QSPI_FLASH

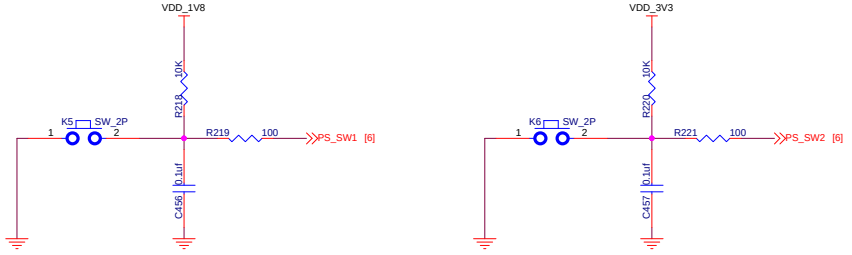


MicroPhase		
Title	ZYNQ7010 EEPROM&QSPI_FLASH&SD	
Size	Document Number MicroZee Schematic	Rev 1.2
Date: Thursday, December 21, 2017	Sheet 15 of 17	

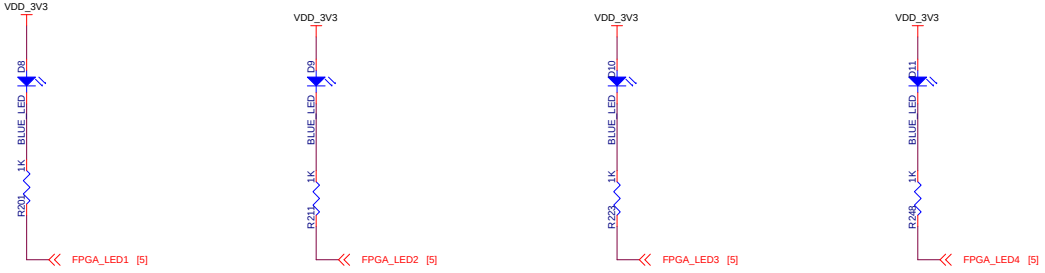
KEY_FPGA



LED_ARM



LED_FPGA

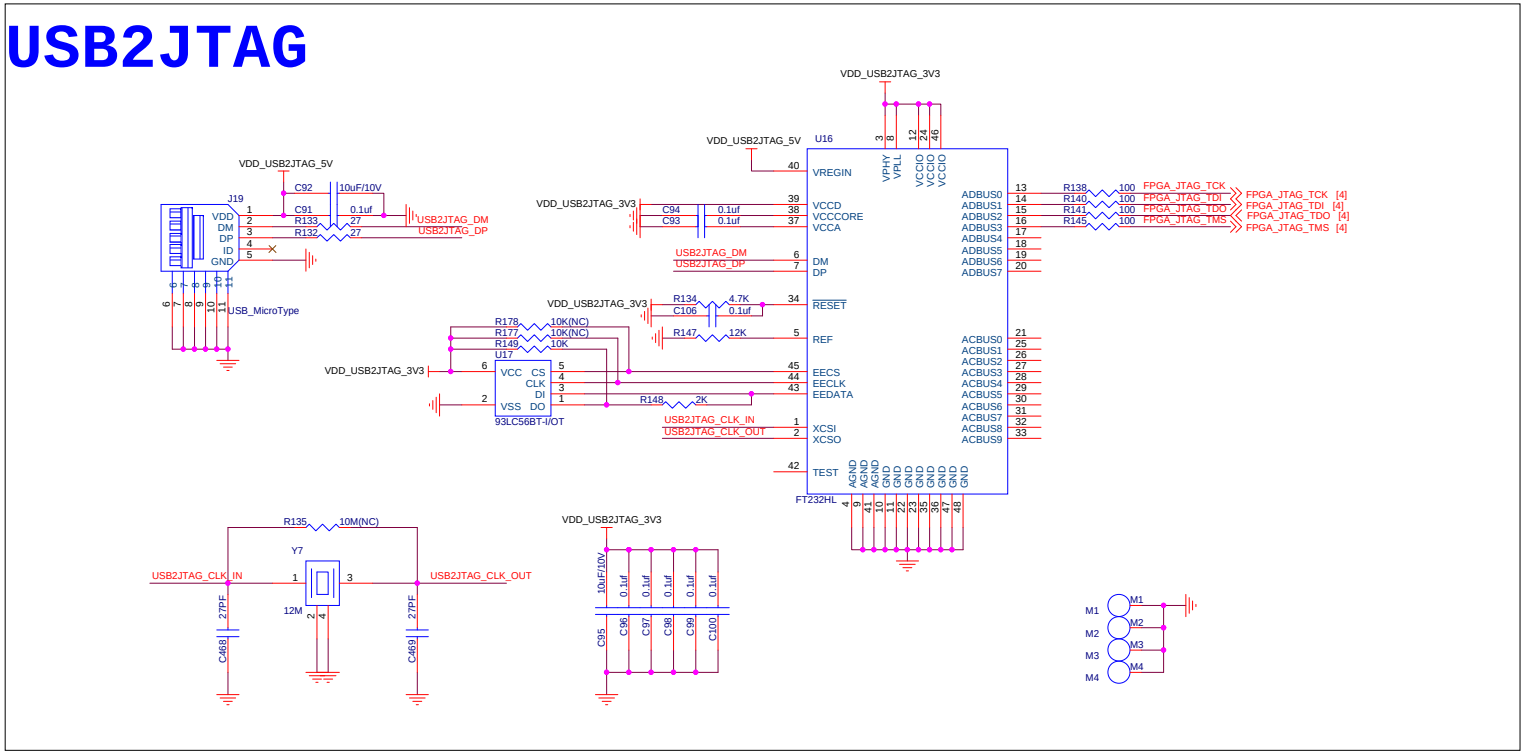


KEY_ARM

MicroPhase

Title	ZYNQ7010 KEY&LED	
Size	Document Number MicroZee Schematic	Rev 1.2
Date: Thursday, December 21, 2017	Sheet 16 of 17	

USB2JTAG



MicroPhase		
Title	ZYNQ7010 USB2JTAG	
Size	Document Number: MicroZee Schematic	Rev: 1.2
Date: Thursday, December 21, 2017	Sheet 17 of 17	