


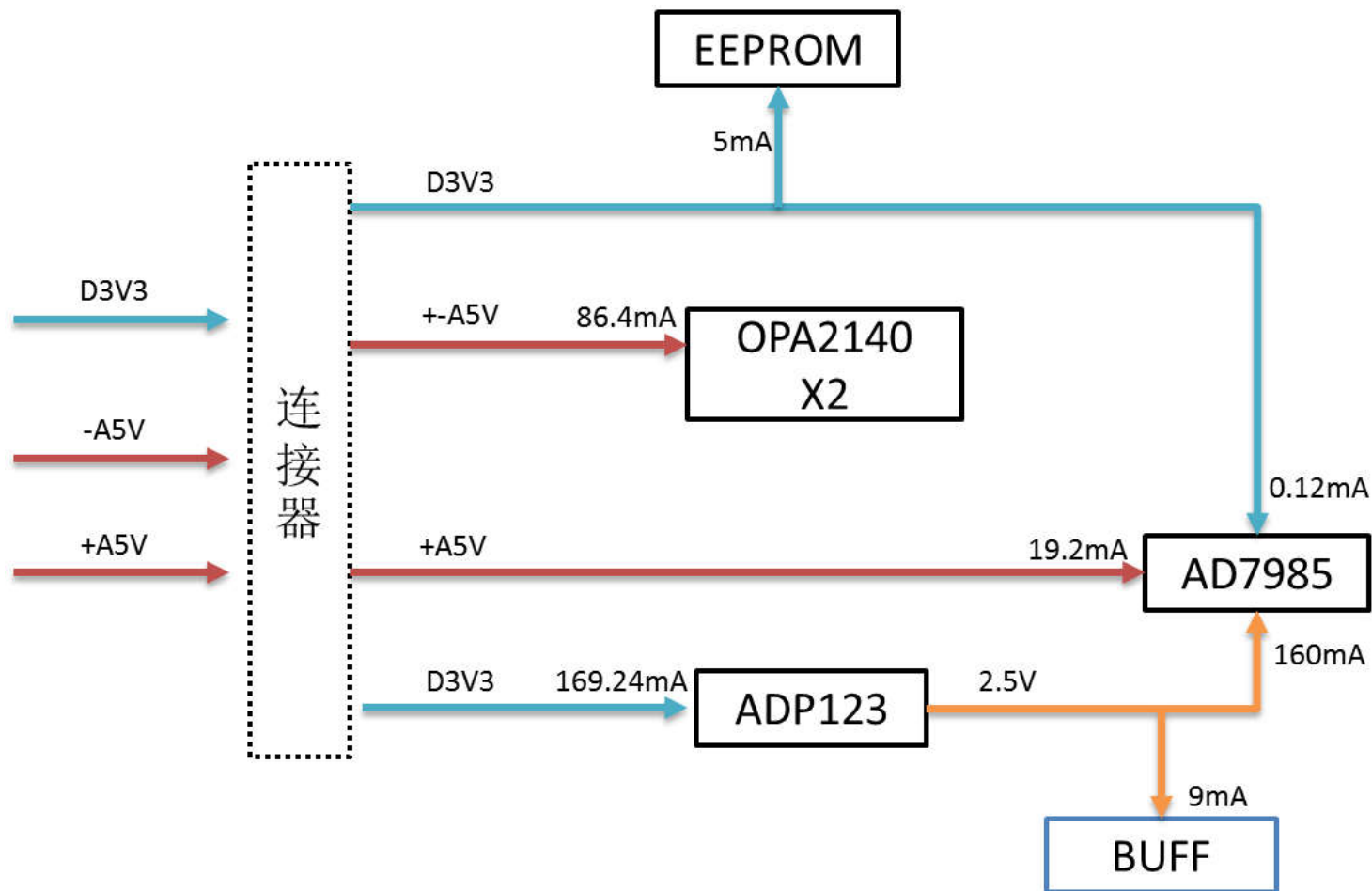
# GT1811-HAC4.0 (Analog ADC Daughter Board )


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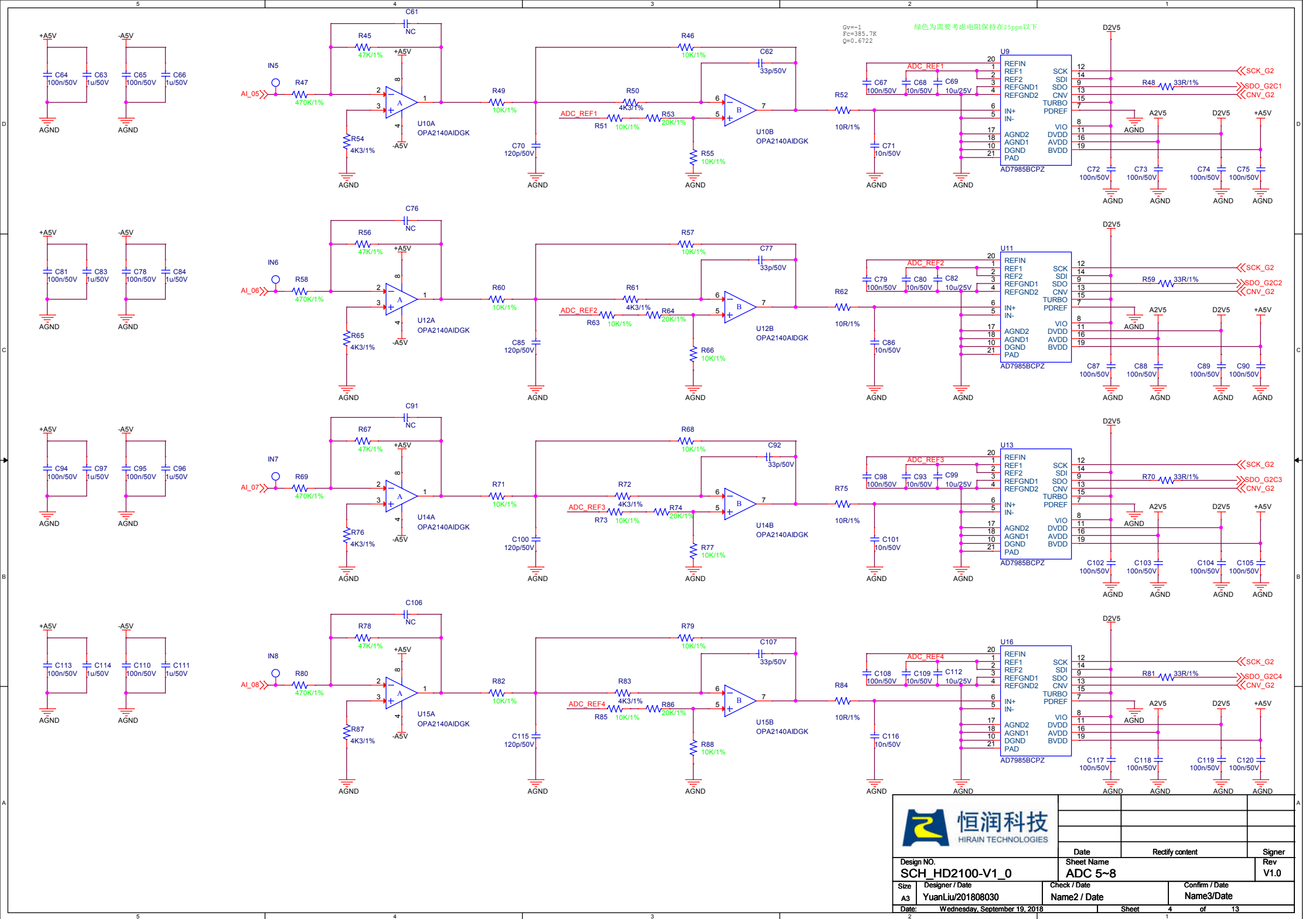
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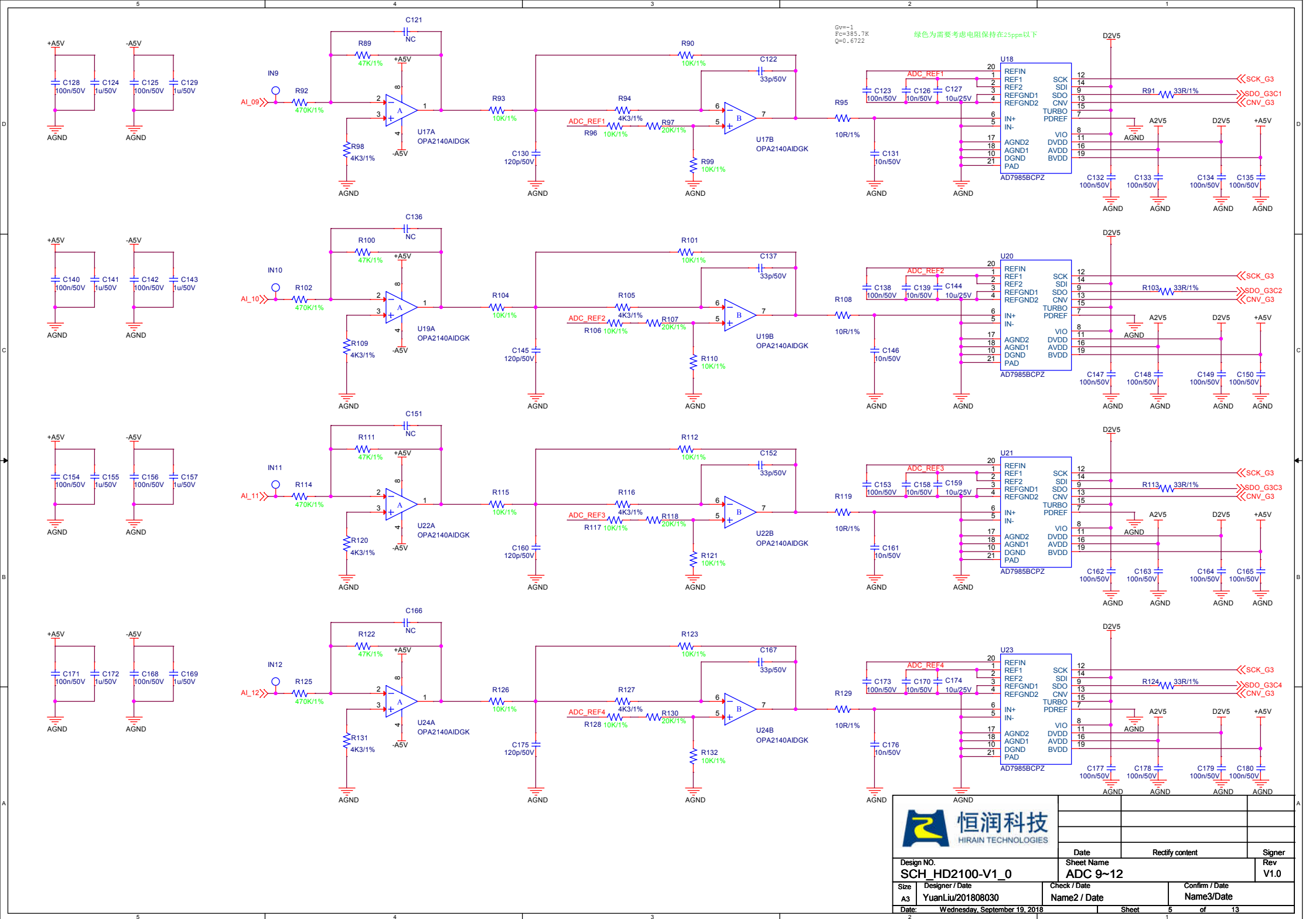
 恒润科技 HIRAIN TECHNOLOGIES				
Design NO. SCH_HD2100-V1_0		Sheet Name Cover Sheet		Rev V1.0
Size A3	Designer / Date YuanLiu/201808030	Check / Date Name2 / Date		Confirm / Date Name3/Date
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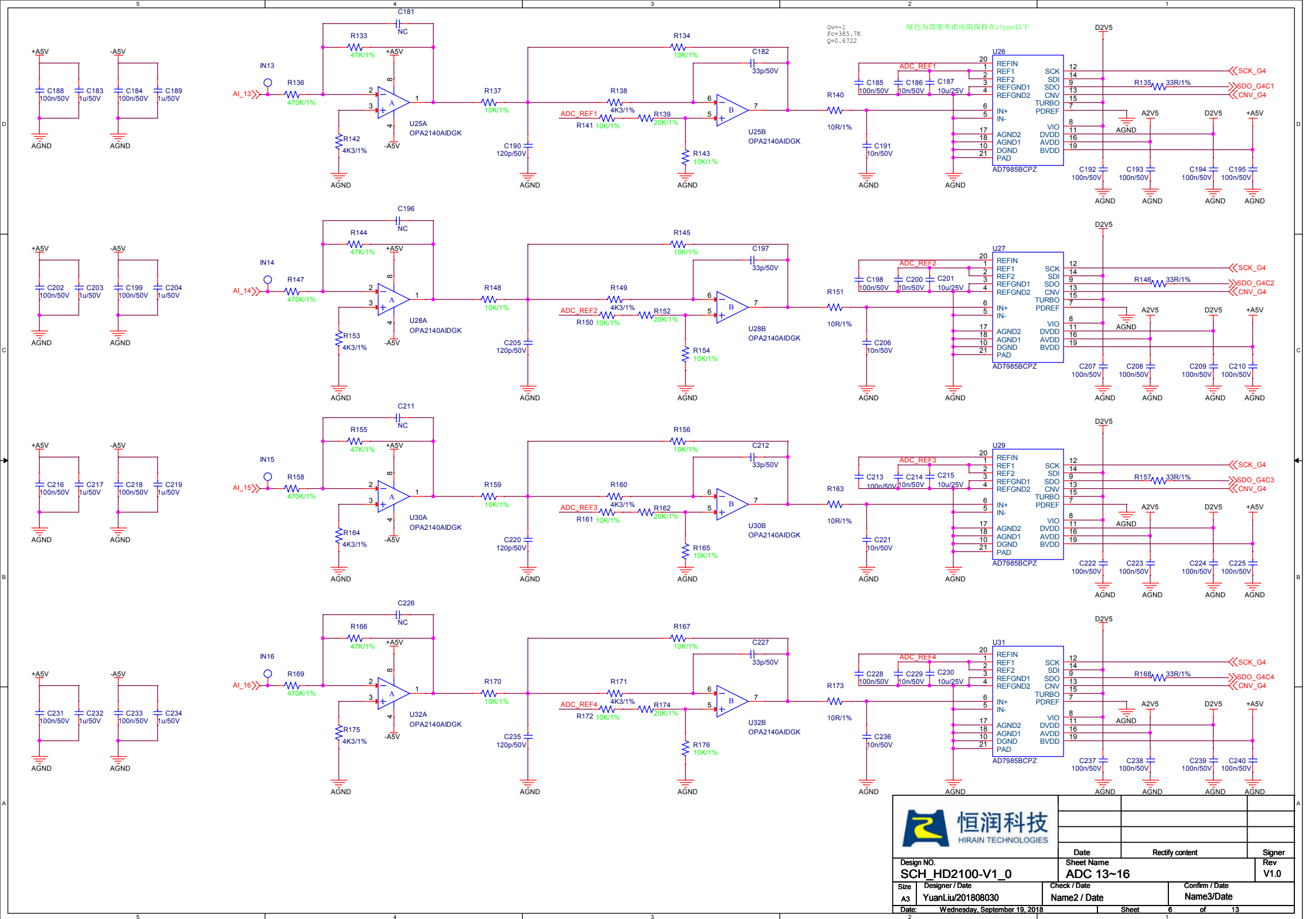


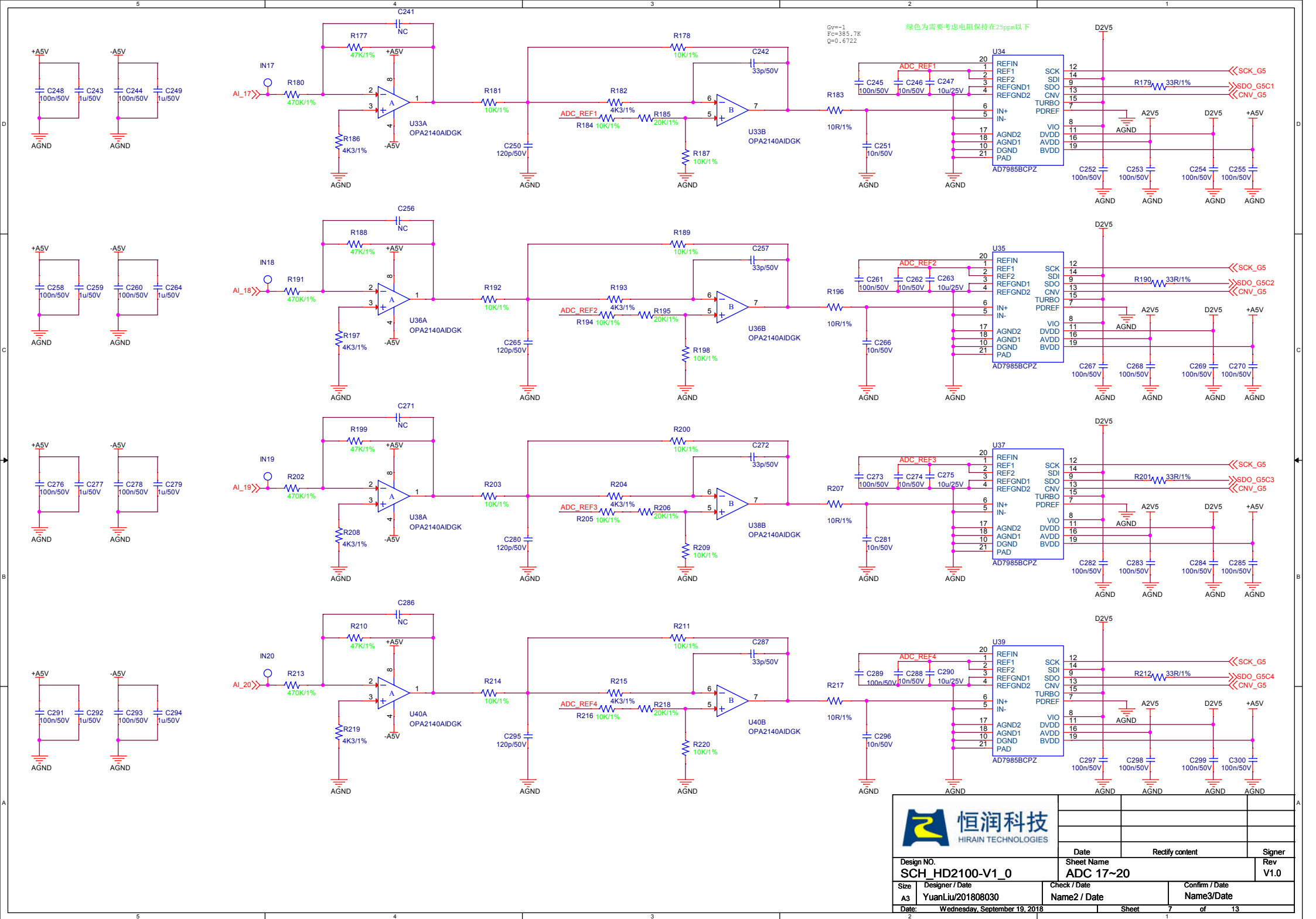
				
Design NO.		Date		Signer
SCH_HD2100-V1_0		Rectify content		Rev
Sheet Name		Name2 / Date		Name3 / Date
ADC_Block_Diagram				
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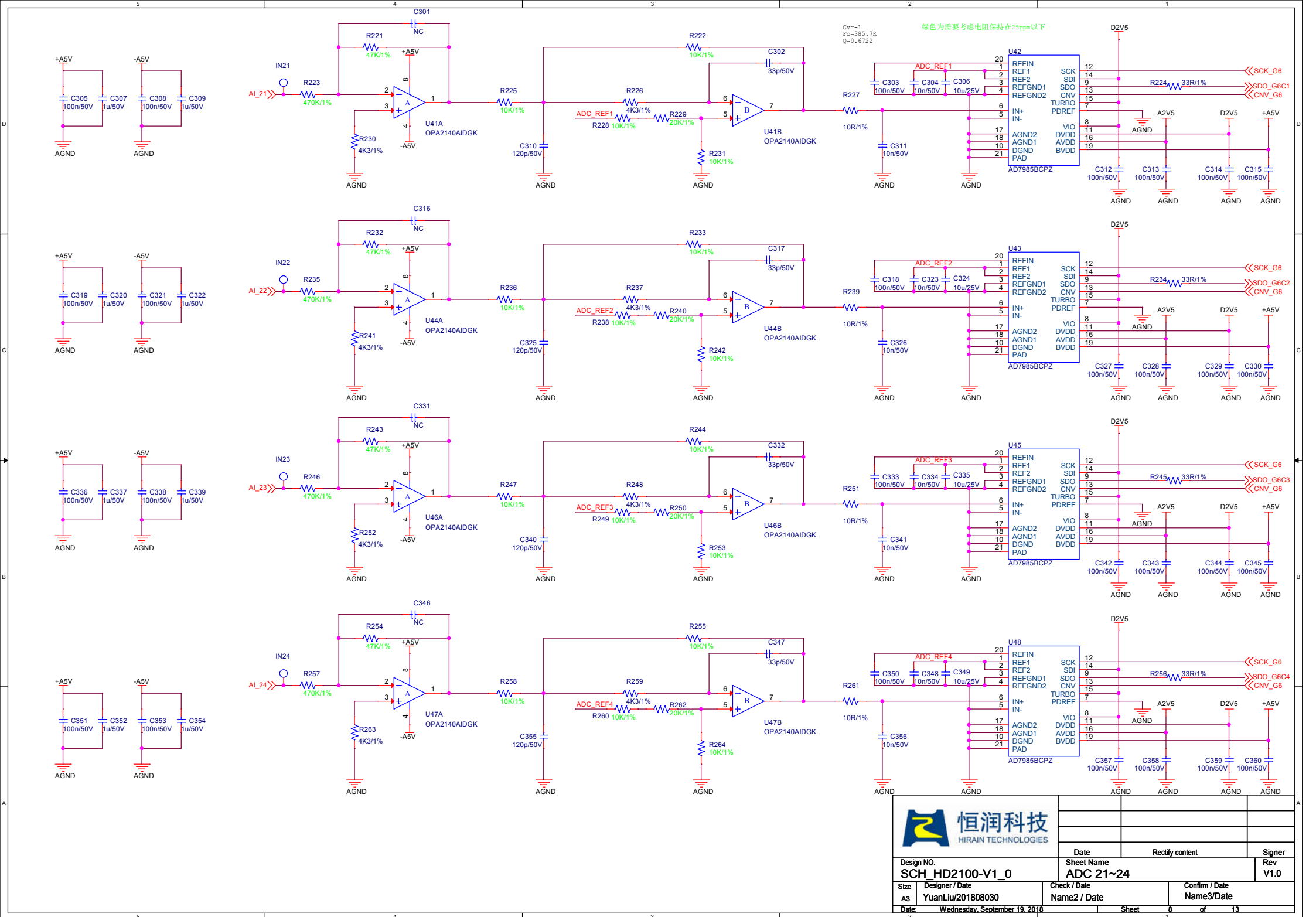




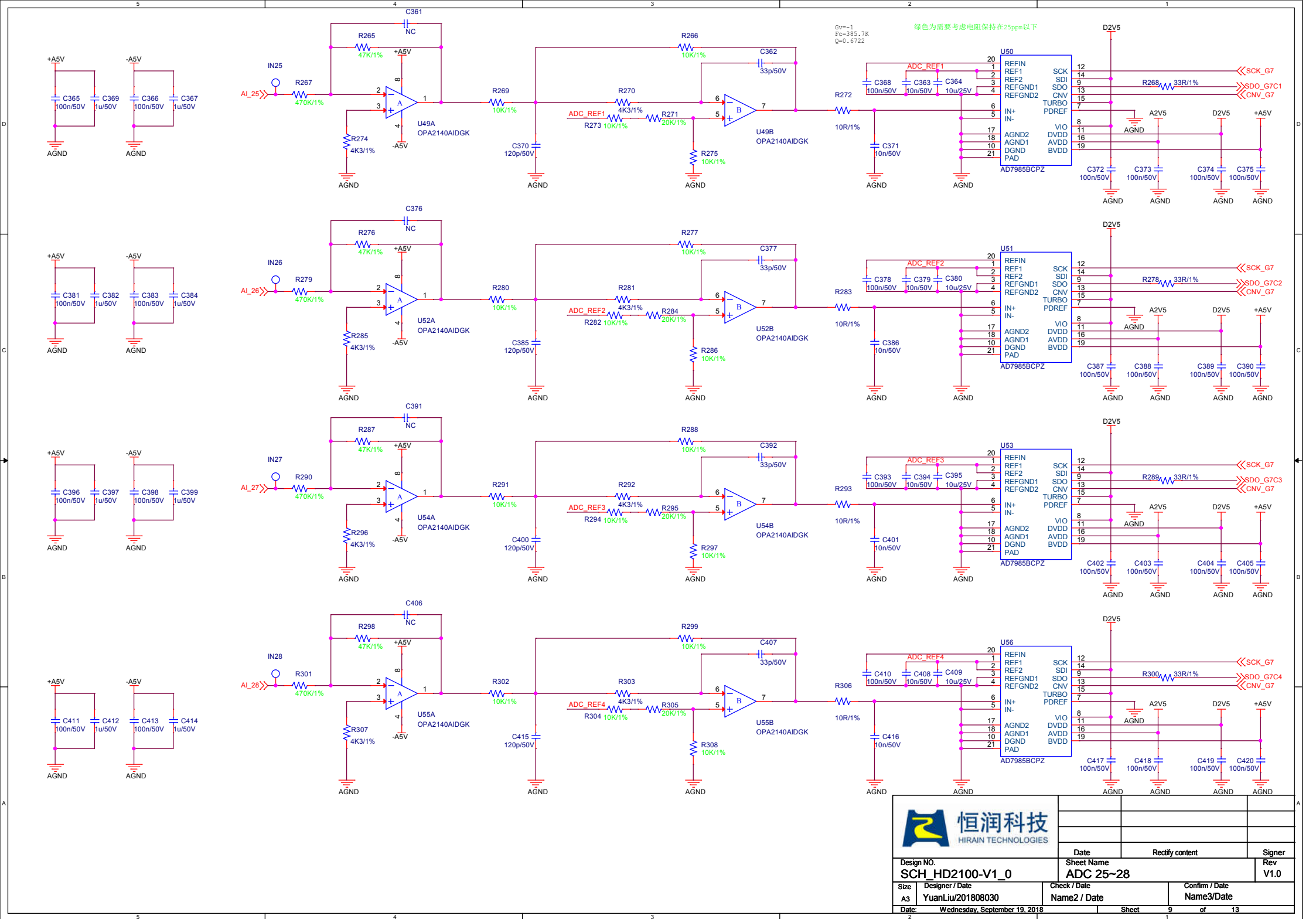




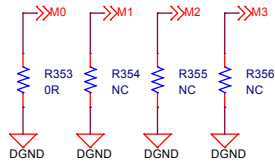
Design NO. SCH_HD2100-V1_0		Sheet Name ADC 17~20		Signer Rev V1.0
Size A3	Designer / Date YuanLiu/201808030	Check / Date Name2 / Date	Confirm / Date Name3/Date	
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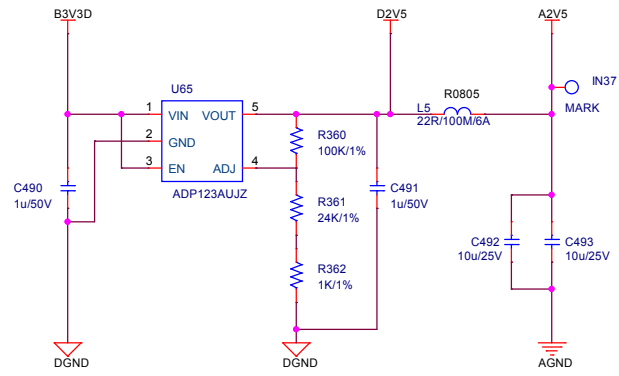
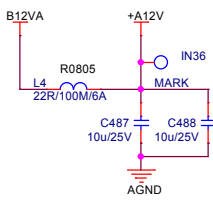
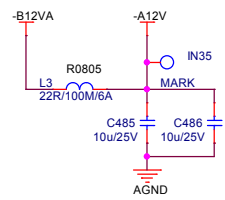
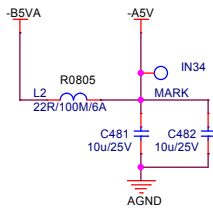
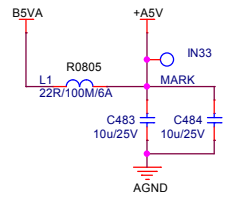




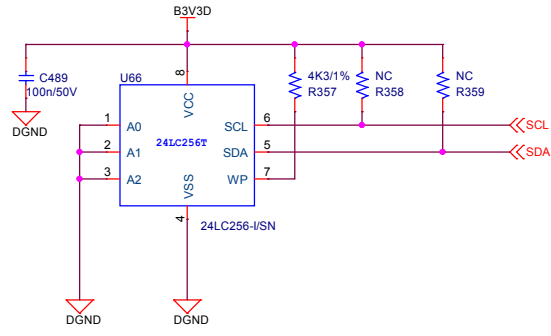





M0	悬空表示没有子板，低电平表示有子板
M1	悬空表示AI、AO子板，低电平表示DIO子板
M2	悬空表示AI子板，低电平表示AO子板
M3	悬空表示I6bit，低电平表示I4bit



$V_{out} = 0.5(1 + R1/R2)$   
 $= 0.5(1 + 100K/25K)$   
 worst condition:  
 $R1 = 101K, R2 = 24750$   
 $V_{out} = 0.5075(1 + 101K/24750)$   
 $V_{out} = 2.5785V$



				
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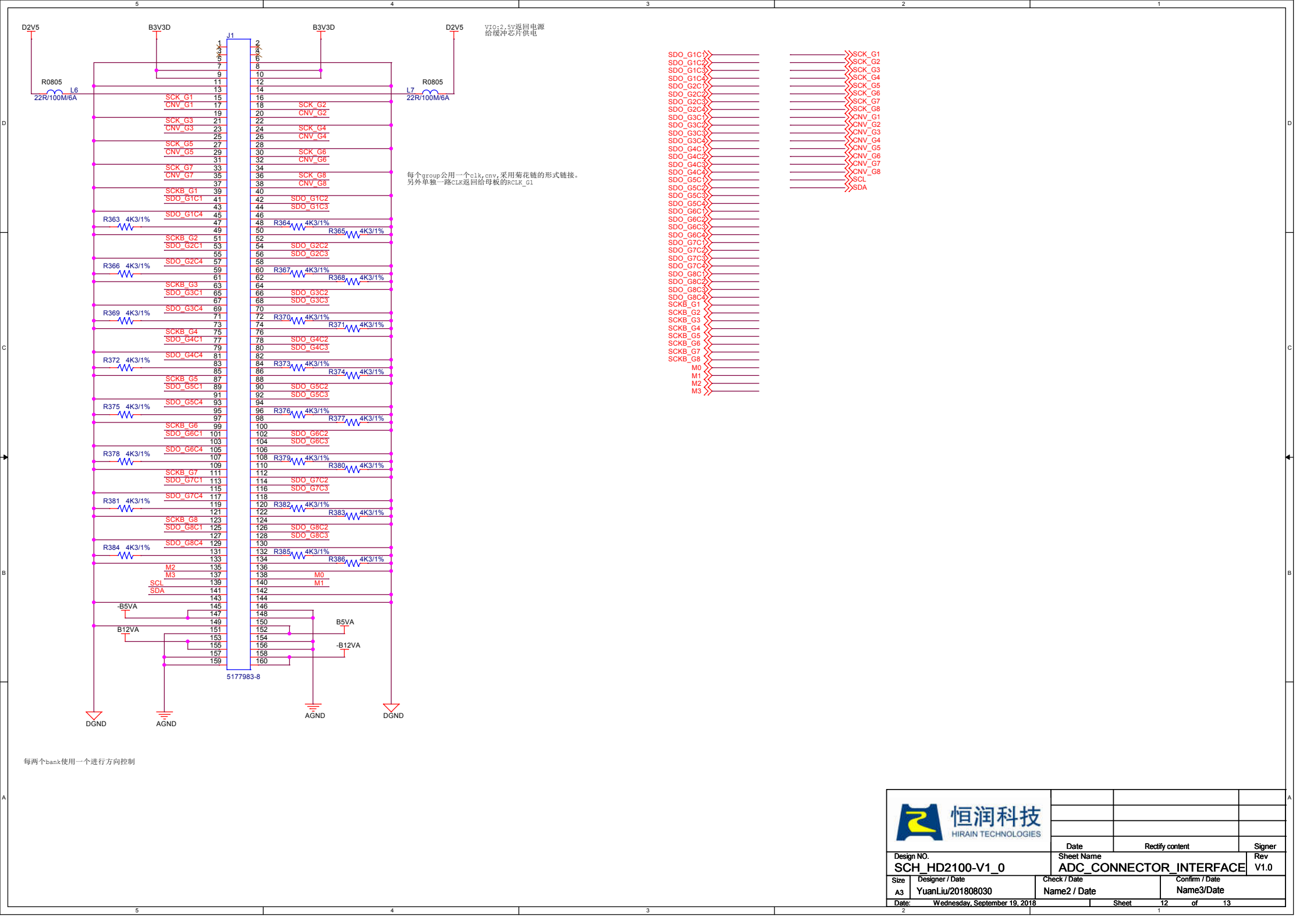



Figure 1 shows the pin connections for the P1A and P1B headers. The headers are 40-pin connectors. The P1A header pins are labeled AI\_01 to AI\_20 on the left and AI\_21 to AI\_40 on the right. The P1B header pins are labeled AI\_41 to AI\_60 on the left and AI\_61 to AI\_80 on the right. The headers are connected to a 40-pin connector labeled VHCI-68-F-D\_90D. The connector pins are labeled B1 to B40. The headers are connected to GND\_EARTH and AGND.

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Design NO.		Date		Rectify content		Signer
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A3	YuanLiu/201808030	Name2 / Date		Name3/Date		
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