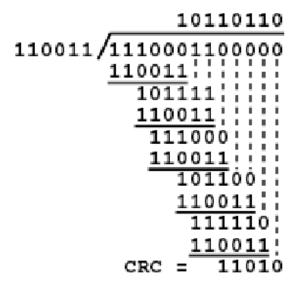
## Problem 6.8

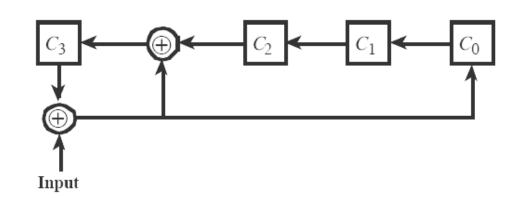
The receiver won't detect the error as an even parity check bit only detects inversion of odd number of bits.

# Problem 6.13



## Problem 6.14





$$M(X) = 1 + X^3 + X^4 + X^6 + X^7 + X^8$$

$$X^{4} * M(X) = X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{4}$$

$$\frac{X^4 * M(X)}{P(X)} = X^{12} + X^{11} + X^{10} + X^8 + X^7 + \frac{X^2}{P(X)}$$

$$R(X) = X^2$$

$$T(X) = X^{4} * M(X) + R(X) = X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{4} + X^{2}$$

Code = 0 0 1 0 1 0 0 1 1 0 1 1 1 0 0

c. Code = 0 0 1 0 1 0 0 0 1 0 1 1 1 0 0

$$\frac{T(X)}{P(X)}$$
 yields a nonzero remainder

## Problem 6.15

- **a.** Divide  $X^{10} + X^7 + X^4 + X^3 + X + 1$  by  $X^4 + X + 1$ . The remainder is  $X^3 + X^2$ . The CRC bits are **1100**. The string **100100110111100** is sent.
- **b.** The string **000110110111100** is received, corresponding to  $X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^3 + X^2$ . The remainder after division by  $X^4 + X + 1$  is  $X^3 + X^2 + X$ , which is nonzero. The errors are detected.
- **c.** The string **000010110111100** is received, corresponding to  $X^{10} + X^8 + X^7 + X^5 + X^4 + X^3 + X^2$ . The remainder after division by  $X^4 + X + 1$  is zero. The errors are not detected.

## Problem 6.16

- **a.** The multiplication of D(X) by  $X^{16}$  corresponds to shifting D(X) 16 places and thus providing the space for a 16-bit FCS. The addition of  $X^K * L(X)$  to  $X^{16} * D(X)$  inverts the first 16 bits of D(X) (ones complement). The addition of L(X) to R(X) inverts all of the bits of R(X).
- **b.** The HDLC standard provides the following explanation. The addition of  $X^K$  \* L(X) corresponds to a value of all ones. This addition protects against the obliteration of leading flags, which may be non-detectable if the initial remainder is zero. The addition of L(X) to R(X) ensures that the received, errorfree message will result in a unique, non-zero remainder at the receiver. The non-zero

remainder protects against the potential non-detectability of the obliteration of trailing flags.

**c.** The implementation is as shown in the below figure, with following strategy. At both transmitter and receiver, the initial content of the register is preset to all ones. The final remainder, if there are no errors, will be **0001 1101 0000 1111**.

