

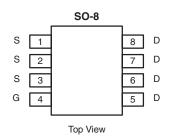
P-Channel 1.8-V (G-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^b	Q _g (Typ.)	
	0.009 at $V_{GS} = -4.5 \text{ V}$	- 13.7		
- 8	0.011 at V _{GS} = - 2.5 V	- 12.4	55 nC	
	0.016 at V _{GS} = - 1.8 V	- 10		

FEATURES

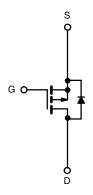
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET
- 1.8 V Rated
- 100 % R_g Tested





Ordering Information: Si4465ADY-T1-E3 (Lead (Pb)-free)

Si4465ADY-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	T _A = 25 °C, unles	ss otherwise r	noted		
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V _{DS}	- 8	V		
Gate-Source Voltage	V_{GS}	± 8	V		
	T _A = 25 °C	I _D	- 13.7		
Continuous Drain Current (T _{.I} = 150 °C) ^{a, b}	T _A = 70 °C		- 11		
Continuous Drain Current (1 _J = 150 °C) ^{4, 2}	T _C = 25 °C		- 20		
	T _C = 70 °C		- 16	Α	
Pulsed Drain Current		I _{DM}	- 40		
Continuous Source Current (Diode Conduction) ^{a, b}		I _S	- 2.5		
		I _{SM}	40	1	
	T _A = 25 °C		3.0	W	
Mariana Bana Biraina in a h	T _A = 70 °C	P _D	1.95		
Maximum Power Dissipation ^{a, b}	T _C = 25 °C		6.5	VV	
	T _C = 70 °C		4.2		
Operating Junction and Storage Temperature Ran	T _J , T _{stg}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Manifestory Investigation to Ambient (MOCEFT)	t ≤ 10 s	R _{thJA}	34	41	°C/W
Maximum Junction-to-Ambient (MOSFET) ^a	Steady State		67	80	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	15	19	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. $t \le 10 \text{ s}$.

Si4465ADY

Vishay Siliconix



SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static				•			
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 0.45		- 1.0	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
Zara Cata Valtaga Drain Current	_	V _{DS} = -8 V, V _{GS} = 0 V V _{DS} = -8 V, V _{GS} = 0 V, T _J = 55 °C			- 1	μΑ	
Zero Gate Voltage Drain Current	I _{DSS}				- 5		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	- 20			Α	
		$V_{GS} = -4.5 \text{ V}, I_D = -14 \text{ A}$		0.0075	0.009		
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = -2.5 \text{ V}, I_D = -12 \text{ A}$		0.0092	0.011	Ω	
		$V_{GS} = 1.8 \text{ V}, I_D = 10 \text{ A}$		0.013	0.016		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 14 A		58		S	
Diode Forward Voltage ^a	V_{SD}	I _S = - 2.1 A, V _{GS} = 0 V		- 0.57	- 1.2	V	
Dynamic ^b			'	•		l	
Total Gate Charge	Q_g			55	85		
Gate-Source Charge	Q_{gs}	$V_{DS} = -4 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -14 \text{ A}$		6		nC	
Gate-Drain Charge	Q_{gd}			10			
Gate Resistance	R_{g}			2.5	3.8	Ω	
Turn-On Delay Time	t _{d(on)}			33	50		
Rise Time	t _r	V_{DD} = - 4 V, R_L = 4 Ω		170	255		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ - 10 A, V_{GEN} = - 4.5 V, R_g = 6 Ω		168	255	ns	
Fall Time	t _f			112	170		
Source-Drain Reverse Recovery Time t _{rr}		I _F = - 2.1 A, dl/dt = 100 A/μs		85	130		
Body Diode Reverse Recovery Charge	Q _{rr}	1μ = - 2.1 π, αι/αι = 100 π/μδ		81	125	nC	

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

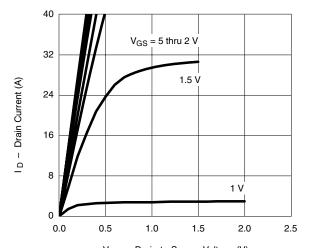
a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$

b. Guaranteed by design, not subject to production testing.



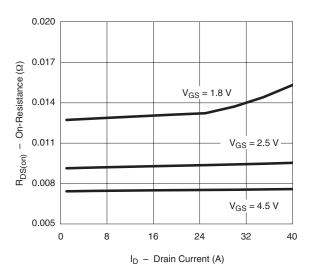


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

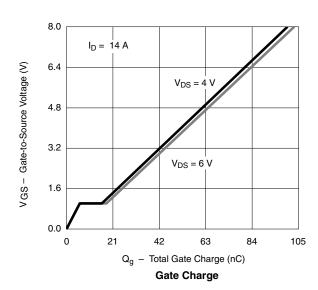


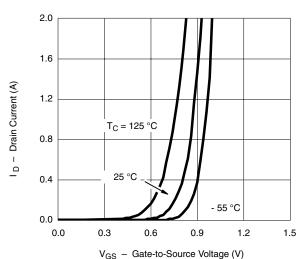
V_{DS} - Drain-to-Source Voltage (V)

Output Characteristics



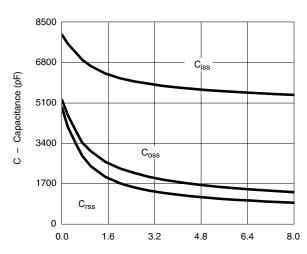
On-Resistance vs. Drain Current





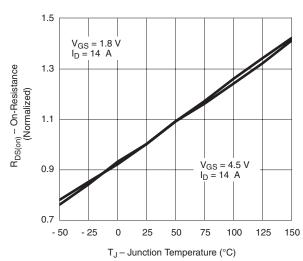
VGS date to bounce voltage (V)





 $V_{DS}\,-\,$ Drain-to-Source Voltage (V)

Capacitance

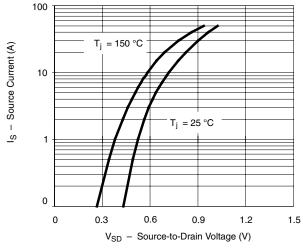


On-Resistance vs. Junction Temperature

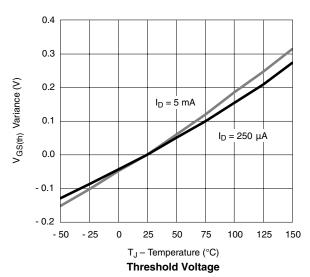
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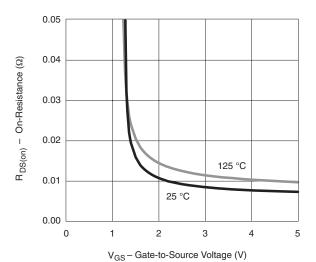
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

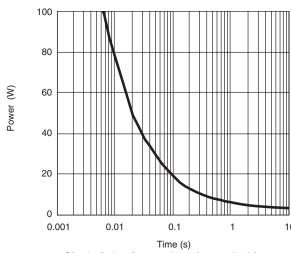


Source-Drain Diode Forward Voltage

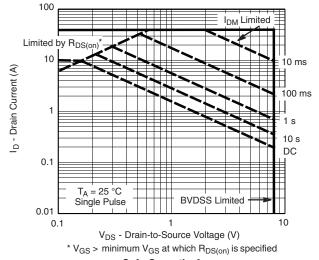




On-Resistance vs. Gate-to-Source Voltage

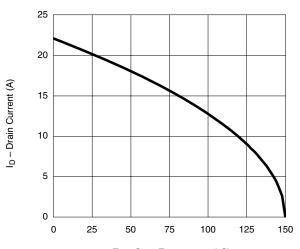


Single Pulse Power, Junction-to-Ambient



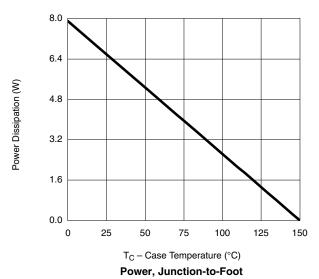


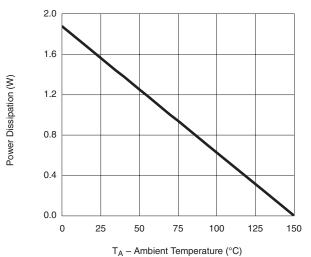
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



T_C – Case Temperature (°C)

Current Derating





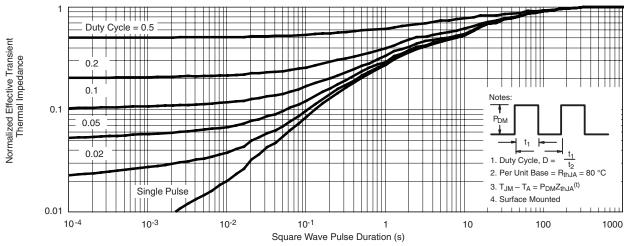
Power, Junction-to-Ambient

^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

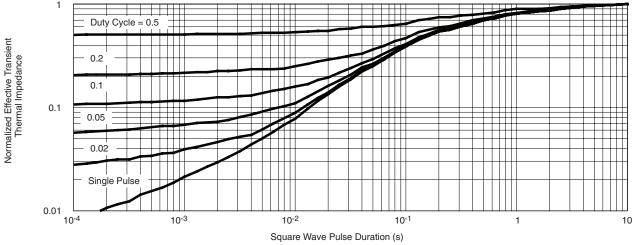
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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