FlashFlex51 MCU
SST89C54 / SST89C58 / SST89C59

Preliminary Specifications

FEATURES:

- **Multi-Purpose 8-bit 8051 Compatible Microcontroller Unit with Embedded SuperFlash Memory for Flexibility**
- **Fully Software and Development Toolset Compatible as well as Pin-For-Pin Package Compatible to Standard 8xC5x Microcontrollers**
- **256 Bytes Register/Data RAM**
- **20/36/64 KByte Embedded High Performance Flexible SuperFlash EEPROM**
  - One 16/32/60 KByte block (128-byte sector size)
  - One 4 KByte block (64-byte sector size)
  - Individual Block Security Lock
  - 87C5x Programmer Compatible
  - Master In-System Programming (ISP) Mode
  - Concurrently Programmable
- **Support External Address Range up to 64 KByte of Program and Data Memory**
- **High Current Drive on Port 1 (5, 6, 7) pins**
- **Three 16-bit Timer/Counter**
- **Programmable Serial Port (UART)**
- **Six Interrupt Sources at 2 Priority Levels**
- **Selectable Watchdog Timer (WDT)**
- **Four 8-bit I/O Ports (32 I/O Pins)**
- **TTL- and CMOS-Compatible Logic Levels**
- **Extended Power-Saving Modes**
  - Idle Mode
  - Power Down Mode
  - Standby Mode
- **0 to 33 MHz Operation at 5 Volts Supply**
- **Low Voltage (3V) Operation (0 to 12 MHz)**
- **PDIP-40, PLCC-44 and TQFP-44 Packages**
- **Temperature Ranges:**
  - Standard (0°C to +70°C)
  - Industrial (-40°C to +85°C)

PRODUCT DESCRIPTION

SST89C54, SST89C58 and SST89C59 are members of the FlashFlex51 family of 8-bit microcontrollers. The FlashFlex51 family is a family of embedded microcontroller products designed and manufactured on the state-of-the-art SuperFlash CMOS semiconductor process technology.

As a member of the FlashFlex51 controller family, the SST89C54/58/59 uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with standard 8xC5x microcontroller devices.

SST89C54/58/59 comes with 20/36/64 KByte of integrated on-chip flash EEPROM program memory using the patented and proprietary Silicon Storage Technology, Inc. (SST) CMOS SuperFlash EEPROM technology with the SST field enhancing tunneling injector split-gate memory cells. The SuperFlash memory is partitioned into 2 independent program memory blocks. The lower 16/32/60 KByte SuperFlash block occupies the standard 8xC54/58/59's 16/32/60 KByte of internal ROM space and the upper 4 KByte SuperFlash block occupies the upper most of the 64 KByte address space for the 8xC5x architecture. The flash memory blocks can be programmed via a standard 87C5x OTP EPROM programmer or a standard flash EEPROM memory programmer fitted with a special adapter and firmware for SST89C54/58/59 devices. During the power-on reset, the SST89C54/58/59 can be configured as a master to a source code storage or as a slave to an external host for In-System-Programming (ISP) operation. SST89C54/58/59 is designed to be programmed "in-place" and "in-field" on the printed circuit board (PCB) assembly for maximum flexibility.

The highly reliable, patented SuperFlash technology and memory cell have a number of important advantages for designing and manufacturing flash EEPROMs, when compared with the thin oxide stacked gate or two transistor approaches. These advantages translate into significant cost and reliability benefits for our customers.

In addition to 20/36/64 KByte of SuperFlash EEPROM program memory on-chip, the SST89C54/58/59 can address up to 64 KByte of program memory external to the chip. The SST89C54/58/59 microcontrollers have 256 x 8 bits of on-chip RAM. Up to 64 KByte of external data memory (RAM) can be addressed.

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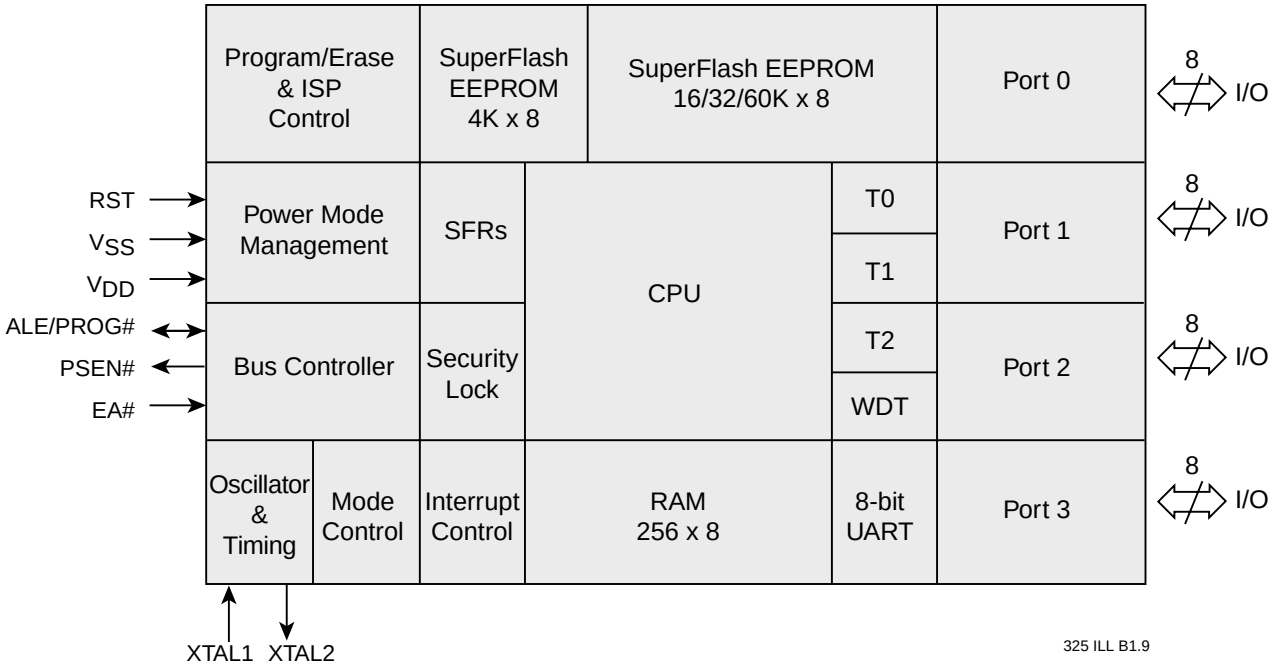
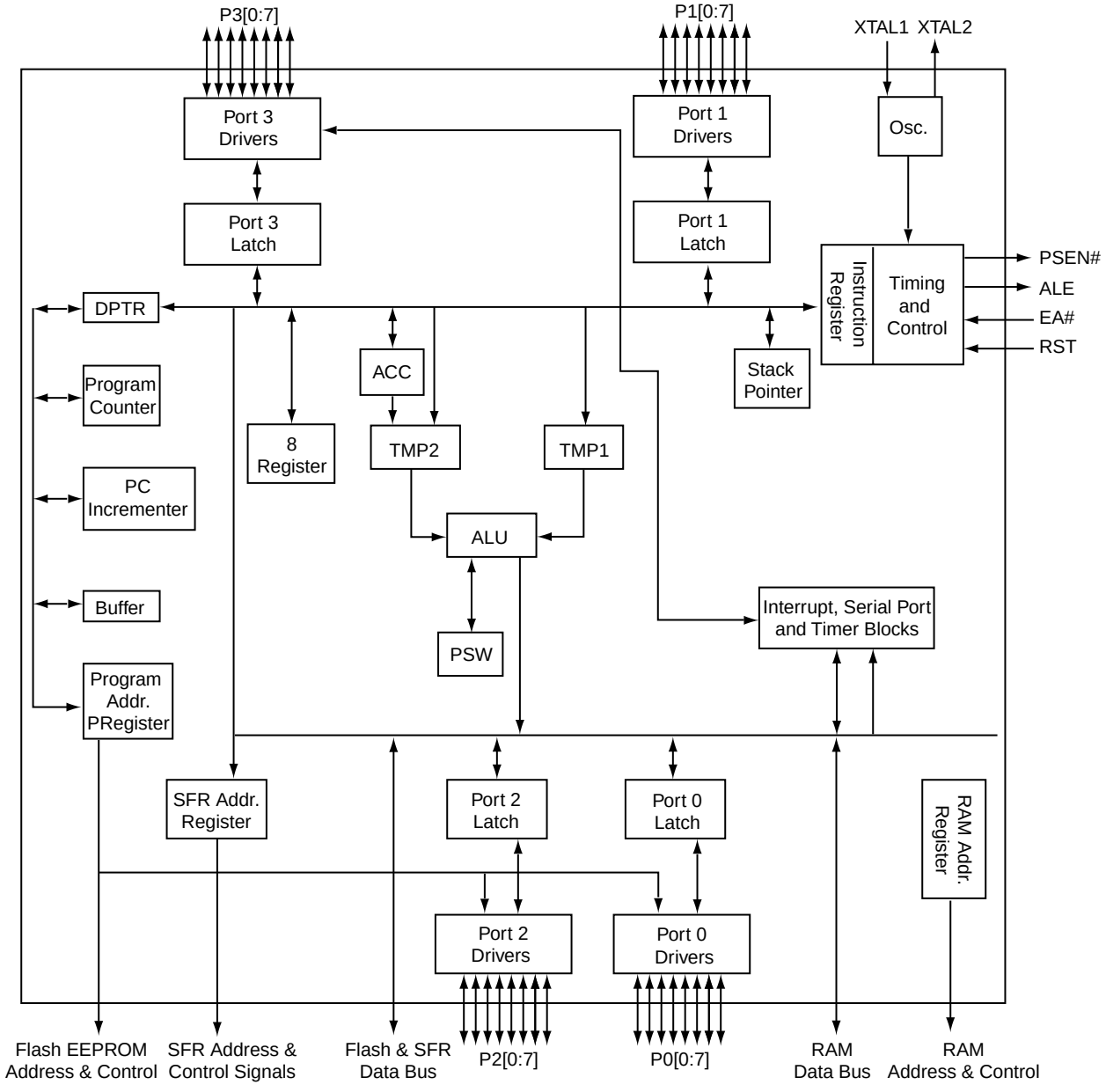
FUNCTIONAL BLOCKS

FUNCTIONAL BLOCK DIAGRAM



MCU CORE


P3[0:7]
P1[0:7]
XTAL1 XTAL2
Port 3 Drivers
Port 1 Drivers
Osc.
Port 3 Latch
Port 1 Latch
Instruction Register
Timing and Control
PSEN#
ALE
EA#
RST
DPTR
Program Counter
ACC
Stack Pointer
8 Register
TMP2
TMP1
PC Incrementer
ALU
Buffer
Interrupt, Serial Port and Timer Blocks
PSW
Program Addr. PRegister
SFR Addr. Register
Port 2 Latch
Port 0 Latch
RAM Addr. Register
Port 2 Drivers
Port 0 Drivers
Flash EEPROM Address & Control
SFR Address & Control Signals
Flash & SFR Data Bus
P2[0:7]
P0[0:7]
RAM Data Bus
RAM Address & Control
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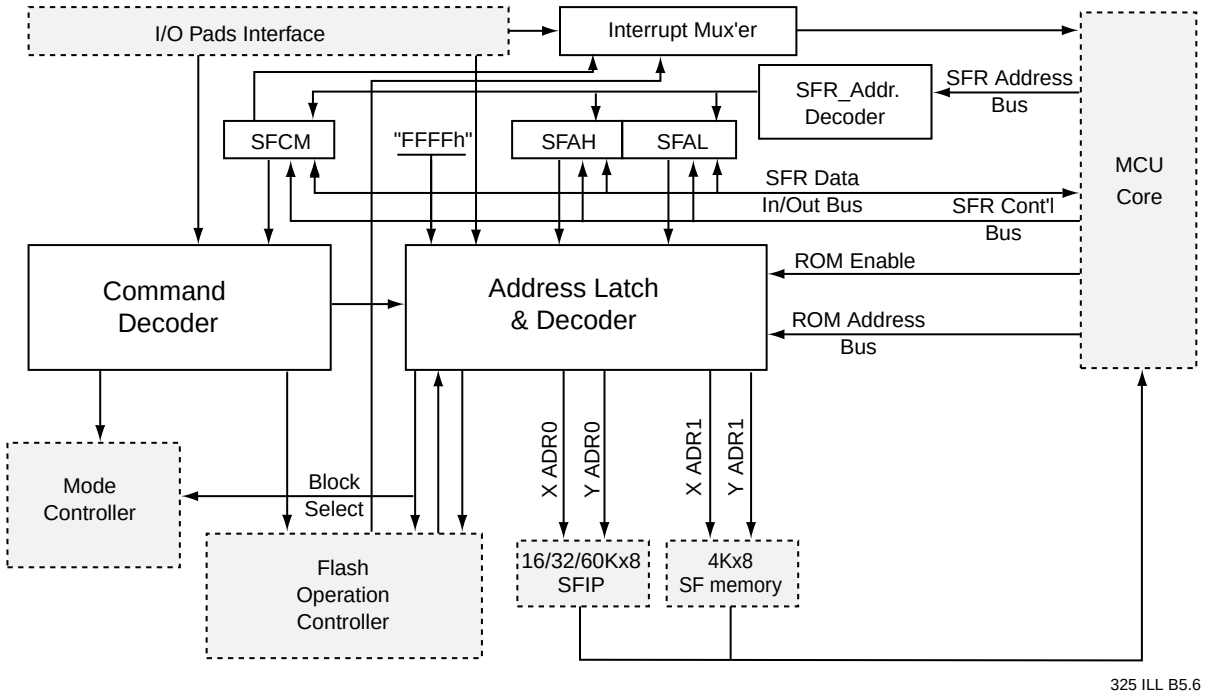
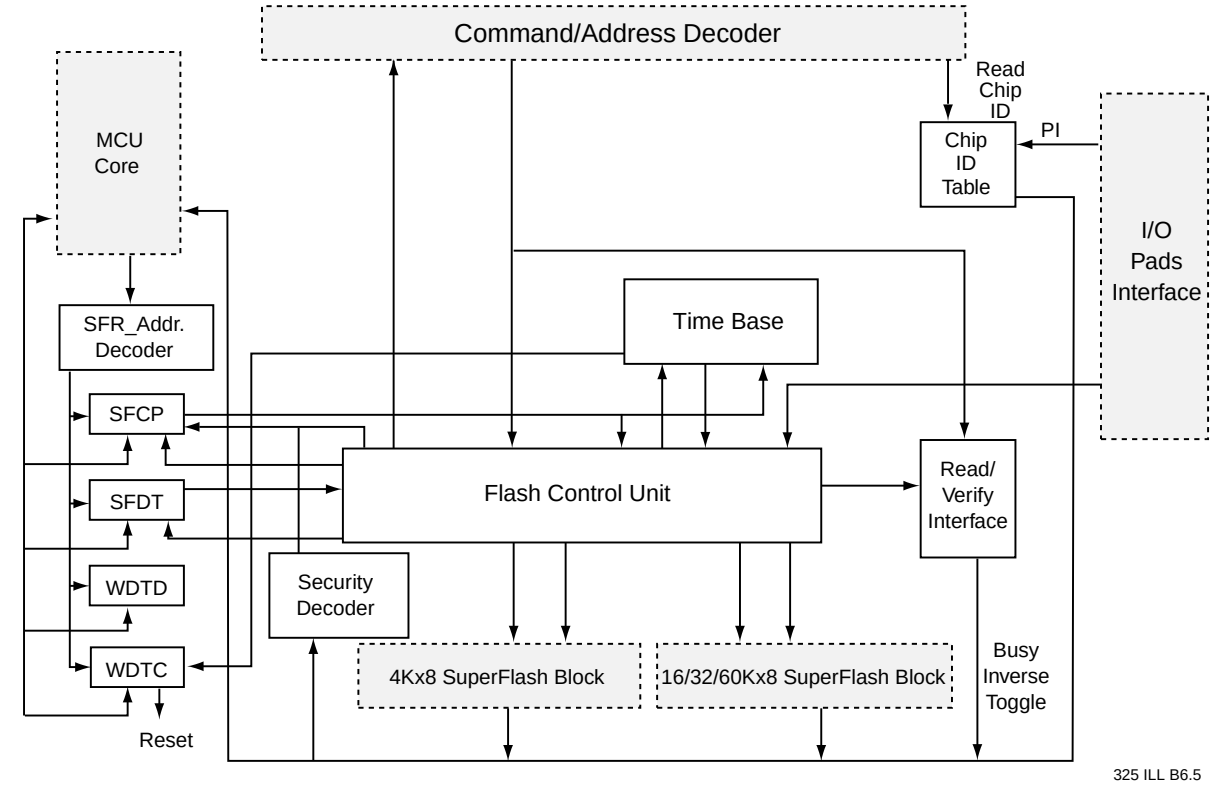
COMMAND/ADDRESS DECODER

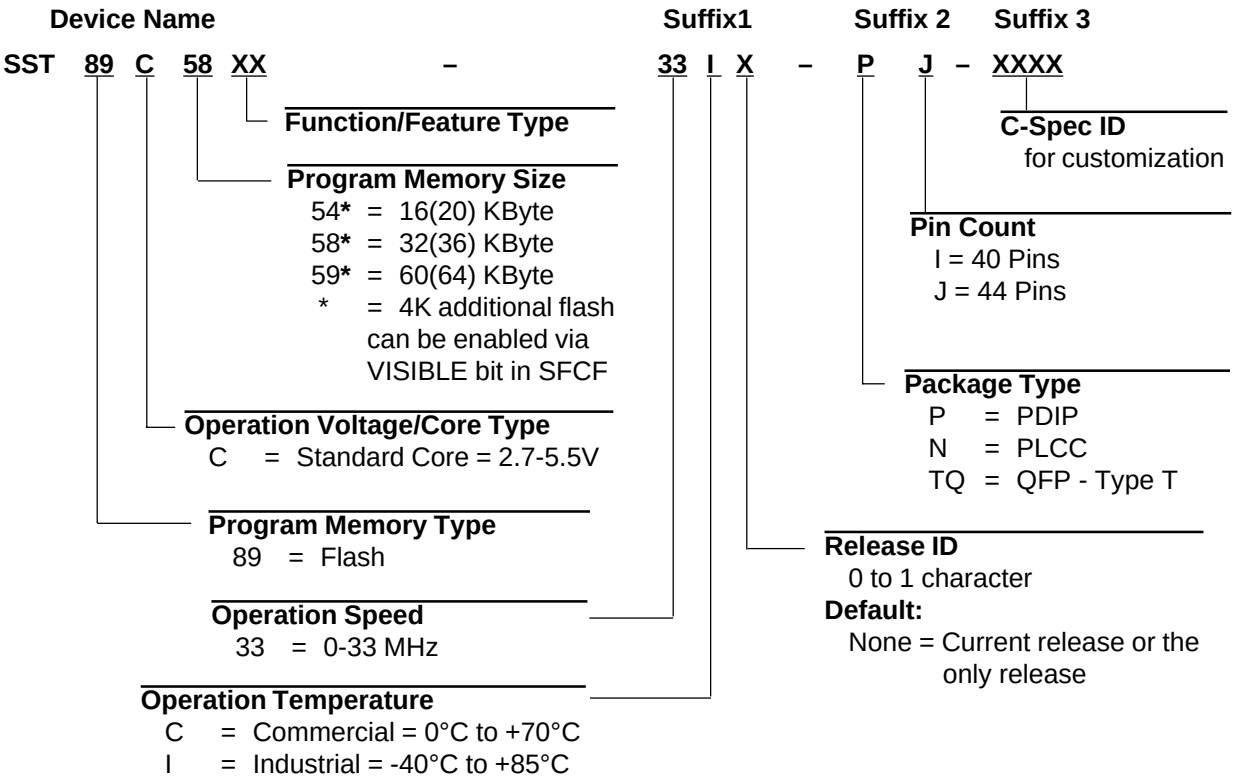


FLASH OPERATION CONTROLLER



PRODUCT ORDERING INFORMATION

Product Identification Descriptor



Part Number Valid Combinations

SST89C54 Valid combinations

Part Number	*Package*	*Pins*	*V_{DD}*	*Speed*	*Temperature*
SST89C54-33C-PI-XXXX	PDIP	40	2.7-5.5	0-33MHz	Commercial
SST89C54-33C-NJ-XXXX	PLCC	44	2.7-5.5	0-33MHz	Commercial
SST89C54-33C-TQJ-XXXX	TQFP	44	2.7-5.5	0-33MHz	Commercial
SST89C54-33I-PI-XXXX	PDIP	40	2.7-5.5	0-33MHz	Industrial
SST89C54-33I-NJ-XXXX	PLCC	44	2.7-5.5	0-33MHz	Industrial
SST89C54-33I-TQJ-XXXX	TQFP	44	2.7-5.5	0-33MHz	Industrial

SST89C58 Valid combinations

Part Number	*Package*	*Pins*	*V_{DD}*	*Speed*	*Temperature*
SST89C58-33C-PI-XXXX	PDIP	40	2.7-5.5	0-33MHz	Commercial
SST89C58-33C-NJ-XXXX	PLCC	44	2.7-5.5	0-33MHz	Commercial
SST89C58-33C-TQJ-XXXX	TQFP	44	2.7-5.5	0-33MHz	Commercial
SST89C58-33I-PI-XXXX	PDIP	40	2.7-5.5	0-33MHz	Industrial
SST89C58-33I-NJ-XXXX	PLCC	44	2.7-5.5	0-33MHz	Industrial
SST89C58-33I-TQJ-XXXX	TQFP	44	2.7-5.5	0-33MHz	Industrial

SST89C59 Valid combinations

Part Number	*Package*	*Pins*	*V_{DD}*	*Speed*	*Temperature*
SST89C59-33C-PI-XXXX	PDIP	40	2.7-5.5	0-33MHz	Commercial
SST89C59-33C-NJ-XXXX	PLCC	44	2.7-5.5	0-33MHz	Commercial
SST89C59-33C-TQJ-XXXX	TQFP	44	2.7-5.5	0-33MHz	Commercial
SST89C59-33I-PI-XXXX	PDIP	40	2.7-5.5	0-33MHz	Industrial
SST89C59-33I-NJ-XXXX	PLCC	44	2.7-5.5	0-33MHz	Industrial
SST89C59-33I-TQJ-XXXX	TQFP	44	2.7-5.5	0-33MHz	Industrial

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability and to determine availability of new combinations.

Part Number Cross-Reference Guide

Intel		**SST**		**package**
i87C54	16K EPROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
i87C58	32K EPROM & 256B RAM	SST89C58	4K Flash, 32K Flash & 256B RAM	D L Q
i87L54	16K ROM (OTP) & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	L Q
i87L58	32K ROM (OTP) & 256B RAM	SST89C58	4K Flash, 32K Flash & 256B RAM	L Q
i87C51FB	16K EPROM & 256B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q
i87C51FC	32K EPROM & 256B RAM	SST89C58*	4K Flash, 32K Flash & 256B RAM	D L Q

Atmel		**SST**		**package**
AT89C52	8K Flash & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
AT89LV52	8K Flash & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
AT89S53	12K Flash & 256B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q
AT89LS53	12K Flash & 256B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q
AT89C55	20K Flash & 256B RAM	SST89C58*	4K Flash, 32K Flash & 256B RAM	D L Q
AT89LV55	20K Flash & 256B RAM	SST89C58*	4K Flash, 32K Flash & 256B RAM	D L Q

Temic		**SST**		**package**
80C51	4K ROM & 256B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q
80C52	8K ROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
83C154	16K ROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
83C154D	32K ROM & 256B RAM	SST89C58	4K Flash, 32K Flash & 256B RAM	D L Q
87C51	4K EPROM & 256B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q
87C52	8K EPROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q

Philips		**SST**		**package**
P80C54	16K ROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
P80C58	32K ROM & 256B RAM	SST89C58	4K Flash, 32K Flash & 256B RAM	D L Q
P87C54	16K EPROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
P87C58	32K EPROM & 256B RAM	SST89C58	4K Flash, 32K Flash & 256B RAM	D L Q
P87C524	16K EPROM & 512B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q
P87C528	32K EPROM & 512B RAM	SST89C58*	4K Flash, 32K Flash & 256B RAM	D L Q
P83C524	16K ROM & 512B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L
P83C528	32K MROM & 512B RAM	SST89C58*	4K Flash, 32K Flash & 256B RAM	D L Q
P89CE558	32K Flash & 1K RAM	SST89C58*	4K Flash, 32K Flash & 256B RAM	

Winbond		**SST**		**package**
W78C54	16K MROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
W78C58	32K MROM & 256B RAM	SST89C58	4K Flash, 32K Flash & 256B RAM	D L Q
W78E54	16K EEPROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
W78E58	32K EEPROM & 256B RAM	SST89C58	4K Flash, 32K Flash & 256B RAM	D L Q

ISSI		**SST**		**package**
IS80C52	8K ROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q

Dallas		**SST**		**package**
DS83C520	16K MROM & 256B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q
DS87C520	16K EPROM (OTP) & 256B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q

Siemens		**SST**		**package**
C501-1R	8K ROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L
C501-1E	8K ROM (OTP) & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L
C513A-H	12K EPROM & 512B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	L
C503-1R	8K ROM & 256B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	L
C504-2R	16K ROM & 512B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	Q

D: PDIP
L: PLCC
Q: TQFP

NOTE: The SST89C58 can be substituted for any SST89C54 listing above.
NOTE: The SST89C59 can be substituted for any SST89C54 or SST89C59 listing above.
* Indicates SST similar function and not direct replacement/socket compatible.

PIN ASSIGNMENTS

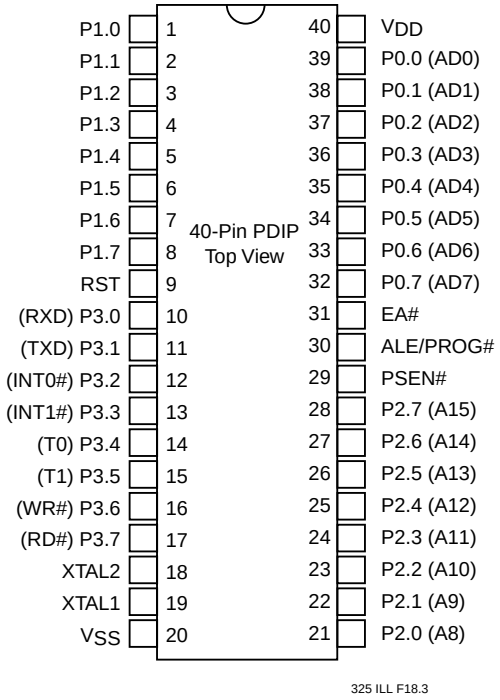


FIGURE 1: PIN ASSIGNMENTS FOR 40-PIN PLASTIC DIP

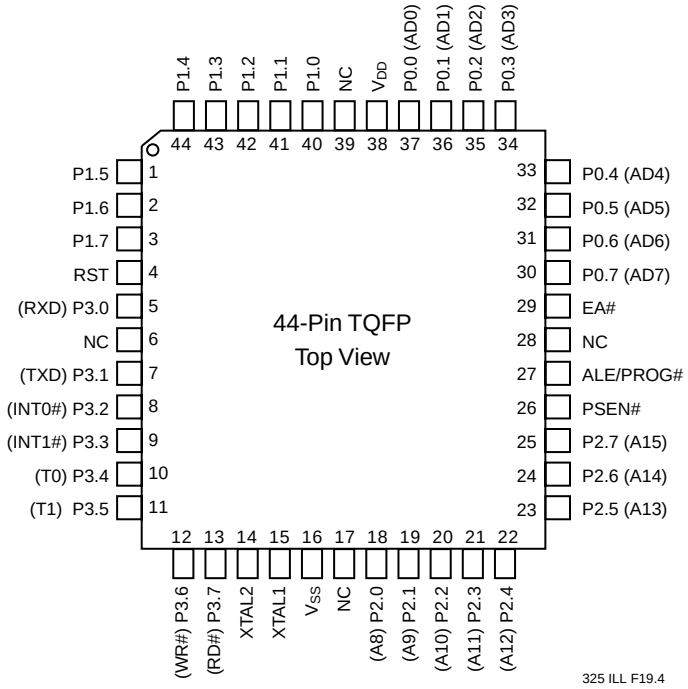


FIGURE 2: PIN ASSIGNMENTS FOR 44-PIN TQFP

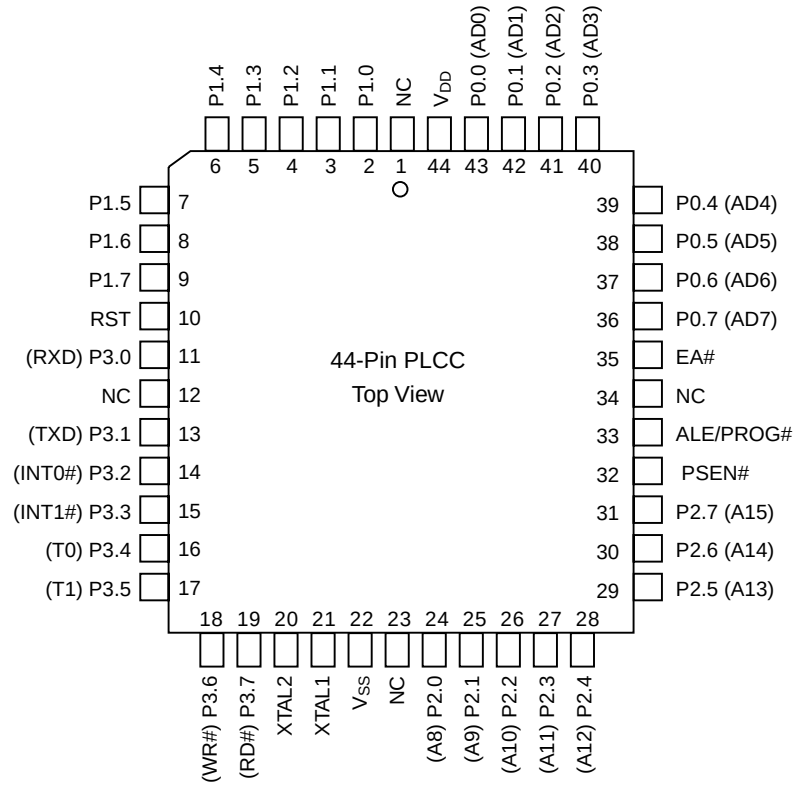


FIGURE 3: PIN ASSIGNMENTS FOR 44-PIN PLCC

Note: NC pins must be left unconnected.

TABLE 1: PIN DESCRIPTIONS

Symbol	Type*	Name and Functions
P0[7:0]	I/O*	***Port 0:*** Port 0 is an 8-bit open drain bi-directional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external memory. In this application it uses strong internal pull-ups when transitioning to 1's. Port 0 also receives the code bytes during FLASH MEMORY programming, and outputs the code bytes during program verification. External pull-ups are required during program verification.
P1[7:0]	I/O with internal pull-ups	***Port 1:*** Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pull-ups. P1(5, 6, 7) have high current drive of 16 mA. Port 1 also receives the low-order address bytes during FLASH MEMORY programming and program verification.
P2[7:0]	I/O with internal pull-ups	***Port 2:*** Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. Port 2 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pull-ups. Port 2 sends the high-order address byte during fetches from external Program memory and during accesses to external Data Memory that use 16-bit address (MOVX@DPTR). In this application it uses strong internal pull-ups when outputting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX@Ri), Port 2 sends the contents of the P2 Special Function Register. Port 2 also receives some control signals and a partial of high-order address bits during FLASH MEMORY programming and program verification.
P3[7:0]	I/O with internal pull-ups	***Port 3:*** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers could drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pull-ups. Port 3 also serves the functions of various special features of the FlashFlex51 Family. Port 3 also receives some control signals and a partial of high-order address bits during FLASH MEMORY programming and program verification.
P3.0	I	***RXD:*** Serial input line
P3.1	O	***TXD:*** Serial output line
P3.2	I	***INT0#:*** External Interrupt 0
P3.3	I	***INT1#:*** External Interrupt 1
P3.4	I	***T0:*** Timer 0 external input
P3.5	I	***T1:*** Timer 1 external input
P3.6	O	***WR#:*** External Data Memory Write strobe
P3.7	O	***RD#:*** External Data Memory Read strobe
PSEN#	O/I	***Program Store Enable:*** PSEN# is the Read strobe to External Program Memory. When the SST89C54/58/59 are executing from Internal Program Memory, PSEN# is inactive (high). When the device is executing code from External Program Memory, PSEN# is activated twice each machine cycle, except that two PSEN# activations are skipped during each access to External Data Memory. While the RST input is continually held high (for more than ten machine cycles), a forced high-to-low input transition on the PSEN# pin will bring the device into the "External Host" mode for the internal flash memory programming operation.

PIN DESCRIPTIONS (CONTINUED)

Symbol	Type*	Name and Functions
RST	I	***Reset:*** A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IH1} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{DD}. After a successful reset is completed, if the PSEN# pin is driven by an input force with a high-to-low transition while the RST input pin is continually held high, the device will enter the "External Host" mode for the internal flash memory programming operation, otherwise the device will enter the "Normal" operation mode.
EA#	I	***External Access Enable:*** EA# must be strapped to V_{SS} in order to enable the SST89C54/58/59 to fetch code from External Program Memory locations starting at 0000h up to FFFFh. Note, however, that if the Security Lock is activated on either block, the logic level at EA# is internally latched during reset. EA# must be strapped to V_{DD} for internal program execution.
ALE/PROG#	I/O	***Address Latch Enable:*** ALE is the output signal for latching the low byte of the address during accesses to external memory. This pin is also the programming pulse input (PROG#).
$XTAL_1$ $XTAL_2$	I O	***Oscillator:*** Input and output to the inverting oscillator amplifier. XTAL1 is input to internal clock generation circuits from an external clock source.
V_{DD}	I	***Power Supply:*** Supply voltage during normal, Idle, Power Down, and Standby Mode operations.
Vss	I	***Ground:*** Circuit ground. (0V reference)

* I = Input
O = Output

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FLASH MEMORY PROGRAMMING

Operation Modes

1. External Host
2. Normal

External Host Mode

The SST89C54/58/59 provide the user with a direct flash memory access that can be used for programming into the flash memory without using the CPU. The direct flash memory access is entered using the External Host Mode. While the reset input (RST) is continually held active (high), if the PSEN# pin is forced by an input with a transition from high-to-low state, the device enters the External Host Mode. The CPU core is stopped from running and all the chip I/O pins are reassigned and become flash memory access and control pins. After the device enters into the External Host Mode, the internal flash memory blocks are accessed through the re-assigned I/O port pins (please see Figure 4 for details) by an external host, such as a PCB tester (ATE), a PC controlled development board or an OTP MCU programmer.

When the chip is in the external host mode, Port 0 pins are assigned to be the parallel data input and output pins. Port 1 pins are assigned to be the non-muxed low order address bus signals for the internal flash memory (A0-A7). The first six bits of Port 2 pins (P2[0:5]) are assigned to be the non-muxed upper order address bus signals for the internal flash memory (A8-A13) along with two of the Port 3 pins (P3.4 as A14 and P3.5 as A15). Two upper order Port 2 pins (P2.6 and P2.7) and two upper order Port 3 pins (P3.6 and P3.7) along with RST, PSEN#, PROG#/ALE, EA# pins are assigned as the control signal pins. The Port 3 pin (P3.3) is assigned to be the ready/busy status signal, which can be used for handshaking with the external host during a flash memory programming operation. The flash memory programming operation (Erase, Program, Verify, etc.) is internally self-timed and can be controlled by an external host asynchronously or synchronously.

The External Host Mode uses seven (7) hardware commands, which are decoded from the control signal pins, to facilitate the internal flash memory erase, test and programming process. The External Host Mode is enabled on the falling edge of PSEN#. The External Host Mode Commands are enabled on the falling edge of ALE/PROG#. The list in Table 2 outlines all the commands and its control signal assignment.

TABLE 2: EXTERNAL HOST MODE COMMANDS

Operation	RST	PSEN#	PROG# /ALE	EA#	P2.6	P2.7	P3.6	P3.7	P0[7:0]	P1[7:0]	P3[5:4] P2[5:0]
0 READ ID	H	L	H	H	L	L	L	L	DO	AL	AH
1 CHIP ERASE	H	L	⇓	H	H	H	H	L	X	X	X
2 BLOCK ERASE	H	L	⇓	H	H	H	H	H	X	X	A15
3 SECTOR ERASE	H	L	⇓	H	H	H	L	H	X	X	AH
4 BYTE PROGRAM	H	L	⇓	H	L	H	H	H	DI	AL	AH
5 BURST PROGRAM	H	L	⇓	H	L	H	L	H	DI	AL	AH
6 VERIFY (Read) BYTE	H	L	H	H	L	L	H	H	DO	AL	AH

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Note: Symbol ⇓ signifies a negative pulse and the command is asserted during the low state of PROG#/ALE input. All other combinations of the above input pins are invalid and may result in unexpected behaviors.

Note: IntEn = Interrupt Enable for flash operation completion;
L = Logic low level; H = Logic high level; X = Don't care; AL = Address low order byte; AH = Address high order byte;
DI = Data Input; DO = Data Output; A15 = Only care for the MSB, i.e. address bit #15.

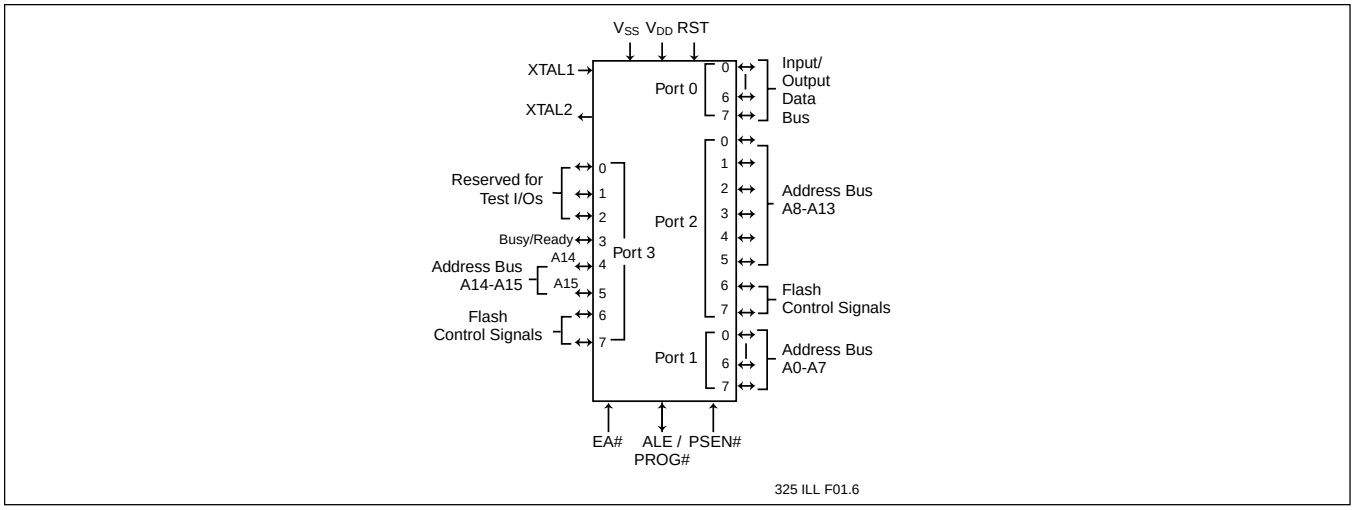

FIGURE 4: I/O PINS ASSIGNMENT FOR EXTERNAL HOST MODE

External Host Mode Commands

The SST89C54/58/59 External Host Mode Commands are 1) READ ID, 2) CHIP ERASE, 3) BLOCK ERASE, 4) SECTOR ERASE, 5) BYTE PROGRAM, 6) BURST PROGRAM, and 7) VERIFY BYTE. The following is a brief description of the commands. See Table 2 for all signal logic assignments and Table 4 for all timing parameter values for the External Host Mode Commands. The critical timing for all Erase and Program commands, is self-generated by the Flash memory controller on-chip. The high-to-low transition of the PROG# signal initiates the Erase and Program commands, which are synchronized internally. The Read commands are static reads, independent of the PROG# signal level.

The READ ID command accesses the on board chip and manufacture's IDs, and identifies the device as an SST89C54/58/59 and the manufacturer as SST. External programmers primarily use these IDs, shown in Table 3, in the selection of programming algorithms. The Read ID command is selected by the byte code of 00h on P2[6:7] and P3[6:7]. See Figure 5 for timing waveforms.

TABLE 3: PRODUCT IDENTIFICATION TABLE

	Address	Data
Manufacturer's Code	30h	BFh
SST89C54 Device Code	31h	E3h
SST89C58 Device Code	31h	E1h
SST89C59 Device Code	31h	E7h

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The following three commands are for erasing all or part of the memory array. All the data in the memory array will be erased to FFh. Memory addresses that are to be programmed must be in the erased state prior to programming. Selection of the Erase command to use, prior to programming the device, will be dependent upon the contents already in the array and the desired programming field size.

The CHIP ERASE command erases all bytes in both memory blocks (16/32/60K and 4K) of the SST89C54/58/59. This command ignores the Security Lock status and will erase the Security Byte. The CHIP ERASE command is selected by the byte code of 0Eh on P2[6:7] and P3[6:7]. See Figure 6 for timing waveforms.

The BLOCK ERASE command erases all bytes in one of the memory blocks (16/32/60K or 4K) of the SST89C54/58/59. This command will not enable if the Security Byte is enabled on the selected memory block. The selection of the memory block to be erased is determined by A15 (P3.5). If A15 is a "0", then the lower flash memory block (16/32/60K) is selected. If A15 is a "1", then the upper flash memory block (4K) is selected. The BLOCK ERASE command is selected by the byte code of 0Fh on P2[6:7] and P3[6:7]. See Figure 7 for the timing waveforms.

The SECTOR ERASE command erases all of the bytes in a sector. The sector size for the lower flash memory (Address buffer locations 0-3FFFh/7FFFh/EFFFh) is 128 bytes. The sector size for the upper flash memory (Address buffer locations F000h-FFFFh) is 64 bytes. This command will not enable if the Security Byte is enabled on the selected memory block. The selection of the memory sector to be erased is determined by P2[0:5] (A8-A13) and P3[4:5] (A14 & A15). The SECTOR ERASE command is selected by the byte code of 0Dh on P2[6:7] and P3[6:7]. See Figure 8 for timing waveforms.

The following two Program commands are for programming new data into the memory array. Selection of which Program command to use for programming will be dependent upon the desired programming field size. The Program commands will not enable if the Security Byte is enabled on the selected memory block.

The BYTE PROGRAM command programs data into a single byte. Ports P0[0:7] are used for data in. The memory location is selected by P1[0:7], P2[0:5], and P3[4:5] (A0-A15). The BYTE PROGRAM command is selected by the byte code of 07h on P2[6:7] and P3[6:7]. See Figure 9 for timing waveforms.

The BURST PROGRAM command programs data to an entire row, sequentially byte by byte. Ports P0[0:7] are used for data in. The memory location is selected by P1[0:7], P2[0:5], and P3[4:5] (A0-A15). The BYTE PROGRAM command is selected by the byte code of 05h on P2[6:7] and P3[6:7]. See Figure 10 for timing waveforms.

The VERIFY BYTE command allows the user to verify that the SST89C54/58/59 correctly performed an Erase or Program command. Ports P0[0:7] are used for data out. The memory location is selected by P1[0:7], P2[0:5], and P3[4:5] (A0-A15). This command will not enable if the Security Byte is enabled on the selected memory block. See Figure 11 for timing waveforms.

If an External Host Mode Command is issued to a secured memory block, the device will immediately reset and be ready for another command.

Programming a SST89C54/58/59

To program new data into the memory array, supply 5 volts to V_{DD} and RST, and perform the following steps.

1. Enable RST, and PSEN# in sequence per the appropriate timing diagram.
2. Raise EA# High (either V_{IH} or V_H).
3. Read the device and manufacturer ID using the READ ID command to ensure using the right programming algorithm.
4. Verify that the memory block for programming is in the erased state, FFh. If the block is not erased, then erase the block using the appropriate Erase command.
5. Select the memory location using the address lines (P1[0:7], P2[0:5], P3[4:5]).
6. Present the data in on P0[0:7].
7. Pulse ALE/PROG#.
8. Wait for low to high transition on READY/BUSY# (P3(3)).
9. Continue steps 5 – 8 until finishing programming.
10. Verify the flash memory contents.

Flash Operation Status Detection (Ext. Host Handshake)

The SST89C54/58/59 provide two firmware means for an external host to detect the completion of a flash memory operation, therefore the external host can optimize the system Program or Erase cycle of the embedded flash memory. The end of a flash memory operation cycle (Erase or Program) can be detected by: 1) monitoring the Ready/Busy# bit at Port 3.3; 2) monitoring the Data# Polling bit at Port 0.7 or Port 0.3. Refer to the SST89C54/58/59 User's Manual for a detailed description.

Ready/Busy# (P3.3)

The progress of the flash memory programming can be monitored by the Ready/Busy# output signal. P3.3 is driven low, sometime after ALE/PROG# goes low during a flash memory operation to indicate the Busy# status of the flash programming controller. P3.3 is driven high when the flash programming operation is completed to indicate the Ready status.

During a Burst Program operation, P3.3 is driven high (Ready) in between each Byte Program among the Burst Programs to indicate the ready status to receive the next byte. When the external host detects the Ready status after a byte among the burst is programmed, it may then put the data/address (in the same page) of the next byte on the bus and drive ALE/PROG# low (pulse) immediately, before the time-out limit expires

Data# Polling (P0.7 & P0.3)

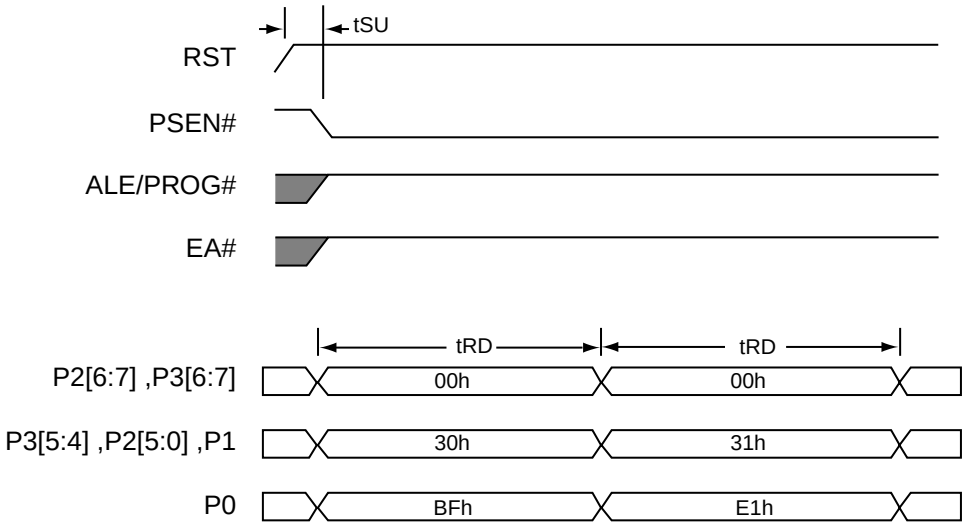
During a Burst Program operation, any attempts to read (Verify Byte), while the device is busy programming the byte among the Burst Programs, will receive the complement of the data of the last byte programmed (logic low, i.e. "0" for an erase) on P0.3 and P0.7 with the rest of the bits "0". During a Burst Program operation, the Verify Byte command is reading the data of the last byte programmed, not the data at the address specified.

The true data will be read from P0.7, when the device completes each Byte Program among the Burst Programs to indicate the Ready status to receive the next byte. When the external host detects the Ready status after a byte among the burst is programmed, it should then put the data/address (in the same page) of the next

byte on the bus and drive ALE/PROG# low (pulse) immediately, before the time-out limit expires (See programming time spec. for details.). The true data will be read from P0.3, when the Burst Program command is terminated and the device is ready for the next operation.

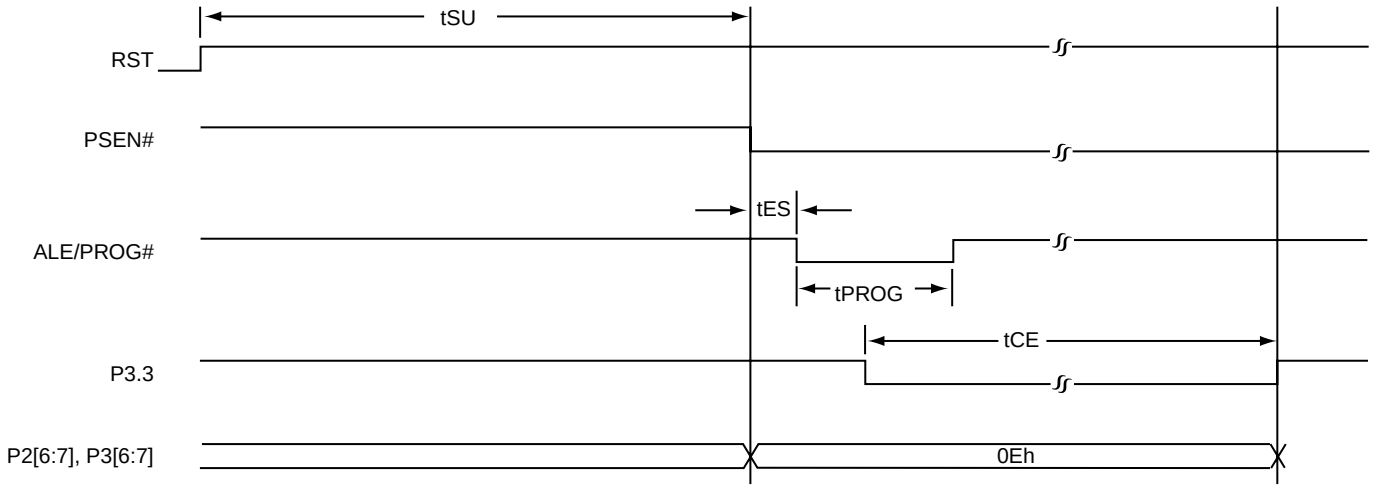
The termination of the Burst Program can be accomplished by: 1) Change to a new X-Addresses (Note: the X-Address range are different for the 4Kx8 flash block and for the 16/32/60K x 8 flash block.); 2) Change to a new command that requires a negative transition of the ALE/PROG# (i.e. any Erase or Program command); 3) Wait for time out limit expires (20 µs); when programming the next byte.

Flash Memory Programming with External Host (Figures 5-11)



325 ILL F02.7

FIGURE 5: READ ID
Read chip signature and identification registers at the addressed location.



325 ILL F03.8

FIGURE 6: CHIP ERASE
Erase both flash memory blocks. Security lock is ignored and the security byte is erased too.

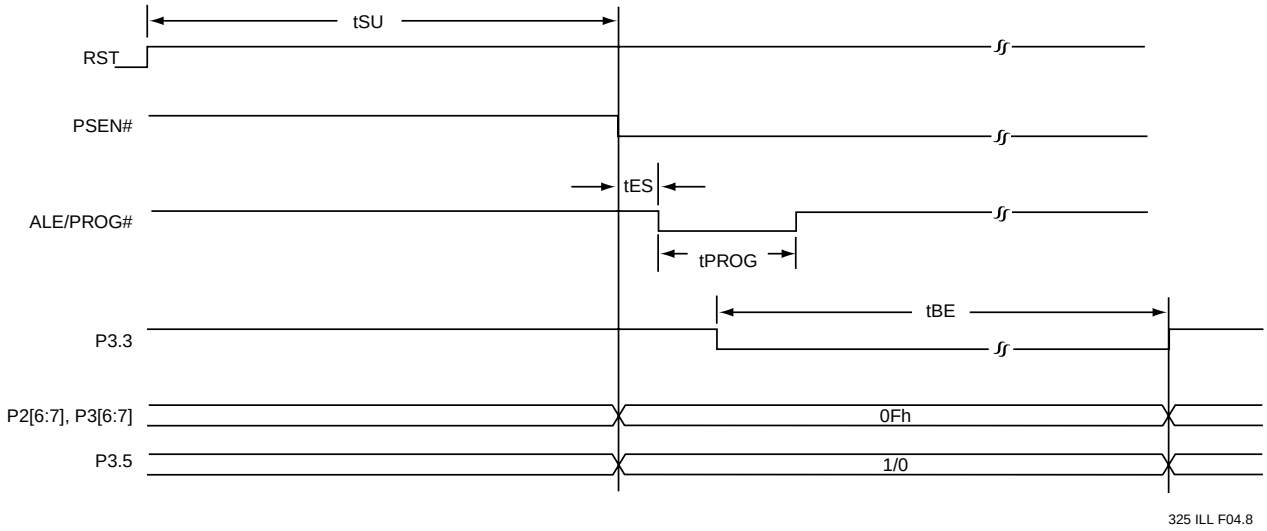


FIGURE 7: BLOCK ERASE

Erase one of the flash memory blocks, if the security lock is not activated on that flash memory block. The highest address bit (A15) determines which block is erased. For example, if A15 is "0", lower flash memory block is erased.

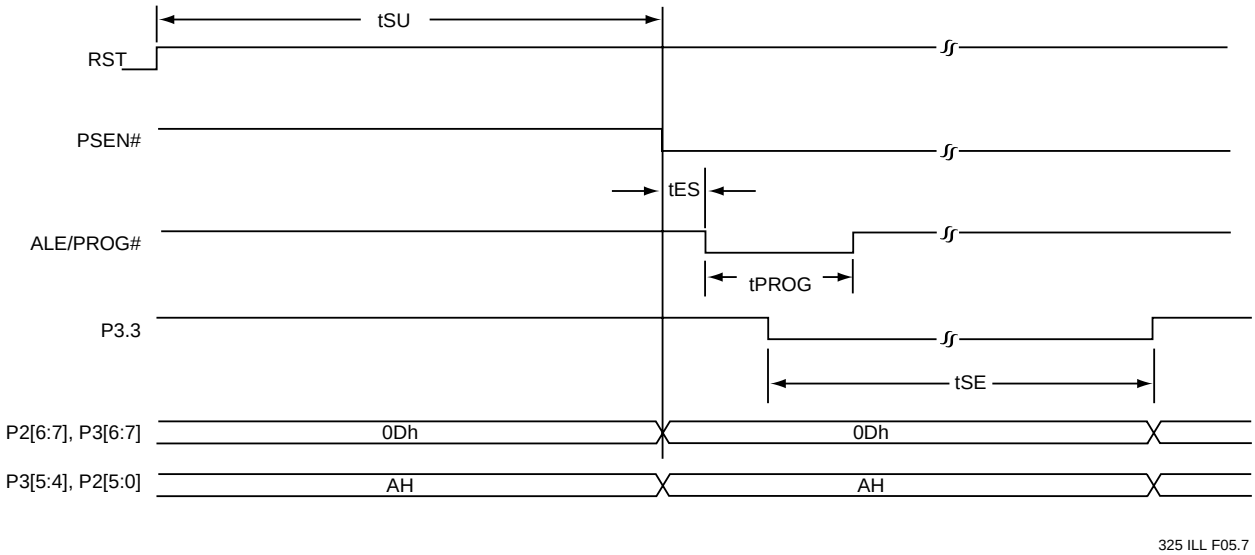


FIGURE 8: SECTOR ERASE

Erase the addressed sector if the security lock is not activated on that flash memory block.

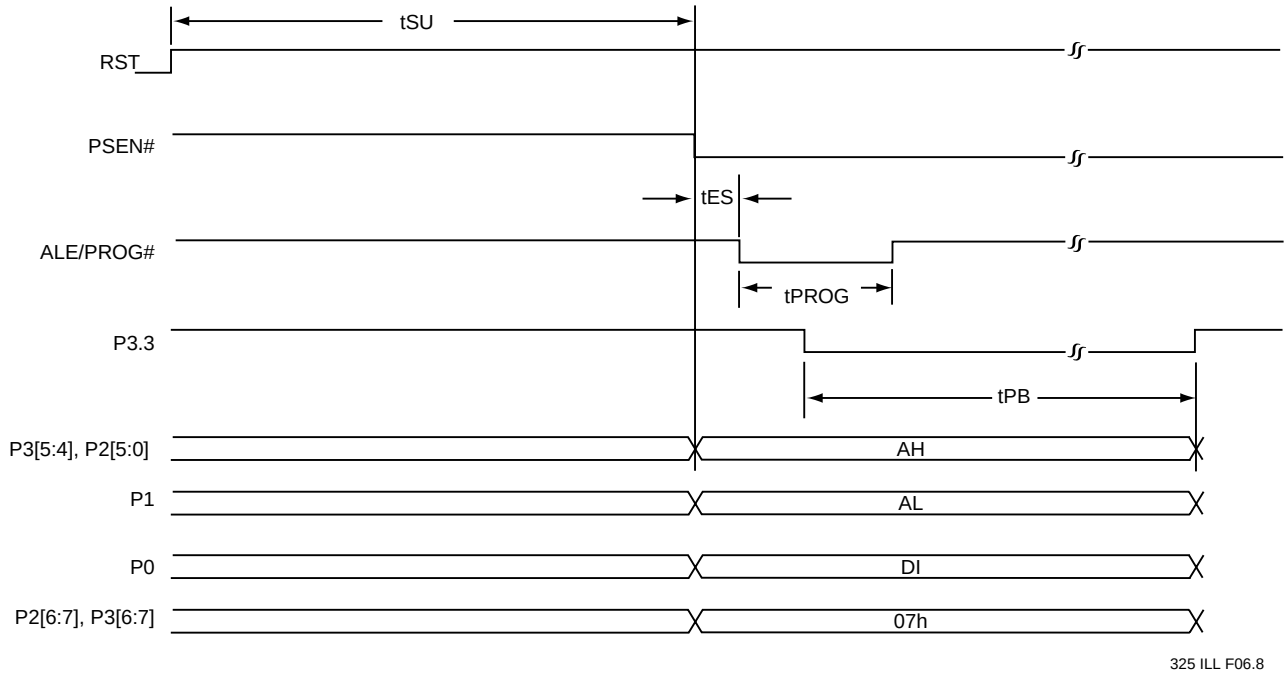


FIGURE 9: BYTE PROGRAM
Program the addressed code byte if the byte location has been successfully erased and not yet programmed. This operation is only allowed when the security lock is not activated on that flash memory block.

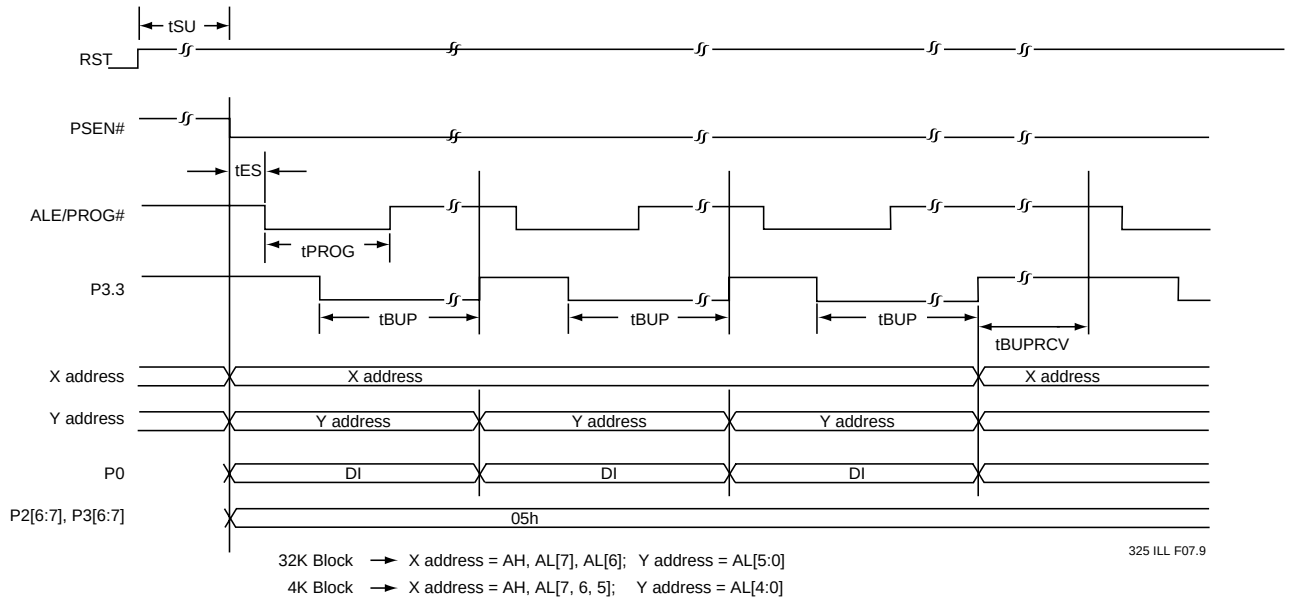


FIGURE 10: BURST PROGRAM
Program the entire addressed row by burst programming each byte sequentially within the row if the byte location has been successfully erased and not yet programmed. This operation is only allowed when the security lock is not activated on that flash memory block.

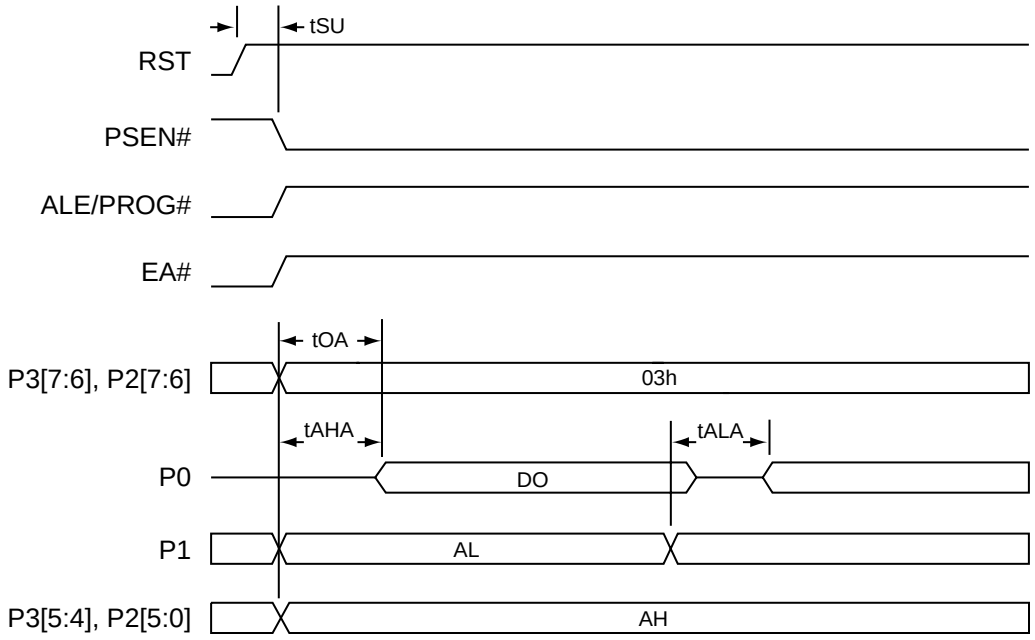


FIGURE 11: VERIFY BYTE

Read the code byte from the addressed flash memory location if the security lock is not activated on that flash memory block.

TABLE 4: FLASH MEMORY PROGRAMMING/VERIFICATION PARAMETERS (T_J = 0°C TO +125°C, V_{DD} = 5V±10%, V_{SS} = 0V)

Parameter (1, 2, 4, 5)	Symbol	SuperFlash Block 10 MHz ±10%		Unit
		Min.	Max.	
Reset Setup Time	tSU	3		µs
Read ID Command Setup Time	tS	0		ns
Read ID Command Width (3)	tRD	250		ns
PSEN# setup Time	tES	250		ns
Chip Erase Time	tCE	4.25		ms
Block Erase Time	tBE	4.25		ms
Sector Erase Time	tSE	1.1		ms
Program Setup Time	tPROG	1.2		µs
Byte Program Time (6)	tPB		97	µs
Verify Command Setup time	tOA	35		ns
Verify High Order Address Setup Time	tAHA	35		ns
Verify Low Order Address Setup Time	tALA	35		ns
Burst Program (6,7)	tBUP	31	51	µs
Burst Program Recovery	tBUPRCV			µs

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Note:

1. All timing numbers are pre-simulation and subject to change before silicon verification.
2. All signals that align together in the timing diagrams should be derived from the same clock edge. Set up and hold times are not critical if they are within 10ns.
3. Reading operation is combinatorial. Sequence of timing edges are not important. The latest valid signal determines the access time.
4. All timing measurements are from the 50% of the input to 50 % of the output.
5. All input waveforms have rise and fall time of 1ns.
6. Don't Program (write "0") any byte twice before next erase.
7. Timing is based on 126ns clock cycles.

Normal Mode

The Normal operational mode consists of both the normal MCU operation and the concurrent programming operation. The internal flash memory acts like a read only memory (ROM) during the normal MCU operation. During the concurrent programming operation, the MCU is executing the program code from one of the internal flash memory blocks or the external program code storage, while another internal flash memory block is erased and programmed. The chip will automatically enter into the Normal Mode after a successful power-on reset (POR) process. A successful power-on reset requires the reset input pin being held logic high level for a minimum of two clock cycles, after the power supply has reached its specification rail range, followed by a high to low transition of the RST input pin.

Concurrent Programming Operation

During the concurrent programming operation, the CPU of the microcontroller is the master (internal host) of the internal flash memory erase and programming process. The chip has to enter into the Normal Mode first, before starting the concurrent programming operation. The chip can start the concurrent programming operation either with the external program code execution being enabled (EA# = L) or disabled (EA# = H). A set of mailbox registers (SFCM, SFAL, SFAH, SFDT and SFCF) located in the SFR address range (B2 to B6) will be controlled by the software to facilitate the internal flash memory erase and programming process.

There are six (6) software commands, which can be issued via the command mailbox register, SFCM, which is located at SFR address B2h. The memory array of the SuperFlash blocks is addressed by a pair of address mailbox registers, SFAL and SFAH. The high order address mailbox register, SFAH is located at SFR address B4h and the low order address mailbox register, SFAL is located at SFR address B3h. The read and write data of the SuperFlash blocks are passed through the data buffer mailbox register, SFDT, which is located at SFR address B5h. The Verify (READ) byte should be followed by a "NOP" instruction, to give enough time for Verify. The configuration register, SFCF, which is located at SFR address B6h, provides the security lock indication and the visibility of the upper flash memory block. The SuperFlash Configuration Register (SFCF) is read only at the writing to SuperFlash Command Register (SFCM) or Watchdog reset. The list in Table 5 outlines all the commands and its associated bit settings of the mailbox registers:

All of the following commands can only be initiated in the Normal/Internal Host Mode. In all situations, writing the control byte to the (SFCM) register will initiate all of the operations. All commands (except CHIP ERASE) will not be enabled if the Security Byte is set and security features are enabled on the selected memory block. The critical timing for all Erase and Program commands, is self-generated by the Flash memory controller on-chip.

The two Program commands are for programming new data into the memory array. The portion of the memory array to be programmed should be in the erased state, FFh. If the memory is not erased, then erase it with the appropriate Erase command. Warning: do not program to a block that is currently running code. This can "hang" the CPU and may even corrupt program data as it is being executed.

The CHIP ERASE command erases all bytes in both memory blocks (16/32/60K and 4K). This command ignores the Security Lock status and will erase the Security Byte. The CHIP ERASE command is initiated as follows:

1.) Move 55h to the SuperFlash Data Register (SFDT) (i.e. "MOV SFDT, 55h" where SFDT is the register address). This serves as a dual level precautionary measure to prevent accidental chip erasure. 2.) Move 3Bh or BBh to the SuperFlash Command Register (SFCM) (i.e., "MOV SFCM, BBh or MOV SFCM, 0BBh"). This is an "arming command" sequence prior to Program and Erase operations to prevent inadvertent program or erase within the SuperFlash memory. 3.) Move the termination mode FIE and Chip Erase command FCM to the SuperFlash Command Register (SFCM) (i.e. MOV SFCM, 87h *or* MOV SFCM, 07h). If FIE is set, INT1# will interrupt the system when the erase is complete. Otherwise you must poll the system to determine when the erase is complete.

The BLOCK ERASE command erases all bytes in one of the two memory blocks (16/32/60K or 4K). The selection of the memory block to be erased is determined by the "A15" bit (SFAH[7]) of the SuperFlash Address Register. If (SFAH[7]) is a "0", the lower flash memory block is selected (16/32/60K). If (SFAH[7]) is a "1", the upper flash memory block is selected (4K). The BLOCK ERASE command is initiated as follows:

1.) Move the block address to (SFAH) (i.e. MOV SFAH, 80h *or* MOV SFAH, 00h). 2.) Move 55h to the SuperFlash Data Register (SFDT) (i.e. "MOV SFDT, 55h" where SFDT is the register address). This serves as a dual level precautionary measure to prevent accidental erasure. 3.) Move 3Bh or BBh to the SuperFlash Command Register (SFCM) (i.e., "MOV SFCM, 3Bh or MOV SFCM, 0BBh"). This is an "arming command" sequence prior to Program and Erase operations to prevent inadvertent program or erase within the SuperFlash memory. 4.) Move the termination mode FIE and Block Erase command FCM to (SFCM) (i.e. MOV SFCM, 8Fh *or* MOV SFCM, 0Fh). If FIE is set, INT1# will interrupt the system when the erase is complete. Otherwise you must poll the system to determine when the erase is complete.

The SECTOR ERASE command erases all of the bytes in a sector. The sector size for the lower flash memory (Address buffer locations 0-3FFFh/7FFFh/EFFFh) is 128 bytes. The sector size for the upper flash memory (Address buffer locations F000h-FFFFh) is 64 bytes. The SECTOR ERASE command is initiated as follows:

1.) Move the sector address to (SFAH) and to (SFAL). 2.) Move 3Bh or BBh to the SuperFlash Command Register (SFCM) (i.e., "MOV SFCM, 3Bh or MOV SFCM, 0BBh"). This is an "arming command" sequence prior to Program and Erase operations to prevent inadvertent program or erase within the SuperFlash memory. 3.) Move the termination mode FIE and Sector Erase command FCM to (SFCM) (i.e. MOV SFCM, 8Bh *or* MOV SFCM, 0Bh). If FIE is set, INT1# will interrupt the system when the erase is complete. Otherwise you must poll the system to determine when the erase is complete.

The BYTE PROGRAM command programs data into a single byte. The BYTE PROGRAM command is initiated as follows:

1.) Move the high order address byte AH to (SFAH). 2.) Move the low order address byte AL to (SFAL). 3.) Move the data to the (SFDT). 4.) Move 3Bh or BBh to the SuperFlash Command Register (SFCM) (i.e., "MOV SFCM, 3Bh or MOV SFCM, 0BBh"). This is an "arming command" sequence prior to Program and Erase operations to prevent inadvertent program or erase within the SuperFlash memory. 5.) Move the termination mode FIE and Byte Program command FCM to (SFCM) (i.e. MOV SFCM, 8Eh *or* MOV SFCM, 0Eh). If FIE is set, INT1# will interrupt the system when the program is complete. Otherwise you must poll the system to determine when the program is complete.

The BURST PROGRAM command programs data to an entire row, sequentially byte by byte. The BURST PROGRAM command is initiated as follows:

1.) Move the high order address byte to (SFAH). 2.) Move the low order address byte to (SFAL). 3.) Move the data to (SFDT). 4.) Move 3Bh or BBh to the SuperFlash Command Register (SFCM) (i.e., "MOV SFCM, 3Bh or MOV SFCM, 0BBh"). This is an "arming command" sequence prior to Program and Erase operations to prevent inadvertent program or erase within the SuperFlash memory. 5.) Move the termination mode FIE and Burst Program command FCM to (SFCM) (i.e. MOV SFCM, 8Ah *or* MOV SFCM, 0Ah). If FIE is set, INT1# will interrupt the system when the program is complete. Otherwise you must poll the system to determine when the program is complete. 6.) Wait for interrupt or poll for end of burst. 7.) If another Burst Program is needed return to step 4 (same row).

The VERIFY BYTE command allows the user to verify that the SST89C54/58/59 has correctly performed an Erase or Program command. The VERIFY BYTE command is initiated as follows:

1.) Move the high order address byte AH to (SFAH). 2.) Move the low order address byte AL to (SFAL). 3.) Move the termination mode FIE and Verify Byte command FCM to (SFCM) (i.e. MOV SFCM, 8Ch *or* MOV SFCM, 0Ch).

Polling

A command that uses the polling method to signify completion must check the BUSY bit (SFCF[3]). Copy the (SFCF) register into temporary memory and mask bit 3. Once it is isolated, the status of the BUSY bit can be checked.

MOVC instruction may also be used for verification of the Programming and Erase operation of the flash memory.

TABLE 5: CONCURRENT PROGRAMMING COMMANDS

Operation	SFAH [7:0]	SFAL [7:0]	SFDT [7:0]	SFCM[1] [7:0]	SFCM[2] [7:0]
1 CHIP ERASE	X	X	55h	3Bh/BBh	87h/07h
2 BLOCK ERASE	80h/00h	X	55h	3Bh/BBh	8Fh/0Fh
3 SECTOR ERASE	AH	X	X	3Bh/BBh	8Bh/0Bh
4 BYTE PROGRAM	AH	AL	DI	3Bh/BBh	8Eh/0Eh
5 BURST PROGRAM	AH	AL	DI	3Bh/BBh	8Ah/0Ah
6 VERIFY (Read) BYTE	AH	AL	DO	3Bh/BBh	8Ch/0Ch

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Notes: X = Don't care; AL = Address low order byte; AH = Address high order byte;
DI = Data Input; DO = Data Output
1. The value 3Bh or BBh for SFCM is needed before performing any Program and Erase operations. It serves as an "arming command" sequence
2. SFCM(7:0) 8X/0X = Interrupt/Polling Enable for flash operation completion

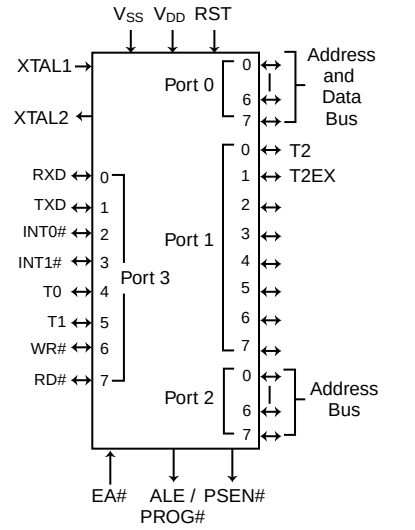

FIGURE 12: NORMAL MODE I/O ASSIGNMENT

TIMERS/COUNTERS

The SST89C54/58/59 have three 16-bit registers that can be used as either timers or event counters. The three Timers/Counters are the Timer 0 (T0), Timer 1 (T1), and Timer 2 (T2) registers. These three registers are located in the SFR as pairs of 8-bit registers. The low byte of the T0 register is stored in the Timer 0 LSB (TL0) special function register and the high byte of the T0 register is stored in the Timer 0 MSB (TH0) special function register. The low byte of the T1 register is stored in the Timer LSB (Tl1) special function register and the high byte of the T1 register is stored in the Timer 1 MSB (TH1) special function register. The low byte of the T2 register is stored in the Timer 2 LSB (TL2) special function register and the high byte of the T2 register is stored in the Timer 2 MSB (TH2) special function register. Please refer to the SST89C54/58/59 User's Manual for detailed descriptions of the Timers/ Counters.

SERIAL I/O (USART)

The SST89C54/58/59 Serial I/O ports is a full duplex port that allows data to be transmitted and received simultaneously in hardware by the transmit and receive registers, respectively, while the software is performing other tasks. The Serial I/O port performs the function of an USART (Universal Synchronous/Asynchronous receiver/transmitter) chip. The transmit and receive registers are both located in the Serial Data Buffer (SBUF special function register. Writing to the SBUF register loads the transmit register, and reading from the SBUF register obtains the contents of the receive registers.

The Serial I/O port has four modes of operation which are selected by the Serial Port Mode Specifier (SM0 and SM1) bits of the Serial Port Control (SCON) special function register. In all four modes, transmission is initiated by any instruction that uses the SBUF register as a destination register. Reception is initiated in mode 0 when the Receive Interrupt (RI) flag bit of the Serial Port Control (SCON) special function register is cleared and the Reception Enable/ Disable (REN) bit of the SCON register is set. Reception is initiated in the other modes by the incoming start bit if the REN bit of the SCON register is set. Please refer to the SST89C54/58/59 User's Manual for a more detailed description of the USART.

INTERRUPT

The SST89C54/58/59 provide 6 interrupt sources, which include two external interrupts (INT0# and INT1#), three Timer/Counter Interrupts (TF0, TF1, and TF2), and one from the serial port (SI or TI). The Interrupt Enable (IE) special function register is the source of the interrupts. Each of the bits that generate the interrupts may be set or cleared by software with the same result as setting or clearing the bits through hardware. Therefore, interrupts may be generated or canceled by software. Also, interrupts can be enabled or disabled by setting or clearing individual bits of the IE register. The SST89C54/58/59 also contain a global enable bit which allows all of the interrupts to be enabled or disabled by setting or clearing the EA bit of the IE register. Please refer to the SST89C54/58/59 User's Manual for a more detailed description of the Interrupt System.

Interrupt Priority Levels

Individual interrupts can be programmed as a low- priority or a high priority interrupt by setting or clearing the corresponding bit in the Interrupt Priority (IP) special function register. A 0 value is designated a low priority and a 1 value is the high priority. Please refer to the SST89C54/58/59 User's Manual for a more vivid description about Interrupt Priority Levels.

WATCHDOG TIMER

The SST89C54/58/59 offer an enhanced programmable watchdog timer for fail safe protection against software "hang" and allows an automatic recovery from such software upset.

To protect the system against software "hang", the user's program has to refresh the watchdog timer within a previously programmed time period. If the software fails to do this periodical refresh, an internal hardware reset will be initiated. The software can be designed such that the watchdog times out if the program does not work properly. It also times out if a software error is based on the hardware related problems.

The watchdog timer in the SST89C54/58/59 share the same time base with the flash operation controller. When the flash operation controller is operating, the time base will be re-started by the hardware periodically, hence elongate the time-out period of the watchdog timer. The higher most 8-bits of the time base register are used as the reload register of the watchdog timer.

Figure 13 provides a block diagram of the Watchdog Timer. Two SFRs (WDTC and WDTD) control watchdog timer operation. During idle mode, WDT operation is temporarily suspended, and resumes upon an interrupt exit from idle.

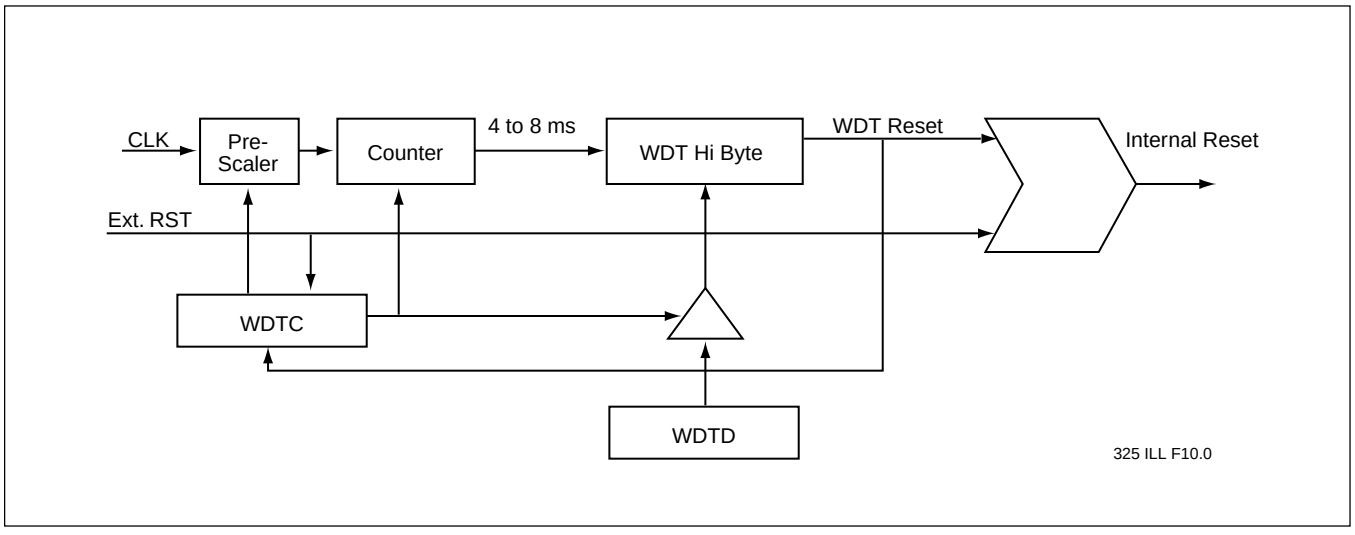

FIGURE 13: BLOCK DIAGRAM OF PROGRAMMABLE WATCHDOG TIMER

SECURITY LOCK

Security lock is a mechanism to prevent program code corruption resulting from accidental sector or block erasing and programming to the internal flash memory locations. Security lock also prevents software piracy by disabling the read access of the internal flash memory contents through port pins and accumulator (Acc) register.

Location of the security byte

The security byte is located in the highest address location, FFFFh, of the The SST89C54/58/59 program memory space.

Activation of the security lock

There are two internal flash memory blocks in The SST89C54/58/59. The security lock can either lock both flash memory blocks or just lock the upper flash memory block (Block 1) independently.

To activate the security lock on both flash memory blocks, the security byte at location FFFFh is programmed with hexadecimal value of 55h.

To deactivate the security lock on both flash memory blocks, the security byte at location FFFFh is programmed with hexadecimal value of FFh. The default value of the security byte set from the factory and after erase is FFh and the security lock is deactivated on both flash memory blocks.

To activate the security lock only on the upper flash memory block, Block 1, the security byte at location FFFFh is programmed with hexadecimal value of F5h.

Normal Operation Mode

If the security lock is activated on both flash memory blocks, no concurrent programming is allowed on the flash memory blocks except the CHIP ERASE operation, which erases both flash memory blocks including the security byte.

If the security lock is activated only on the upper flash memory block, Block 1, concurrent programming from internal program code execution (from Block 1) is allowed on the lower flash memory block (Block 0).

If the security lock is activated, the following concurrent programming operation commands are not allowed on the locked flash memory blocks:

- Sector Erase
- Block Erase
- Byte Program
- Burst Program
- Verify Byte

Only CHIP ERASE operation can deactivate or change the level of the security lock after it is set. CHIP ERASE will set the security byte to the value of FFh. The concurrent programming operation with program code execution from either internal flash memory or external program code storage can write to the security byte and activate the security lock.

If the security lock is activated either on both of the flash memory blocks or just on the upper flash memory block, i.e. the value of the security byte is not FFh, the “move constant” (MOVC) instruction is prevented from accessing constants in locked flash memory locations when the program counter (PC) is pointing at addresses of an unlocked flash memory location or an external memory location (see Table 7). Therefore, the contents of the internal flash memory cannot be read undesirably when any level of security lock is activated.

TABLE 6: SECURITY LOCK OPTIONS

Sec Byte	SFCF [6:5]	EA#	blk Sel	Block Erase	Sector Erase	Byte Program	Burst Program	Verify Byte	Description
FF	00	X	X	Y	Y	Y	Y	Y	no lock, (default)
55	11	X	X	N	N	N	N	N	both locked
F5	01	X	0	Y	Y	Y	Y	Y	only block 1 (4KB) is locked
		X	1	N	N	N	N	N	
05	10	X	1	N	N	N	N	N	both locked but block 0 is programmable by software code residing in block 1
		0	0	N	N	N	N	N	
		1	0	Y	Y	Y	Y	Y	

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NOTE: **SecByte** = Value of Security Byte at location FFFFh; **SFCF(6:5)** = Bit 5 and 6 of SFCF register; **EA#** = Ext. Access enable input pin: 1 – running code from internal memory, 0 – running code from external enable; **blkSel** = Block Select signal (internal): 1 – block 1 (4Kx8), 0 – block 0 (32Kx8); **X** = don’t care; **Y** = command allowed; **N** = command not allowed.

TABLE 6: INTERNAL AND EXTERNAL PROGRAM MEMORY ACCESS WITH SECURITY LOCK ACTIVATED (THE VALUE OF THE SECURITY BYTE IS NOT FFH).

MOVC INSTRUCTIONS fetched from	ACCESS TO LOCKED PROGRAM MEMORY	ACCESS TO UNLOCKED OR EXTERNAL PROGRAM MEMORY
locked program memory	YES	YES
unlocked or external program memory	NO	YES

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External Host Operation Mode

If the security lock is activated, the following external host mode commands are not allowed on the locked flash memory blocks:

- Sector Erase
- Block Erase
- Byte Program
- Burst Program
- Verify Byte

Only CHIP ERASE operation can deactivate or change level of the security lock after it is set. CHIP ERASE will set the security byte to the value of FFh. The concurrent programming operation with program code execution from either internal flash memory or external program code storage can write to the security byte and activate the security lock.

RESET

A system reset initializes the MCU and begins program execution at program memory location 0000h. The reset input for the SST89C54/58/59 is the RST pin. In order to reset the SST89C54/58/59, a logic level high must be applied to the RST pin for at least two machine cycles (24 clocks), after the oscillator becomes stable. ALE, PSEN# are weakly pulled high during reset. During reset, ALE and PSEN# output a high level in order to perform correct reset. This level must not be affected by external element. A system reset will not affect the 256 bytes of on-chip RAM while the SST89C54/58/59 is running, however, the contents of the on-chip RAM during power up are indeterminate. All Special Function Registers (SFR) return to their reset values, which are outlined in Tables 9A to 9E.

Power-On Reset

At initial power up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has written one's all the pins. Powering up the device without a valid reset could cause the CPU to start executing instructions from an indeterminate location. Such undefined states may inadvertently corrupt the code in the flash.

To ensure a good power-on reset, it is required that the V_{DD} rise time does not exceed 1 ms and the oscillator start up time does not exceed 10 ms. Figure 15 shows the maximum delay time allowed between initial power up and reset. V_{DD} should lag no more than 10 ns behind RST at voltages above 1.4 V. A common method to extend the RST signal is to implement a RC circuit by connecting the RST pin to V_{DD} through a 10 µF capacitor and to V_{SS} through an 8.2K resistor as shown in Figure 14. This method maintains the necessary relationship between V_{DD} and RST to avoid programming at an indeterminate location, which may cause code corruption in the flash.

In addition to the external Power-On Reset circuit, the SST89C54/58/59 have an internal fail-safe mechanism that protects the flash during a Power-On Reset or during a Brown-Out condition. The internal Power-On Reset/ Brown-Out circuit further prevents inadvertent information to be programmed to the flash. It should be noted that the internal Power-On Reset/ Brown-Out circuit only provides additional protection for the flash, an external circuit is still necessary to ensure both the flash and the CPU resets properly.

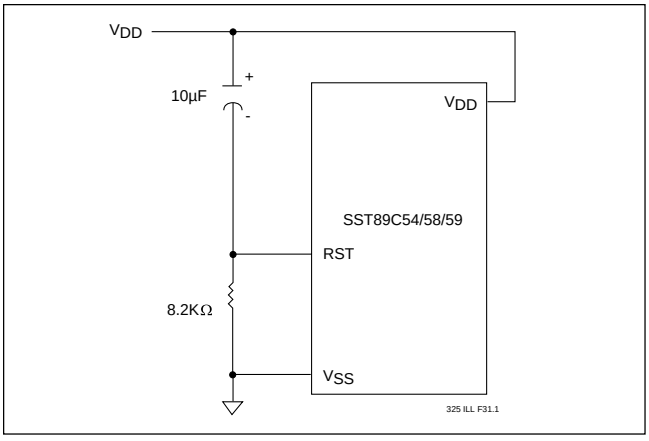

FIGURE 14: POWER-ON RESET CIRCUIT

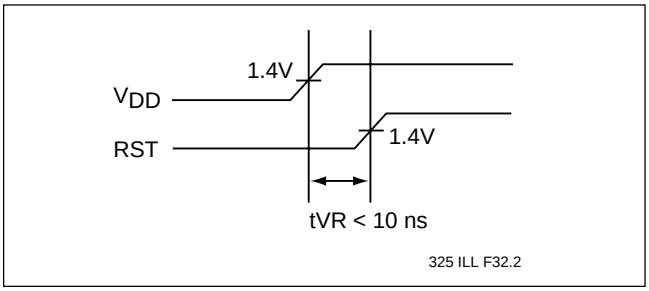

FIGURE 15: MINIMUM V_{DD} TO RST FOR POWER-ON RESET

POWER-SAVING MODES

The FlashFlex51 Family of MCUs provide three power-saving modes of operation for applications where power consumption is critical. The three power-saving modes are Idle, Power Down and Standby modes. In the Idle mode, the current drain is approximately 25% of the current drain when the device is fully active, and the clock signal is gated off to the MCU, but remains operating to all other functions within the device (e.g., interrupts, timers and serial port). Idle mode is initiated by software. The Power Down and Standby modes are similar, both reduce device current drain to approximately 15 micro-amperes. However, entry to the two modes is different, Power Down mode is entered by software, while Standby mode is controlled by hardware (gating on and off the system clock). Table 8 below outlines the different power-saving modes, indicating entry and exit procedures and functionality within the MCU during the power-saving modes.

TABLE 8: FLASHFLEX51 POWER SAVING MODES

Mode	Initiated by	Current Drain	State of MCU	Exited by
Idle Mode	Software (Set IDL bit in PCON)	25% of I_{DD} level when device is fully active	CLK running. Interrupts, serial port and timers/ counters continue to be clocked, but the MCU clock is gated off. ALE and PSEN# sigs at a HIGH level during Idle. All registers remain unchanged.	Enabled interrupt or hardware reset. Start of interrupt clears IDL bit and exits Idle mode, and after the ISR RETI instruction, the program resumes nomal processing (note 1). A hardware reset starts the device similar to power-on reset. (See note 2.)
Power Down Mode	Software (Set PD bit in PCON)	Approximately 15 microamps. And V_{DD} can be reduced by ext. hardware to 2V during (after entry and before exit) power down mode.	CLK gated Off to MCU, serial port, timer/ counters and internal interrupts. On-chip SRAM and SFR data is maintained. ALE and PSEN# signals at a LOW level during Power Down.	External interrupt or hardware reset. From external interrupt, on-chip RAM and SFRs retain their data. Once the ISR ends, normal processing (note 1) resumes. A hardware reset starts the device similar to power-on reset.
Standby Mode	External hardware gates OFF the external clock input to the MCU. This gating shall be synchronized with an input clock transition (low-to-high or high-to-low).	Approximately 15 microamps. And V_{DD} can be reduced by ext. hardware to 2V during (after entry and before exit) power down mode.	Internal state of the MCU is totally preserved.	Gate ON external clock, and begin executing at next clock in normal processing.

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Notes: 1. Normal processing refers to program execution beginning at the instruction following the one that invoked this particular power reduction mode.
2. When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. If needed in a specific application, a user could consider placing two or three NOP instructions after the instructions that invoke idle mode to eliminate any problems

MEMORY ORGANIZATION

The The SST89C54/58/59 has separate address spaces for program and data memory.

Program Memory

There are two internal flash memory blocks in the SST89C54/58/59. The lower flash memory block (Block 0) has 16/32/60 KByte and occupies the address space 0000h to 3FFFh/7FFFh/EFFFh. The upper flash memory block (Block 1) has 4 KByte and occupies the address space F000h to FFFFh.

The 16 K by 8 SuperFlash block is organized as 256 rows (128 of 128-byte sections/pages, 8 X-address lines) and 256 columns (64 bytes per row, 6 Y-address lines).

The 32 K by 8 SuperFlash block is organized as 512 rows (256 of 128-byte sectors/pages, 9 X-address lines) and 512 columns (64 bytes per row, 6 Y-address lines).

The 60 K by 8 SuperFlash block is organized as 960 rows (480 of 128-byte sectors/pages, 10 X-address lines) and 960 columns (64 bytes per row, 6 Y-address lines).

The 4 K by 8 SuperFlash block is organized as 128 rows (64 of 64-byte sectors/pages, 7 X-address lines) and 256 columns (32 bytes per row, 5 Y-address lines).

In the Normal Mode, the upper flash memory block is hidden from the user for code fetching when the chip is powered up even when the internal code execution is enabled (EA#=1). However, the upper flash memory is always visible through the SuperFlash mailbox registers (SFCM, SFCF, SFAL, SFAH and SFDT) for the concurrent programming operation. In order to make the upper flash memory block visible for code fetching, the user has to set the MSB of the SuperFlash Configuration mailbox register, SFCF at SFR address B6h, i.e. SFCF:7 = 1.

The lower flash memory block is always visible. The MCU starts the program execution from it after the hardware reset, if the external enable is not asserted (EA#=1). Please see Figure 16, 17 and 18 for details of the three program memory options.

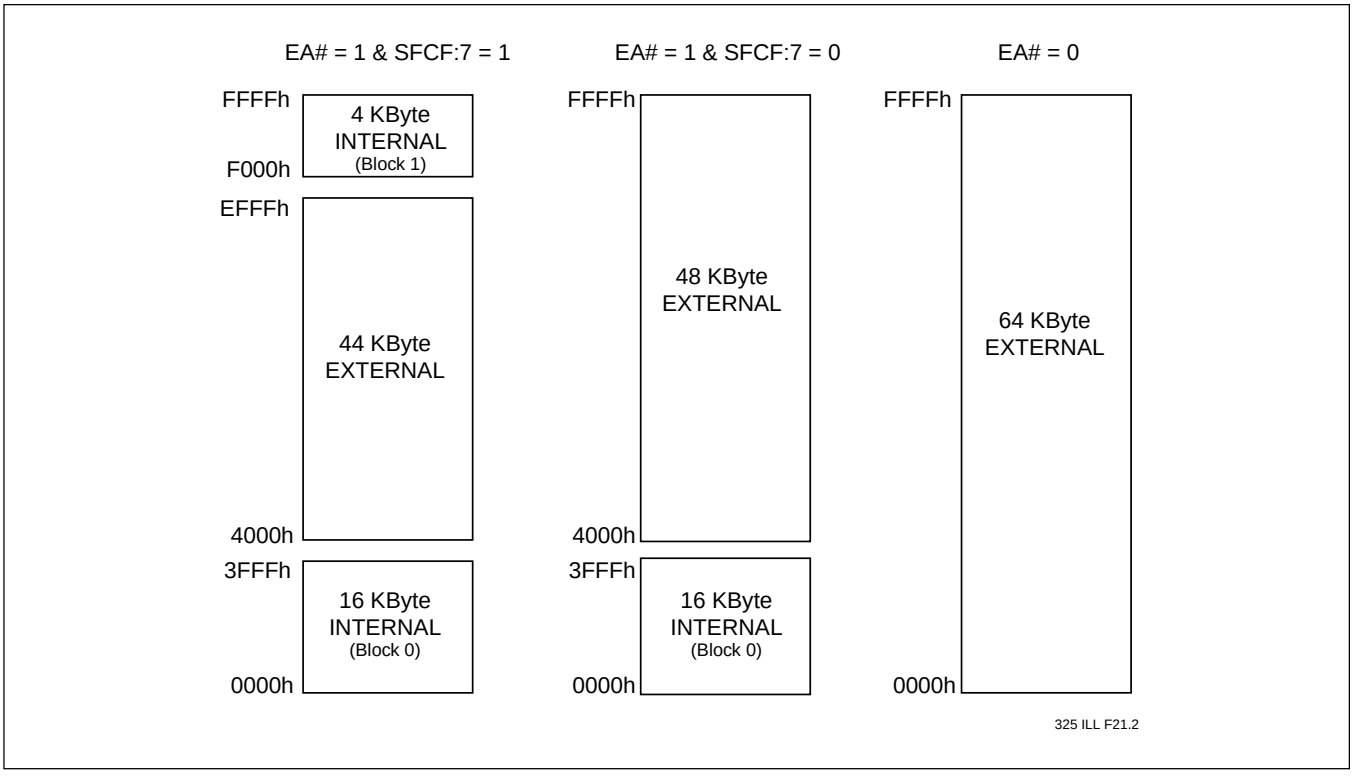

FIGURE 16: SST89C54 PROGRAM MEMORY ORGANIZATION

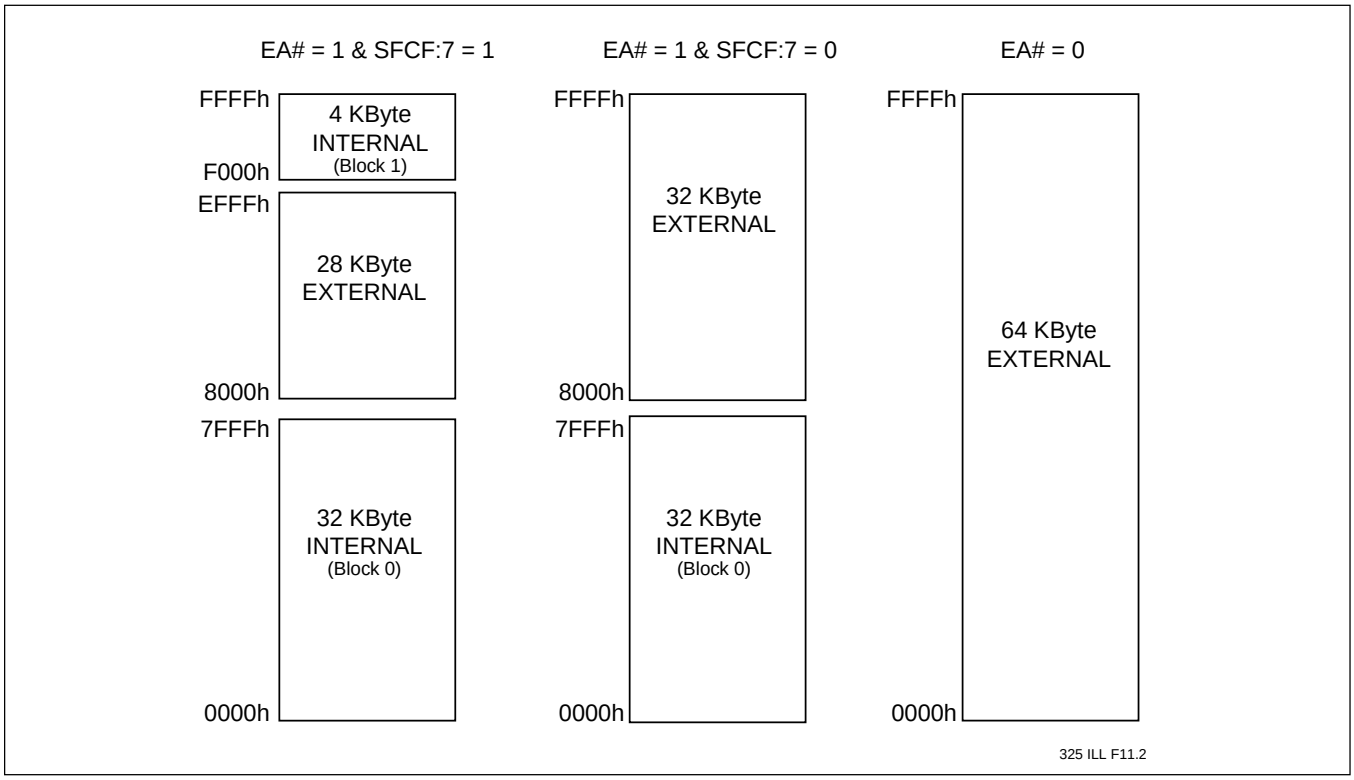

FIGURE 17: SST89C58 PROGRAM MEMORY ORGANIZATION

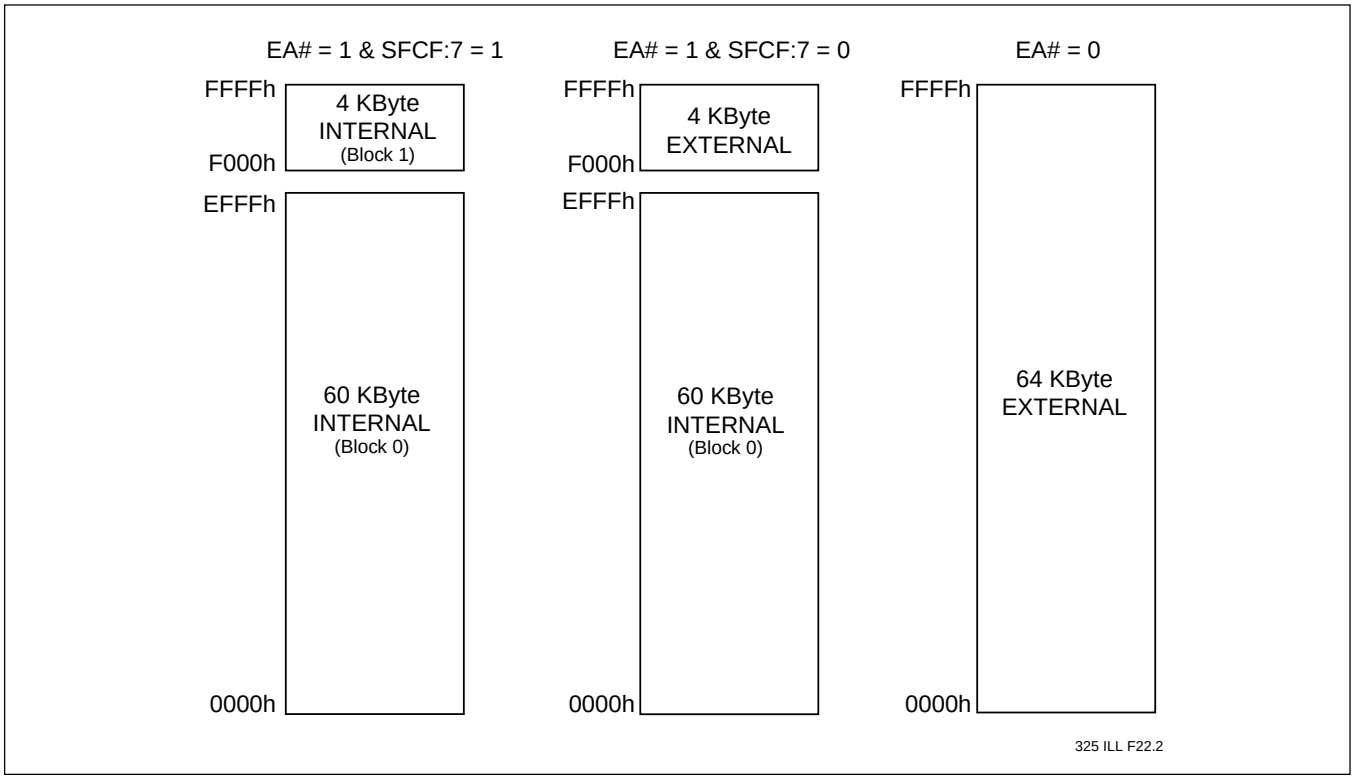

FIGURE 18: SST89C59 PROGRAM MEMORY ORGANIZATION

Data Memory

SST89C54/58/59 have 256 X 8 bits on chip RAM and can address up to 64 KByte of off-chip data memory.

Special Function Registers (SFR)

Most of the unique features of the SST89C5x microcontroller family are controlled by bits in special function registers (SFRs) located in the SST89C5x SFR Memory Map shown below. Individual descriptions of each SFR are provided and Reset values indicated in Tables 9A to 9E.

	8 BYTES								
F8									FF
F0	B*								F7
E8									EF
E0	ACC*								E7
D8									DF
D0	PSW*								D7
C8	T2CON*		RCAP2L	RCAP2H	TL2	TH2			CF
C0	WDTC								C7
B8	IP*								BF
B0	P3*		SFCM	SFAL	SFAH	SFDT	SFCF		B7
A8	IE*								AF
A0	P2*								A7
98	SCON*	SBUF							9F
90	P1*								97
88	TCON*	TMOD	TL0	TL1	TH0	TH1			8F
80	P0*	SP	DPL	DPH			WDTD	PCON	87

SST89C5x SFR Memory Map

* = BIT ADDRESSABLE

All addresses are hexadecimal

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SST89C54/58/59 Special Function Registers

TABLE 9A: CPU RELATED SFRS

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	RESET Value
ACC*	Accumulator	E0h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00h
B*	B Register	F0h	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00h
PSW*	Program Status Word	D0h	CY	AC	F0	RS1	RS0	OV	F1	P	00h
SP	Stack Pointer	81h	SP[7:0]								07h
DPL	Data Pointer Low 0	82h	DPL[7:0]								00h
DPH	Data Pointer High 0	83h	DPH[7:0]								00h
IE*	Interrupt Enable	A8h	EA	-	ET2	ES0	ET1	EX1	ET0	EX0	00h
IP*	Interrupt Priority	B8h	-	-	PT2	PS	PT1	PX1	PT0	PX0	xx000000B

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TABLE 9B: FLASH MEMORY PROGRAMMING SFRS

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	RESET Value
SFCF	SuperFlash Configuration	B6h	VIS	SECD		-	BUSY	-	-	-	00h
SFCM	SuperFlash Command	B2h	FIE	-	-	-	FCM				00h
SFDT	SuperFlash Data	B5h	SuperFlash Data Register								00h
SFAL	SuperFlash Address Low	B3h	SuperFlash Low Order Byte Address Register – A7 to A0 (SFAL)								00h
SFAH	SuperFlash Address High	B4h	SuperFlash High Order Byte Address Register – A15 to A8 (SFAH)								00h

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TABLE 9C: CHIP OPERATIONAL SFRS

PCON	Power Control	87h	SMOD	-	-	-	GF1	GF0	PD	IDL	0xxx0000B
WDTC	Watchdog Timer Control	C0h	-	-	-	-	WDRE	WDTS	WDT	SWDT	X0h
WDTD	Watchdog Timer Data/Reload	86h	WDRL								00h

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TABLE 9D: TIMER/COUNTERS SFRS

TMOD	Timer/Counter Mode Control	89h	Timer 1				Timer 0				00h
			GATE	C/T#	M1	M0	GATE	C/T#	M1	M0	
TCON*	Timer / Counter Control	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h
TH0	Timer 0 MSB	8Ch	TH0[7:0]								00h
TL0	Timer 0 LSB	8Ah	TL0[7:0]								00h
TH1	Timer 1 MSB	8Dh	TH1[7:0]								00h
TL1	Timer 1 LSB	8Bh	TL1[7:0]								00h
T2CON*	Timer / Counter 2 Control	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00h
TH2	Timer 2 MSB	CDh	TH2[7:0]								00h
TL2	Timer 2 LSB	CCh	TL2[7:0]								00h
RCAP2H	Timer 2 Capture MSB	CBh	RCAP2H[7:0]								00h
RCAP2L	Timer 2 Capture LSB	CAh	RCAP2L[7:0]								00h

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TABLE 9E: INTERFACE SFRS

SBUF	Serial Data Buffer	99h	SBUF[7:0]								Indeterminate
SCON*	Serial Port Control	98h	SM0	SM1	SM2	REN	TB8	RB8	T1	R1	00h
P0*	Port 0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFh
P1*	Port 1	90h	-	-	-	-	-		T2EX	T2	FFh
P2*	Port 2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	FFh
P3*	Port 3	B0h	RD#	WR#	T1	T0	INT1#	INT0#	TXD0	RXD0	FFh

* SFRs are bit addressable

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CLOCK INPUT OPTIONS

Shown in Figure 19 are the input and output of an inverter amplifier, which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven. The internal clocking circuitry is through a flip-flop (divide-by-two). Minimum and maximum high and low times specified on the data sheet must be observed, but there are no requirements on the duty cycle of the external clock signal.

At start-up, the external oscillator may encounter up to a 100 pF load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 20 pF once the external signal meets the V_{IL} and V_{IH} specifications.

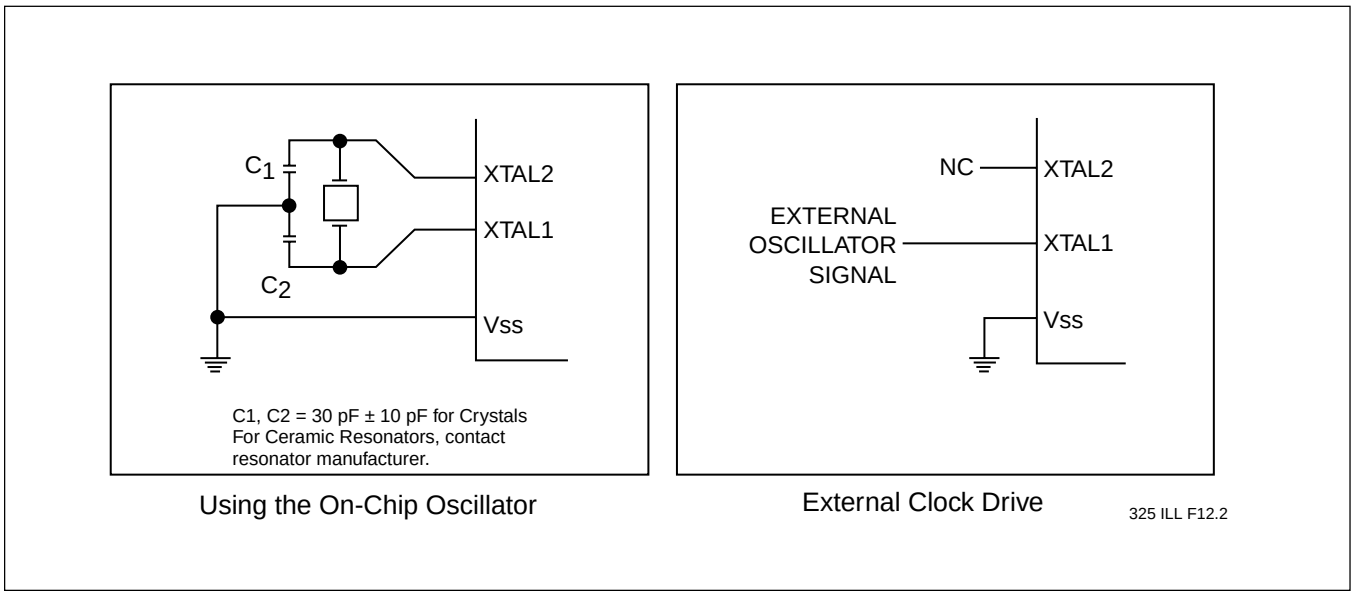

FIGURE 19: OSCILLATOR CHARACTERISTICS

ELECTRICAL SPECIFICATION

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Ambient Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to + 150°C
Voltage on EA# Pin to V_{SS} ..... -0.5V to +14.0V
Transient Voltage (<20ns) on Any Other Pin to V_{SS} ..... -1.0V to +6.5V
Maximum I_{OL} per I/O Pin ..... 15 mA
Package Power Dissipation Capability (T_A = 25°C) 1.5W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note (1) Outputs shorted for no more than one second. No more than one output shorted at a time.
(Based on package heat transfer limitations, not device power consumption.)

NOTICE: This specification contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

Operation Range

TABLE 10: OPERATING RANGE

Symbol	Description	Min.	Max	Unit
T_A	Ambient Temperature Under Bias			
	Standard	0	+70	°C
	Industrial	-40	+85	°C
V_{DD}	Supply Voltage	2.7	5.5	V
f_{OSC}	Oscillator Frequency	0	33	MHz
	For Concurrent Programming	0.25	33	MHz

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TABLE 11: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	10,000	Cycles	MIL-STD-883, Method 1033
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	2000	Volts	JEDEC Standard A114
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	300	Volts	JEDEC Standard A115
I_{LTH}[1]	Latch Up	100+I_{DD}	mA	JEDEC Standard 78

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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TABLE 12A: DC ELECTRICAL CHARACTERISTICS

T_{AMB} = O°C TO + 70°C OR -40°C TO +85°C, 33MHZ DEVICES; 5V ±10%; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
V_{IL}	Input Low Voltage	4.5 < V_{DD} < 5.5	-0.5	0.2V_{DD} - 0.1	V
V_{IH}	Input High Voltage (ports 0,1,2,3)		0.2 V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)		0.7 V_{DD}	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V_{DD} = 4.5 V I_{OL} = 16 mA		1.0	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3) [5]	V_{DD} = 4.5 V I_{OL} = 100 µA [1] I_{OL} = 1.6 mA [1] I_{OL} = 3.5 mA [1]		 0.3 0.45 1.0	 V V V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#) [4,5]	V_{DD} = 4.5 V I_{OL} = 200 µA [1] I_{OL} = 3.2 mA [1] I_{OL} = 7.0 mA [1]		 0.3 0.45 1.0	 V V V
V_{OH}	Output High Voltage (Ports 1, 2, 3) [2]	V_{DD} = 4.5 V I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA	 V_{DD} - 0.3 V_{DD} - 0.7 V_{DD} – 1.5		 V V V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode, ALE, PSEN#) [2]	V_{DD} = 4.5 V I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA	 V_{DD} - 0.3 V_{DD} - 0.7 V_{DD} – 1.5		 V V V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.4V	-1	-50	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3) [3]	V_{IN} = 2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	0.45 < V_{IN} < V_{DD}-0.3		±10	µA
R_{RST}	RST Pulldown Resistor		40	225	kΩ
C_{IO}	Pin Capacitance	@ 1 MHz, 25°C		2	pF
I_{DD}	Power Supply Current [6] Concurrent Mode @ 12 MHz @ 33 MHz Active Mode @ 12 MHz @ 33 MHz Idle Mode @ 12 MHz @ 33 MHz Standby Mode Power Down Mode	V_{DD} = 5V V_{DD} = 2V	 	 70 88 25 45 9.5 15.5 50 50	 mA mA mA mA mA MA µA µA

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TABLE 12B: DC ELECTRICAL CHARACTERISTICS

T_{AMB} = O°C TO + 70°C OR -40°C TO +85°C, 12 MHZ DEVICES; 3V ±10%; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
V_{IL}	Input Low Voltage	2.7 < V_{DD} < 3.3	-0.5	0.7	V
V_{IH}	Input High Voltage (ports 0,1,2,3)		0.2 V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)		0.7 V_{DD}	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V_{DD} = 2.7 V I_{OL} = 16 mA		1.0	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3) [5]	V_{DD} = 2.7 V I_{OL} = 100 µA [1] I_{OL} = 1.6 mA [1] I_{OL} = 3.5 mA [1]		0.3 0.45 1.0	 V V V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#) [4,5]	V_{DD} = 2.7 V I_{OL} = 200 µA [1] I_{OL} = 3.2 mA [1] I_{OL} = 7.0 mA [1]		0.3 0.45 1.0	 V V V
V_{OH}	Output High Voltage (Ports 1, 2, 3) [2]	V_{DD} = 2.7 V I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA	 V_{DD} - 0.3 V_{DD} - 0.7 V_{DD} – 1.5		 V V V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode, ALE, PSEN#) [2]	V_{DD} = 2.7 V I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA	 V_{DD} - 0.3 V_{DD} - 0.7 V_{DD} – 1.5		 V V V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.4V	-1	-50	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3) [3]	V_{IN} = 2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	0.45 < V_{IN} < V_{DD}-0.3		±10	µA
R_{RST}	RST Pulldown Resistor		40	225	kΩ
C_{IO}	Pin Capacitance	@ 1 MHz, 25°C		2	pF
I_{DD}	Power Supply Current [6] Concurrent Mode Active Mode Idle Mode Standby Mode Power Down Mode	V_{DD} = 3 V V_{DD} = 2 V		 70 18 6.5 50 50	 mA mA mA µA µA

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NOTES:

1. Capacitive loading on Ports 0 & 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and Ports 1 & 3. The noise due to external bus capacitance discharging into the Port 0 & 2 pins when the pins make 1 -to- 0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. Capacitive loading on Ports 0 & 2 may cause the V_{OH} on ALE and PSEN# to momentarily fall below the V_{DD} - 0.7 specification when the address bits are stabilizing.
3. Pins of Ports 1, 2 & 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when Vin is approximately 2V.
4. Load capacitance for Port 0, ALE & PSEN#= 100pF, load capacitance for all other outputs= 80pF.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum I_{OL} total for all outputs: 71mA
   If I_{OL} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
6. See Figures 20, 21, 22 and 23 for test conditions. Minimum V_{DD} for Power Down is 2 V.

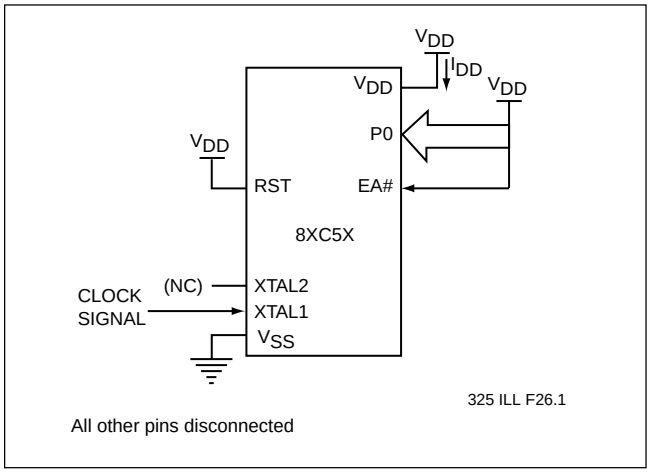

FIGURE 20: I_{DD} TEST CONDITION, ACTIVE MODE

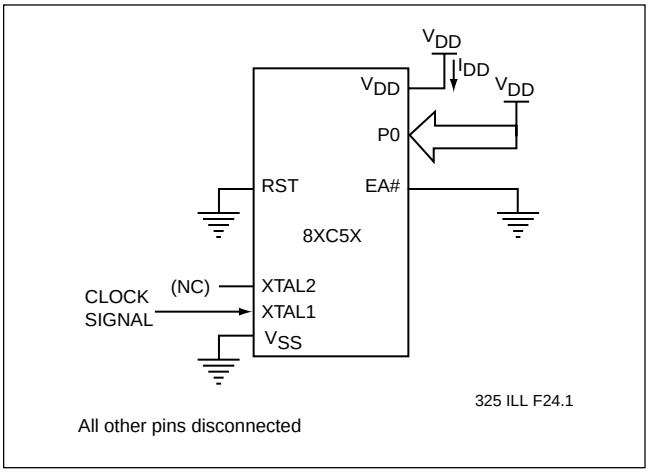

FIGURE 21: I_{DD} TEST CONDITION, IDLE MODE

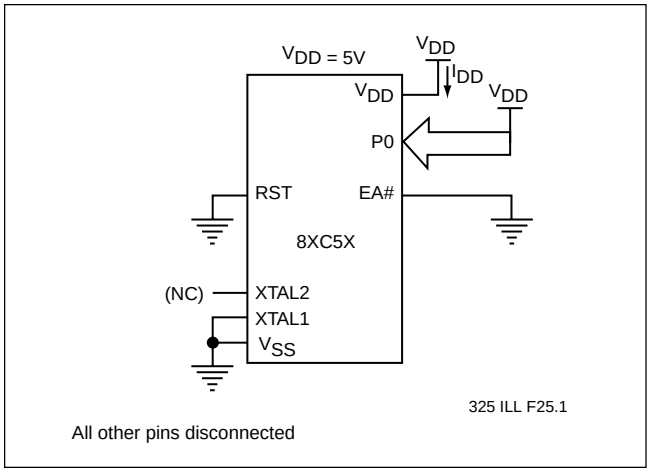

FIGURE 22: I_{DD} TEST CONDITION, POWER DOWN MODE

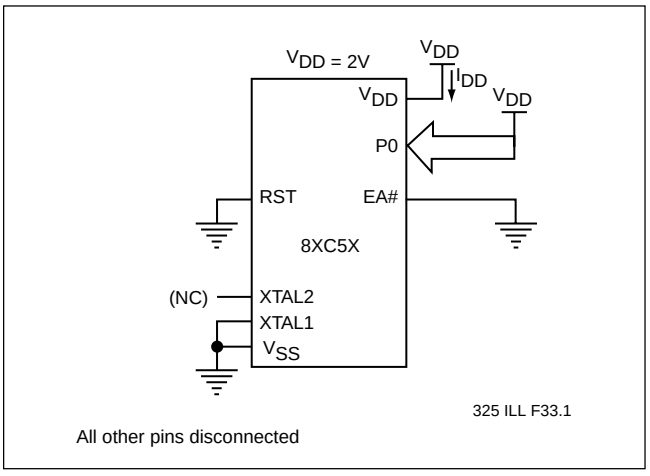

FIGURE 23: I_{DD} TEST CONDITION, STANDBY MODE

Preliminary Specifications

AC ELECTRICAL CHARACTERISTICS

AC Characteristics: (Over Operating Conditions; Load Capacitance for Port 0, ALE, and PSEN# = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

TABLE 13: AC ELECTRICAL CHARACTERISTICS

T_{AMB} = 0°C TO +70°C OR -40°C TO +85°C, V_{DD} = 3V ±10% @ 12 MHZ, 5V ±10% @ 33 MHZ, V_{SS} = 0

Symbol	Parameter	Oscillator						Units
		12 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min.	Max.	
1/tCLCL	Oscillator Frequency					0	33	MHz
tLHLL	ALE Pulse Width	127		20		2tCLCL - 40		ns
tAVLL	Address Valid to ALE Low	43		5		tCLCL - 40 tCLCL - 25		ns ns
tLLAX	Address Hold After ALE Low	53		5		tCLCL - 30 tCLCL - 25		ns ns
tLLIV	ALE Low to Valid Instr In		234		56		4tCLCL - 100 4tCLCL - 65	ns ns
tLLPL	ALE Low to PSEN# Low	53		5		tCLCL - 30 tCLCL - 25		ns ns
tPLPH	PSEN# Pulse Width	205		46		3tCLCL - 45		ns
tPLIV	PSEN# Low to Valid Instr In		145		35		3tCLCL - 105 3tCLCL - 55	ns ns
tPXIX	Input Instr Hold After PSEN#					0		ns
tPXIZ	Input Instr Float After PSEN#		59		5		tCLCL - 25 tCLCL - 25	ns ns
tAVIV	Address to Valid Instr In		312		71		5tCLCL - 105 5tCLCL - 80	ns ns
tPLAZ	PSEN# Low to Address Float		10		10		10	ns
tRLRH	RD# Pulse Width	400		82		6tCLCL - 100		ns
tWLWH	Write Pulse Width (WE#)	400		82		6tCLCL - 100		ns
tRLDV	RD# Low to Valid Data In		252		61		5tCLCL - 165 5tCLCL - 90	ns ns
tRHDX	Data Hold After RD#	0		0		0		ns
tRHDZ	Data Float After RD#		107		35		2tCLCL - 60 2tCLCL - 25	ns ns
tLLDV	ALE Low to Valid Data In		517		150		8tCLCL - 150 8tCLCL - 90	ns ns
tAVDV	Address to Valid Data In		585		180		9tCLCL - 165 9tCLCL - 90	ns ns
tLLWL	ALE Low to RD# or WR# Low	200	300	40	140	3tCLCL - 50	3tCLCL + 50	ns
tAVWL	Address to RD# or WR# Low	203		46		4tCLCL – 130 4tCLCL – 75		ns ns
tQVWX	Data Valid to WR# Transition	33		0		tCLCL - 50 tCLCL - 30		ns ns
tWHQX	Data Hold After WR#	33		3		tCLCL - 50 tCLCL - 27		ns ns
tQVWH	Data Valid to WR# High	433		140		7tCLCL - 150 7tCLCL - 70		ns ns
tRLAZ	RD# Low to Address Float		0		0		0	ns
tWHLH	RD# to WR# High to ALE High	43	123	5	55	tCLCL - 40 tCLCL - 25	tCLCL + 40 tCLCL + 25	ns ns
tVR[1]	V_{DD} to Reset					10		ns

Note: 1. Refer to Figure 15 for minimum timing requirements for Power-On Reset.

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AC CHARACTERISTICS

Explanation of Symbols

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address

C: Clock

D: Input data

H: Logic level HIGH

I: Instruction (program memory contents).

L: Logic level LOW or ALE

P: PSEN#

Q: Output data

R: RD# signal

T: Time

V: Valid

W: WR# signal

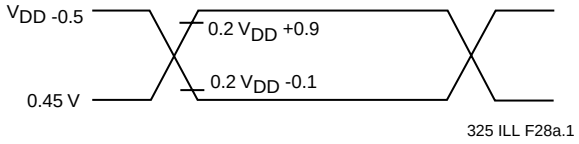
X: No longer a valid logic level

Z: Float

For example:

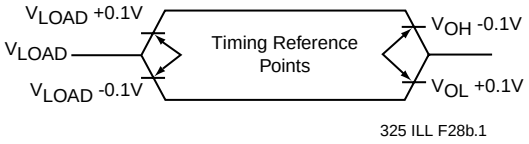
tAVLL=Time from Address Valid to ALE Low

tLLPL=Time from ALE Low to PSEN# Low



AC Inputs during testing are driven at V_{DD} -0.5V for Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

AC TESTING INPUT/OUTPUT



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. I_{OL}/I_{OH} = ± 20mA.

FLOAT WAVEFORM

FIGURE 24: AC TESTING INPUT/OUTPUT, FLOAT WAVEFORM

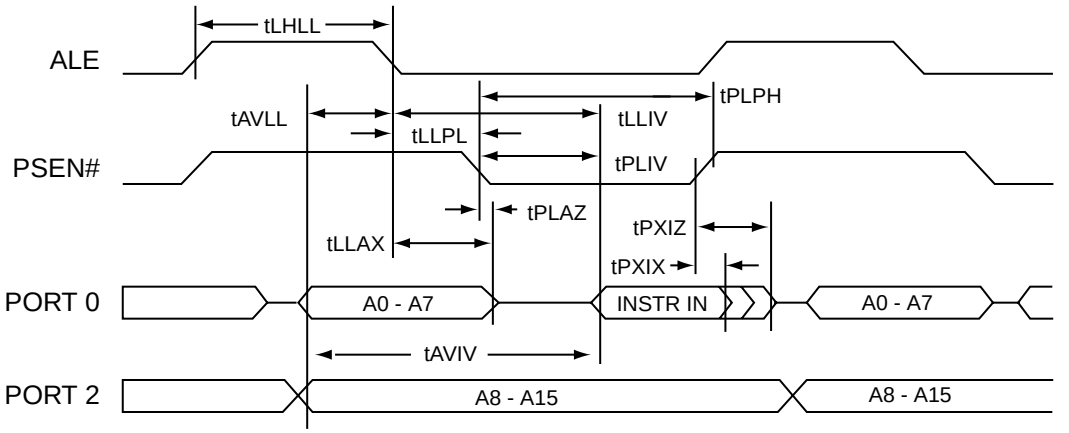


FIGURE 25: EXTERNAL PROGRAM MEMORY READ CYCLE

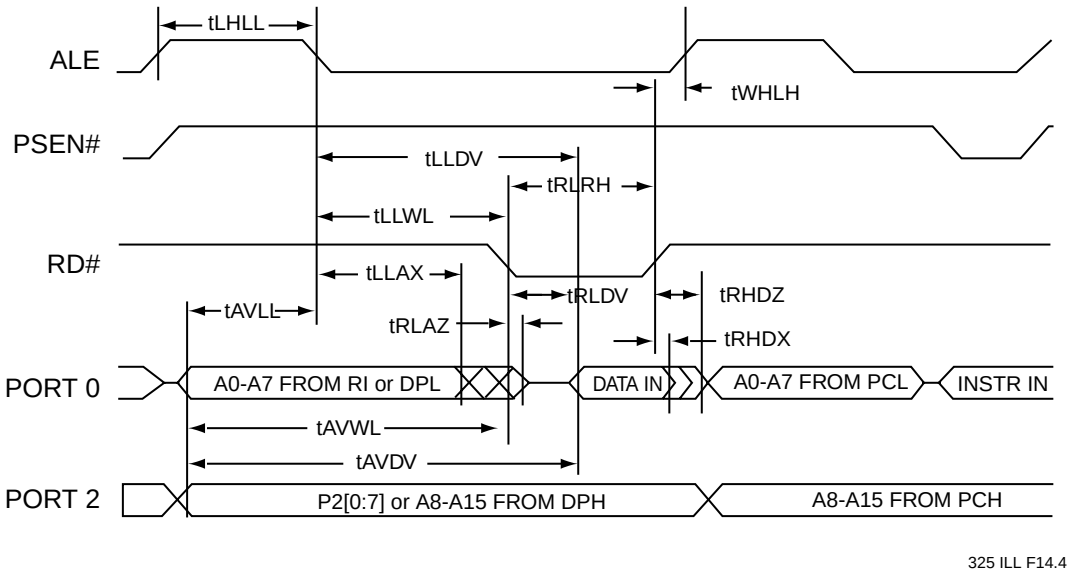


FIGURE 26: EXTERNAL DATA MEMORY READ CYCLE

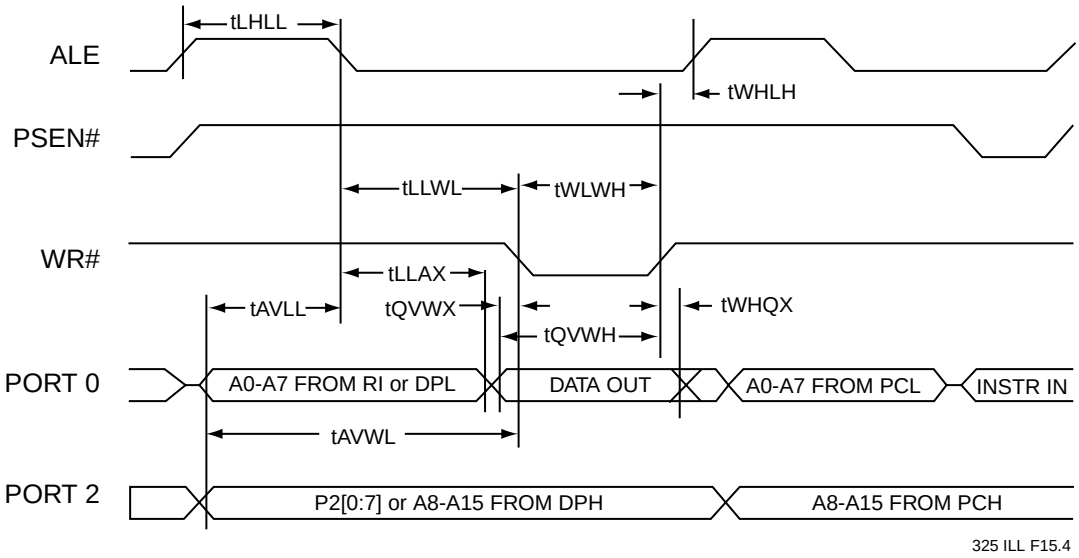


FIGURE 27: EXTERNAL DATA MEMORY WRITE CYCLE

TABLE 14: EXTERNAL CLOCK DRIVE

Symbol	Parameter	Oscillator						Units
		12 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min.	Max.	
1/tCLCL	Oscillator Frequency					0	33	MHz
tCHCX	High Time					0.35tCLCL	0.65tCLCL	ns
tCLCX	Low Time					0.35tCLCL	0.65tCLCL	ns
tCLCH	Rise Time				5		20	ns
tCHCL	Fall Time				5		20	ns

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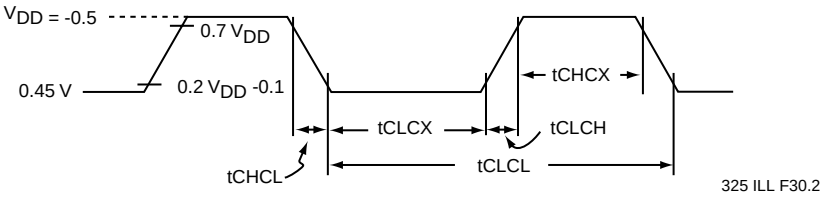

FIGURE 28: EXTERNAL CLOCK DRIVE WAVEFORM

TABLE 15: SERIAL PORT TIMING

Symbol	Parameter	Oscillator						Units
		12 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min.	Max.	
tXLXL	Serial Port Clock Cycle Time	0		0.36		12tCLCL		ms
tQVXH	Output Data Setup to Clock Rising Edge	700		167		10tCLCL - 133		ns
tXHQX	Output Data Hold After Clock Rising Edge	50		10		2tCLCL - 117 2tCLCL - 50		ns ns
tXHDX	Input Data Hold After Clock Rising Edge	0		0		0		ns
tXHDV	Clock Rising Edge to Input Data Valid		700		167		10tCLCL - 133	ns

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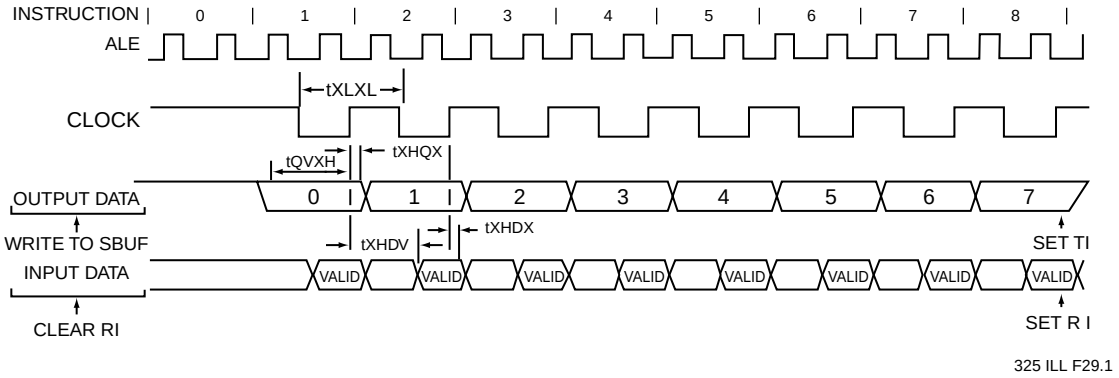

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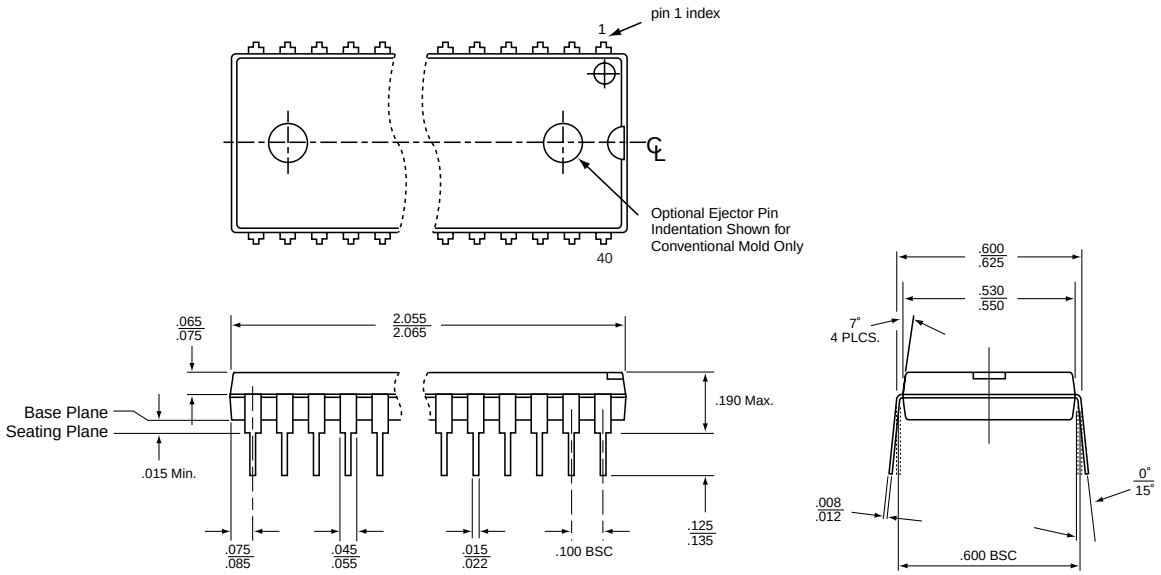
FIGURE 29: SHIFT REGISTER MODE TIMING WAVEFORMS

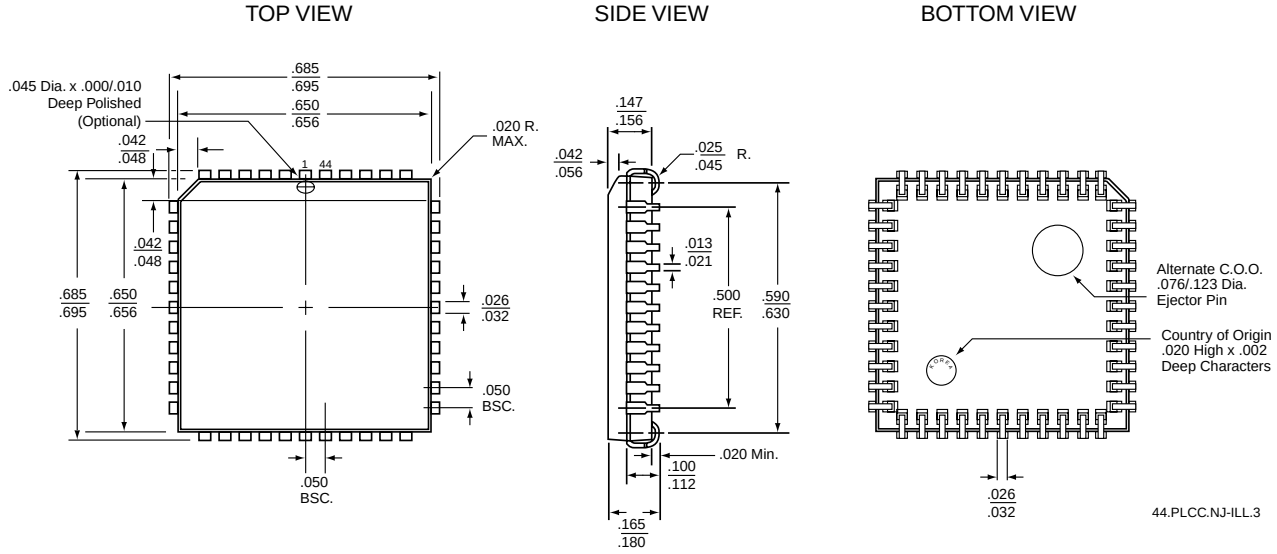
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-011 AC dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

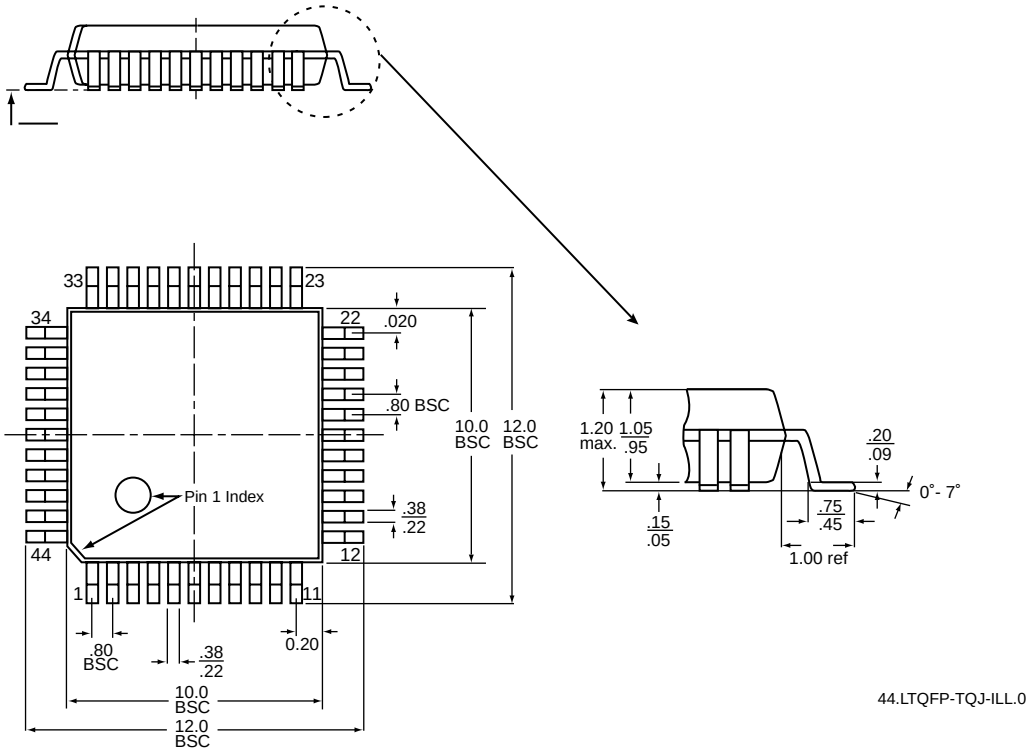
40.pdipPD-ILL.4

40-LEAD PLASTIC DUAL-IN-LINE PACKAGE (PDIP)
SST PACKAGE CODE: PI



Note: 1. Complies with JEDEC publication 95 MS-018 AC dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.

44-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NJ



Note: 1. Complies with JEDEC publication 95 MS-026 BCB dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in mm (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .254 mm.

44-LEAD THIN QUAD FLAT PACK (TQFP)
SST PACKAGE CODE: TQJ

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