第六章　时序逻辑电路

6.1　概述

6.2　时序逻辑电路的分析

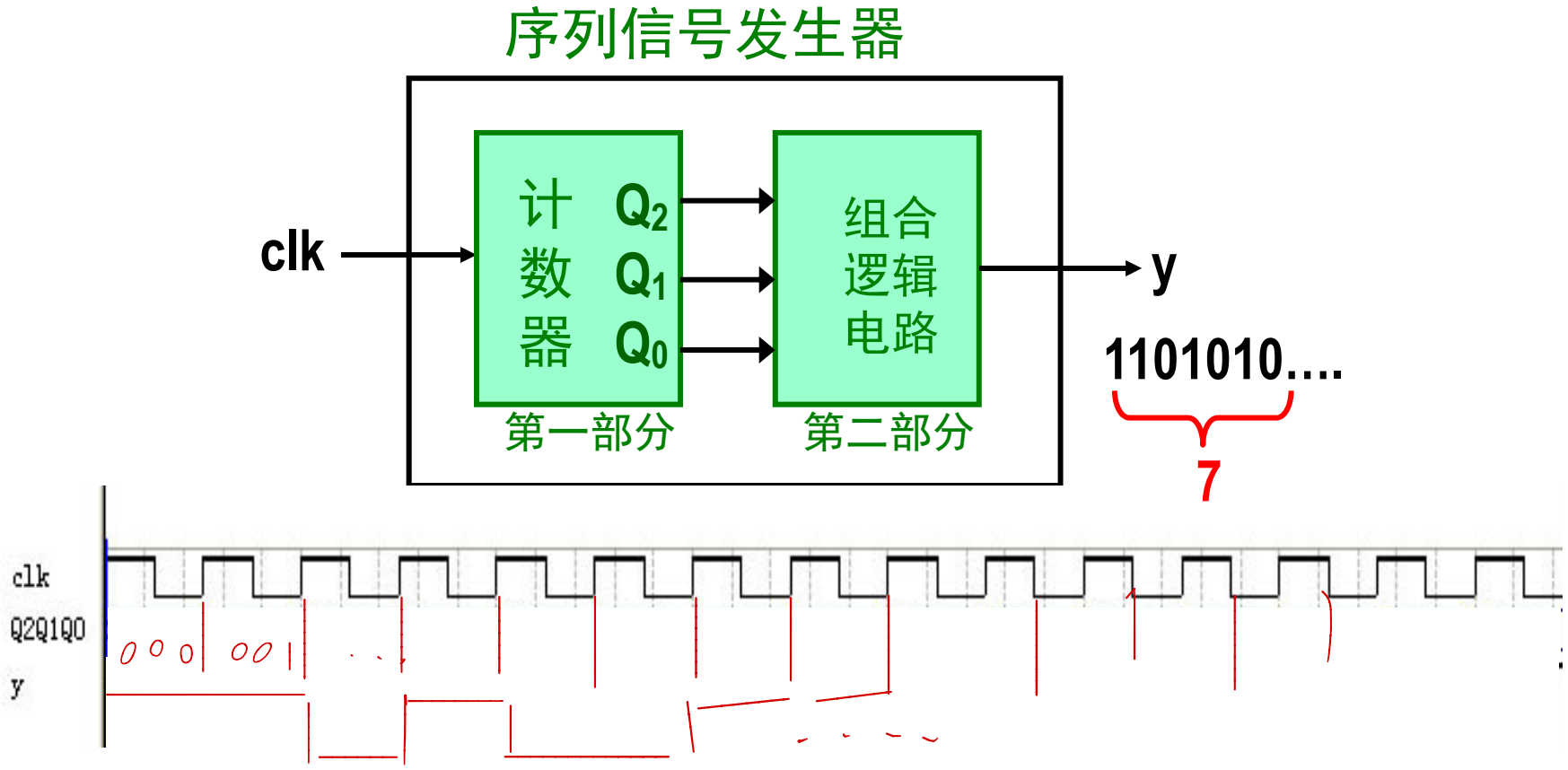
6.3,6.4　常用时序逻辑电路

- 计数器(74161, 74160)
- 寄存器 (74175)
- 移位寄存器 (74194)

6.5　时序逻辑电路的设计

- 计数器
- 序列信号 检测器
- 序列信号 发生器
  - 方法I (计数器+逻辑门)
  - 方法II (计数器+选通器)
  - 方法III (计数器+译码器)
  - 方法IV (移位寄存器+逻辑门)

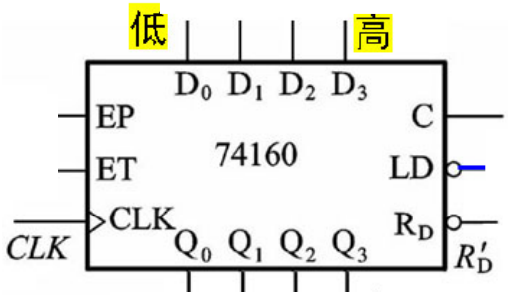
6.5.3 序列信号发生器

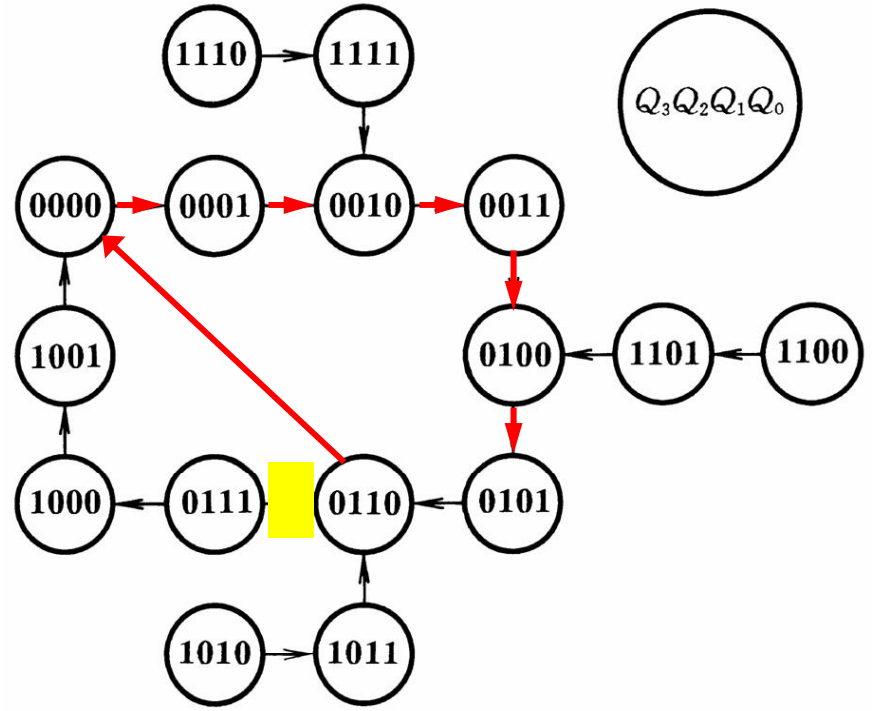

序列信号发生器
clk
计数器
Q_2
Q_1
Q_0
组合逻辑电路
y
1101010....
7
第一部分
第二部分
clk
Q2Q1Q0
y

例1：设计序列信号发生器 1110011（L=7）

方法I：计数器(74160)+逻辑门，置0法

1） 模7计数器

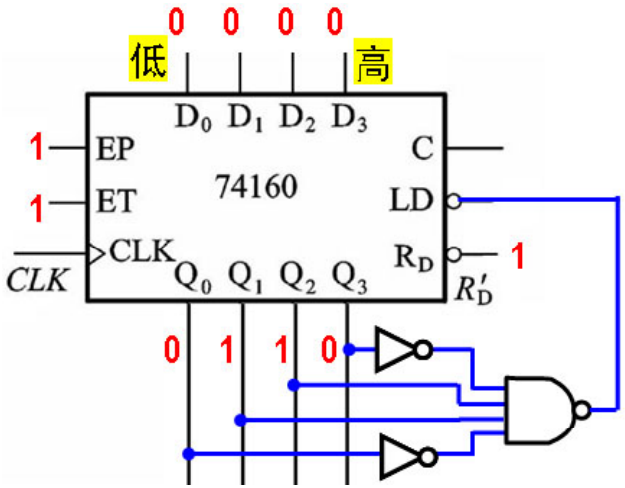




例1：设计序列信号发生器 1110011（L＝7）

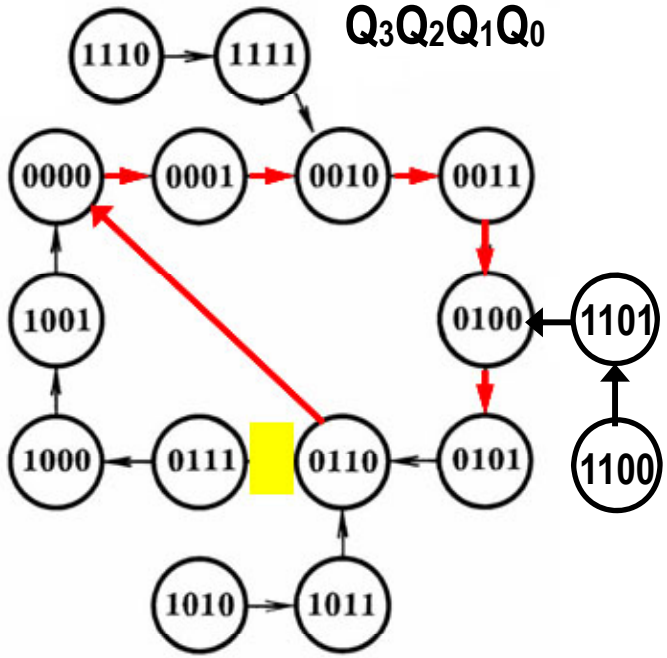
方法I：计数器(74160)+逻辑门, 置0法

1） 模7计数器



2） 组合逻辑真值表

clk	$Q_2Q_1Q_0$	Y
0	0 0 0	1
1	0 0 1	1
2	0 1 0	1
3	0 1 1	0
4	1 0 0	0
5	1 0 1	1
6	1 1 0	1



3）K图化简

Q_2 \ Q_1Q_0	00	01	11	10
0	1	1	0	1
1	0	1	x	1

Y

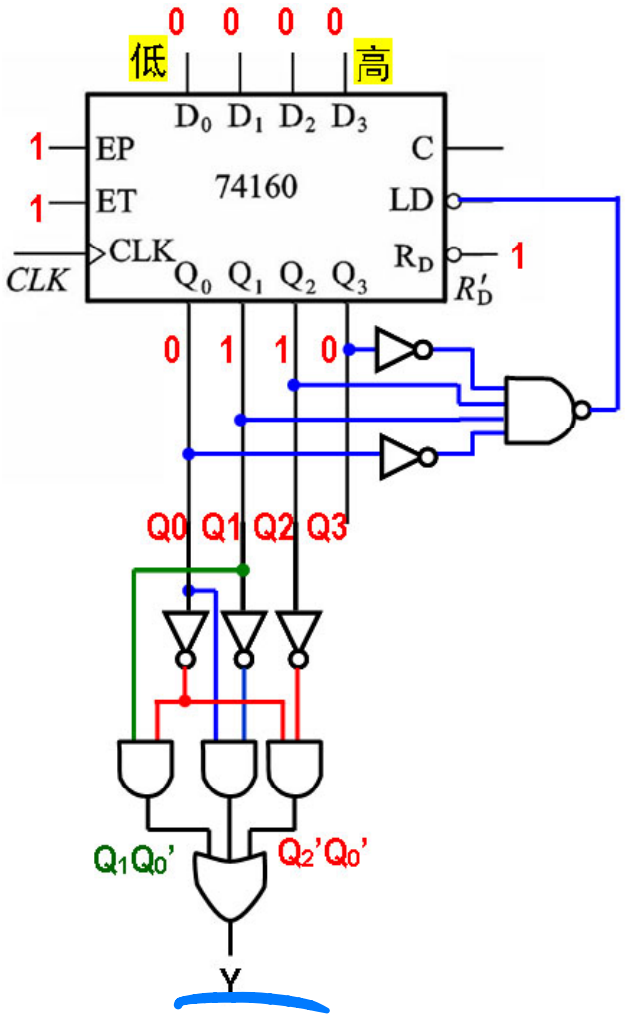
$Y = Q_2'Q_0' + Q_1'Q_0 + Q_1Q_0'$

4） 总电路图

例1：设计序列信号发生器 1110011（L＝7）

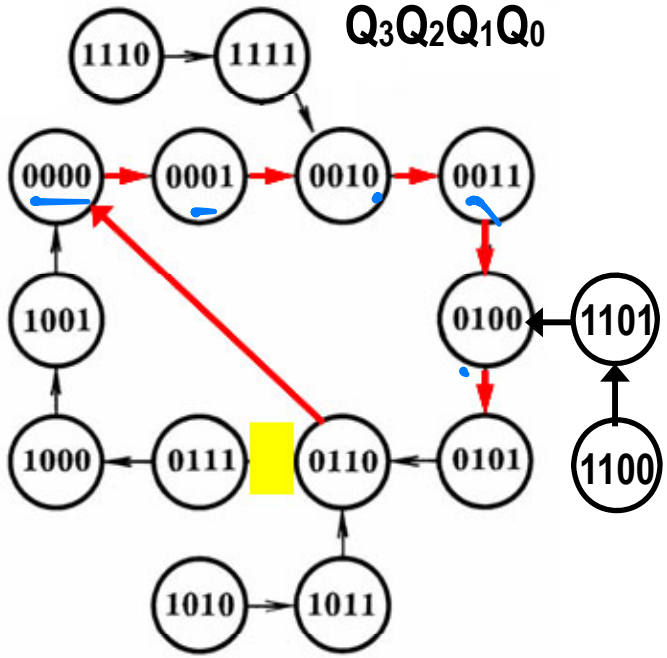
方法I：计数器(74160)+逻辑门，置0法

1） 模7计数器



2）组合逻辑真值表

clk	$Q_2Q_1Q_0$	Y
0	0 0 0	1
1	0 0 1	1
2	0 1 0	1
3	0 1 1	0
4	1 0 0	0
5	1 0 1	1
6	1 1 0	1



3）K图化简

Q_2 \ Q_1Q_0	00	01	11	10
0	1	1	0	1
1	0	1	x	1

Y

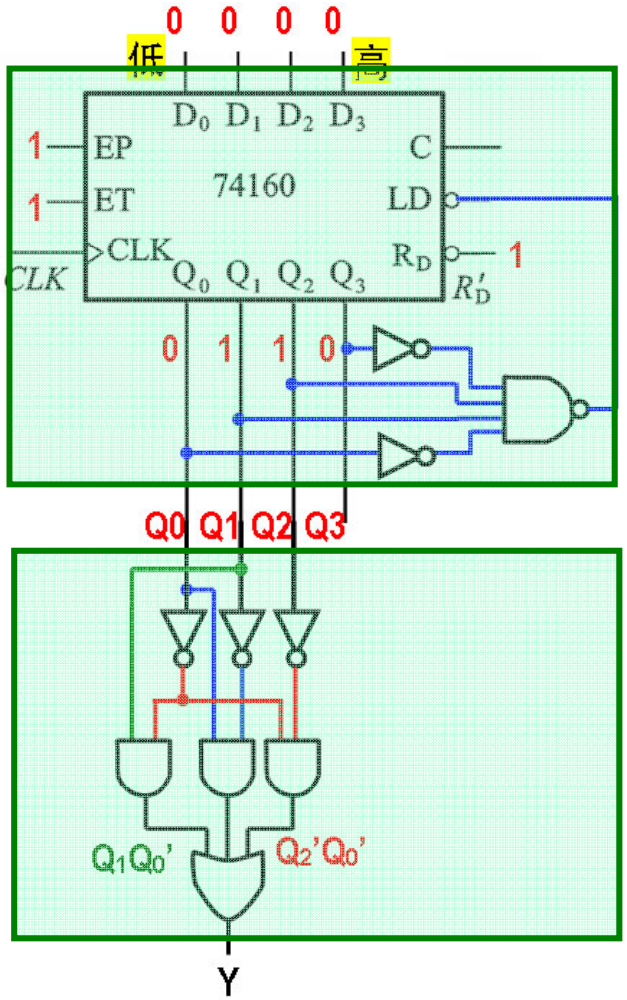
$Y = Q_2'Q_0' + Q_1'Q_0 + Q_1Q_0'$

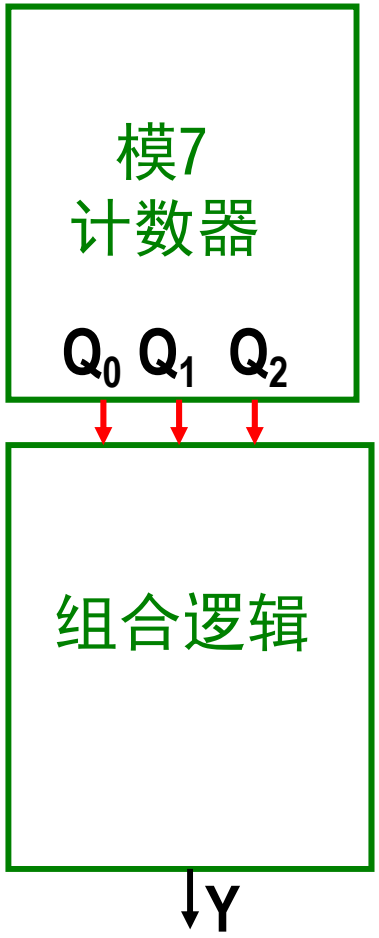
4） 总电路图

例1：设计序列信号发生器 1110011（L＝7）

方法I：计数器(74160)+逻辑门, 置0法

1） 模7计数器



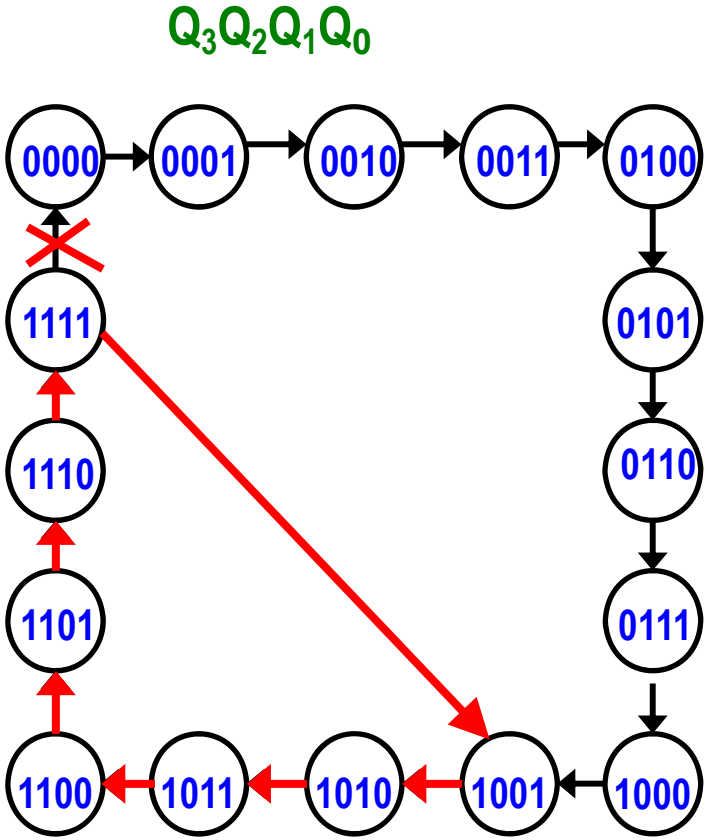


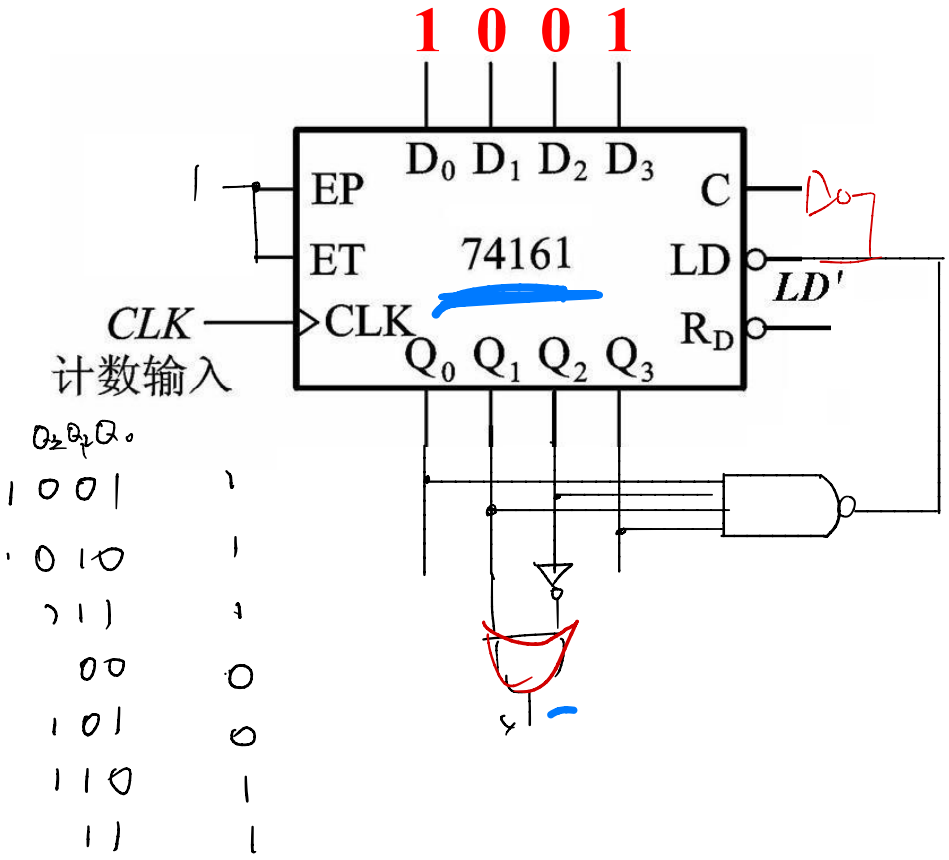
3） 总电路图

练习1 设计序列信号发生器 1110011（L=7），74161加逻辑门，置补法

1） 模7计数器，74161置补法

$$7_{补}=16-7=9=(1001)_2$$



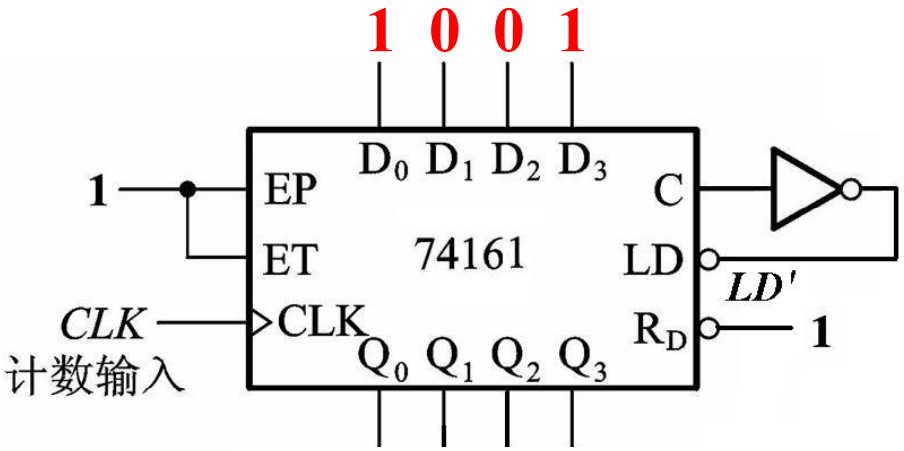


练习1 设计序列信号发生器 1110011（L＝7），74161加逻辑门，置补法

1） 模7计数器，74161置补法

2）组合逻辑真值表

CLK	Q_3	Q_2	Q_1	Q_0	Y
0	1	0	0	1	1
1	1	0	1	0	1
2	1	0	1	1	1
3	1	1	0	0	0
4	1	1	0	1	0
5	1	1	1	0	1
6	1	1	1	1	1



3）K图化简

Q_2 \ Q_1Q_0	00	01	11	10
0	x	1	1	1
1	0	0	1	1

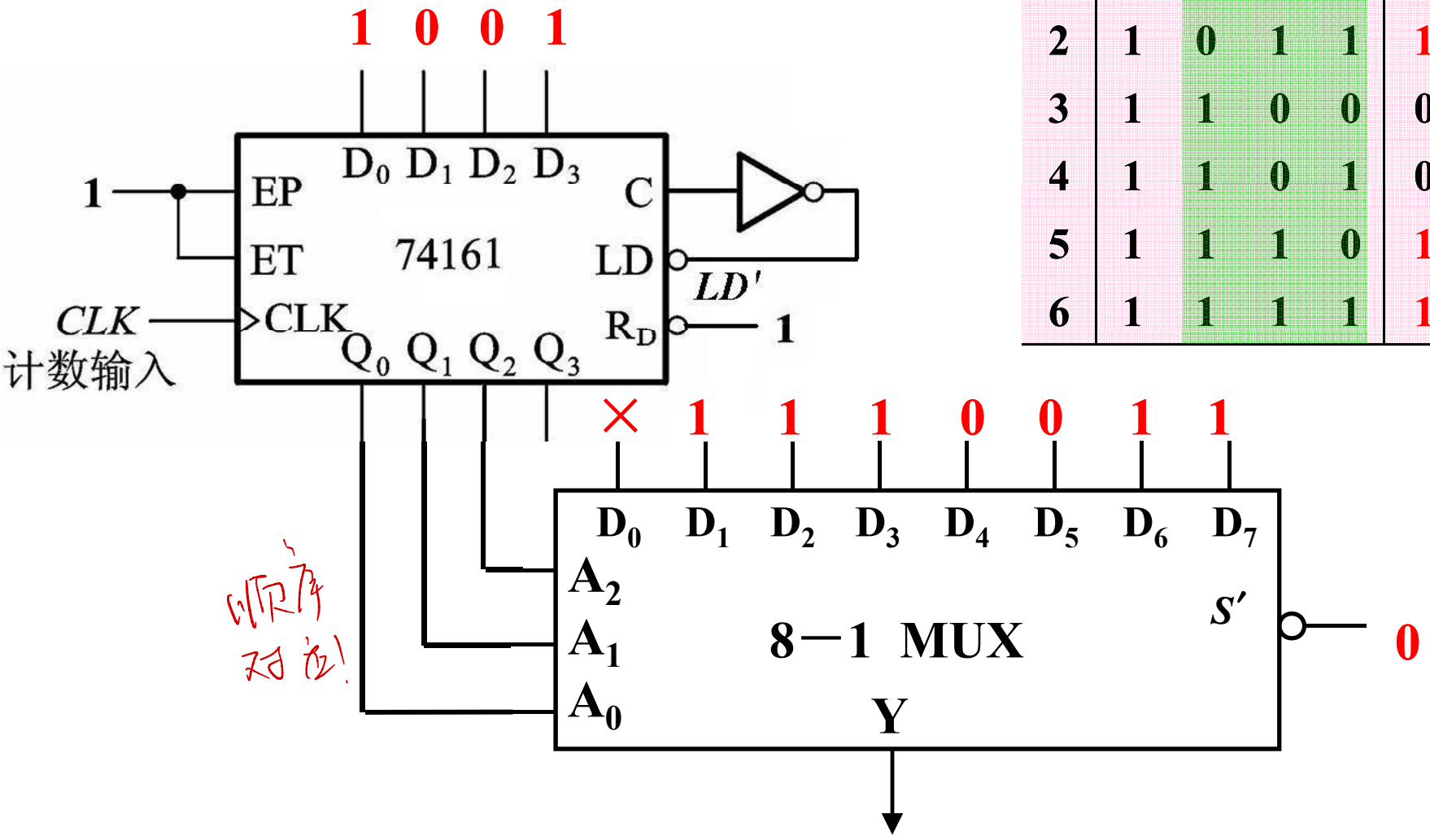
Y

$$Y = Q_2' + Q_1$$

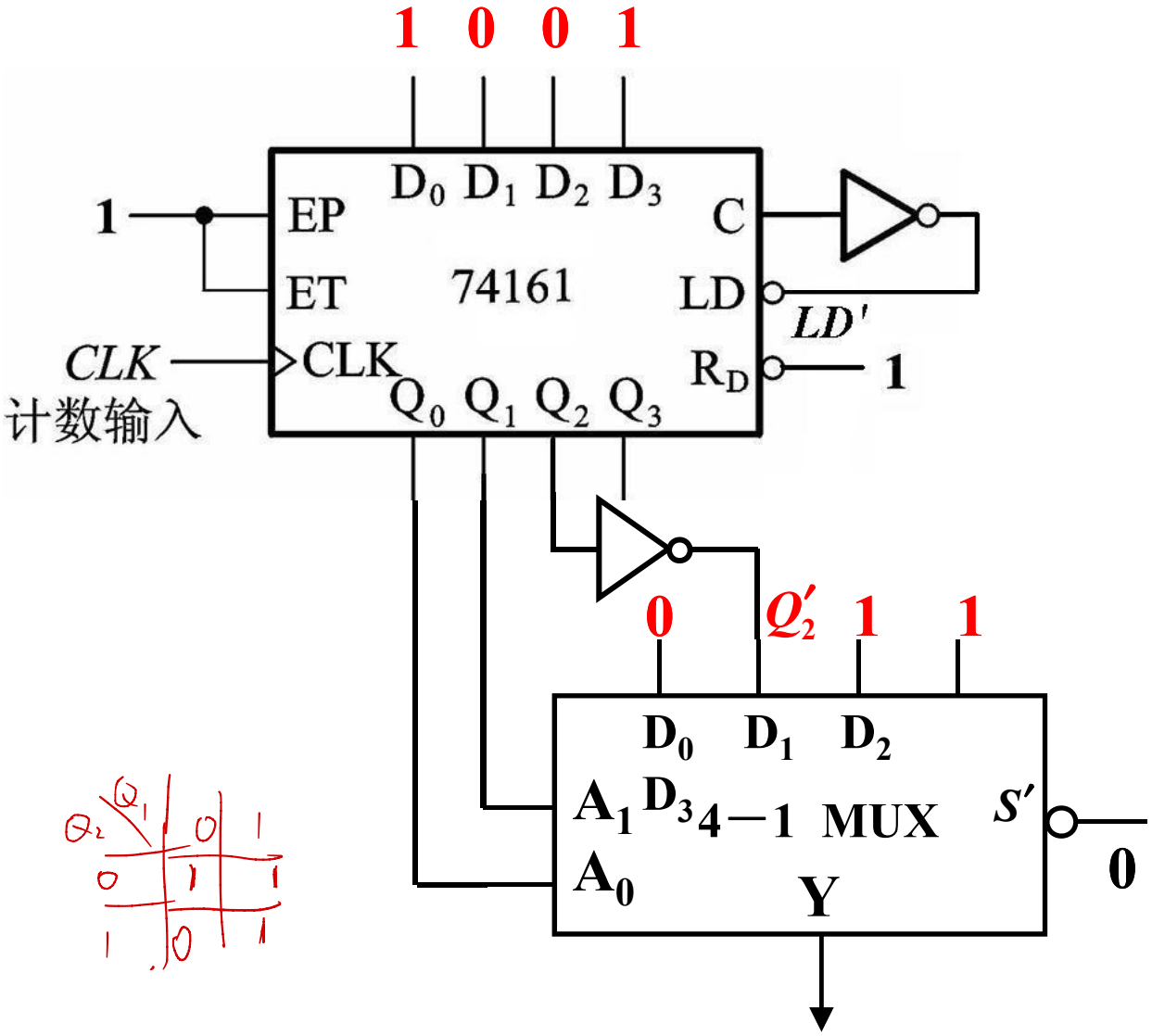
例1方法II：　用74161+8-1MUX

设计1110011序列信号发生器

	A_2	A_1	A_0		
CLK	Q_3	Q_2	Q_1	Q_0	Y
0	1	0	0	1	1
1	1	0	1	0	1
2	1	0	1	1	1
3	1	1	0	0	0
4	1	1	0	1	0
5	1	1	1	0	1
6	1	1	1	1	1



练习2 用74161+4-1MUX设计1110011序列信号发生器



CLK	Q_3	Q_2	Q_1	Q_0	Y
0	1	0	0	1	1
1	1	0	1	0	1
2	1	0	1	1	1
3	1	1	0	0	0
4	1	1	0	1	0
5	1	1	1	0	1
6	1	1	1	1	1

Q_2 \ Q_1Q_0	00	01	11	10
0	X	1	1	1
1	0	0	1	1

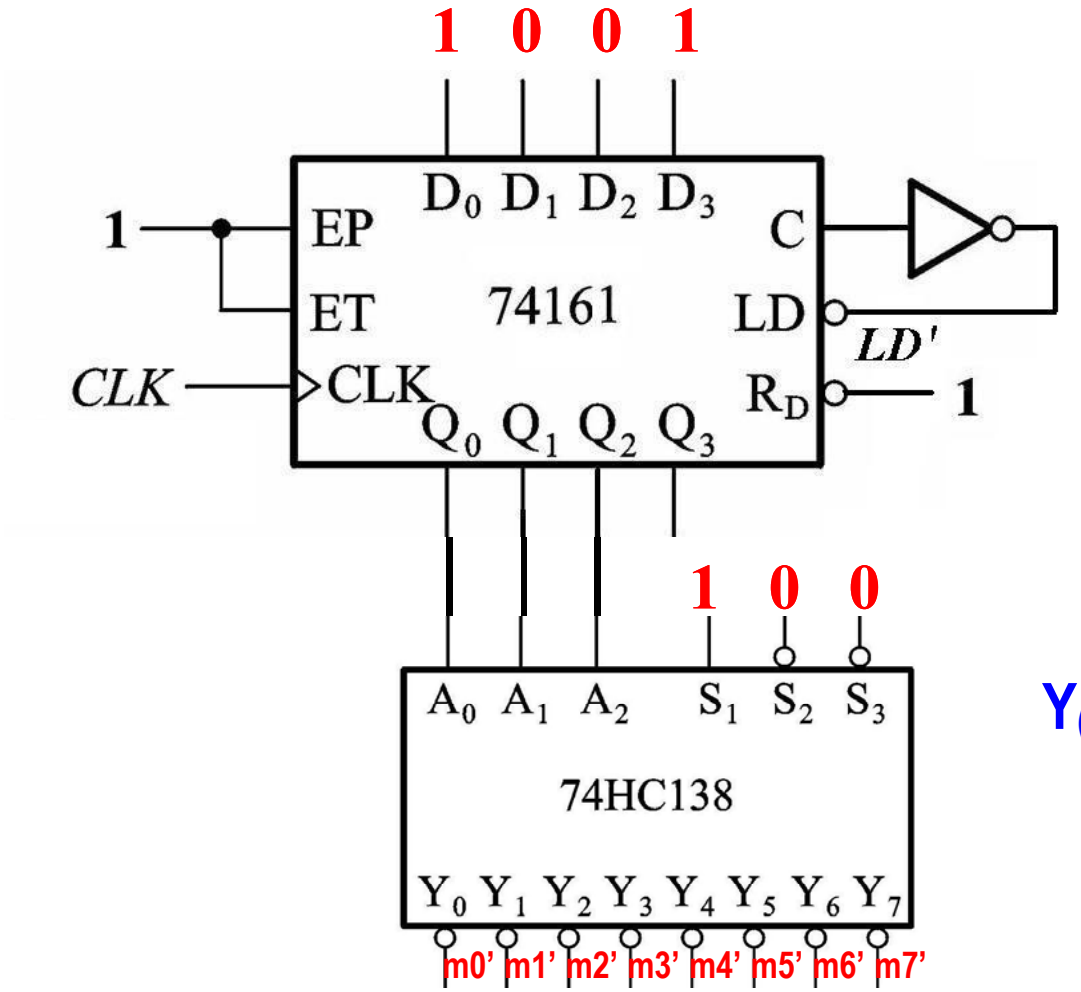
Y

A_1 \ A_0Q_0	0	1
0	0	Q_2'
1	1	1

Y

例1方法III： 用74161+3-8译码器

设计1110011序列信号发生器

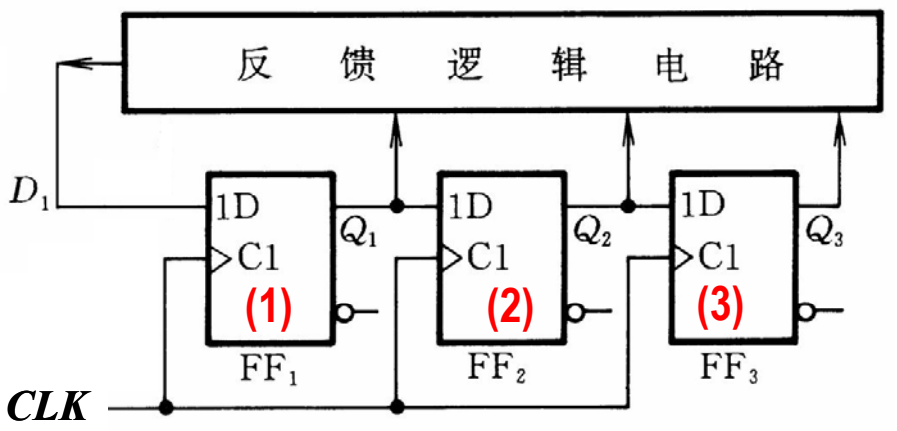


		A_2	A_1	A_0	
CLK	Q_3	Q_2	Q_1	Q_0	Y
0	1	0	0	1	1
1	1	0	1	0	1
2	1	0	1	1	1
3	1	1	0	0	0
4	1	1	0	1	0
5	1	1	1	0	1
6	1	1	1	1	1

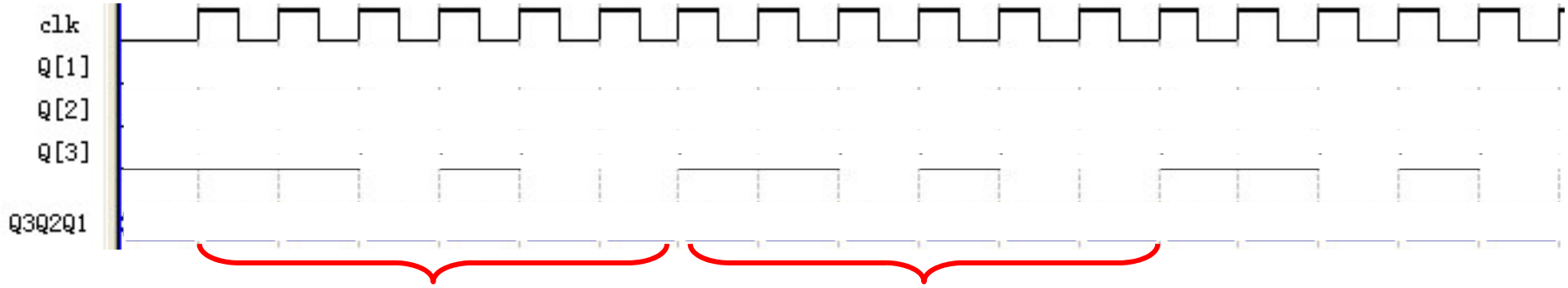
$$Y_{(A2,A1,A0)} = m_1 + m_2 + m_3 + m_6 + m_7$$

$$= (m_1' m_2' m_3' m_6' m_7')'$$

例2 方法IV:移位寄存器+逻辑门
设计101100序列信号发生器(L=6)

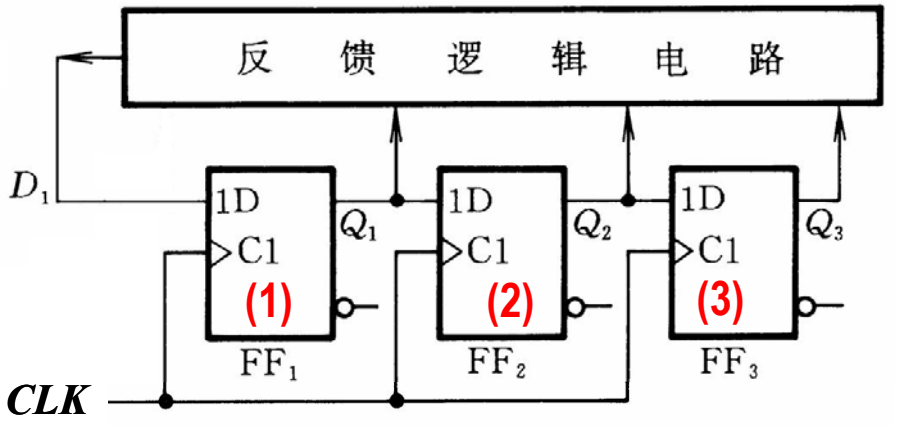


CLK	Q_3	Q_2	Q_1
0	0	0	1
1	0	1	0
2	1	0	1
3	0	1	1
4	1	1	0
5	1	0	0



例2 方法IV:移位寄存器+逻辑门

设计101100序列信号发生器(L=6)



1) 状态转换表

CLK	Q_3	Q_2	Q_1
0	0	0	1
1	0	1	0
2	1	0	1
3	0	1	1
4	1	1	0
5	1	0	0

Q_1^*

2) 状态转换K图及化简

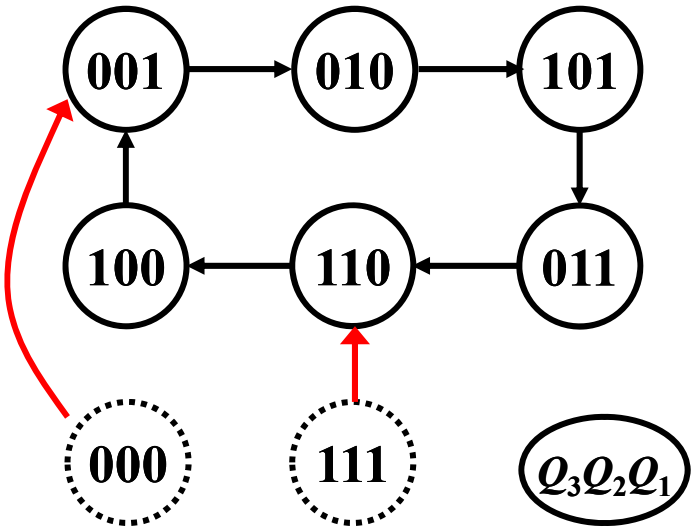
Q_3 \ Q_2Q_1	00	01	11	10
0	00X	010	110	101
1	001	011	11X	100

$(Q_3Q_2Q_1)^*$

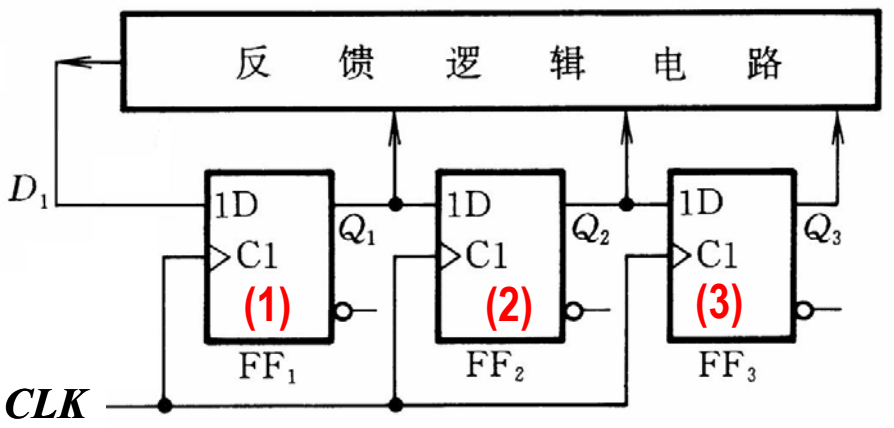
Q_3 \ Q_2Q_1	00	01	11	10
0	X	0	0	1
1	1	1	X	0

Q_1^* $D_1=Q_1^*=Q_3'Q_1'+Q_2'Q_3$

2) 状态图



4) 检查自启动 可以自启动



1) 状态转换表

clk	$Q_3Q_2Q_1$
0	0 0 **1**
1	0 1 **0**
2	1 0 **1**
3	0 1 **1**
4	1 1 **0**
5	1 0 **0**

3) 状态转换K图及化简

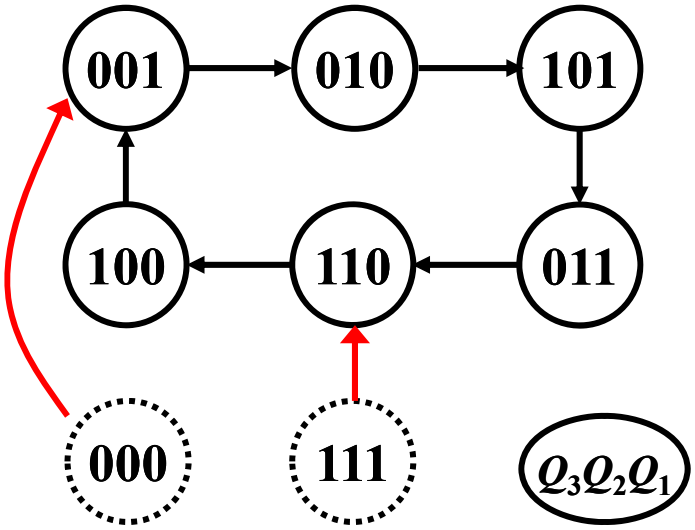
Q_3 \ Q_2Q_1	00	01	11	10
0	00X	010	110	101
1	001	011	11X	100

$(Q_3Q_2Q_1)^*$

Q_3 \ Q_2Q_1	00	01	11	10
0	X	0	0	1
1	1	1	X	0

Q_1^* $D_1=Q_1^*=Q_3'Q_1' + Q_2'Q_3$

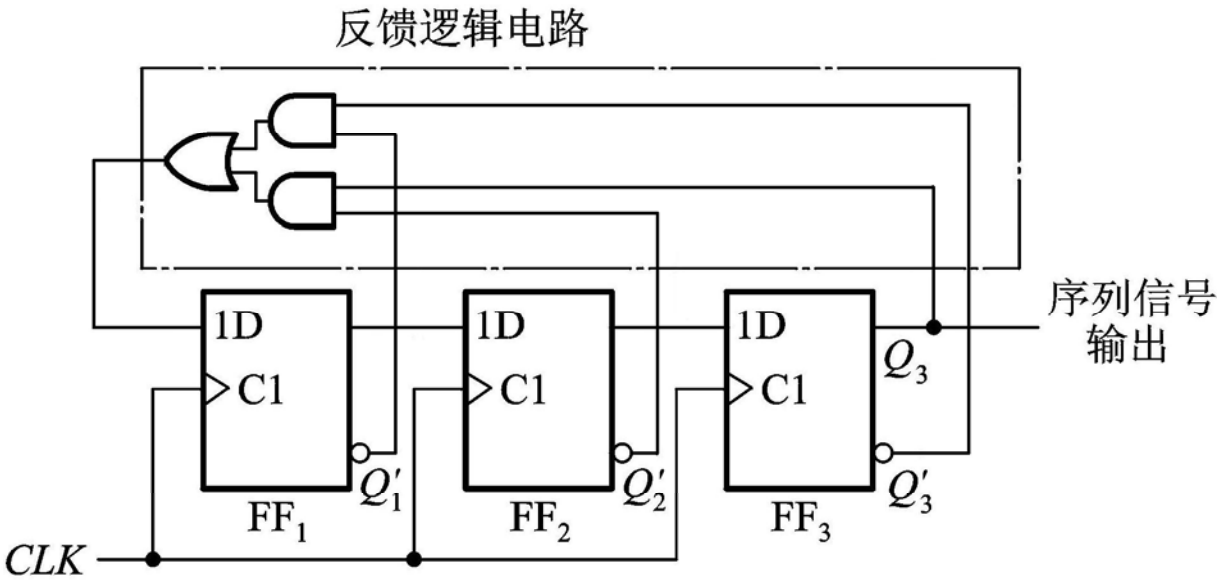
2) 状态图



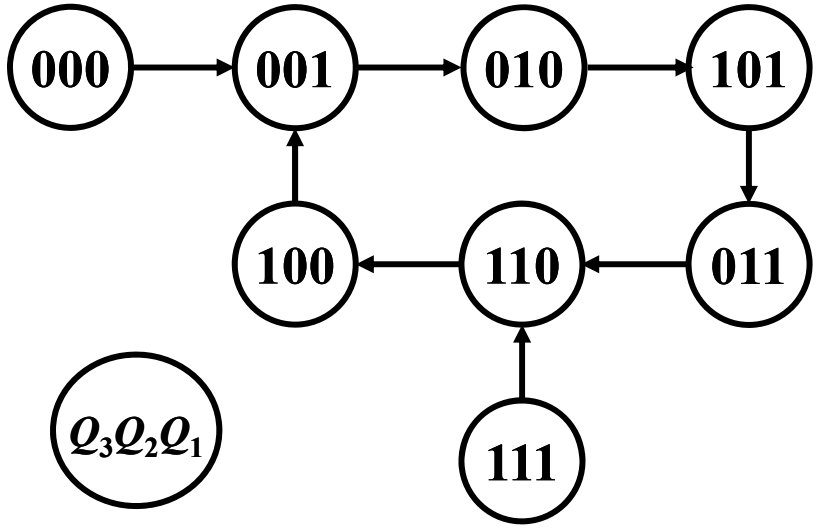
4) 检查自启动 可以自启动

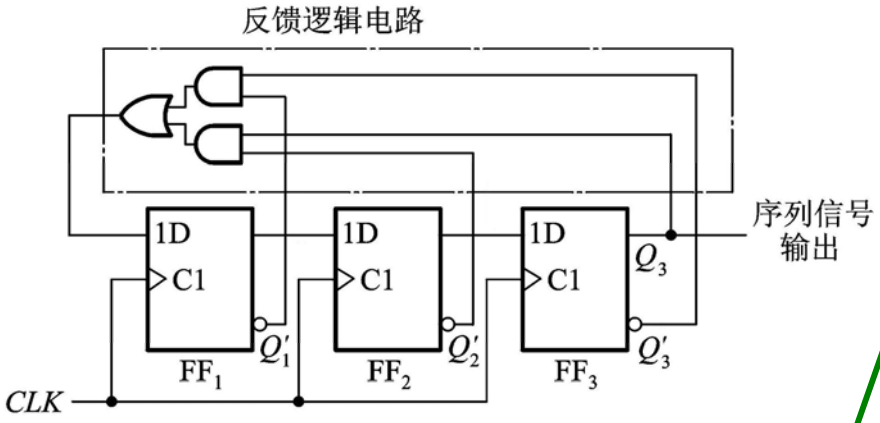
$D_1=Q_1^*=Q_3'Q_1'+Q_2'Q_3$

- 电路图



- 状态转换图

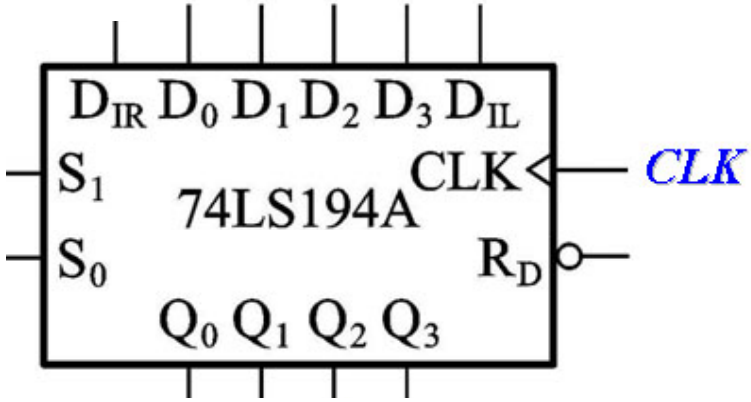




$D_1=Q_1^*=Q_3'Q_1'+Q_2'Q_3$

$D_0=D_{IR}=Q_0^*=Q_2'Q_0'+Q_1'Q_2$

也可以采用74LS194实现
101100序列信号发生器

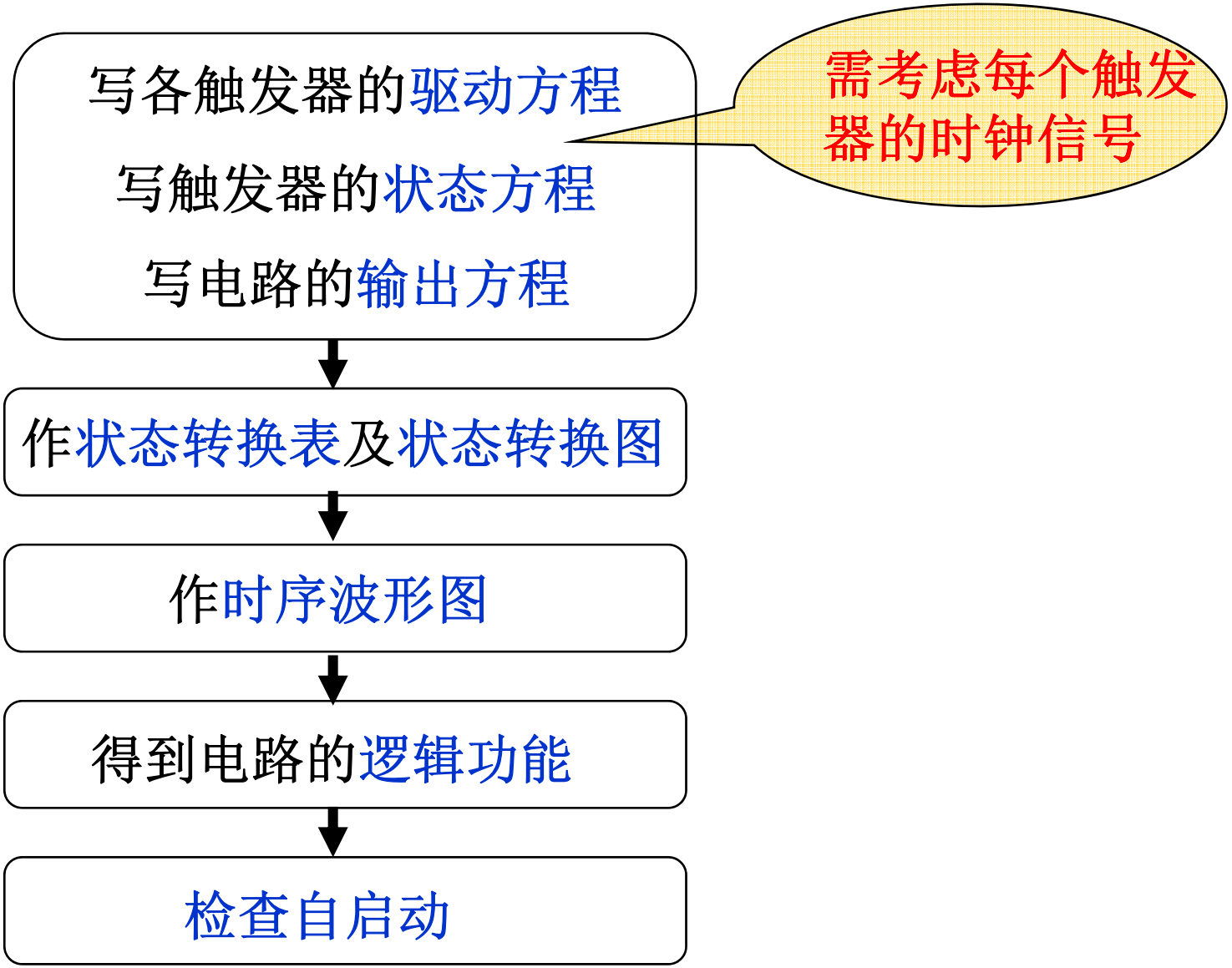


双向移位寄存器74LS194的功能表

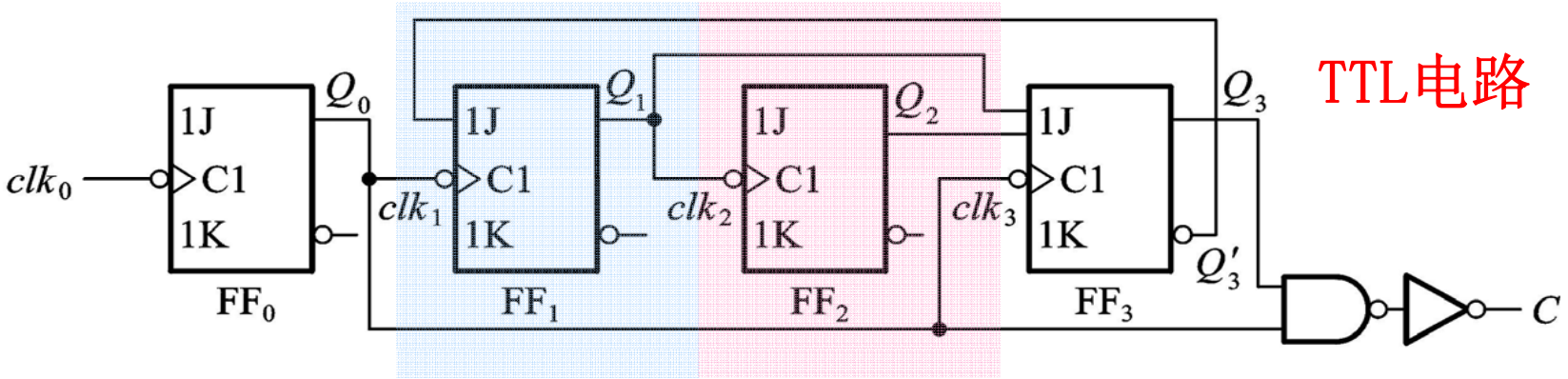
R'_D	S_1	S_0	工作状态
0	X	X	置零
1	0	0	保持
1	0	1	右移
1	1	0	左移
1	1	1	并行输入

6.2 时序逻辑电路的分析方法

1) 同步电路分析 2）异步电路分析



例：试分析下图异步时序电路的逻辑功能。



1. 写方程

各触发器的时钟不同时发生

1)驱动方程：

$$\begin{cases} J_0 = K_0 = 1 \\ J_1 = \overline{Q_3},\ K_1 = 1 \\ J_2 = K_2 = 1 \\ J_3 = Q_2 Q_1,\ K_3 = 1 \end{cases}$$

2)状态方程：

$$\begin{cases} Q_0^* = \overline{Q_0} \\ Q_1^* = \overline{Q_3}\,\overline{Q_1} \\ Q_2^* = \overline{Q_2} \\ Q_3^* = Q_2 Q_1 \overline{Q_3} \end{cases}$$

3)输出方程：$C = Q_3 Q_0$

$Q_0 \rightarrow clk_1$

$Q_1 \rightarrow clk_2$

$Q_0 \rightarrow clk_3$

2. 列状态转换表

$Q_0^* = Q_0' \cdot clk_0\downarrow$

$Q_1^* = Q_3' Q_1' \cdot clk1\downarrow$ $Clk1=Q_0$

$Q_2^* = Q_2' \cdot clk2\downarrow$ $Clk2=Q_1$

$Q_3^* = Q_2 Q_1 Q_3' \cdot clk3\downarrow$ $Clk3=Q_0$

Q_3	Q_2	Q_1	Q_0	clk3	clk2	clk1	Q_3^*	Q_2^*	Q_1^*	Q_0^*	C
0	0	0	0						0	1	0
0	0	0	1			↓			1	0	0
0	0	1	0						1	1	0
0	0	1	1			↓			0	0	0
0	1	0	0						0	1	0
0	1	0	1			↓			1	0	0
0	1	1	0						1	1	0
0	1	1	1			↓			0	0	0
1	0	0	0						0	1	0
1	0	0	1			↓			0	0	1
1	0	1	0						1	1	0
1	0	1	1			↓			0	0	1
1	1	0	0						0	1	0
1	1	0	1			↓			0	0	1
1	1	1	0						1	1	0
1	1	1	1			↓			0	0	1

$Q_0 \rightarrow clk_1$

$Q_1 \rightarrow clk_2$

$Q_0 \rightarrow clk_3$

$$\begin{cases} Q_0^* = Q_0' \ clk_0\downarrow \\ Q_1^* = Q_3' Q_1' \ clk_1\downarrow \\ Q_2^* = Q_2' \ clk_2\downarrow \\ Q_3^* = Q_2 Q_1 Q_3' \ clk_3\downarrow \end{cases}$$

1)首先列出Q_0

2)Q_0从1→0时，clk_1和clk_3为↓

3)Q_1从1→0时，clk_2为↓

2. 列状态转换表

$Q_0^* = Q_0' \cdot clk_0\downarrow$

$Q_1^* = Q_3' Q_1' \cdot clk1\downarrow$ $Clk1=Q_0$

$Q_2^* = Q_2' \cdot clk2\downarrow$ $Clk2=Q_1$

$Q_3^* = Q_2 Q_1 Q_3' \cdot clk3\downarrow$ $Clk3=Q_0$

Q_3	Q_2	Q_1	Q_0	clk3 (Q_0)	clk2	clk1 (Q_0)	Q_3^*	Q_2^*	Q_1^*	Q_0^*	C
0	0	0	0				0	0	0	1	0
0	0	0	1	↓		↓	0	0	1	0	0
0	0	1	0				0	0	1	1	0
0	0	1	1	↓	↓	↓	0	1	0	0	0
0	1	0	0				0	1	0	1	0
0	1	0	1	↓		↓	0	1	1	0	0
0	1	1	0				0	1	1	1	0
0	1	1	1	↓	↓	↓	1	0	0	0	0
1	0	0	0				1	0	0	1	0
1	0	0	1	↓		↓	0	0	0	0	1
1	0	1	0				1	0	1	1	0
1	0	1	1	↓	↓	↓	0	1	0	0	1
1	1	0	0				1	1	0	1	0
1	1	0	1	↓		↓	0	1	0	0	1
1	1	1	0				1	1	1	1	0
1	1	1	1	↓	↓	↓	0	0	0	0	1

$Q_0 \rightarrow clk_1$

$Q_1 \rightarrow clk_2$

$Q_0 \rightarrow clk_3$

$$\begin{cases} Q_0^* = Q_0' \ clk_0\downarrow \\ Q_1^* = Q_3' Q_1' \ clk_1\downarrow \\ Q_2^* = Q_2' \ clk_2\downarrow \\ Q_3^* = Q_2 Q_1 Q_3' \ clk_3\downarrow \end{cases}$$

1)首先列出Q_0

2)Q_0从1→0时，clk_1和clk_3为↓

3)Q_1从1→0时，clk_2为↓

2. 列状态转换表

Q_3	Q_2	Q_1	Q_0	clk3 (Q_0)	clk2 (Q_1)	clk1 (Q_0)	Q_3^*	Q_2^*	Q_1^*	Q_0^*	C
0	0	0	0							1	0
0	0	0	1							0	0
0	0	1	0							1	0
0	0	1	1							0	0
0	1	0	0							1	0
0	1	0	1							0	0
0	1	1	0							1	0
0	1	1	1							0	0
1	0	0	0							1	0
1	0	0	1							0	1
1	0	1	0							1	0
1	0	1	1							0	1
1	1	0	0							1	0
1	1	0	1							0	1
1	1	1	0							1	0
1	1	1	1							0	1

$Q_0 \rightarrow clk_1$

$Q_1 \rightarrow clk_2$

$Q_0 \rightarrow clk_3$

$Q_0^* = Q_0' \; clk_0\downarrow$

$Q_1^* = Q_3'Q_1' \; clk_1\downarrow$

$Q_2^* = Q_2' \; clk_2\downarrow$

$Q_3^* = Q_2Q_1Q_3' \; clk_3\downarrow$

1)首先列出Q_0

2)Q_0从1→0时，clk_1和clk_3为↓

3)Q_1从1→0时，clk_2为↓

2. 列状态转换表

Q_3	Q_2	Q_1	Q_0	clk3 (Q_0)	clk2 (Q_1)	clk1 (Q_0)	Q_3^*	Q_2^*	Q_1^*	Q_0^*	C
0	0	0	0					0	0	1	0
0	0	0	1	↓		↓		0	1	0	0
0	0	1	0					0	1	1	0
0	0	1	1	↓	↓	↓		1	0	0	0
0	1	0	0					1	0	1	0
0	1	0	1	↓		↓		1	1	0	0
0	1	1	0					1	1	1	0
0	1	1	1	↓	↓	↓		0	0	0	0
1	0	0	0					0	0	1	0
1	0	0	1	↓		↓		0	0	0	1
1	0	1	0					0	1	1	0
1	0	1	1	↓	↓	↓		1	0	0	1
1	1	0	0					1	0	1	0
1	1	0	1	↓		↓		1	0	0	1
1	1	1	0					1	1	1	0
1	1	1	1	↓	↓	↓		0	0	0	1

$Q_0 \rightarrow clk_1$

$Q_1 \rightarrow clk_2$

$Q_0 \rightarrow clk_3$

$$Q_0^* = Q_0' \; clk_0\downarrow$$
$$Q_1^* = Q_3'Q_1' \; clk_1\downarrow$$
$$Q_2^* = Q_2' \; clk_2\downarrow$$
$$Q_3^* = Q_2Q_1Q_3' \; clk_3\downarrow$$

1)首先列出Q_0

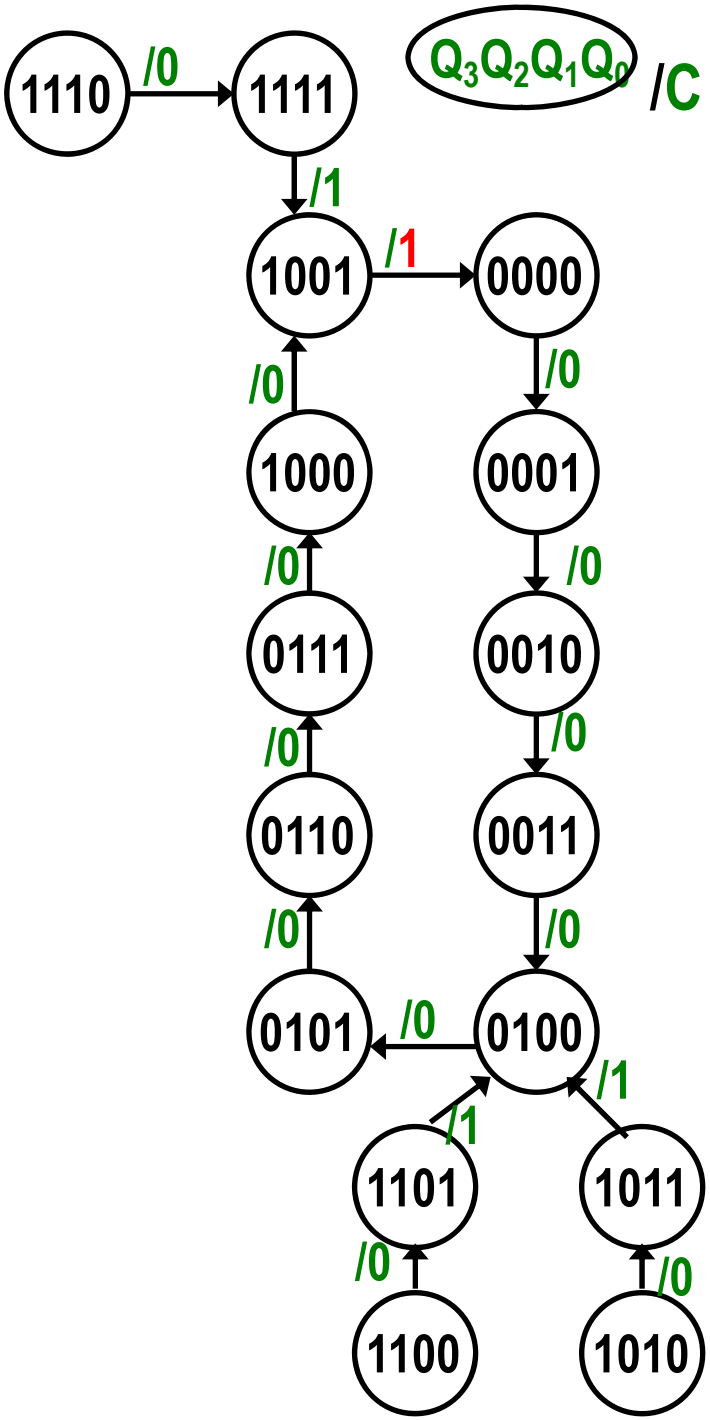
2)Q_0从1→0时，clk_1和clk_3为↓

3)Q_1从1→0时，clk_2为↓

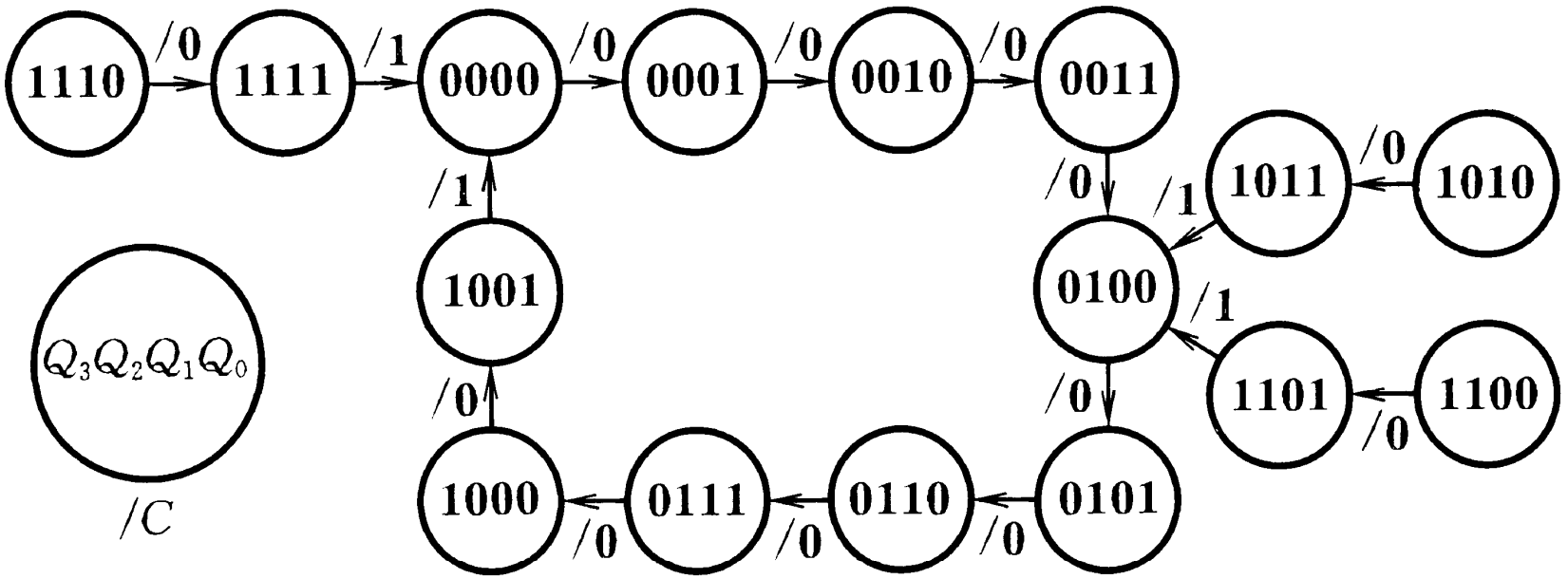
2. 列状态转换表

Q_3	Q_2	Q_1	Q_0	Q_3^*	Q_2^*	Q_1^*	Q_0^*	C
0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	1	0	0
0	0	1	0	0	0	1	1	0
0	0	1	1	0	1	0	0	0
0	1	0	0	0	1	0	1	0
0	1	0	1	0	1	1	0	0
0	1	1	0	0	1	1	1	0
0	1	1	1	1	0	0	0	0
1	0	0	0	1	0	0	1	0
1	0	0	1	0	0	0	0	1
1	0	1	0	1	0	1	1	0
1	0	1	1	0	1	0	0	1
1	1	0	0	1	1	0	1	0
1	1	0	1	0	1	0	0	1
1	1	1	0	1	1	1	1	0
1	1	1	1	0	0	0	0	1

3. 画状态图



3. 画状态图（书上画法）



4.分析电路的功能

为异步十进制加法计数器

作业

6.29 设计序列信号发生器”**0010110111**”，序列长度 **L=10**

方法1：计数器(74160)+逻辑门

方法2：计数器(74161)+选通器(8-1MUX)

方法3：计数器(74161)+译码器（两个74138扩展成4-16译码器）