2023 COMP3222 Lab 1 Requirements, Marking Guide and Additional Notes

General Comments

From previous experience, the COMP3222 teaching staff have concluded some tweaks to the Altera labs would improve the learning outcomes. In addition to the video introductions to each lab, which outline the objectives, steps and desired results, we will publish additional guidance and explain in more detail what we are looking for. Don't forget to attend one of the two weekly online lab sessions or your registered face-to-face lab during the week the lab is scheduled to get help, but please come prepared by having read the specifications to get the most out of these.

As explained in the video introduction, we are using two different FPGA boards for COMP3222 – the original DE1 board, and its more recent substitute, the DE0 board. These boards are very similar but differ in some significant respects, e.g. they contain different FPGAs, and they have different LED and push-button resources. The lab specifications (exercise sheets) have been edited to accommodate use of either board. Most importantly, different pin assignment files need to be used to connect the board resources, such as switches and LEDs, to the FPGA. Please ensure that you *import the correct pin assignment file* for your board before implementing your design.

Lab 1 Specific Comments

For Lab 1 all signal assignment statements in your VHDL code for every part should just be simple gate level (Boolean) expressions. You must not use any complex assignment statements or behavioural statements. You will lose marks if you do not follow this requirement.

There are 6 marks available for completing Lab 1. You are required to complete and submit solutions for Parts III, IV and V. You are encouraged to complete Parts I, II and VI, but we will not mark these parts. We will award up to 1 mark for each correct solution to Parts III, IV and V, as specified in the Lab 1 exercise sheet. In addition, we will award up to 1 mark for each of your paper designs for Parts IV and V, as specified below, and award up to 1 mark overall for your coding style.

Part I

- Please ensure you substitute LEDG for LEDR in both the ENTITY and ARCHITECTURE of Figure 1 if you are using the DE0 board.

Part III

- Create your 3-to-1 MUX by cascading two 2-to-1 MUXes (see Figure 4a).

Part IV

- The goal is to describe the signal for each display segment in terms of a Boolean expression involving c_1 and c_0
- Derive a truth table for each of the 7 display segments given the character that is to be displayed for each setting of c_1 and c_0
- Then, derive the logic expression for each segment in terms of c_1 and c_0
- A neat copy of your truth tables and logic expressions must be submitted together with your solution to Part IV – no marks will be awarded for Part IV if these are not submitted.

Part V

- Prior to coding (please don't hack!) develop your design for Part V.
- Sketch a block diagram for your design. This should be at the same level of detail as illustrated in Figure 7 and focus on the interconnections between the switches and the inputs of your 2-bit 3-to-1 MUXes. Note that it is not necessary to detail the internals of the multiplexers, decoders or 7-segment displays.
- Submit a neat copy of your block diagram together with your solution to Part V – no marks will be awarded for Part V if no sketch is submitted.

Coding style

Apart from correctness, the guiding principle for code style in COMP3222 is understandability and maintainability. Up to ONE mark will be awarded for your coding style across the three assessable parts of the lab. Points to be taken into account include:

- Adherence to the lab specifications
- Alignment between your paper designs for Parts IV and V and your code
- Correct VHDL use
- Use of meaningful names for entities, architectures, signals and labels
- Appropriate decomposition of a design into sub-components
- Proper indentation

Submission

1. Create a *Project* $\rightarrow$ *Archive* for Parts III, IV and V of Lab 1 – use meaningful names to distinguish each project archive. Include your surname, student number, lab and part number in the archive name e.g. Diessel-3002283-L01P4.qar
2. Create a PDF or JPEG file for the paper designs for Parts IV and V. Use the same naming convention as above, but append -design.pdf or -design.jpg
   e.g. Diessel-3002283-L01P4-design.pdf
3. Create a zip file including the above 5 files and submit it using the *Make Submission* tab on the *Lab 1 additional guidelines and questions* link of the course website. Submissions are **due at 23:59 on 25 September**.