2023 COMP3222 Lab 4 Requirements, Marking Guide and Additional Notes

There are 5 marks available for completing Lab 4. You are required to complete and submit solutions for Parts I, II and IV. You are encouraged to complete Parts III and V as well, but we will not mark your solutions for these parts. We will award up to 1 mark for each correct solution to Parts I, II and IV, as specified in the Lab 4 exercise sheet. In addition, we will award up to 1 mark for your paper design for Part IV, as specified below, and award up to 1 mark overall for your coding style.

To assist with your completion of the lab, project archives containing VHDL file stubs and simulation waveforms for Parts I (Steps 1 & 3), II and IV have been provided in the Lab 4 section of the course website. ***To help streamline our testing of your solutions, please don't edit the ENTITY description of any VHDL designs we have provided you with other than to select the appropriate LEDs for your board.***

Part I

- HINT: use a FOR…GENERATE statement – refer to L04/S39
- You may create a behavioural model of a T-type flip-flop with asynchronous clear
- Note that the number of logic elements (LEs) used and F_{max} can be found in the compilation report (*Processing → Compilation Report*). These are to be reported in your submission.
- You will find F_{max} under *TimeQuest Timing Analyzer → Slow Model*.
- Please submit your code for step 3.

Part II

- Explain the difference in F_{max} between the 8- and 16-bit versions of the counters (Parts I & II)?

Part IV

Prior to implementing your counter you should prepare an outline of your design on paper. This design is worth up to ONE mark. *You will not receive any marks for the design or your solution to Part IV if you do not provide a paper design.*

You are required to prepare a so-called *block diagram* of your design that includes the interconnection of all Input/Output (IO) signals (ports) of the following three components:

1. A one-second timer with asynchronous clear. This timer, which is controlled by a 50MHz clock signal, outputs a pulse for one clock period every second. Connect your clear signal to the KEY(0) push button.
2. A BCD counter with enable and asynchronous clear. This counter is also to be connected to the 50 MHz clock signal. You should design, implement and simulate this component before connecting it to the one-second timer.
3. The 7-segment display from Lab 3, part 5 or L04/S53.

Your diagram should include the connections of the circuit to the resources provided by the DE board.

Coding style

Apart from correctness, the guiding principle for code style in COMP3222 is understandability and maintainability. Up to ONE mark will be awarded for your coding style on all three assessable parts of the lab. Points to be taken into account include:

- Adherence to the lab specifications
- Alignment between your paper designs and your code
- Appropriate decomposition of a design into sub-components
- Correct VHDL use, including appropriate use of behavioural statements and component instantiation
- Use of meaningful names for entities, architectures, signals and labels
- Proper indentation

Submission

1. Create a *Project → Archive* for Parts I, II and IV of Lab 4 – use meaningful names to distinguish each project archive. Include your surname, student number, lab and part number in the archive name e.g. Diessel-3002283-L04P4.qar
2. Create a PDF or JPEG file of the paper design for Part IV. Use the same naming convention as above, but append -design.pdf or -design.jpg
   e.g. Diessel-3002283-L04P4-design.pdf
3. Create a zip file including the above 4 files and submit it using the *Make Submission* tab on the *Lab 4 additional guidelines and questions* link of the course website. Submissions are **due at 23:59 on 16 October, 2022**.