2023 COMP3222 Lab 2 Requirements, Marking Guide and Additional Notes

Reminders:

- Don't forget to attend a face-to-face or online lab session during the week the lab is scheduled to get help, but please **come prepared** to get the most out of it.
- As explained for Lab 1, please ensure that you *import the correct pin assignment file* for your board before implementing your design.

Warning: Except where indicated below, for Lab 2 all signal assignment statements in your VHDL code for all parts should just be simple Boolean logic expressions. There is no need to use any complex assignment statements or behavioural statements. You will lose marks if you do not follow this requirement.

There are 7 marks available for completing Lab 2. You are required to complete and submit solutions for Parts II, IV and V. You are encouraged to complete Parts I, III and VI as well, but we will not mark your solutions for these parts. We will award up to 1 mark for each correct solution to Parts II, IV and V, as specified in the Lab 2 exercise sheet. In addition, we will award up to 1 mark for each of your paper designs for Parts I, II and IV, as specified below, and award up to 1 mark overall for your coding style. We will not provide any marks for Parts I, II or IV if you do not submit your paper designs.

To assist with your completion of the lab, project archives containing VHDL file stubs and simulation waveforms for Parts II, III, IV and V have been provided in the Lab 2 section of the course website. ***To help streamline our testing of your solutions, please don't edit the ENTITY description of any VHDL designs we have provided you with other than to select the appropriate LEDs for your board.***

Part I

- You are required to submit a neat copy of your paper design for Part I.
    - List the truth table for each of the 7-segment display segments. Derive the logic function for each segment based on the 4 input switch settings. Use Karnaugh maps to demonstrate that your logic expressions are minimal.

Part II

- You are required to submit a neat copy of your paper design for Part II.
    - List the truth table for the Circuit A outputs and derive minimal Boolean logic expressions for each output bit
    - Determine the logic function *z*
    - Assuming Circuit B does not use an instance of the 7-segment decoder internally, but rather drives the segments of HEX1 directly, determine the logic expressions for each segment

Part III

- You may use a conditional assignment expression to specify the 2-to-1 mux in this part and subsequent parts of the lab.

Part IV

- You are required to submit a neat copy of your paper design for Part IV.
    - Sketch a circuit diagram similar to that of Figure 1 for this part. Note that Circuit A will have 4-bit inputs and outputs. Include connections to the input switches, the 4-bit adder, and the output LEDGs and HEXadecimal displays.
    - List the truth table for the outputs of Circuit A and derive minimal logic expressions for each bit. Pay attention to don't care output conditions.
    - Derive a logic expression for $LEDG_7$

Part V

- This part contrasts a behavioural VHDL architecture with the structural/logic level design of the previous part. Lines 1, 9 and 10 can be implemented using straightforward mathematical assignment statements. Lines 2-9 should be coded using a combinational PROCESS statement.

Coding style

Apart from correctness, the guiding principle for code style in COMP3222 is understandability and maintainability. Up to ONE mark will be awarded for your coding style on all three assessable parts of the lab. Points to be taken into account include:

- Adherence to the lab specifications
- Alignment between your paper designs for Parts II and IV and your code
- Correct VHDL use, including appropriate use of behavioural statements
- Use of meaningful names for entities, architectures, signals and labels
- Appropriate decomposition of a design into sub-components
- Proper indentation

Submission

1. Create a *Project* → *Archive* for Parts II, IV and V of Lab 2 – use meaningful names to distinguish each project archive. Include your surname, student number, lab and part number in the archive name e.g. Diessel-3002283-L02P2.qar
2. Create a PDF or JPEG file for the paper designs for Parts I, II and IV. Use the same naming convention as above, but append -design.pdf or -design.jpg
   e.g. Diessel-3002283-L02P2-design.pdf
3. Create a zip file including the above 6 files and submit it using the *Make Submission* tab on the *Lab 2 additional guidelines and questions* link of the course website. Submissions are **due at 23:59 on 2 October, 2022**.