2023 COMP3222 Lab 3 Requirements, Marking Guide and Additional Notes

Reminders:

- Don't forget to attend one of the lab sessions during the week the lab is scheduled to get help, but please **come prepared** to get the most out of it.
- As explained for Lab 1, please ensure that you target the correct FPGA device and *import the correct pin assignment file* for your board before implementing your design.

Before attempting Lab 3, please watch the first 35 minutes of the video for lecture 5. Flip-flops, registers & counters (corresponding to the first 13 slides) so as to gain the theoretical background for the designs you will undertake.

There are 5 marks available for completing Lab 3. You are required to complete and submit solutions for Parts II (Steps 1 – 3), IV and V. You are encouraged to complete Parts I and III as well, but we will not mark your solutions for these parts. We will award up to 1 mark for each correct solution to Parts II (Steps 1 – 3), IV and V, as specified in the Lab 3 exercise sheet. In addition, we will award up to 1 mark for your paper design for Part V, as specified below, and award up to 1 mark overall for your coding style.

To assist with your completion of the lab, project archives containing VHDL file stubs and simulation waveforms for Parts II (Steps 1 – 3) and IV have been provided in the Lab 3 section of the course website. ***To help streamline our testing of your solutions, please don't edit the ENTITY description of any VHDL designs we have provided you with other than to select the appropriate LEDs for your board.***

Part II

- You are required to submit a project archive for Steps 1 – 3 of Part II. A project archive containing a VHDL code stub for Part II and a simple vector waveform file have been provided in the Lab 3 section of the course website. Complete the VHDL design as specified and provide a comprehensive set of input tests in the vector waveform file you submit.
- Create a new project in a new directory to complete Steps 4 – 6 of Part II but **do not submit** your solutions to these steps.

Part III

- Use *File* → *Open…* to open your VHDL code for the gated D-latch from Part II Step 1 within the project for Part III. Use *File* → *Save as… to* save this D-latch code within your project for Part III. Your D latch code from Part II can then be declared as a COMPONENT in the signal declaration section of your ARCHITECTURE for Part III. Instantiate two instances of your D-latch in the body of your ARCHITECTURE for Part III

Part IV

- You are required to submit a project archive for your solution to Part IV. A project archive containing a VHDL code stub for Part IV and the vector waveform file illustrated in Figure 6 have been provided in the Lab 3 section of the course website. Complete the VHDL design as specified and confirm the simulation output before archiving your project for submission.

Part V

- Prepare and submit a neat copy of a diagram for your circuit of Part V similar in level of detail to those you prepared for Lab 2. Include connections to the switches, push buttons, hex displays and LEDs. Clearly mark the bit widths of all signals. In order to receive any marks for Part V, you must submit this diagram.
- You are also required to submit a project archive of your solution to Part V.
- **Note:** the pin assignments files for both DE boards assign the rightmost push buttons to KEY_0 and the push button to its left to KEY_1.
- **Hint:** you will need to include an 8-bit register (a bank of 8 flip-flops) with asynchronous reset for this design.

Coding style

Apart from correctness, the guiding principle for code style in COMP3222 is understandability and maintainability. Up to ONE mark will be awarded for your coding style on all three assessable parts of the lab. Points to be taken into account include:

- Adherence to the lab specifications
- Alignment between your paper designs and your code
- Appropriate decomposition of a design into sub-components
- Correct VHDL use, including appropriate use of behavioural statements and component instantiation
- Use of meaningful names for entities, architectures, signals and labels
- Proper indentation

Submission

1. Create a *Project* → *Archive* for Parts II (Steps 1 – 3), IV and V of Lab 3 – use meaningful names to distinguish each project archive. Include your surname, student number, lab and part number in the archive name e.g. Diessel-3002283-L03P5.qar
2. Create a PDF or JPEG file of the paper design for Part V. Use the same naming convention as above, but append -design.pdf or -design.jpg
   e.g. Diessel-3002283-L03P5-design.pdf
3. Create a zip file including the above 4 files and submit it using the *Make Submission* tab on the *Lab 3 additional guidelines and questions* link of the course website. Submissions are **due at 23:59 on 9 October, 2022**.