COMP 3601 – Design Project A
Design Proposal

Group 4

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Overview of the project

In this project, our team will design a custom microphone system using the Xilinx Kria KV260 FPGA MPSoC. The microphone system has the ability to allow users to individually customise different aspects of the music captured from the I2S MEMS microphone, such as volume, frequency to suit their needs. To further optimise the users' experience, users can easily adjust the tone of the original music to resemble the sound of different instruments through the FPGA board. These features are particularly useful for a large variety of users, whether they want to relax by listening to music or they want to enjoy music at a party without having the need to invite professional musicians to come and perform.

Current progress towards basic requirements

7/10/2023 (Saturday) – Completed bclk and ws
Over the past week, our team has been spending a lot of time to get ourselves familiarised with the project, as well as polishing our skills on using VHDL. This is not easy compared with the LED kickstart as there are very limited instructions given on how to implement the project (unlike the LED task which contains very detailed instructions). Together with the fact that most team members have little experience with working with an FPGA and audio processing, we encountered a lot of challenges in understanding the key concepts underpinning this project (e.g. the i2s protocol).

To overcome these challenges, as a team we decided to look for online resources, and to our surprise, there are quite limited amount of resources available, and they are all extremely informative, so it took us a while to understand the concepts. Then we started writing the section of code that generates the bclk and ws using clock division. While this is not hard as we have done a similar task before in the LED task, we need to test the code individually to ensure that they function as expected before combining to minimise debugging time. This gave rise to another challenge – we cannot test by playing music through the speaker as nothing will happen (the code has not been completed yet). We asked our TA and as we expected, it turned out that we have to write a test bench to do the testing, which is something that most of us have not learned and there are very limited resources online.

With the assistance from the TA, we finally managed to finish the test bench and the simulation results verified that our clocks are running at the required frequencies. What a big accomplishment we have achieved as a team!

Plan to complete the rest of the basic requirements

In order to complete the basic requirements, we will need to write code for the i2s finite state machine and the handshake procedure for the FIFO data type. We have divided the workload evenly amongst the team as follows:

- Ziyao and Zhihang: Finite state machine
- Stanley and Asher: Handshake

However, to our surprise, these tasks are harder than what they seem to be. While we were able to grasp the basic concept behind the working principles and implement the code, when we compile the program and load it onto the FPGA board on Tuesday, there is no current running through the board! This left us all in panic as the due date for marking is already passed and we all stared at the code for a long time and couldn't figure out the problem. Thankfully, we talked to our TA about the issue, and he pointed us in the correct direction by saying that there is some issue with the handshake section of the code. We will continue to debug the code as a team and hopefully it will work!

Current vision for application extension

At this stage, our team is considering the option to add another layer of complexity to the custom microphone system by implementing the sound mixing and musical instruments feature. These two options are chosen in particularly because their working principles are relatively easy to understand due to their extensive applications in the real world and more importantly, they are features that are extremely popular amongst users in the market. Given that all of our group members have very limited knowledge on topics such as networking and DSP filter design, these turn out to be the best options for us as we have very limited timeframe to implement the rest of the project, which does not allow us extra time for understanding how other applications (e.g. networking) function. It also makes the product more appealing to consumers due to its ease of use and flexibility.