University of Central Florida

Department of Computer Science

CDA 5106: Fall 2023

Machine Problem 1: Cache Design, Memory Hierarchy Design

by

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Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

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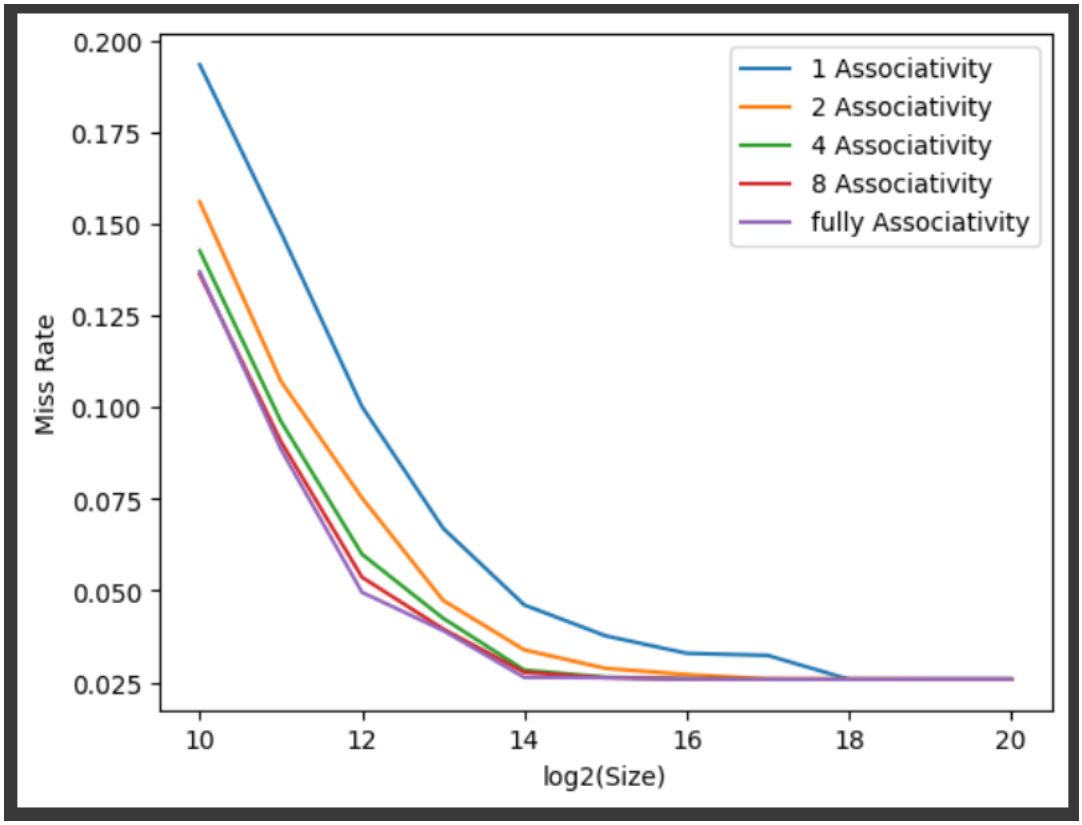
8.1. L1 cache exploration: SIZE and ASSOC

GRAPH #1 (total number of simulations: 55)



1. From the graph we can observe that Miss Rate decreases exponentially for each associativity as size increases, as we will have more space to allocate blocks. For a given cache size as we increase associativity Miss Rate decreases, Fully associative cache with larger size will have minimum miss rate.
2. Compulsary miss rate is defined as the misses that occur during the intial stage when cache is empty. It is unavoidable as there is no data in cache.
   Compulsary miss rate is invariant of associtivity and is typically 1.1% of total miss rate.

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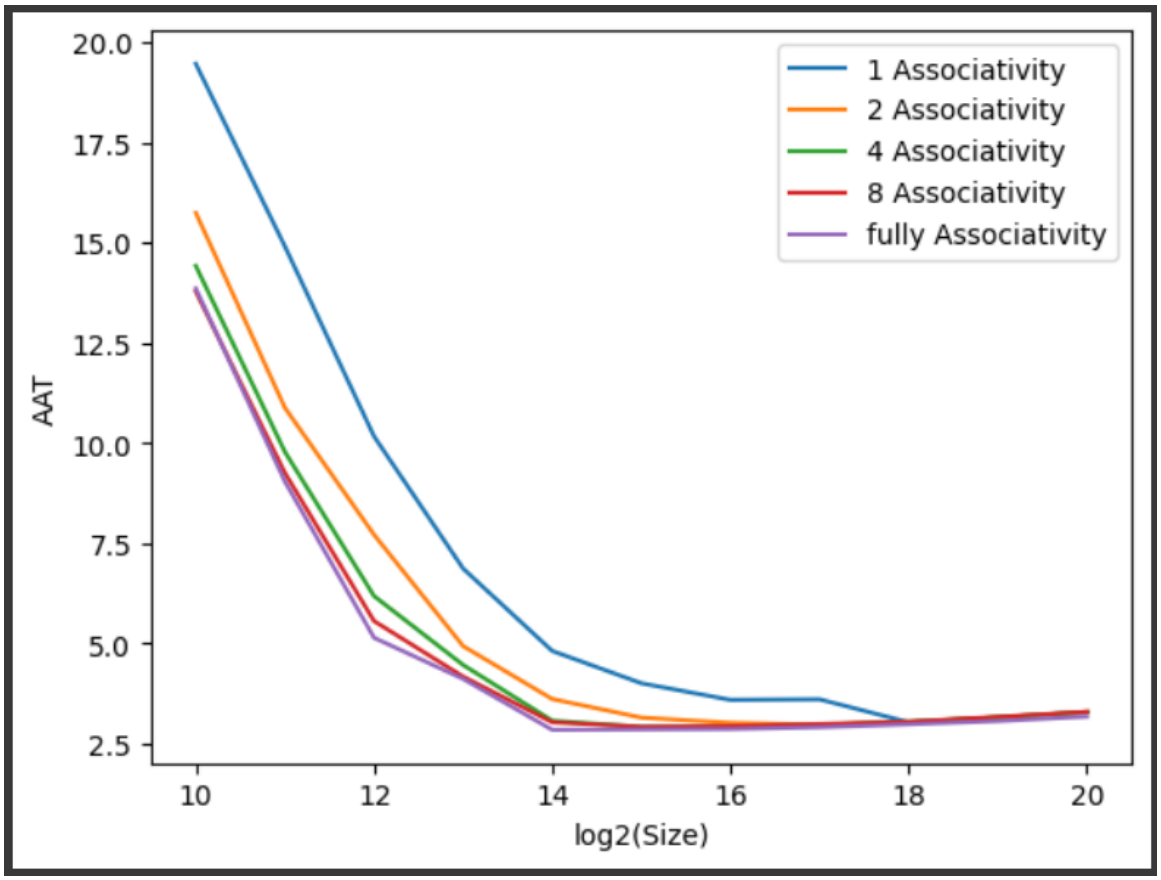
   Miss Rate(1MB - Fully Associativity) is  0.02582
   ```

   Hence compulsary miss rate of 1 MB cache with fully associative is 1.1*(0.02582) / 100 = **0.00028402 %** of total misses
3. Conflict miss rate is defined as the misses occur in a set as it is filled fully and some victim block needs to be removed. These depend on the associtivity where fully associative having least confict miss rate as all block go to same set.
   From the graph we can see that miss rate decreases as associativty increases and as conflict miss rate is a portion of total miss rate, conflict miss rate also decreases with increasing associativity
   ex.
   For 1MB 1-way associative cache conflict misses are 33% => 33*(0.02582) / 100 = **0.0085206**%

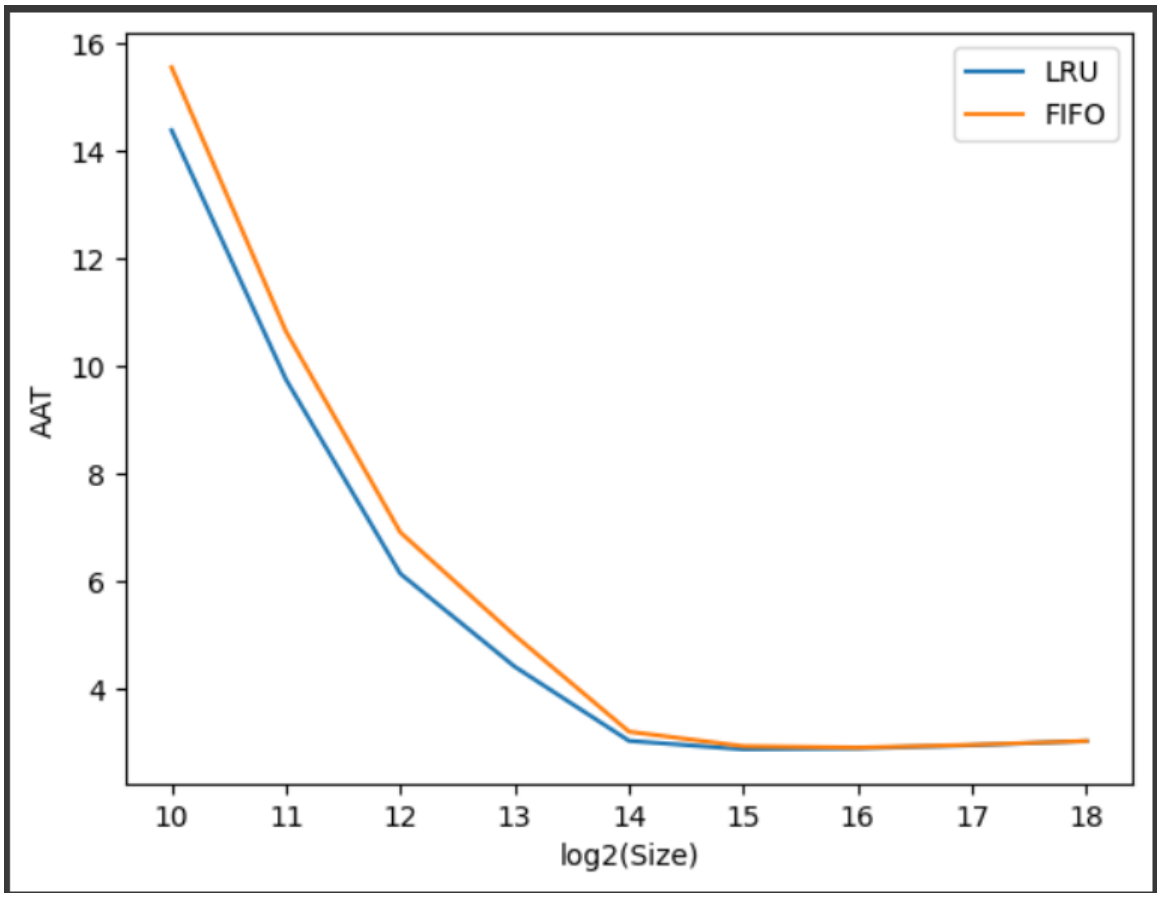
For 1MB 2-way associative cache conflict misses are 28% => 28 *(0.02582) / 100 = **0.0072296**%
For 1MB 4-way associative cache conflict misses are 8% => 8 *(0.02582) / 100 = **0.0020656**%
For 1MB 8-way associative cache conflict misses are 4% => 4 *(0.02582) / 100 = **0.0010328**%
Hence, we can see that conflict miss rate decreases as associativity increases.

GRAPH #2



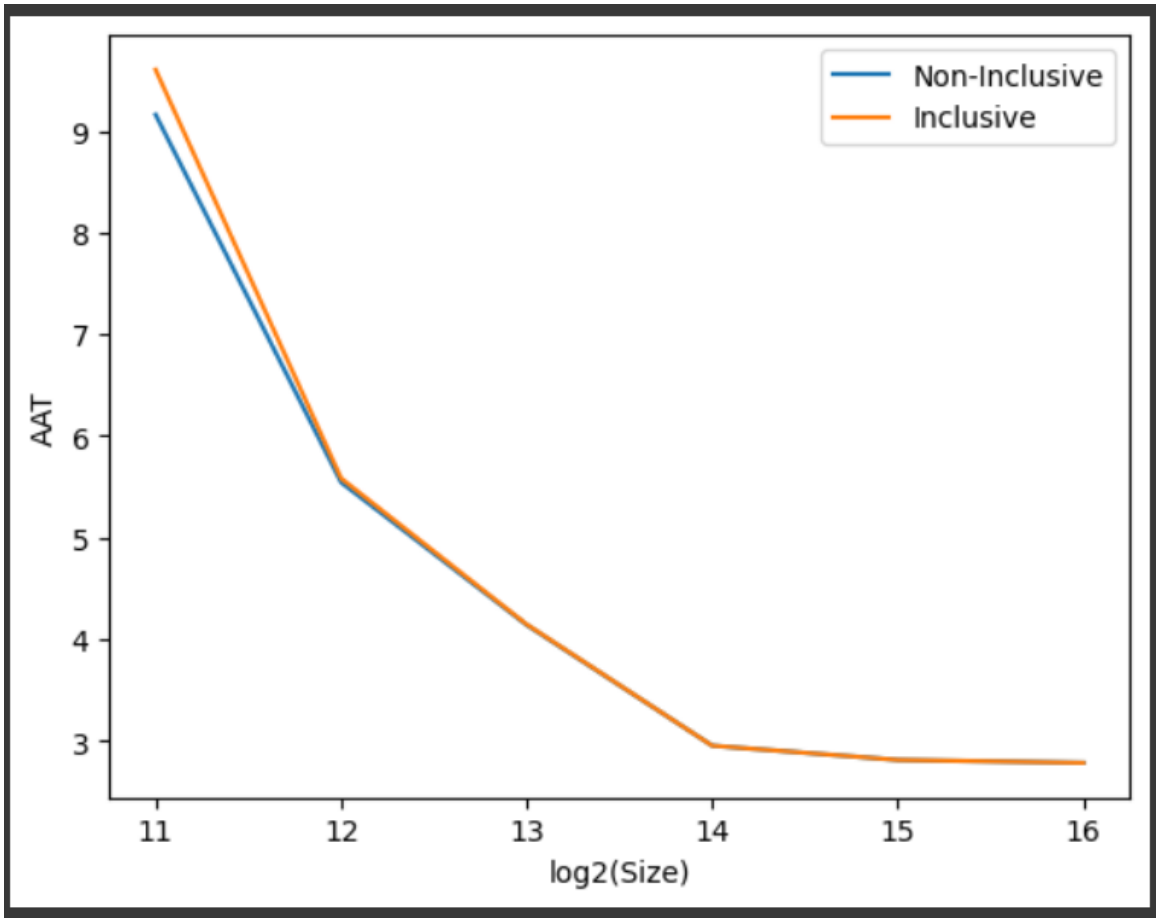
1. For memory hierarchy with only L1 and block size 32 the configuration that has least AAT(`2.839608`) is
   cache size = 16KB with
   associativity = Fully associative

8.2. Replacement policy study



1. LRU has less AAT in comparision to FIFO when the size is less, but as size increases both AATs come closer to each other. Overall LRU yields better results when compared to FIFO.
   Lowest is observed at cache_size = 32KB with LRU (`2.91125`)

8.3. Inclusion property study



1. As we can see in the graph above Non-inclusive property works better in lower sizes but as size increases miss rate become same for both inclusive and non-inclusive case. But on an average from the graph we can say that Non-inclusive property yields better results.
   Lowest is observed at cache size = 64KB , same for Both policies(`2.7845110951`)