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Combinatorial Problem Solving
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Logic Synthesis

1 Variables

Given the number of input signals n, the depth d, and the specification (truth table) of the logical circuit, I defined the following variables:

- $\mathbf{c_i}$:= "Code of the node i", for $i \in \{0, 1, ..., 2^{d+1} - 2\}$.
- $\mathbf{b_i^t}$:= "Boolean value of the node i for the row t of the truth table", for $i \in \{0, 1, ..., 2^{d+1} - 2\}$ and $t \in \{0, 1, ..., 2^n\}$.

For example, for a NOR-circuit that implements the functionality of an AND gate (see figure 1), with $n = d = 2$, one possible solution for the variables c_i and b_i^0, with $i \in \{0, 1, ..., 6\}$, is shown in figures 2b and 2c, respectively.

x_1	x_2	y	t
0	0	0	0
0	1	0	1
1	0	0	2
1	1	1	3

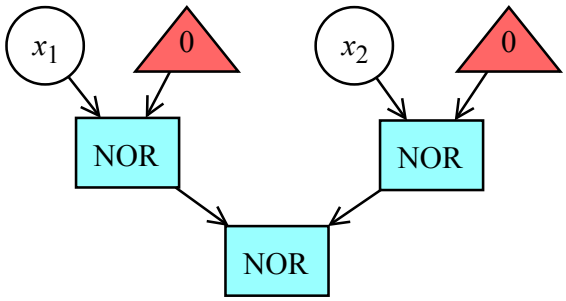
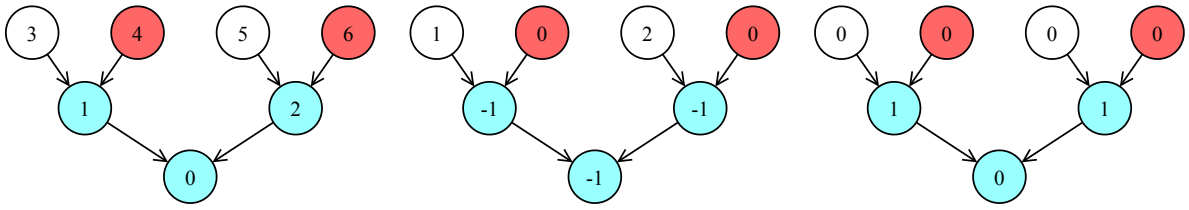


Figure 1: Truth table of $y = \text{AND}(x_1, x_2)$ and NOR-circuit implementing it.



(a) i (b) c_i (c) b_i^0

Figure 2: Visual representation of some parameters and variables.

2 Constraints

In order to simplify the definition of the constraints, I define two functions. Given the variable x_i, with $x_i = c_i$ or b_i^t,

- $\mathbf{left}(x_i)$:= "Variable corresponding to the one on the left of x_i"
- $\mathbf{right}(x_i)$:= "Variable corresponding to the one on the right of x_i"